PV Systems Reliability: Final Technical Report


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# FINAL Report

**Project Title:** PV System Reliability  
**Project Period:** 10/01/13-09/30/15  
**Budget Period:** 10/01/13-09/30/15  
**Reporting Period:** 10/01/13-09/30/15  
**Reporting Frequency:** FINAL  
**Submission Date:** 12/30/15  
**Recipient:** Sandia National Laboratories  
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**Date**
Project Objective:
The continued exponential growth of photovoltaic technologies paves a path to a solar-powered world, but requires continued progress toward low-cost, high-reliability, high-performance photovoltaic (PV) systems. High reliability is an essential element in achieving low-cost solar electricity by reducing operation and maintenance (O&M) costs and extending system lifetime and availability, but these attributes are difficult to verify at the time of installation. Utilities, financiers, homeowners, and planners are demanding this information in order to evaluate their financial risk as a prerequisite to large investments. Reliability research and development (R&D) is needed to build market confidence by improving product reliability and by improving predictions of system availability, O&M cost, and lifetime. This project is focused on understanding, predicting, and improving the reliability of PV systems. The two areas being pursued include PV arc-fault and ground fault issues, and inverter reliability.

PV arc-faults and ground faults have caused hundreds of fires in the U.S. and around the world [1]. In cases of faults on rooftop systems, the resulting fire can burn down the building and put the occupants’ lives at risk. In 2011 arc-fault circuit interrupter (AFCI) safety devices were required by the National Electrical Code® [2] on rooftop systems. AFCI products are being listed to the UL 1699B Outline of Investigation, but Standards Technical Panel (STP) experts strongly disagree on which UL requirements should be revised, retained, or modified when converting the UL Outline into a Standard. The STP does agree that the current Outline requires modification because UL-listed AFCIs are experiencing unwanted tripping in the field. Thus, in order to reach a consensus on these topics and convert the Outline of Investigation into a UL Standard, Sandia is performing extensive research into consistent arc-fault generation and nuisance tripping testing. Similarly, the International Electrotechnical Commission (IEC) Technical Committee 82 (TC 82) is creating an arc-fault certification standard and Sandia is collaborating closely with the international group to make the testing procedure realistic for PV installations, establish methods to avoid unwanted tripping, and ensures repeatability of the tests. When an arc-fault or ground fault detector trips in a PV system, no information is provided to the operator about the location of the fault. Determining the location is especially challenging in large PV systems consisting of acres of PV modules. If the problem is not identified quickly, the system operator will continue to lose money and could potentially assume the trip was the result of a nuisance trip and mistakenly turn the system back on. Developing a technology to locate the arc or ground faults will give PV system operators a means to resume operations quickly and minimize the risk that system will restart occurs without repairing the problem.

The challenge of locating PV arc and ground faults has been studied by a limited number of researchers [3-6]. The most successful technique is time-domain reflectometry (TDR) in which a step/pulsed voltage signal is sent through the conductors. A short or open circuit condition is manifest as a deviation in the reflected voltage pulse. Open connections (and some types of shorts) occurring in the PV wiring could be found with certain TDR devices [7].

As BOS connectors and solder joints degrade, they become potential locations for arc faults. There are still a number of scientific questions surrounding the degradation process that leads to arc-faults in PV systems. In addition, there is currently no data-driven predictive capability for the degradation of BOS connectors that is built on, and verified by, accelerated tests and field measurements. Such capability has been identified as a critical knowledge gap in the PV industry. While degradation models for solder joints exist, an assessment of the arc fault risk associated with damaged solder joint is necessary to provide context to weakened solder joints.
Characterization of interconnect degradation has potential for significant O&M applications due to the diagnostic, prognostic, or preventative tools that can be developed with sufficient understanding of the failure mechanisms. In summary, two accomplishments are needed to fully address the arc fault risk of interconnects: 1) Determine a definition of failure based on a risk assessment of arc faults in interconnects; 2) Develop a proven reliability model that can predict the lifetime of interconnects before an arc fault risk is significant.

This work addresses two needs in the PV industry: 1) data-driven, predictive capability that informs system operators on the expected rate of degradation for BOS connectors and solder joints; and, 2) an understanding on the effect that this degradation has on series arc-fault risk. Arc-fault damage at these interconnects can cause significant damage but its risk as a function of degradation has not been characterized. Establishing and quantifying the relationship could have significant O&M applications due to the diagnostic, prognostic, and preventative tools that can be developed with a sufficient understanding of the underlying physics and failure mechanisms. If known lifetime estimates are provided and failure precursors are identified, arc-fault detectors could proactively detect a dangerous situation before the fault occurs. Such a shift in operation would be a significant improvement over the current reactive nature of current state-of-the-art arc-fault detectors.

One cause of multiple fires is the “blind spot” in the detection area of the GFDI (Ground Fault Detector/Interrupter) protection fuse, which is common in US installations [8, 9]. A GFDI cannot detect a fault on the grounded current-carrying conductor (CCC), which could allow for unrestricted fault current flow bypassing the GFDI if a second fault is initiated in the array. In FY13, Sandia with the SolarABCs steering committee investigated ground faults and the ground fault detection blind spot [8, 9]. The conclusion of this work was that fuse-based GFDI (Ground Fault Detector/Interrupter) designs were vulnerable to faults to the grounded current-carrying conductor. This problem has caused multiple rooftop fires in the past [10]. Sandia and Solar ABCs identified new ground fault detection approaches (isolation monitors, residual current detectors, ground bond current monitors, etc.) [8], but there is little experience with these technologies in the U.S.

A team consisting of Sandia, SunPower, and DNV KEMA was established to determine the effectiveness of these new technologies and make recommendations about appropriate thresholds for the detection. If the trip threshold is too low, there will be nuisance trip events; but if the threshold is too high, certain ground faults will go undetected. Proper understanding of detection thresholds maximizes the balance between system performance (uptime), reliability, and safety.

As of 2010, the installed cost of PV systems was $3.40/Watt [11]. While most research, both historically and currently, has focused on the production costs of PV module technology, the cost of the necessary grid-connected DC-to-AC inverters has been largely ignored. As the price of PV modules drops, the price of inverters becomes more important. Inverters now constitute 8-12% of the total lifetime PV cost [12]. As of 2010, the inverter and associated power conditioning components accounted for $0.25/Watt [13], well above the DOE benchmark of $0.10/Watt by 2017 [11].

One of the key price drivers of the inverter component is inverter reliability [14, 15]. PV modules have long lifetimes with warranties offered up to 20 years. The mean time between failure (MTBF) of these systems have been shown, in the field, to be up to 522 years for residential and 6,666 years for utility systems [16]. In contrast, the inverter component has shown a field MTBF of between 1 and 16 years [16, 17]. Typical warranties on these devices
last only five to ten years [15], with a few manufacturers offering extended warranties for purchase up to 15 years. Even with the most optimistic view of inverter lifetime, it will be necessary to replace or repair an inverter multiple times over the lifetime of a PV module. Repairing the inverter is costly not only due to replacement parts and work crews, but also incidental costs, such as the loss of power not generated during downtime, purchasing replacement power unsupplied by the offline system, and any performance degradation before failure identification [15].

Inverter issues are especially problematic since, depending on the PV topology, they may affect the power production of a large number of modules and/or strings. According to SunEdison, a North American-based PV plant operator with over 750 PV plants across the world, inverter performance was responsible for 36% of total energy losses between January 2010 and March 2012 [18].

The inverter is less reliable than other components in the PV system because it is a complicated switching/monitoring system with a number of responsibilities. The main purpose of an inverter is to output power meeting power quality standards (e.g., IEEE 1547 [19] in North America or IEC61727 [20] in Europe). However, depending on the local/national ordinances or complexity of the device, the inverter may also be required to manage power output of the PV module, connect/disconnect from the grid, manage var, read and report status, or monitor islanding [12]. Added inverter functionalities exponentially increase the difficulty in creating both reliable and affordable components. In addition to having a number of functionalities, the inverter must also operate in relatively harsh, changing environments. Inverters may experience large temperature swings from -30 to 70°C, humidity conditions from 0 to 100%, and/or salty, corrosive environments.

PV inverters are responsible for most of the reliability issues in the solar energy system [15]. Among different components in a PV inverter, power semiconductor devices and soldering failure are responsible for more than 20% of all failures [21]. Die-attachment degradation is the most common type of failure mechanism in switches and will result in an increase in on-state resistance of MOSFETs during its natural aging process [22]. Thus, the ON-resistance, Rds (on), is considered as an indicator of MOSFET aging [23]. Several techniques have been proposed to estimate the life of PV inverters based on their circuit structures. The authors of [15] suggested a model framework to decompose the inverter into subsystems, and different circuit topologies have been evaluated to decide the reliability in [24] and [25], respectively. For these two methods mentioned above, it is extremely difficult to forecast a failure before it occurs which limits their applications in condition monitoring of PV inverters. To overcome this shortcoming, additional probes, hardware circuits as well as digital controllers are being added to inverters in order to monitor the operation status of power devices [26]. Although the real-time condition of power devices can be successfully decided by using these extra components, it is not a cost-effective solution.

In short, inverters must fulfill a complicated and ever expanding power handling role in harsh environments while still meeting the extremely cost-sensitive needs of the PV economic environment. In the future, inverter technology cost must decrease by 50%, with a 2X increase in reliability to facilitate grid parity of solar energy in the future [15, 27].
Simulation of modern inverter sub-systems and power electronics is an attractive performance and reliability tool due to its ease, flexibility, and cost compared to experimental methods. However, power electronics simulations have always been a challenge due to the non-linear behavior or power switches, connection to continuous sub-systems, and design of discrete-time control. Recent changes in inverter circuit topologies and switching schemes have made simulation scalability, modularity and optimization more challenging and time-intensive [28]. A realistic mission profile normally includes millions of switching events [28], making compact models [29, 30] (though accurate) very slow and not necessarily scalable.

**Task 1: Provide Technical Guidance to UL, IEC, and NEC to Improve Codes and Standards**

**Task Objective:** Provide Technical Guidance to UL, IEC, and NEC to Improve Codes and Standards

To improve fire safety in PV systems, the 2014 National Electric Code (NEC) requires arc-fault protection on all PV systems [31]. Arc-fault circuit interrupters (AFCI) meet this requirement by containing an arc-fault detector (AFD), which identifies an arc-fault and circuit interrupter, which de-energizes the PV system. In order to create robust arc-fault detection algorithms, tests must be completed on a range of PV systems: the algorithm must not nuisance trip on different inverter noise signatures, while also detecting arcing within the times prescribed in the UL 1699B requirement [32]. Additionally, AFD certification testing is permitted on real PV systems and on PV simulators since testing could be stopped for weeks or months in cloudy areas (e.g., Germany). PV simulators induce noise on the DC system because they are switching devices and this can cause unwanted tripping of the AFD. This leads to questions about the validity of the test procedure. Sandia investigated the validity of testing AFDs on PV simulators to provide results to the UL STP committee for considering the revision of the UL 1699B draft. Creating a consensus-based certification and safety standards for arc-fault circuit interrupters (AFCIs), arc-fault detectors (AFDs) will ensure faults are successfully detected and de-energized.

For this investigation, to accelerate robust AFD algorithm development, Sandia National Laboratories collected noise signatures from different arc-faults, inverters and combiner boxes. An example of these types of arc-fault signatures can be seen in Fig. 1. In order to test AFDs at Nationally Recognized Test Laboratories (NRTLs) there is a provision for using PV simulators because real PV may not be practical in some locations. There has been no scientific investigation into the difference of using PV simulators to test arc-fault detectors and because they are switching devices that may cause nuisance tripping (this has happened at DETL multiple times), so the validity of the test may be called into question. Sandia will investigate the difference in real PV and simulated PV when conducting arc-fault detector testing and report the findings to the UL STP.

Through this task, Sandia also supported the UL STP, IEC, and NEC CMPs.

**Task 1 Results**

**Milestone 1.1:** Generate arc-faults on real PV systems and in artificial configurations created by PV simulators. Measure the high frequency current content in the PV system.
This task has been completed during Q2 FY15. Tests were conducted at a variety of arc power levels, variety of arc start configuration and on a variety of connectors with different materials. Results have been previously summarized and will be re-iterated in the final report.

**Figure 1.** Second Generation Arc-Fault Generator with adaptable mounts, unified instrumentation and 600V, 30A power ratings.

**Milestone 1.2:** Compare the system baseline noise and arc-fault noise signatures from the real PV systems and the artificial PV systems.

The Sandia team collaborated with Texas A&M University to investigate novel methodologies for assessing arc-fault signatures, such as the Replay method. This methodology, as presented by McConnel et. al. [33] assesses the FFT signatures of the DC current during operation to evaluate the onset of an arc-fault. This method will enable the detection of real arc discharges using AFDs, while ensuring that nuisance tripping issues do not occur. In addition, collaborators at Texas A&M University have begun to develop novel algorithms, which can utilize the arc-fault signatures obtained at Sandia to determine the onset of a real arc-fault event. Fig. 2 presents a graphical representation of one of the methodologies:
Figure 2. Novel potential method for arc fault detection algorithm.

Milestone 1.3: Provide recommendations to UL 1699B STP and IEC TC 82 on the viability of using PV simulators to perform arc-fault detection testing in UL and IEC standards.

The UL 1699B STP has met at the UL Northbrook Office May 19-20, 2015. Jay Johnson presented the results from the last 2 years to the standards technical panel to drive the Outline of Investigation draft toward a consensus testing procedure. UL1699B ballot went to a vote for inclusion as an ANSI standard, however the proposal was voted down. Sandia is continuing to work with the Task UL force to address the issues. TAMU and Sandia have been in detailed discussions with the UL 1699B task group about PV simulators. This work will still continue in Q4.

Task 2: Invent novel methods for locating faults in PV systems

Task Objective: Develop a tool for determining the location of arc and ground faults on PV systems once arc-fault and ground fault detectors have tripped. Compare this method with other commercial options to evaluate the new tool relative to search accuracy and efficiencies.

When an arc-fault or ground fault detector trips in a PV system, no information is provided to the operator about the location of the fault. Determining the location is especially challenging in large PV systems consisting of acres of PV modules. If the problem is not identified quickly, the system operator will continue to lose money and
could potentially assume the trip was the result of a nuisance trip and mistakenly turn the system back on. Developing a technology to locate the arc or ground faults will give PV system operators a means to resume operations quickly and minimize the risk that system will restart occurs without repairing the problem.

The challenge of locating PV arc and ground faults has been studied by a limited number of researchers [42, 43, 44, 45]. It is preferred to remotely determine the location of the fault (as opposed to measuring the system locally for problems) so there has been a lot focus on reflectometry technologies (used for a long time to detect faults in long transmission lines). The most successful technique is time-domain reflectometry (TDR) in which a step/pulsed voltage signal is sent through the conductors. A short or open circuit condition is manifest as a deviation in the reflected voltage pulse [42, 43, 44, 45]. There are also a few commercial devices that can locate certain types of faults on PV systems. For instance, opens caused by series arc-faults can be located with Togami Line-Checkers, although these devices require tracing the electrical path to determine the fault locations. Open connections (and some types of shorts) occurring in the PV wiring could be found with certain other TDR devices [46]. Unfortunately, these devices are not designed for conductive paths with semiconductors or branch circuits, so remote fault finding is not effective in PV systems.

It is believed that some of the technical limitations with TDR can overcome with spread spectrum time domain reflectometry (SSTDR) because this technique uses multiple frequencies so harmonics and reflections in connectors can be minimized. Sandia and the University of Utah are collaborating on creating a novel method of determining the location of an arc and ground fault in large PV systems using SSTDR.

**Task Approach:** In certain fault cases, SSTDR data has identified the fault location using the method illustrated in Fig. 3. However, it is far easier to locate an open in the PV system cause by an arc-fault than it is to locate a parallel arc-fault or ground fault. The associated SSTDR electrical connections and analysis must be determined for each of these cases. Two additional barriers will be investigated in the future: effects of large, branched circuits in MW PV systems and methods to avoid creating a “health” scan baseline against which the results are compared. In addition, the SSTDR results will be compared with alternative fault-finding technologies on the market to determine which are most applicable to PV applications.
Figure 3: Methodology for determining the location of arc or ground faults on PV systems.

SSTDR autocorrelation data have been collected on two PV systems for the following fault types:

1. Ground faults between each of the modules of a single string and ground in a 1-string array. One example is provided in Fig. 4.
2. Open fault (caused by a series arc-fault) between each of the modules of a single string in a 1-string array
3. Line-to-line fault (caused by a parallel arc-fault) between modules of a single string in a 1-string array

The autocorrelation data are being analyzed using the difference between the “healthy” unfaulted system and the faulted data. Examples of the differences are shown in Fig. 3. It is possible to increase the efficiency of the detection algorithm by increasing the threshold for comparison between the average autocorrelation plots of a healthy PV string and a PV string with fault. This is accomplished by adding the autocorrelation differences only when the average amplitude of the healthy PV string is higher than a threshold value. However, this trend is reversed at very high center frequencies such as 96 MHz. Therefore, it could be possible to use the lower center frequencies to determine if a fault exists and the higher center frequencies for locating fault after detection.
Figure 4: Schematic diagram of the setup used at DETL. The SSTDR hardware was connected between the ground and the negative wire of the PV array.

The University of Utah has written, "A Comprehensive Review of Catastrophic Faults in PV Arrays: Types, Detection and Mitigation Techniques" and submitted it to the IEEE Journal of Photovoltaics. This sets the basis for their work in arc/ground fault detection and location identification.

"PV Arc-Fault Detection Using Spread Spectrum Time Domain Reflectometry (SSTDR)" has also been submitted to IEEE ECCE. This paper discusses how SSTDR can also be used to detect faults.

**Task 3: Establish arc-fault diagnostics and prevention methods via analysis of catastrophic arcing failures in BOS connectors and solder joints**

**Task Summary**

Three balance of systems (BOS) connector designs common to industry were investigated as a means of assessing reliability from the perspective of arc fault risk. These connectors were aged in field and laboratory environments and performance data captured for future development of a reliability model. Comparison of connector resistance measured during damp heat, mixed flowing gas, thermocycling and outdoor field exposure indicated disparities in performance across the three designs. Performance was, in part, linked to materials of construction. A procedure was developed to evaluate new and aged connectors for arc fault risk and tested for one of the designs. Those connectors exposed to mixed flowing gas corrosion exhibited considerable Joule heating that may enhance arcing behavior, suggesting temperature monitoring as a potential method for arc fault prognostics. These findings, together with further characterization of connector aging, can provide operators of photovoltaic installations the information necessary to develop a data-driven approach to BOS connector maintenance as well as opportunities for arc fault prognostics.

This task centered on a physics-based, data-driven approach to characterize the lifetime of BOS connectors. The primary objectives were to (1) generate connector aging data associated with field and accelerated tests for model development and input and (2) understand the effect of connector aging on arc fault risk. Motivating questions include: how do field and laboratory exposures compare in terms of performance degradation rate and damage modes? How does connector materials of construction and design affect aging performance? What is the impact of connector contact degradation on arc fault risk?

To meet these objectives, three connector designs common to industry were aged in laboratory and field conditions while simultaneously measuring changes in electrical contact resistance. A cumulative damage model was developed from paired field and laboratory data to demonstrate how this data could be used to predict contact resistance. Post-mortem analyses of aged connectors were carried out to characterize damage mode as a function of environment.
Furthermore, arc fault risk of new and aged connectors was assessed via a novel experimental platform and test methodology developed for this program. The following is a summary of this work.

Task Methods

A. Aging Tests

Four exposure environments were chosen to characterize the effects of various environmental stress factors on electrical contact resistance and materials degradation. Three common latching BOS connector designs, from three different manufacturers, were exposed in these environments. Two of these exposures were comprised of laboratory accelerated tests commonly used for robustness screening of photovoltaic components and electrical contacts- mixed flowing gas (MFG) and damp heat. The damp heat test was conducted using conditions stated in IEC60068 for laboratory air at 85°C/85% RH. Grime simulants for coastal and desert environments were applied to a subset of samples exposed to the damp heat to examine the effect of contamination on contact performance. Mixed flowing gas exposure was according to ASTM B845, Method G, which involves exposure to a gas mixture of H₂S, Cl₂, NO₂ at ppb levels, 70% RH and 30 °C. This test has been demonstrated to emulate and accelerate damage of in-service electrical contacts in sheltered light industrial atmospheric conditions. The third laboratory exposure consisted of temperature cycling of as-received and MFG-aged connectors between -40 °C and 100 °C at a ramp rate of 10 °C·min⁻¹ between these points. This ΔT range is between 5 and 10 °C outside of the min and max average manufacturer-stated temperature specs of the three connector types.

The fourth exposure was carried out at an outdoor test site at Sandia National Labs in Albuquerque, which can be classified as a light industrial, high desert environment. Connectors were mounted on a boldly exposed polycarbonate panel at 45° relative to the ground and facing south. Four-wire resistance measurements were made across the connectors on an hourly basis during all tests using calibrated and multiplexed milliohm meters, Figure 5.

B. Materials Analysis

Both as-received and aged connector pins and sockets were cross-sectioned and examined using optical and electron microscopy. Regarding the latter, analysis was performed using a Zeiss Supra 55VP field emission SEM under high vacuum, 20 kV accelerating voltage, and a working distance of 10 mm in both secondary and backscattered electron modes. A Bruker SDD EDS detector and software were utilized for compositional analysis.
C. Arc Fault Tests
The arc fault behavior of select as-received and aged connector pins and socket sets was characterized using an arc fault generator described earlier in this report. A PV simulator running a constant power 300W I-V curve was used as the power source. Voltage, current and connector surface temperature were captured at a rate of 2 Hz during these tests using methods.

In these experiments, power was run across a set of connectors under test while simultaneously separating a fully mated connector at 0.09 mm/s using a motorized linear stage until a sustained arc occurred. Resistance across the connector pin and socket rises during separation due to a gradual decrease in contact area. If a decreased amount of translation is necessary to produce a sustainable arc, then the resistance increases and the connector disturbance needed to cause an arc-fault event also increases. The separation distance prior to the first detected spark as well as that required for a sustainable arc was examined as a means to infer the relative risk of arcing between contacts in a connector. The intermittent and sustained arcing events were visually observed and position noted during the experiments. The separation velocity utilized was found to provide sufficient time for a sustained arc to develop as a result of separation.

Results and Discussion
A. Aging Tests
Resistance measurements taken across connectors during the damp heat and MFG tests are given in Figures 6 and 7. Figure 6 exhibits resistance measurements taken during damp heat exposure of 27 connectors. Average resistance increased on the order of 0.1 mΩ across all connector and contamination types between 350 h and 10,000 h. From this figure, it is evident that a portion of the Type 1 connectors contaminated with coastal and desert grime exhibited the largest increase in resistance of ~ 1 mΩ. Figure 7 exhibits resistance measured across 99 connectors exposed to the MFG environment. Relative to the damp heat test, resistance increases were rather minimal, with the exception of one Type 1 connector that indicated gradual degradation that accelerated after the 4000 hour mark.

Figure 6 Resistance measured during over 10,000 hours of damp heat testing. Connectors contaminated with coastal grime simulant are represented as dotted lines; those with desert contaminant simulant are dashed lines and those without contamination are solid lines.
Temperature cycling for 100 connectors was carried out for 610 cycles. The results for 25 as-received Type 2 connectors are given in Figure 8. A comparison between room temperature resistance measured prior to cycling and room temperature resistance during a pause in cycling (1080 hours) indicates an average resistance increase of 7 mΩ. One connector, not included in this statistic, exhibited increasingly frequent intermittent resistance between near baseline and near 10 Ω, as seen with a number of the outdoor exposed Type 2 connectors. The average increase in resistance is approximately an order of magnitude greater than that exhibited by 10,000 hours of damp heat exposure and 5000 hours of mixed flowing gas exposure (~ 1 mΩ).

The results for 1.5 years of outdoor exposure of 55 connectors are given in Figure 9. Noise in the data is due to diurnal and seasonal temperature variance. Comparison of average resistance measurements across all connectors during similar temperature regimes (2000 and 10,000 hours) indicated that values increased on the order of 1 mΩ, excluding one Type 3 connector and nine Type 2 connectors. These connectors exceptionally exhibited the greatest change in resistance, up to 100 mΩ, amongst connectors across all three laboratory exposure tests.

Comparison between the different environments shows that, with the exception of thermal cycling, outdoor exposure generally invoked higher resistance increases at faster rates than the laboratory tests. Temperature variance is one of the major environmental stressor differences between the outdoor test and MFG and damp heat tests. Given this and the fact that thermal cycling was able to invoke higher contact resistance increase rates, it appears that thermal...
variance is a primary driver for contact resistance increase. There are a number of potential degradation modes related to thermal cycling that could be responsible for resistance increase, including fretting and corrosion of the corrosion due to differential thermal expansion and contraction of the materials.

A linear cumulative damage model was developed from paired field and thermal cycling data to demonstrate how field and laboratory accelerated tests could be used to predict contact resistance. Specifically, the data was fit to the Coffin-Manson model:

\[
\frac{L_f}{L_t} = \left(\frac{\Delta T_t}{\Delta T_f}\right)^m
\]

Where \( L_f \) is the time to failure in the field; \( L_t \) is the time to failure in the lab test; \( \Delta T_t \) is the range of temperature swing in the lab test and \( \Delta T_f \) is the range in the field; and \( m \) is an experimental constant. For the laboratory thermal cycling test, \( \Delta T_t = 140 \, ^\circ C \) and \( L_f \) was determined as the mean time to failure for those connectors that exceeded an arbitrarily chosen increase in resistance of 0.1 or 1 \( \Omega \). Major temperature cycles witnessed during the field exposure were characterized using a rainflow-counting algorithm. \( L_f \) was subsequently determined for each of the temperature cycle ranges (\( \Delta T_f \)) in Figure 10, assuming \( m \) values from 0.25 to 3.

Figure 8 Resistance measured across 25 new, as-received Type 2 connectors during laboratory thermal cycling.

Figure 9 Resistance (upper) and temperature (lower) measured on connectors boldly exposed to 1.5 years of a high-desert light industrial outdoor environment.
Mean times to failure in the field were then predicted using the Palmgren-Miner linear damage hypothesis to cumulatively account for the fraction of time spent at each temperature cycle range. The predicted mean time to failure as a function of $m$ is given in Figure 11. The intersection of the prediction curves with the actual $L_f$ determined from the field data suggests $m$ should be between 0.25 and 0.5 for the 0.1 and 1 $\Omega$ failure thresholds. Carrying out thermal cycling across a range of $\Delta T$ values would allow for estimation of $m$ with greater confidence.

It is important to emphasize that this model serves as a demonstration of an approach that could be taken to develop quantitative BOS connector degradation predictive capabilities. A number of liberal assumptions are inherent to this approach that would necessarily need to be relaxed or confirmed in order to provide confidence. These include (a) that thermal cycling is the only environmental stressor leading to considerable contact resistance increase; (b) damage linearly scales across all ranges and rates in temperature swings; and (c) damage is deterministic in nature. Regarding the latter, more sophisticated damage accumulation models, such as the inverse power model, could be utilized to capture the probabilistic nature of performance degradation.

**B. Materials and Post-Mortem Analysis**

The materials of construction of pins and sockets for the three connector types are listed in Table 1. This information was derived from SEM/EDS analysis of cross-sections of as-received components. It is notable that Types 2 and 3 are similar in materials make-up.
Post-mortem analysis was carried out on connector pins that were boldly exposed (no housing) to the MFG environment to ascertain extent of corrosion damage. In general, the tin-plated Type 2 and 3 connectors qualitatively suffered less corrosion than the silver-plated Type 1 connectors. Micrographs in Figure 12 exemplify this. Type 2 and 3 connectors exhibited sparse and localized attack of the underlying base metal in areas of thinner plating or porosity, as exemplified in Figure 8c. This is in contrast to the relatively uniform and nearly complete mineralization of the silver plating (a) and attack of underlying base metal (b) of the Type 1 connectors. The thickness of the mineralized silver layer on one cross-section averaged 7 ± 4 µm.

The disparity in performance across the three connector types is attributed to variance in corrosion response related to materials of construction, Table 1. In contrast to the minimal corrosion seen on the tin-plated Type 2 and 3 connector pins when boldly exposed without their housing, the boldly exposed Type 1 pins exhibited severe corrosion, Figure 8. Relative to tin, silver is vulnerable to corrosion in sulfur-rich environments representative of the MFG test and industrial atmospheres, so this could be expected. The results of these tests suggest that if the housing of the Type 1 connectors, which presumably shielded the contacts from the corrosive MFG atmosphere, were to be compromised in a sulfur-rich atmosphere for an appropriate amount of time, corrosion-induced joule heating could lead to arc fault conditions. Post-mortem

<table>
<thead>
<tr>
<th>Type</th>
<th>Base Alloy</th>
<th>Underplate, Nominal Thickness (µm)</th>
<th>Overlayer, Nominal Thickness (µm)</th>
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<td>Cu</td>
<td>Ni, 1</td>
<td>Sn, 5-9</td>
</tr>
</tbody>
</table>

Table 1 Material Construction of Connector Types under Study
analyses similar to those carried out for the MFG tests are necessary to relate the resistance trends in the damp heat tests to the realized degradation of the electrical contacts.

Post-mortem analyses of connectors exposed to damp heat, thermal-cycling, and outdoor exposure were not carried out due to time and resource constraints, but would provide valuable information with regard to damage pathways. Comparison of field and lab exposed connectors would elucidate the degree to which the lab exposures were able to replicate field data. For example, evidence of fretting or fretting corrosion, common electrical contact degradation modes associated with differential thermal expansion and contraction, on outdoor and thermal cycled connectors would provide basis for utilization of thermal cycling as a laboratory accelerated test.

**Arc Fault Tests**

The arc fault behavior of a Type 1 set of 10 new and 6 connector pins that were boldly exposed (no housing) to the MFG test environment was explored using the arc generator. Figure 13 is a plot of the resistance and temperature measured as a function of position for these connectors. The position at -8 mm is the fully mated connector and 0 mm is indicative of the last point of ohmic contact of the pin and socket upon separation as determined by a digital multimeter prior to each experiment. The average resistance of the fully mated aged connectors was 30 m$\Omega$ higher than that of the new connectors. The impact of this higher resistance is apparent in the temperature measurements that are near 100 °C for most of the aged connectors prior to separation. The onset of arcing is reflected in spikes in the temperature and resistance trends near the 0 mm position. Once sustained arcing was achieved during the separations, the power was cut off, which is seen as decreasing temperature after the spikes.

Figure 12 Measured resistance (top) and temperature (bottom) as a function of separation distance during arc fault pull-apart experiments on Type 1 connectors. The position at -8 mm is the fully mated connectors and 0 mm represents the point of separation where ohmic contact was last detectable between the pin and socket by a multimeter. Positive position values indicate separation distance from this point.

Comparison of the separation positions at which the first intermittent arc and a sustained arc were observed during each experiment is given in Figure 14. There appears to be no significant difference between new and aged connectors with regard to the positions at which arcs occurred. Similarly, examination of the position at which resistance spiked during the experiments revealed no clear differentiation between the new and aged connectors.
The results for the connector arc fault revealed using a small sample size yielded no considerable difference between the separation distance needed to arc new and MFG-aged connectors, but several important conclusions can be drawn from these results. The results do show that arcs occur before the specified gap spacing of several millimeters indicated in the UL1699B standard for arc fault tests between two electrodes. In this work we found both intermittent and sustained arcing to occur within several hundred microns of contact separation, and in some cases before separation. This suggests that the UL standard spacing should be revisited for arc fault testing of connector pin and socket geometries. Additionally, visual observation of arcs as a function of position during connector separation is subjective with respect to the observer and may be a major source of the variance seen in the results. One means of reducing this uncertainty would be to determine the onset of an arc through FFT analysis of the current signal during the separation test.

Figure 14 Distribution of positions at which the first intermittent and sustained arcs were observed during arc fault experiments on Type 1 connectors. The position of 0 mm represents the point of separation where ohmic contact was last detectable between the pin and socket by a multimeter. Positive position values indicate separation distance from this point.

Conclusions

- BOS connectors were found to be robust to the corrosion-related laboratory tests they were subjected to in this study. Outdoor field exposure invoked considerably higher resistance increase at faster rates than these tests.

- Thermal cycling was the only laboratory test able to accelerate contact resistance increase relative to outdoor exposure. This result merits further exploration of thermal cycling as a parameter to be incorporated in accelerated tests for BOS connectors.

- An approach for development of a quantitative empirical performance model for connector degradation was demonstrated based on a pairing of laboratory thermal cycling and field data. Additional thermal cycling and field data are needed in order to further this approach.
• Performance disparity across connector designs was linked to materials of construction for the mixed flowing gas corrosion laboratory test via post-mortem analyses of exposed connectors. Similar analyses for the other laboratory tests and field-exposed connectors would provide key information necessary for advancement of accelerated tests that invoke damage pathways similar to that of the field environment.

• A procedure to evaluate arc fault risk of new and degraded connectors was tested. The results yielded no discernable difference between the separation distance needed to arc new and mixed flowing gas-aged connector. The results do show that arcs occur before the specified gap spacing of several millimeters indicated in the UL1699B standard for arc fault tests between two electrodes. Suggestions for further improvement of the test methodology were given.

Task 4: Ground fault detector technology evaluation and threshold determination

Task Objectives: In FY13, Sandia with the SolarABCs steering committee investigated ground faults and the ground fault detection blind spot [65-67]. The conclusion of this work was that fuse-based GFDI (Ground Fault Detector/Interrupter) designs were vulnerable to faults to the grounded current-carrying conductor. This problem has caused multiple rooftop fires in the past [68]. A number of alternative technologies were suggested [67], but there is little experience with these technologies in the U.S. A team consisting on Sandia, SunPower, and DNV KEMA was established to determine the effectiveness of these new technologies and make recommendations about appropriate thresholds for the detection. If the trip threshold is too low, there will be nuisance trip events; but if the threshold is too high, certain ground faults will go undetected. This balance is very important to the performance and reliability of the PV system and the safety of those around the system.

This task consisted of a combination of SPICE simulations and field measurements to determine the appropriate thresholds for Residual Current Detectors (RCDs), isolation resistance periodic checkers (Riso), and Current Sense Relays (CSRs). A major component of this work is determining what is nominal and the largest current leakage for “health” PV systems. This value effects the lower bound of the Riso, RCD, and CSR measurements before nuisance tripping occurs. To this end, leakage currents were being measured in the field and on PV simulators to determine the influence of different PV components and technologies on the leakage. The size of the array also plays a large part, so smaller systems at SNL’s DETL lab were compared to the leakage seen in the SunPower fleet.

Leakage data was collected on different systems at Sandia using the new Bender instrumentation to determine (a) the effect of metrological conditions on leakage, (b) which PV components are contributing the majority of the leakage current, and (c) the variability in leakage current between systems with identical PV components. The test configuration is shown in Figure 15.
Additionally, more simulations of different ground fault detectors (RCD, Riso, and CSR) were performed for (a) different module leakage values in “healthy” arrays and (b) in the presence of ground fault at different locations and with different impedances. Sandia presented an oral presentation at IEEE PVSC on the “Recommendations for RCD and Riso Ground Fault Detector Trip Thresholds” with DNV GL and SunPower. These results will come from the simulations and experiments listed above. Lastly, Sandia has submitted an abstract to EU PVSEC on RCD currents from larger (500 kW) inverters installed in the US. The dataset covers more than a year for dozens of these inverters.

The system leakage values of 340 500 kW co-located inverters in a desert environment were measured at one-minute intervals for over a year (1 January 2013 to 3 August 2014) using RCDs. In compliance with UL 1741, each inverter has a GFDI fuse rated at 5 A to protect against ground faults. This conservative threshold was chosen to maximize the detection of ground faults while eliminating unwanted tripping events due to electromagnetic interference (EMI), module/inverter leakage, and meteorological events (i.e. lightning). Figure 16 shows leakage data from a single inverter (data is typical for all the 500 kW inverters) at one-minute intervals over the course of a year (blue trace) as well as the 24-hour average of the leakage current (black dots) and the ambient temperature (red trace). As can be seen from the data, at no point during the year did the leakage current exceed 2.57 A. Excluding transient spikes in leakage current due to inverter start-up or shut-down when the DC contactor was closed, the maximum daily inverter leakage is approximately 1.1 A with a minimum daily inverter leakage of approximately 0.38 A at night. This minimum is influenced both by the RCD detection threshold and nighttime inverter behavior. At night, the inverter isolates from the AC and DC-side and relies on a 3 A GFDI fuse on the ground bound for ground fault detection rather than the RCD. Therefore, the actual minimum leakage current is most likely lower than the
recorded nighttime RCD current of 0.38 A. These historical RCD values indicate that there is significant overhead in the 5 A UL 1741 GFDI rating and the RCD trip threshold could be reduced to 3 A or less.

Figure 16: Typical leakage current data from a 500 kW inverter taken at one-minute intervals (blue trace) and averaged over a 24-hour window (black dots). The ambient temperature is also shown over one-minute intervals (red trace).

Figure 17 shows a weeklong subset of the data from seven inverters. The inverter-to-inverter variation in leakage current is nearly identical during the turn-on/turn-off periods. During the turn-on/turn-off period, the RCD current temporarily stagnates at a value of approximately 0.7 A. This shoulder lasts approximately 30 minutes while there is sufficient voltage (~175 V) to turn on the RCD and power electronics components in the inverter, but not enough photocurrent to initiate the inversion process. Once the available array current increases to a sufficient value (~700 V), the inverter begins MPPT and the leakage current steps to around 1.1 A. Throughout the day, the inverter-to-inverter variation in the leakage current is around 200 mA. The RCD morning shoulder also exists during inverter turn-off as the bus voltage decreases at the end of the day.

During the week shown, one of the CTs attached to Inverter 7 measured a current spike—also seen in Figure 17. These spikes are not correlated between inverters (even those in geographical and electrical proximity to each other) and seem to occur at random, although they are always associated with inverter turn-on or turn-off. The inset of Figure 17 shows a detailed view of the current spike. The turn-on spike lasts from 07:26 to 07:34 with a linear increase in current leakage from a “shoulder” turn on leakage of 0.685 A to a maximum leakage of 1.676 A. After the maximum, the leakage current quickly decreases to a steady on-state leakage current value of 1.058 A. It is believed the DC contactor operation at the beginning and end of the day is causing the spikes in the current as the array capacitance is discharged. This only appears for some mornings/afternoons because it is a quick transient that is not always caught by the data acquisition system. The multi-minute spike in the inset is most likely the result of the data historian compression and only a single measurement is recorded during the current impulse. Since this is a quick transient with an extremely small number of readings, it is unknown if these spikes will trip the RCD protection circuit if the threshold
is set below the magnitude of the spike. Single, isolated measurements in the data above the 5 A trip threshold do not result in inverter shutdown, so it is unlikely that these transients will cause the RCD to detect the presence of a fault and initiate inverter shutdown. Notably, GFDI fuses intrinsically have resistance to transient events because they are thermally actuated; therefore, as ground fault detection in the U.S. is converted to electrical measurements, it is important to engineer in trip logic robustness with respect to transient currents.

When describing proper RCD thresholds for ground fault protection, there are three statistical parameters that are of great importance: the average functional leakage of a group of inverters, their standard deviation, and the maximum measured leakage values. The leakage average and standard deviation of a group of inverters is useful for advanced fault detection techniques such as decision tree or outlier detection [13-15]. The maximum leakage values are used for simple thresholding to determine the presence of a fault.

Figure 18 (top) shows the raw cumulative distribution functions (CDFs) of all 340 RCDs for one year. Each CDF has a similar multi-tiered shape with a large increase in frequency of measurements at ~0.35 A corresponding to the nighttime baseline of the inverters. A second increase to 50% frequency occurs at ~0.7 A, corresponding to the turn-on/turn-off shoulder leakage. Finally, about 50% of the leakage frequency occurs in the 0.8 to 1.2 A range, corresponding to daytime leakage values. For a given CDF curve, a shift to the right indicates higher leakages in the inverter possibly due to an incorrect baseline value or a high impedance ground fault. A shift up and down typically indicate data drop-outs where the RCD monitor repeats certain values for extended periods of time. Data dropouts and incorrect baseline values contribute to the spread in the CDFs of the inverters. If these effects are corrected (which can be done via simple, on-board programming), such as baselining the inverter leakage each night when the inverter is disconnected and eliminating repeated data due to drop-outs, the CDFs of all 340 inverters are surprisingly tightly distributed (Figure 18 bottom). When inverters are properly baselined and data drop-outs are accounted for, all but five of the 340 inverters...
(colored in blue in Figure 10 bottom) lie within a range of 1.14–1.51 A at 99.99% frequency. The five inverters that act as outliers (CDFs are different colors) demonstrate either higher lower leakage values than average. The RCD values over a six-day period of these outlier inverters along with a “typical inverter” (blue) are shown in the inset.

The inverters corresponding to the magenta, green, and black curves show higher measured leakage values during the day while the red curve corresponds to a lower measured leakage value. It should be noted that, although the baseline for each inverter is the same, the turn-off/turn-on shoulder values scale with the daytime leakage of the inverter, indicating that the increased or decreased RCD current may be due to a proportionality (gain) problem in the RCD rather than an actual increase of leakage in the inverter.

The 4σ and 6σ confidence bands of the average CDF of all the inverters (both “normal” and the five outlier inverters) is shown as dashed black lines in (Figure 18 bottom). Note that these curves represent RCD values that are exceeding rare given the data population: Pr(x ≥ μ + 4σ) = 0.00317% and Pr(x ≥ μ + 6σ) = 9.87·10⁻⁸%. These statistical metrics can be used to establish thresholding rules based on the requirements of the inverter manufacturer, O&M company, plant owner, or standards-making panel. For example, there is a 4σ confidence that 99.999% of measured leakage values are below 3.1994 A and a 6σ confidence that 99.999% of the RCD values are below 3.8616 A (Table II). A set point of 5 A (as currently mandated by UL 1741) corresponds to an eight-nines confidence of the 4σ confidence band.

For simple thresholding practices, the distribution of leakages for an inverter is of little importance as only the instantaneous leakage value is used to detect the presence of a fault. Therefore, the maximum leakage values of monitored inverters are most important. Figure 19 shows a series of histograms of the measured leakage values of all 340 inverters. At the global level (Figure 19 top), the leakage values cluster into three groups corresponding to the nighttime baseline (~0.32-0.38 A), the turn-on/turn-off shoulder (~0.64-0.72 A), and the daytime leakage (~0.92-1.39 A).
Table II: High frequency values of the CDFs for the average of all inverters as well as the $4\sigma$ and $6\sigma$ confidence bands.

<table>
<thead>
<tr>
<th>Frequency (%)</th>
<th>Average</th>
<th>$4\sigma$</th>
<th>$6\sigma$</th>
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<td>99</td>
<td>1.1825</td>
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<td>99.9</td>
<td>1.6437</td>
<td>2.9679</td>
<td>3.6300</td>
</tr>
<tr>
<td>99.99</td>
<td>1.8028</td>
<td>3.1270</td>
<td>3.7892</td>
</tr>
<tr>
<td>99.999</td>
<td>1.8752</td>
<td>3.1994</td>
<td>3.8616</td>
</tr>
<tr>
<td>99.9999</td>
<td>2.4891</td>
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<tr>
<td>99.99999</td>
<td>2.8759</td>
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<td>3.6827</td>
<td>5.0069</td>
<td>5.6690</td>
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Figure 19: Histogram of baseline and dropout corrected leakage values for 340 inverters. The majority of points are contained in three groups below 2 A (nighttime baseline, turn-on/turn-off shoulder, and daytime leakage). Between 2.5 and 3.75 A, a small number of points were measured, although many of these single measured points can most likely be attributed to noise in RCD measurement.

At higher RCD currents, there is another distribution of values from 1.50-1.82 A (Figure 19 middle) most likely corresponding to the capacitive discharge spikes that occur when the inverter first connects to the array. At even larger currents, there are a small number of points (<10) in the 2.5-4.0 A range (Figure 11 bottom). Due to the large number of data points collected and the compression algorithm of the server, it is assumed that these high current, low frequency data points are noise in the measurement, recording or transient events. This is corroborated by the fact that a
single leakage value of ~8 A was recorded for one inverter. This single measured RCD current above the trip threshold of 5 A did not cause the inverter to trip due to a ground fault. Therefore, single, high current leakage values are most likely measurement errors that can be safely discounted when determining appropriate trip points for the RCD monitor. As can be determined from the large-scale, long-term data presented here, trip points for the inverter could easily be lowered from 5 A to 3 A with no observable increase in nuisance tripping events.

**Task 5: Evaluate and compare arc-fault detectors on the market**

Task Objectives: The Sandia National Laboratories PV Arc and Ground Fault Detection and Mitigation program ran from 2010 until 2015 and made a number of significant contributions to the field of photovoltaic system safety and reliability. During the course of the program, Sandia worked with over a dozen solar and original equipment manufacturers and investigated:

- series and parallel arc-fault detection methods;
- improvements to the draft arc-fault circuit interrupter (AFCI) certification standard, UL 1699B;
- arc plasma physics models and burn characteristics;
- array electrical behavior during ground faults (including those constituting the detection ‘blind spot’); and
- recommendations for novel and traditional ground fault detectors.

A brief summary of the research program and its successes is described below.

The arc-fault research program initially focused on methods of arc-fault detection in DC systems and an extensive literature review found that DC arc-fault detection could be performed via time-based or frequency-based methods. While the Sandia team researched the time-domain techniques initially, frequency-domain methods were found to be more robust and the program focused on this area. By working with one of the early PV AFCI developers, Eaton Corporation, the team investigated the conducted arc noise in a number of frequency ranges and discovered that the arc-fault energy was elevated over the baseline noise most significantly in the 1-100 kHz decades [69]. This discovery, led to a more thorough investigation of the frequency-dependent filtering characteristics of PV modules and cables; there was excellent transmission between 1-100 kHz for PV modules [70], but above 100 kHz, antenna effects, radiative and capacitive coupling, and reflections from impedance mismatches were present [71]. The team concluded that arc-fault detection at higher frequencies was possible but more difficult because of unwanted tripping from radio frequency (RF) effects and the 1/f “pink” noise generated by arc-faults decays at higher frequencies.

AFCI designs were starting to come on to the market to meet the 2011 National Electrical Code (NEC) 690.11 requirement at the end of 2011 [72] Sandia worked to educate the public on the code requirements and the AFCI development status [73,74]. Sandia also worked directly with a number of companies to test and improve their AFCI designs [75,76,77] and funded work to investigate more robust detection algorithms using wavelet decomposition as opposed to the traditional Fourier transformation methods [78].
Sandia National Laboratories was also highly active in the development and revisions of the PV AFCI certification outline of investigation, UL 1699B. Between 2011 and 2015, there were a number of open questions brought up by the UL 1699B Standards Technical Panel that Sandia investigated. Firstly, since there are nearly limitless combinations of modules, cabling, and power electronics combinations for PV systems, it was unknown if the few arc-fault detection experiments in the draft certification standard would ensure the AFCIs work universally. One potential solution was to inject hundreds of pre-recorded arcing and unfaulted noise signatures into a test circuit to show the AFCI solution was robust to a range of array hardware, configurations, and topologies—a concept that was used to accelerate the development of the Sensata Technologies AFCI [79]. A similar idea was to artificially inject arcing noise into a health PV system at different signal-to-noise ratios to validate or test arc-fault detector algorithm [80]. Another area of great interest to the UL 1699B STP was determining the arcing energy levels that caused ignition of polymers because these defined the trip limits for AFCIs. Extensive experimentation and modeling of arcs in proximity to multiple polymers confirmed the UL 1699B trip times were effective at preventing fires in PV systems [81]; but, a low power (100 W) test was recommended to be added to the standard [82]. For years, the method of generating the arc-fault (electrode types, geometry, use of steel wool initiator vs. the pull-apart method, etc.) was debated. One of the primary concerns was that different generation methods produced different noise signals—elevated noise signals were easy to detect so there could be AFCIs on the market that would not trip on some arc-faults. AFCI vendors on the other hand argued that the los noise arc-faults were not representative of field faults. To provide some data to the discussion, Sandia ran hundreds of arc-fault parametric experiments and compared the noise signatures and found that there was a 20 dB amp difference in the arc-fault signatures [83], which could easily be the difference between tripping and not tripping. The discussion within the UL 1699B STP continues today with new electrode geometry proposal. Lastly, the number and type of UL 1699B tests that should address unwanted tripping was contentious. Sandia offered suggestions on the type of tests along with the difficulty in passing them by performing a number of experiments with 10 arc-fault detectors and AFCIs to determine their ability to withstand unwanted tripping scenarios [84]. There were widespread unwanted tripping failures which indicated the need to included additional unwanted tripping tests in UL 1699B.

Sandia supported the 2014 and 2017 National Electrical Code© 690.11 development process as well. There was strong debate over the expansion of the arc-fault detection requirement to include parallel arc-faults. Sandia found a number of options for differentiating series and parallel arc-faults [85] and submitted a patent on these ideas [86]. Electrical simulations of series and parallel arc-faults showed that it was possible to detect the fault type through proper instrumentation [87]. But, ultimately, the requirement for parallel arc-fault detection has not been included in the NEC because of the low occurrence rate and difficult mitigation method: either shorting the array or module-level electronics [88].

Locating the arc-fault once the AFCI tripped has been a long standing problem for the industry. It was determined that the electrical characteristics of the array were not sufficient to determine the fault location [89]. Alternative methods of locating arc and ground faults were later discussed in a review paper [90]. One purported advantage of string-level arc-fault detectors was the arc-fault could be easily located and only a subsection of the array would need to be de-energized. Sandia confirmed this hypothesis and verified there was a low probability of the arc-fault noise tripping adjacent AFCIs [91]. Sandia also developed a concept of using filters to determine which PV string contained the fault [92].
Sandia was also interested in understanding and modeling PV failure mechanisms and arc dynamics. Corrosion of a bypass diode solder joint was shown to generate enough Joule heating that an arc-fault could be initiated in a junction box [93]. A more thorough investigation of plasma heat transfer was then performed which confirmed the appropriateness of the UL 16998 trip limits [94].

Experimental investigations of connector failure mechanisms via accelerated life testing were performed to determine the impedance changes with time and estimate the risk of arcing [95]. The life expectancies of AFCIs themselves were also investigated and the burn-in process was found to be essential for fielded components [96].

Early in the project, it was clear that predicting when an arc-fault was going to happen would be better than responding to it. “The best arc-fault is one that never happens.” Sandia researched a range of prognostics and health management (PHM) concepts to find arc-fault ‘canaries’ that could indicate the PV array was degrading and at risk of experiencing an arc-fault. Some of the methods that were investigated for arc-fault PHM were impedance spectroscopy [97], impedance increases in solder joints and connectors [98] and temperature increases from Joule heating [99]. The idea of using learning algorithms to detect when PV arrays were experiencing unexpected degradation was also studied.

Ground fault program

Sandia began studying ground-faults, following the revelation that traditional fuse-based Ground-Fault Detector/Interrupters (GFDIs) were not effective in preventing certain fires – a situation referred to as the ground fault detection blind spot. Using a high-fidelity SPICE electrical simulation, Sandia discovered the extent of the problem and found that adjusting the fuse-rating was not effective at solving the problem.

Working with the Solar America Board for Codes and Standards (Solar ABCs), Sandia identified a number of alternative ground fault detection technologies that would reduce the fire risk and eliminate the detection blind spot [96]. These alternatives included isolation monitors ($R_{iso}$) that measured the array impedance to ground, current sense monitors (CSMs) that monitor the ground current in DC-grounded systems, and residual current detectors (RCDs) that measure the differential current in the DC source circuits, typically at the inverter. Sandia also funded the University of Utah to research new methods of ground fault detection and location identification using time domain reflectometry.

The team worked with industry to find the ideal ground fault detection thresholds for each of these techniques where the largest number of ground faults would be detected without any unwanted tripping events. RCD measurements from 340 healthy utility-scale inverters were studied for over a year to determine the distribution of normal RCD measurements [96]. The considerations for applying ground fault detection thresholds are numerous: the leakage from the modules, inverter and other BOS components changes the most sensitive setting before unwanted tripping occurs, and measurement errors from the environment (e.g., lightning) and are also a challenge. The thresholds for isolation monitors and $R_{iso}$ ground fault detectors were derived using analytical models, but these are highly dependent on the system size, leakage characteristics, and instrument noise. Sandia proposed that ground fault detectors that have a programmable range of adjustment so that they can be tuned to the equipment that they are designed to protect.
Sandia is also working with the UL 62109-2 Standards Technical Panel (STP) to revise the IEC 62109-2 inverter requirements for the US market. In that standard, there are requirements for isolation and RCD/CSM detection thresholds. Based on this project’s results, the new recommendations will likely be adjustable for larger PV installations to account for the variability in baseline measurements.

Sandia worked with a large engineering, procurement and construction (EPC) firm to implement the CSM solution and pick the appropriate trip thresholds. The new ground fault detector technology reduced the fires the EPC firm experienced to zero and, after calibration, the number of unwanted tripping events were approximately 3/year.

**Task 6: Electro-thermal performance model**

Task objectives: The broad programmatic problems have already been stated in FY14. In FY15 the inverter reliability research area will utilize the capabilities developed in FY14 to achieve the goal of a PLECS electro-thermal model that provides the design recommendations needed to reduce inverter LCOE to DOE goals of $0.10/W.

As previously noted for FY14, by investigating the reliability of proposed circuit topologies and optimizing the design of currently used circuit topologies and/or components, the inverter lifetime can be increased to reduce inverter LCOE to achieve DOE SunShot goals of $0.10/W. Achieving this goal will result in a minimum of 2.5x in cost reductions, consistent with DOE targets.

For this investigation, Sandia will develop the Matlab Simulink/SymPowerSystems inverter electro-thermal performance model to predict the necessary changes to lower LCOE in a cost-effective manner under varying operating conditions and environments. Doing so will demonstrate an inverter design, derived from the Simulink/SymPowerSystems model, that can realistically achieve a 25-year lifetime under normal and advanced functionality usage conditions with manufacturing costs conducive to industry adoption.

![Fig. 20. Overall layout of top-level Simulink model used for lifetime/ageing simulation of inverter performance.](image-url)
A significant amount of work concentrated on setting up device-level detailed description of existing Simulink models and planning for further detailed models.

- Device-level subsystems, which include both the thermal and electrical input functions, have been developed for the diode and n-channel MOSFET (see Fig. 20 and Fig. 21 for an image of a diode and IGBT subsystem). A number of simulations have been run to determine an acceptable range of thermal parameters for a given device, with assumptions being made for heatsinking, electrical inputs, etc.

![Diode Subsystem in Simulink](image1)

**Fig.21**  Diode Subsystem in Simulink

![IGBT Subsystem in Simulink](image2)

**Fig.22**  IGBT Subsystem in Simulink

Based on the accuracy of these device models, additional subsystems will be developed including the IGBT and the capacitor. This work will continue in the next quarter of this project. Some of the thermal parameters to be included are shown in Fig. 23.
• Thermal Mass, (in J/°K), Thermal Time Constant (s), and/or Thermal resistances have been compiled (or approximately calculated) for several devices, based on datasheet values or estimated from device size, geometry, density, and specific heats. Sandia staff and a graduate intern in Mechanical engineering are being consulted on the methodology used in these calculations. Next steps will include using experimental data obtained in Task 9 of this project and using experimental values such as changes shown in Figure 24.

![Fig. 23. Thermal transfer parameters](image)

![Fig. 24. Change in ICE after 1000 cycles at different temperatures obtained experimentally at Sandia National Laboratories](image)
Note: Considerable effort is being placed into verifying that the models produce the expected thermal effects (i.e. the thermal response) and that both the thermal and electrical responses are reasonable. This involves reading literature published by manufacturers (e.g. white papers) and speaking with industry contacts, etc. Small assemblies of the thermal-compensated devices are being assembled into thermal environments (as shown in Fig. 25 below):
• Former grid-tied inverters have been disassembled (e.g. SMA 1800 W Sunny Boy) and the power electronic, capacitors, and heat-sinking elements have been catalogued and rendered as closely as possible in the models. Additional units across a variety of power ratings are available and will be examined as well.
• A rough method for device and ultimately, system-level stress (thermal, operational, and electrical) accumulation has been developed. The thermal history properties are expected to impact reliability, performance, and lifetime estimates. This is explained in more details in the following section.

Thermal Degradation Parameters:
To facilitate reliability, durability, and performance modeling, both the thermal history and age-related degradation should be modeled, and currently this capability needs to be added to the model (i.e. does not exist in SimElectronics). Typically the junction produces a great deal of heat, and depending on the operational mode (continuous or pulsed), different thermal response curves are used. We will focus on pulse-mode operation with heatsinks present and high, but variable, ambient temperatures, as this corresponds to the real-world conditions we are interested in understanding.

Thermal parameters are characterized by the following table, where failures are estimated at 25% over common

<table>
<thead>
<tr>
<th>Device</th>
<th>Failure Temp (°C)</th>
<th>Failure Temp-Seconds (°C-Secs)</th>
<th>Age Failure (years) at 25 °C</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode – Exponential</td>
<td>190</td>
<td>1.0E11</td>
<td>20</td>
<td>Unusual effect on lifetime for electrolytics. Caps used for filtering and as snubbers.</td>
</tr>
<tr>
<td>Capacitor – Electrolytic</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>IGBT</td>
<td>190</td>
<td>7.5E10</td>
<td>20</td>
<td>Mortality assumed at 125% of maximum junction temperature</td>
</tr>
<tr>
<td>MOSFETs</td>
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<td></td>
<td>25</td>
<td>Mortality assumed at 125% of maximum junction temperature</td>
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<tr>
<td>H-Bridge</td>
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</tbody>
</table>

Our model will keep track of cumulative operation parameters, at various temperatures, and will aggregate operation into Temp-Second or Temp-Minutes as appropriate. Based on particular wear-out or failure mechanisms of each component, a warning or an error message is generated, as shown in Figure 27 below. For example, if a device has been operating at a dangerously high temperature levels, a warning “Device ## temperature too high” will appear. But, if a device
reached its’ end of life operating conditions, a warning “Device ### end of life reached” warning will appear.

**Fig. 27. Examples of error or warning messages generated as part of our simulation.**

**Task 7.**

**Task Objectives:** Sandia has set up and instrumentation of reliability and lifetime testing capability at SNL. The environmental chamber was finally installed and functional. The chamber is capable of temperature range of -40C to +150C, and humidity range up to 95RH. This environmental chamber was used for long-term testing of inverters under harsh environmental conditions as per SOPO. The tests placed stresses on the dc and ac components and have adverse effects of the performance of the inverter. The inverters have been instrumented at the dc and ac sides of the inverter with voltage and current transducers that have sufficient bandwidth to capture voltage and current transient that may be caused by the implementation of support functions. The temperature rise on critical components while the DUT was monitored.

**Environmental chamber testing results.**
The following variables and timing diagram describes environmental chamber operation:

**Fig. 28. Temperature profile used for inverter HTOL testing**
At the beginning of the test, DUTs was tested as per standard test, described in the table below. This will be used as t=0 test results. Following this, temp and humidity are to be ramped up (ramp up and down time depend on the chamber) and are to stay at these values for time $t_1$ (200 hrs). After that time elapsed, the chamber is to be ramped down (ramp down time depending on the chamber) and DUT is to be tested again, as per procedure in the table below. The same pattern was to be repeated until the overall time at high temp, high humidity reached 1000hrs. This test is intended to resemble IED 61215 or 62093 test specs. All operating and characteristic values (such as component temperature) will be recorded during tests.

Scheduled tests sequence for each testing interval:

<table>
<thead>
<tr>
<th>Test num</th>
<th>Test name</th>
<th>Setting 1</th>
<th>Setting 2</th>
<th>Duration</th>
<th>Other notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Nominal P, PF</td>
<td>$P=3000$ W</td>
<td>PF=1</td>
<td>5 min</td>
<td>Powered up</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$P=1500$ W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Nominal P, var PF</td>
<td>$P=3000$</td>
<td>PF=0.9</td>
<td>5 min</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PF=0.8</td>
<td>5 min</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>PF=-0.9</td>
<td>5 min</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td>PF=-0.8</td>
<td>5 min</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A typical performance profile is shown in Figure 29 below:
Task 9: Component Reliability

Task Objectives: Accurate component degradation profile lifetimes and failure modes are important to ensure adequate representation of long-term inverter operation in the electro-thermal model of Task 8. To account for secondary and tertiary inter-component effects during inverter operation, it is vital to understand isolated component degradation and failure mechanisms. Currently, manufacture-specific component-level reliability data does not necessarily include application-specific environments found in PV usage. In FY14, a single phase, single stage PV inverter test bed was developed. In FY15, analysis of this test bed under specific device degradation will be studied.

Component Degradation

The first component to study was chosen to be the IGBT semiconductor switches, since their degradation directly affects the performance of the inverter. Infineon BSM50GB120DLC (1200 V, 100 A) full-bridge IGBT devices were chosen to test under long-term thermal cycling stress. Thermal cycling of IGBTs will affect the die...
attachment to the copper board (DCB) due to CTE mismatch; causing void formation and fatigue-induced cracking from shear strain due to thermal cycles (Fig. 30). Voiding of the die attach layer will affect electrical control of the die, increasing parasitic resistance during the ON-state (and thus the power dissipated). CTE mismatch will also affect the attachment of bond wires to the die, resulting in an increase in $V_{CE(on)}$.

![Diagram of IGBT packaging](image)

**Figure 30:** Packaging of a generic IGBT module. The module consists of a die and the elements used to control its electronic and thermal properties.

The IGBTs devices were electrically characterized using pulsed IV characterization and underwent thermal cycling stress in a thermal oven (room temperature to 150°C at 10°C/min ramp rate). This thermal stress was carried out for 500 cycles, when the devices were removed, re-characterized, and a sub-population returned to the thermal chamber for another 500 cycle stressing when they were again be removed, re-characterized, and a sub-population returned to the oven. This process continued until the entire population of IGBTs had varied degrees of degradation. Data presented here detailed the characterization of the IGBTs after 500 and 1000 cycles as compared to a pristine unit. After thermal cycling in the over, there is a clear change in current carrying capacity of the IGBT (Figure). The change in $I_{CE}$ in the stressed devices compared to pristine due to thermal stress is small for $V_{GE}$ less than 5 V or greater than 11V. This is due to the fact that the absolute value of current is very low in the subthreshold region ($V_{GE} < 5V$). In the large $V_{GE}$ region ($V_{GE} > 11$ V), the shift is very small because the power supply used to measure the IGBTs goes into current compliance at 50 A, so the shift in current quickly goes to zero. However, in the threshold region of interest, there is clearly a change in the IV characteristics as the IGBT is stressed. The change in IV characteristics is more clearly seen in Figure 31 and 32, which shows the IV threshold curves of the IGBT population before (red line) and after (pink dots) thermal stress. The blue line indicates the shift in $I_{CE}$ value due to stressing. At 150°C in the region of threshold turn-on ($V_{GE}$~ 6 V), the current through the stressed devices is lower than the pristine devices. However, at high current carrying gate voltages ($V_{GE}$ ~ 10 V), the cycled devices actually carry more current than the pristine devices.
Figure 31: Change in $I_{CE}$ vs $V_{GE}$ at different temperatures for IGBT units after 1000 cycles.

Figure 32: Change in threshold IV characteristics of an IGBT at 150°C before and after 1000 thermal cycles.
This information can be summarized for all temperatures and devices in Fig. 33. The maximum value of $\Delta I_{CE}$ (immediately before power supply current compliance) is shown as a function of unit temperature for 500 (red dots) and 1000 (black dots) thermal cycles. After 500 thermal cycles, there is a slight change in $I_{CE}$ at temperatures less than 100°C. At 150°C, there is a decrease in $I_{CE}$ in the stressed units. This bipolar temperature dependence is frequently seen in MOSFET devices due to material quality effects in the conduction channel.

After 1000 cycles, the same bipolar effect is seen, although the baseline $\Delta I_{CE}$ has shifted to greater values. The change in $I_{CE}$ from a pristine to a device after 1000 cycles can vary by 5-6 A.

Through the work in this last quarter, it has been demonstrated that thermal cycling has altered the parameters of the IGBT current conduction significantly compared to pristine units. In the next quarter, the performance of pristine IGBTs as well as units which have been stressed at 500, 1000, and 1500 cycles will be compared in an to determine effect on inverter performance and power quality.

**Inverter Reliability Workshop**

In FY15, Sandia has also been working in conjunction with Sarah Kurtz at NREL to host an inverter reliability workshop in parallel with NREL’s module-focused PVQAT workshop. This workshop took place on Wednesday, February 25th in Golden, CO and had focus areas ranging from component-level failure mechanisms to system-level testing (see agenda below). The workshop had 54 participants from a wide variety of industry stakeholders. There was vigorous discussion during all the sessions with many sessions going over time due to the amount of debate.

**Utility-Scale Inverters—Greg Ball (Chair), DNV GL**

- “Inverter Reliability”—Matt Ursino, Solectria
- “Accelerated Reliability Testing of Commercial and Utility PV Inverters”—Ron Vidano, Advanced Energy

**Module Level Power Electronics—Jack Flicker (Chair), Sandia National Laboratories**
• “Standardization and Reliability Testing of Module-Level Power Electronics (MLPE)” — Govindasamy Tamizhmani, TUV PTL
• “Determination of Mean Time to Failure” — Eric Boskin, Maxim Integrated
• “Managing Large Inverter Fleets” — Mark Baldassari, Enphase Energy

**Advanced Inverter Functionality — Faraz Ebneali (Chair), ReneSola**
• “Smart Inverter Grid Support Functions and Potential Impact on Reliability” — Aminul Huque, EPRI
• “The Impact of Smart Inverters: How Rule and Regulation Will Transform DG into Smart Systems” — John Berdner, Enphase Energy

**Failure Modes — Chris Deline (Chair), NREL**
• “IGBT Failure Modes in Inverters” — Diganta Das, CALCE
• “Corrosion of Electronics” — Rob Sorensen, Sandia National Laboratories
• “Nanocoatings: The Solution to All of Our Environmental Protection Problems?” — Greg Caswell, DfR Solutions

**Accelerated Testing — Tim Peshek (Chair), Case Western Reserve University**
• “PV Inverter Accelerated Testing for High-Humidity Environments” — Paul Parker, SunPower
• “Reliability Testing of Inverters” — Michael Mills-Price, DNV GL
• “Predictive Reliability Modeling for Inverters Based on Electro-Thermal Phenomena” — Ken Armijo, Sandia National Laboratories

All attendees were required to take part in a survey that details inverter performance, usage, and reliability across the industry. Survey results were compiled and published at the workshop. The survey results, as well as all the presentations are available for download at [http://www.nrel.gov/pv/performance_reliability/pvmrw_20150225_wed_inverter.html](http://www.nrel.gov/pv/performance_reliability/pvmrw_20150225_wed_inverter.html)

**Component Losses for Inverter Advanced Functionality**
The large-scale penetration of variable and intermittent distributed resources into the electrical grid can have significant effects on frequency and voltage stability of the grid. It is predicted that as penetration ratios increase, the number and severity of grid parameter deviations from nominal will also increase (especially far away from distribution feeders).

Historically, distributed generation has had such a low penetration ratio that, in low-voltage events, PV inverters have been asked to disconnect from the grid in order to prevent an islanding situation from occurring (since removing the active power of a small numbers of inverters on the grid was not sufficient to exacerbate the voltage deviation). However, as the penetration ratio increases and the power generated by distributed resources becomes non-negligible, PV inverters that disconnect from the grid can exacerbate the voltage deviations, decreasing grid reliability issues in the future. Therefore, new rules, such as the California Public Utility Commission’s (CPUC) Rule 21 interconnect requirements, are being implemented which demand that inverters ride-through a low (or high) voltage event. In Hawaii, where upwards of 12% of
households have rooftop solar, the ride through requirements had to be expanded due to the larger voltage fluctuations on the island grid (which has significantly less inertia than other grids).

In the future, as the number of distributed resources on the grid increases, the frequency of voltage excursion may increase. Thus, the increased losses of a PV inverter during a ride-through event may become a non-negligible aspect to the unit reliability over its lifetime.

In the new interconnection requirements, the voltage level of the ride through event determines the mode of operation of the inverter. For example, for Rule 21, in the event of a voltage sag lower than 0.5 PU ($V_{\text{sag}} < 0.5 \text{ PU}$), the device under test must cease to energize and ride through the voltage sag for a duration of 1 second. If the voltage recovers above 0.5 PU within 1 second, then the inverter must resume energizing the utility up to 90% of pre-event power level within 1 second. An example of an inverter riding through in this manner is shown below (Fig. 35).

During the ride through event, the ac current has a 36% transient spike and the dc voltage experiences a 24.3% voltage transient as the DC bus immediately returns to open circuit. During the low grid voltage condition, the inverter ceases to energize the utility. When the grid voltage returns to nominal, the dc voltage experiences a ringing transient voltage waveform. This ringing results in an increase in bus voltage above open circuit, to 500 V, which applies additional voltage stress to the DC-side components. After this transient, the inverter commences to return to its previous operating conditions and commences maximum power point tracking and power export.

A residential inverter with EPS support capability was evaluated in a laboratory setting to investigate possible stresses on the dc and ac components and any adverse effects of the performance of the inverter when the inverter goes through a grid voltage

Fig. 35: System voltages and current from a LVRT event
anomaly. The inverter analyzed has L/HVRT capabilities, but does not adhere to Rule 21 requirements due to the lack of a momentary cessation function. Voltage and current waveforms of MOSFET switches were recorded simultaneously along with system-level information in a 3 kW residential inverter during low voltage ride through events ranging from 0-1.5 s with $V_{\text{sag}}$ ranging from 0-220 V. MOSFET voltage was monitored via Tektroniks voltage probes with drain-source current measured via a mini Rogowski coil. To minimize variations in the readings, DC power was provided by an Ametek PV simulator. Grid transients were simulated using a California instruments RS90 grid simulator. Tests were conducted at PV input powers of 3.29 kW provided by 14 Sanyo HIT 200 and 44 Astro-Power 75 simulated modules, respectively. Electrical data was collected via an Agilent DPO 3014 oscilloscope and analyzed with MATLAB.

Fig. 36.: Normalized energy loss per switch for LVRT events of different $V_{\text{sag}}$ values from 0-240 V with durations of 1-1.5 s (in the “cease to energize” regime for $V_{\text{sag}}=0$-120 V).

Fig. 37: Normalized energy loss per switch for LVRT events ($V_{\text{sag}}$=43 V) of different durations from 0-1.5 s. The energy loss per switch is independent of ride-through time, indicating that the inverter is actively exporting energy for all LVRT events.
Cumulative MOSFET switching loss during each voltage transient event was calculated and then normalized by the duration of the event in order to determine the relative severity of the LVRT event. The results of normalized energy loss per switch as a function of ride through time and $V_{\text{sag}}$ are shown in Fig. 36 and Fig. 37, respectively. As can be seen from Fig. 36, the rate of energy loss during the event is independent of event length with a value of approximately $682 \pm 40$ J/s. This indicates that for all LVRT events the inverter attempts to export energy. Since the inverter in question does not adhere to Rule 21, it never enters the “cease to energize” state ($0-0.5$ PU for $t_{\text{event}} < 1$ s, shown by the dashed blue line) nor does it disconnect when the ride through event is longer than 1 s. Such behavior would be evident from Fig. 36. Since, at 0.195 PU, the corresponding Rule 21 behaviors are “momentary cessation” and “disconnect”, the normalized energy loss of a Rule 21 compliant inverter would be close to zero.

For the residential inverter studied, the rate of energy loss during an LVRT event is linearly related to the value of $V_{\text{sag}}$ (Fig. 37) with a maximum normalized energy loss equal to 879 J/s for $V_{\text{sag}} = 0$V. The energy loss decreases at a rate of approximately $-3.5$ J/V as $V_{\text{sag}}$ increases until the energy loss is zero at a PU of unity. Each of the ride through events represented in Fig. has a duration greater than 1 s. This means that to be Rule 21 compliant, the inverter should cease to export power and for all $V_{\text{sag}} < 0.5$ PU (120 V), shown as the solid blue line. So a Rule 21 inverter should have a linear increase in normalized energy loss until 0.5 PU. For $V_{\text{sag}} < 0.5$ PU, the normalized energy loss should be nearly zero due to the “momentary cessation” operation mode. Based on the data presented here, it is apparent that an inverter that rides through a low voltage event experiences increased losses compared to normal operation. The new CPUC Rule 21 interconnection requirements, especially the “momentary cessation” operation mode, will tend to decrease the LVRT losses of inverters for voltage transients below 0.5 PU.

References:


[31] H. Schmidt and F. Reil, "Welcome to the 2nd Workshop ‘PV Fire’,," presented at the PV Brandsicherheit Workshop, Freiburg, Jan 2013 (in German).


