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PV Systems Reliability Final Technical Report: Ground Fault Detection

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Executive Summary: We have examined ground faults in PhotoVoltaic (PV) arrays and the efficacy of fuse, current detection (RCD), current sense monitoring/relays (CSM), isolation/insulation (R_{iso}) monitoring, and Ground Fault Detection and Isolation (GFID) using simulations based on a Simulation Program with Integrated Circuit Emphasis SPICE ground fault circuit model, experimental ground faults installed on real arrays, and theoretical equations.

SPICE model and analytical results were used to determine trends for various ground fault conditions and to ascertain potential benefits of reducing the fuse ratings in PV systems. Decreasing the Ground fault protection device GFPD ratings to 1 A would protect against a wider range of ground faults. However, further decreasing the fuse ratings below 1 A does not improve the number of faults that can be detected due to larger internal GFPD resistances and a subsequent decrease in fault current. It is necessary to carefully consider the GFPD rating and resistance to optimize the types of ground faults that can be detected.

To demonstrate the efficacy of CSM and/or RCD fault detection techniques, Sandia partnered with a major PV engineering procurement and construction (ECP) firm for aggressive field deployment of advanced ground fault detection equipment that significantly reduced the fire risk in PV systems. Over three years, they have refined the detection thresholds for their systems to minimize unwanted tripping events while maintaining a perfect safety record. Additionally, analysis of one-minute RCD leakage values of 340 co-located inverters found a 5 A trip point to be overly conservative. For these inverters, RCD trip point could be lowered from 5 A to as low as 2.5 A with six 9's confidence that any unfaulted RCD current measurement would be lower than the ground fault setpoint. Statistically, this would correspond to 0.5 trips/year/inverter if single, raw RCD measurement points were considered. In practice, this number would be drastically reduced through the proper use of data windowing, averaging, or other simple data analysis techniques.

Finally, theoretical equations related to R_{iso} were derived for grounded and ungrounded arrays, which can be used to determine appropriate trip thresholds based on allowed fault power. Equations were also developed to allow the calculation of trip threshold without knowledge of the specific array topology. However, in this case, selection of the default R_{iso} value for leaky modules leads to potential safety issues if well-isolated modules are installed; while using well-isolated modules to select the default R_{iso} trip threshold leads to possible unwanted tripping issues in systems with leaky modules. Said another way, a default R_{iso} value cannot be determined for a given PV inverter because leaky systems will have unwanted tripping and highly isolated systems will not trip before a fire hazard.

Therefore, it is apparent that any *a priori* calculation of trip threshold cannot mitigate both fire risk and unwanted tripping issues for all possible arrays. Some system knowledge is necessary for the determination of trip points. In general, there is no *one-size-fits-all* solution and standards bodies may have to determine a *range of values* that can be set by array operators based on specific details of the array. Therefore, inverter manufacturers and testing organizations should allow for a range of R_{iso} thresholds that can be determined on a case-by-case basis, most likely as part of array commissioning.

Currently, there are major efforts underway to refine the industry-wide requirements for PV system ground fault protection in U.S. safety standards. The Underwriters Laboratories Standards Technical Panel (STP) for Underwriters Laboratories (UL) Standard 1741 (UL 1741) and UL 62109-2 are presently reviewing trip limit proposals for CSM/RCD and R_{iso} isolation monitors. The simulations, experiments, and theoretical questions presented here are being used by the UL Standards Technical Panel (STP) to justify considerably lower trip limits for PV system ground fault protection than had been required in the past. The updated requirements are being incorporated into UL 62109-2, which will likely be available in 2016. While it is difficult to balance the unwanted tripping with detection sensitivity, one thing is certain: PV systems will be far safer in the future.

Background:

PV ground faults are a shock hazard [1] and have caused many fires in the U.S. and around the world [2, 3]. In cases of faults on rooftop systems, the resulting fire can incinerate buildings and put the first responders and occupants' lives at risk. Further, publicity surrounding these fires is changing public perception of solar in harmful ways. The Solar American Board of Codes and Standards (Solar ABCs) steering committee investigated ground faults and the ground fault detection blind spot [4-6] in 2011-2013. The conclusion of this work was that fuse-based GFDI (Ground Fault Detector/Interrupter) designs were vulnerable to faults to the grounded current-carrying conductor (CCC).

A GFDI is unlikely to detect a fault on the grounded CCC, which could allow unrestricted fault current flow to bypass the GFDI if a second fault is initiated elsewhere in the array. This problem has caused multiple rooftop fires in the past [2, 3, 7]. A number of alternative ground fault technologies and methods were suggested [5], including isolation/insulation monitoring (R_{iso}) [8, 9], residual current detection (RCD) [10], and current sense monitoring/relays (CSM/R) [6], but there is little experience with these technologies in the U.S.

Project Objectives:

Solar PV systems long-term reliability, availability, predictability and control are important as systems continue to age and installed capacity continues to grow. The ability to automatically detect and mitigate ground faults is critical to broaden adoption of PV in the U.S. and ultimately lower the levelized cost of electricity by improving bankability of PV systems.

The ultimate goal of this project has been to advise UL and the International Electrotechnical Commission (IEC) on appropriate trip thresholds for new ground fault detector technologies entering the U.S. market (previously ~90% of PV systems utilized ground fault fusing solutions). Currently, inverter manufacturers and 3rd party providers of ground fault solutions use rudimentary calculations of possible leakage or fault current to select ground fault detection thresholds. In order to reduce unwanted tripping, these calculations are frequently conservative with insufficient knowledge of appropriate threshold overhead. There have been no comprehensive studies of these emerging technologies, so as manufacturers switch to the new technologies, there is a need to have updated recommendations and experimentally validated best practices for determining appropriate ground fault detector settings.

In FY14, Sandia analyzed baseline ground fault measurement values for healthy (unfaulted) systems using R_{iso} , RCD, and CSM technologies. In FY15, Sandia, DNV GL, and SunPower created faults on SunPower PV systems to determine how much headroom should be provided on the trip thresholds to maintain the maximum buffer for unwanted tripping while still detecting blind spot ground faults occurring to the grounded current-carrying conductor.

A number of alternatives to ground fault fuses have been identified, but there is limited historical use of these devices in the United States. This research was specifically focused on residual current detection (RCD), current sense relays/current sense monitors (CSR/CSM), and R_{iso} . RCDs operate by monitoring the differential current flow in the positive and CCCs. Any current imbalance between the two CCCs above a preset threshold is assumed to be caused by a ground fault and the RCD trips. In non-AC-isolated systems with transformerless inverters, the fault current is fed from the AC side of the system as well, so the RCD can be installed on the AC side of the inverter.

CSR/CSMs techniques detect ground faults by replacing the GFDI fuse with a current shunt resistor or monitoring the current through the GFDI fuse. This allows the inverter to disconnect from the DC system when there is a heightened current flow through the ground bond but before the fuse clears.

The adoption of a sensitive, reliable ground fault detection system will ensure improved safety, reduced fire risk and lower insurance rates for the PV industry. Detailed knowledge of R_{iso} , CSM, and RCD measurements during fault situations provided clear thresholding needs for each of the technologies. The findings were generalized using SPICE simulations and trip threshold recommendations were provided to UL 1741 to improve ground fault sensitivity in the U.S.

This research project determined the optimal thresholds for RCD, CSR, and R_{iso} measurements so that these technologies do not cause unwanted tripping from leakage currents while still being highly sensitive to high-impedance ground faults. Experimental measurements on multiple PV arrays were used to calibrate the Sandia SPICE model for various fault impedances and fault locations. Data collection was performed using the SunPower instruments and data logging equipment. Sandia created the test procedure and oversaw the execution of the utility-scale fault experiments. The experimental variables were be (a) the fault location, (b) fault impedance, and (c) PV system, i.e., PV array topology, inverter type, etc.

Project Results and Discussion:

A PV array ground fault is an electrical pathway between one or more of the array's conductors and earth ground. Such faults are usually the result of mechanical, electrical, or chemical degradation of PV components or mistakes made during installation. In order to protect the array against continued operation during a ground fault event, a ground fault protection device (GFPD) or Ground Fault Detector/Interrupter (GFDI) is used to detect ground fault currents [9].

Recently, a detection limit, or "blind spot", in traditional ground fault protection systems has been identified for the DC-grounded, AC-isolated PV systems, most common in the United States [10]. Historically, the ground-fault detection blind spot has caused many latent ground faults and ultimately resulted in several PV fires in North America. Latent ground faults can either be grounded conductor-to-ground faults (Figure 1) or high-impedance ground faults on

ungrounded conductors. The initial ground fault is generally not a fire hazard, but will remain latent because the fault current is too low to trip the inverter's GFDI fuse.

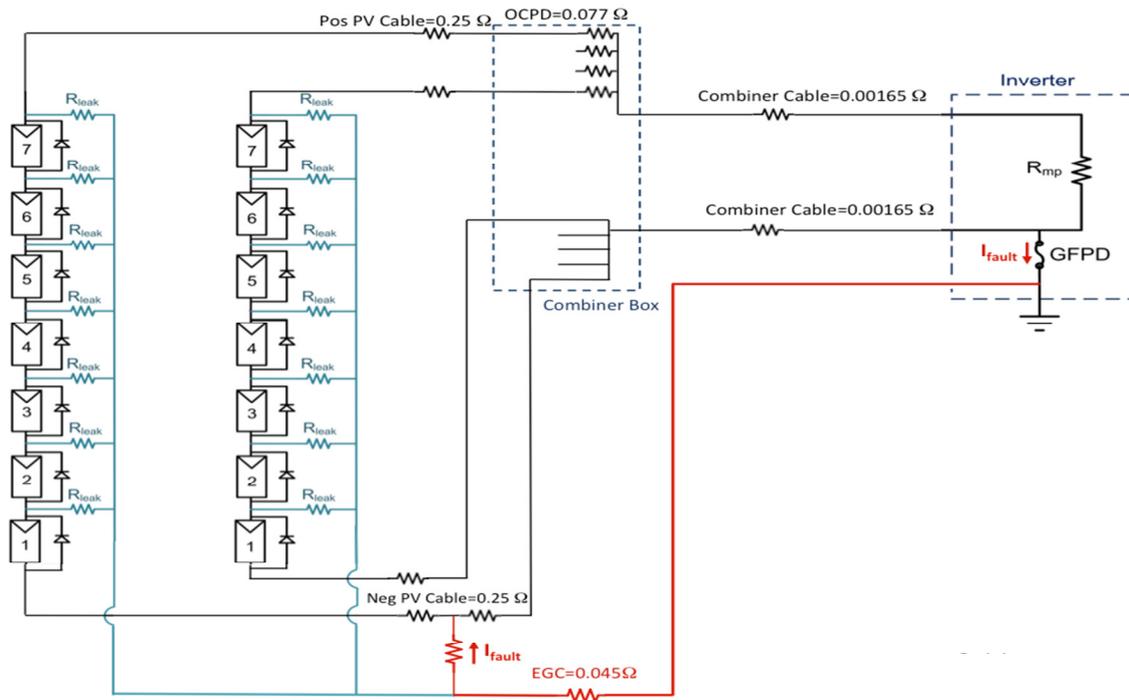


Figure 1: Schematic for an array with parasitic impedances measured from a fielded system and non-zero GFDP impedance. The teal line denotes the leakage current path. The path of the ground fault on the negative CCC is denoted in red.

In the event that a second ground fault occurs in the array, fault current, which may be very large, will bypass the GFDP, and the inverter's ground-fault protection system will not work as intended to prevent a fire.

Although the latent first fault may produce a small fault current that can go undetected by GFDPs, the danger of undetected ground faults in the Equipment ground conductor (EGC) is twofold:

- (1) an energized EGC can be a shock hazard, resulting in severe injury
- (2) if there is a second ground fault in parallel, the array can be shorted through the EGC, bypassing the GFDP and allowing fault current to flow through the system undetected and with no means of interruption resulting in damage to the array (Figure 2).

The historical fire events presented in [10] have highlighted the incomplete protection provided by ground fault fuses in grounded arrays in the United States. Field experiments have confirmed the existence of the ground fault blind spot [11]. Note that in ungrounded, non-isolated, and hybrid systems, the ground fault blind spot does not exist.

PV Fault Modeling

PV modules are non-linear circuits. Their behavior is difficult to describe analytically without transcendental equations. However, the use of computer circuit simulation tools can describe the behavior of a PV system for a wide variety of fault conditions [12]. A common method of circuit simulation is the use of the SPICE. SPICE, originally developed at the University of California, Berkeley Electronics Research Laboratory in 1973 [13], is a general-purpose, open source,



Figure 2: A blind spot in a listed inverter's fuse-based ground-fault protection scheme resulted in this damage.

analog circuit simulator used to predict circuit behavior. In order to understand the behavior of an array under a wide variety of different electrical fault conditions as well as analyze the detection thresholds of different GFDI technologies, a PV array circuit simulation tool was created. Details of the model and a description of the array under various faulted and unfaulted conditions are described at length in [14].

In order to validate the SPICE model, a number of the simulated fault types [15] were compared to field experimental studies performed at the Distributed Energy Technologies Laboratory (DETL) at Sandia National Laboratories using a set of power resistors as a fault pathway in an array connected to either an inverter or a variable load bank surrogate set to the maximum power point (MPP) of the unfaulted array.

The real PV arrays at DETL are composed of two parallel strings of seven 200 W monocrystalline Si modules connected in series. In each experiment, the fault is installed between modules using MC4 T-branch connectors. The fault and array current and voltage are collected with a Tektronix DPO3014 oscilloscope, two Tektronix P5200 differential voltage probes, and two Tektronix TCP303 current probes.

To calibrate the SPICE model to the unfaulted array and validate the model for the faulted array, IV curves were taken of the array using a Daystar, Inc DS-100C IV curve tracer. After input of the unfaulted single diode module parameters (I_{sc} , R_s , R_{sh} , N , and I_{leak}) [16] to correctly replicate the IV curve, the SPICE model closely predicts the IV curve for both 5.1 and 3.2 Ω cases, listed as 2+ to 1- (N^+ indicates the positive terminal of the N^{th} module from the grounded conductor) in Figure 3.

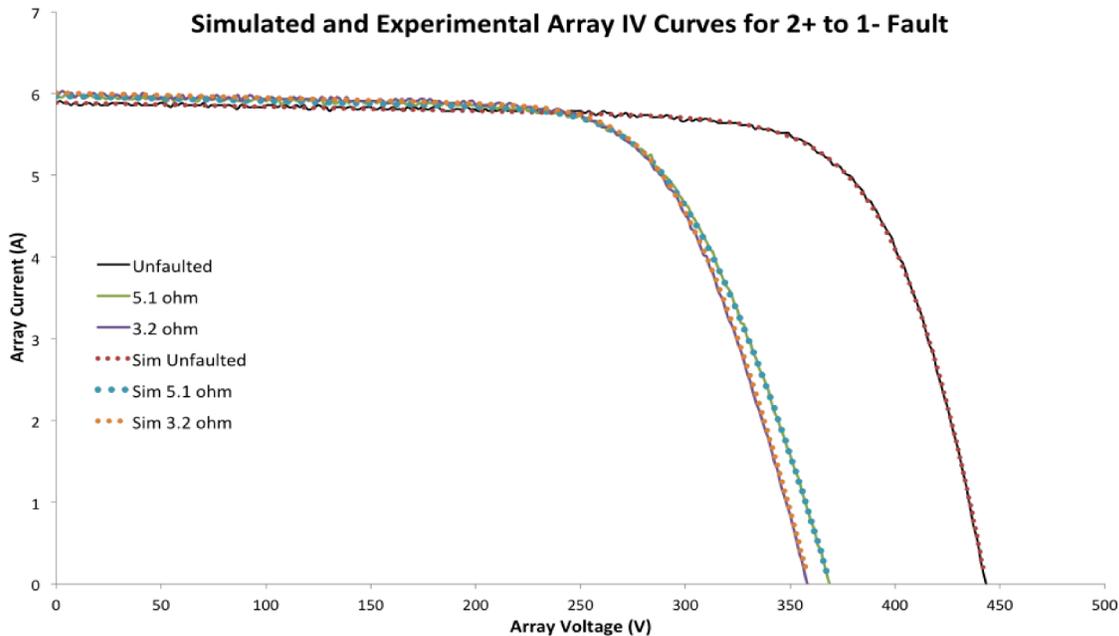


Figure 3: Experimental IV curves of faulted and unfaulted states (solid lines) overlaid with SPICE simulations (dots) for different resistance ground faults.

To validate the SPICE model without any complicating behavior from an operational inverter, the DETL PV array was connected to a load bank with impedance (55.6Ω) approximately equal to the array MPP. Resistive faults of 3.2, 5.1, 10.5, and 22.4Ω were established for a variety of different fault types. Only ground faults are in the scope of this work, although the full collection of ground, intra-string, inter-string, series, and arc faults is included in [17].

Figure 4 shows the results of experimental ground fault tests of the PV array using power resistors as the array load as well as the ground fault pathway. The dashed lines indicate the different resistances (3.2, 5.1, 10.5, and 22.4Ω) used for the faults. The figure shows excellent correlation between the simulated fault current/voltage and that measured experimentally.

The SPICE simulations match the experimental data points well (<5% error) for all fault conditions studied. Similar matching results were obtained for fault types other than ground faults as well. However, as more modules are faulted, the SPICE simulations slightly underpredict both the fault current and fault voltage. This error can be due to differences in the fault resistance between the values used in simulation and the actual resistors, a slight mismatch in the series resistance of the module model, or parasitic resistances due to PV wiring and interconnects.

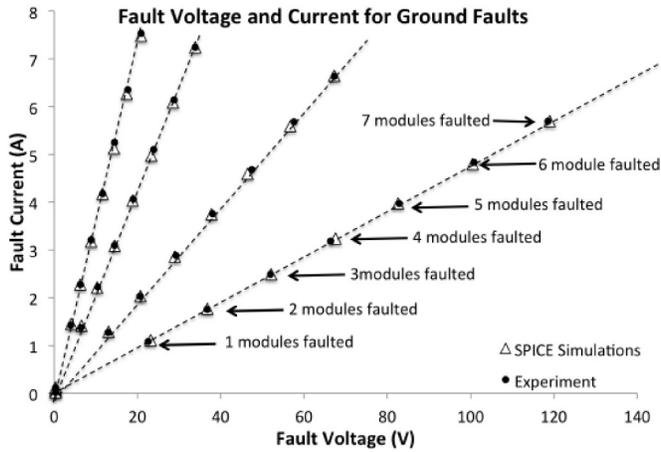


Figure 4: Fault voltage/current for resistive ground faults.

In order to test if the SPICE simulations could accurately predict inverter operation under fault conditions, the array was connected to a 5.0 kW inverter without arc-fault protection. A 5.1 Ω ground fault was created. The inverter impedance was measured during inverter operation and used for the SPICE simulations. Figure 5 shows the measured data before, during (0-143 s), and after the fault. The results of the SPICE simulation are denoted by black lines. As can be seen from Figure 5, the SPICE simulations match all the measured values well and can completely describe both array and inverter behavior before, during, and after the fault.

Since this fault only bypassed a single module, the inverter attempts to maximum power point track (MPPT) throughout duration of the fault (inverter behavior varies with the impedance of the fault as well as the number of modules faulted to ground [17]). Before the fault, the inverter impedance is 49 Ω, which corresponds to $R_{mp-unfaulted}$. When the fault occurs at $t=0$, the inverter “immediately” changes its impedance to 67 Ω in order to hold the array voltage constant (the change is not immediate; however the time step in the experiment is too large to see the voltage transient. After the fault initiation, the inverter impedance tracks slightly in the incorrect direction (it increases linearly from 67 Ω to 78.6 Ω for 4.4 seconds) before the MPPT algorithm begins to decrease the inverter impedance towards $MPP_{faulted}$ ($R_{mp-faulted}=45.83$ Ω).

The MPPT algorithm holds the value of R_{load} relatively steady at $R_{mp-faulted}$ until the fault is cleared at 143 seconds. The inverter then “immediately” decreases its impedance to 41.7 Ω in order to keep the array voltage constant before the MPPT algorithm increases the inverter impedance to $R_{mp-unfaulted}$.

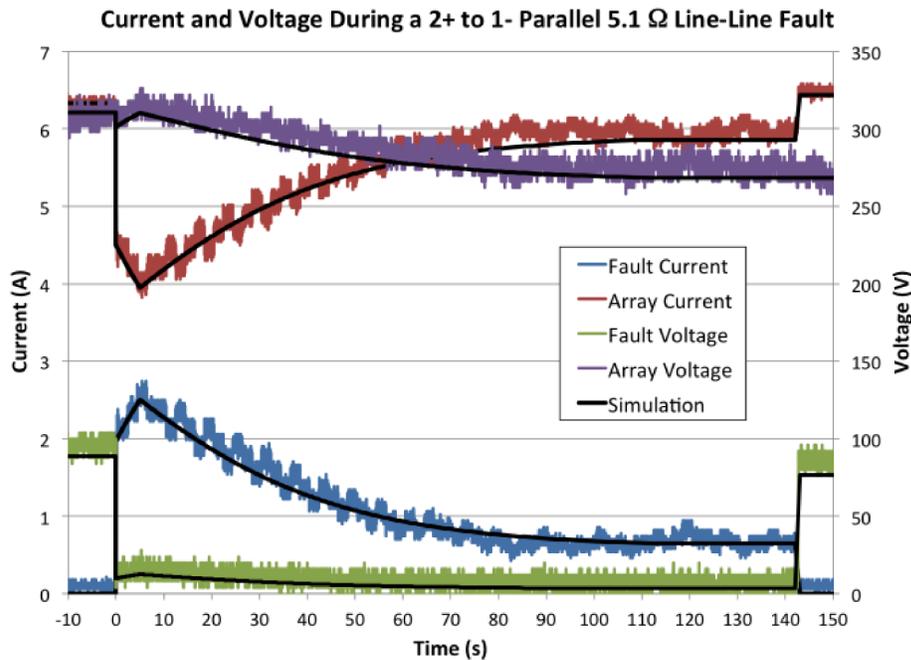


Figure 5: Array and fault current vs. time for an arcing ground fault connected to an inverter. The black lines show expected fault and array currents from the SPICE model.

With a fully functional and validated SPICE model, different mitigation methods for a wide variety of GFDI solutions are investigated. The solutions investigated are based on the recommendations of the SolarABCs steering committee, which first studied ground faults and the ground fault detection blind spot and identified a number of alternative technologies to eliminate this blind spot. These solutions include

1. Replacing the rated fuse with a lower rating
2. Isolation monitoring (Riso)
3. Residual current detection (RCD)
4. Current sense monitoring/relay (CSM/R)

Using the SPICE models developed previously as well as historical data from the field, each of these methods are discussed along with the basis for proper thresholding techniques in order to minimize both the number of unwanted tripping events as well as the undetectable area of each GFDI solution.

Fuse-based GFDI

In general, due to the non-linear nature of PV modules, the fault current for a fault located somewhere mid-string does not have a non-transcendental solution. However, when the fault exists at either of the CCCs, the fault acts as a current divider and an analytical solution is possible. In the following section, an analytical solution for the fault current for a fault located at the grounded CCC (a classic blind spot fault scenario) is briefly presented (a full derivation is

described at length in [18]). This analytical solution is corroborated by the validated SPICE simulations described earlier and used to determine the efficacy of replacing the listed fuse rating with a more sensitive type in order to close the ground fault blind spot.

To model current flow during a ground fault, the internal resistances of the conductors and the GFPD must be included because the current division between the fault path and the intended conduction path is heavily dependent on small internal resistances of the conductors.

UL 1741 mandates the maximum sizing of these protection devices based on the array size [19]. It is, possible to install a lower rated fuse than mandated by UL1741, although replacing the fuse may invalidate the inverter’s nationally recognized testing laboratory (NRTL) listing. In the ideal case, fuse ratings could be decreased freely without affecting the GFPD current, However, in reality, fuse impedance changes with fuse ampere rating and thus has an effect on the fault current. Figure 7 shows a graph of fuse resistance vs. fuse rating for a number of 10x38mm style fuses for a variety of manufacturers.

The resistance of the fuse is inversely related to the fuse rating, so fuses with low trip ratings can have significant resistances. For example, the 0.1A Littelfuse KLKD fuse has a resistance of 85.5 Ω . Such large resistances have significant effects on the GFPD current and fuse resistance must be balanced with fuse trip point in order to maximize GFPD fault detection capabilities.

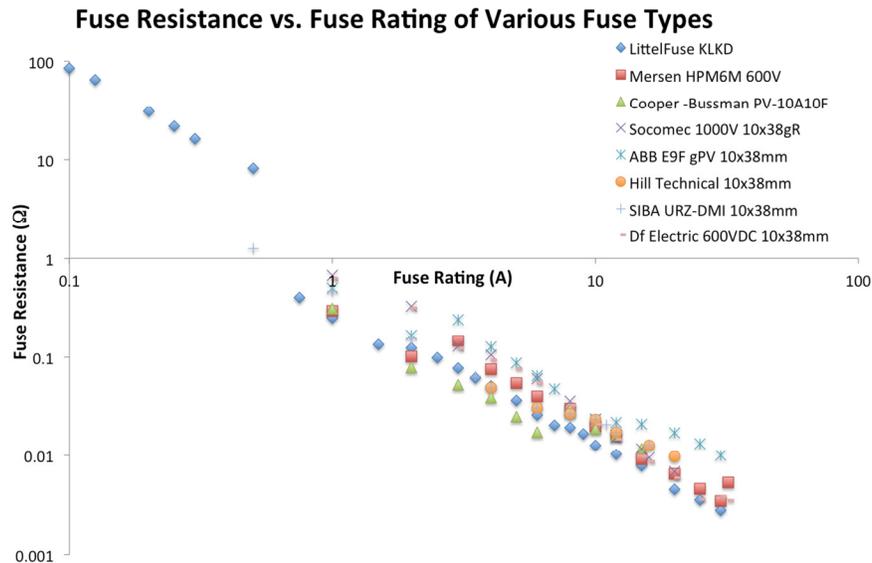


Figure 6: GFPD resistance vs. rating for a variety of 10x38 mm (“midget”) fuses by various PV fuse manufacturers. In general, the more sensitive the fuse, the higher the intrinsic resistance [1-8].

This GFPD impedance means that the grounded CCC (typically the negative conductor) is no longer at ground potential, but instead *functionally* grounded by the fuse. When a fuse with

internal resistance is included in the model of a PV system, the conductor is at a voltage above ground potential, which introduces the possibility of ground faults from the grounded CCC through the EGC.

The circuit diagram in Figure 7 shows the current paths for a single string providing a current (I) that has a fault in the grounded CCC at some point in the PV cabling. The fault bisects the PV cable at some arbitrary point and acts as current divider with part of the current (I_{GFDP}) flowing through the GFDI and the remainder ($I - I_{GFDP}$) flowing through the CCC as normal. R_x denotes the resistance of the PV cabling included in the loop parallel to the GFDI current, while R_y denotes the portion of PV cabling resistance that is not included in the fault loop. The sum of R_x and R_y is equal to R_{PV} and the ratio of the two resistances is equal to the percentage of PV cabling that is faulted.

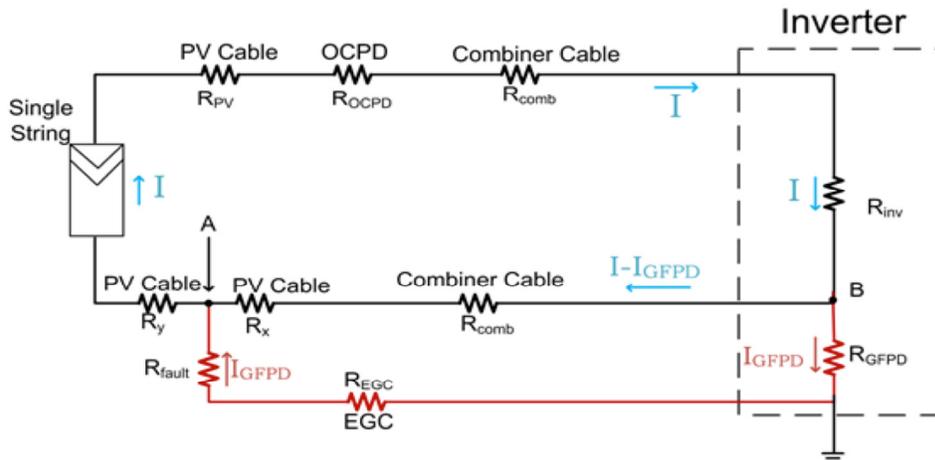


Figure 7: Circuit diagram of negative CCC fault with a single string at an arbitrary point in the negative PV cabling. The ratio of R_x and R_y indicates the percentage of PV cabling faulted. Resistances and currents used in Kirchoff's Voltage Law equations are shown.

By Kirchoff's Current and Voltage Laws (KCL) and Ohm's Law, the voltage drop between A and B can be written as:

$$\Delta V_{A,B} = I_{GFDP} \cdot (R_{GFDP} + R_{EGC} + R_{fault}) = (I - I_{GFDP}) \cdot (R_{comb} + R_x) \quad (1)$$

By distributing and refactoring in terms of I and I_{GFDP} and solving for I_{GFDP} , Eq. (1) can be written as:

$$I_{GFDP} = \frac{I \cdot (R_{comb} + R_x)}{R_{GFDP} + R_{EGC} + R_{comb} + R_x} \quad (2)$$

The ground fault on the grounded CCC is a minor perturbation from normal operating conditions of the array. Therefore, the operating points of the modules on the I-V curve are nearly unaltered during a negative CCC ground fault. Therefore:

$$I = I_{mp} \quad (3)$$

and,

$$I_{GFPD} = \frac{I_{mp} \cdot (R_{comb} + R_x)}{(R_{GFPD} + R_{EGC} + R_{fault} + R_{comb} + R_x)} \quad (4)$$

This same procedure can be generalized to apply for a much more complicated array picture than is presented in Figure 7 [18]. For an array with recombiner boxes, each having D parallel combiner boxes composed of C parallel strings per combiner box and supplying current (I) to a load (Figure 8). It is assumed that (C-1) parallel strings are unfaulted and source current equal to I_2 and that all strings have a leakage to the EGC equal to I_{leak} .

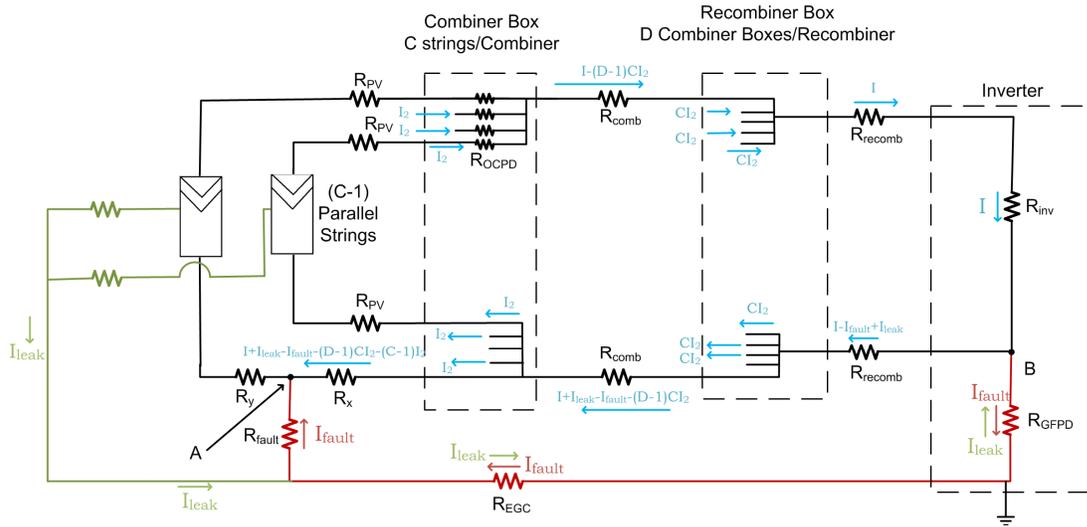


Figure 8: Circuit diagram of grounded CCC fault of an array with leakage current and combiner and recombiner boxes. Resistances and currents used in KVL/KCL equations are shown.

The KVL analysis of the circuit between points A and B can be described by:

$$\begin{aligned} & (I + I_{leak} - I_{fault}) \cdot R_{recomb} + (I + I_{leak} - I_{fault} - (D-1)CI_2) \cdot R_{comb} + (I + I_{leak} - I_{fault} - (D-1) \cdot C \cdot I_2 - (C-1) \cdot I_2) \cdot R_x \\ & = (I_{fault} - I_{leak}) \cdot R_{GFPD} + (I_{fault} - I_{leak}) \cdot R_{EGC} + I_{fault} \cdot R_{fault} \end{aligned} \quad (5)$$

As before, the modules are at maximum power so they can be described by:

$$\begin{aligned} I &= D \cdot C \cdot I_{mp} \\ I_2 &= I_{mp} \end{aligned} \quad (6)$$

So, by inserting Eq. (6) into Eq. (5) and solving for I_{fault} , the fault current can be described by:

$$I_{fault} = \frac{I_{mp} \cdot (D \cdot C \cdot R_{recomb} + C \cdot R_{comb} + R_x) + I_{leak} \cdot (R_{recomb} + R_{comb} + R_x + R_{GFPD} + R_{EGC})}{(R_{GFPD} + R_{EGC} + R_{fault} + R_{recomb} + R_{comb} + R_x)} \quad (7)$$

The GFPD current is the difference in the fault and leakage currents (by convention, I_{fault} is taken to be negative), so I_{fault} can be transformed into I_{GFPD} by:

$$I_{\text{GFPD}} = I_{\text{leak}} - I_{\text{fault}} \quad (8)$$

Finally, Eq. (7) can be solved in terms of I_{GFPD} by substituting Eq. (8):

$$I_{\text{fault}} = I_{\text{leak}} - \frac{I_{\text{mp}} \cdot (D \cdot C \cdot R_{\text{recomb}} + C \cdot R_{\text{comb}} + R_x) + I_{\text{leak}} \cdot (R_{\text{recomb}} + R_{\text{comb}} + R_x + R_{\text{GFPD}} + R_{\text{EGC}})}{(R_{\text{GFPD}} + R_{\text{EGC}} + R_{\text{fault}} + R_{\text{recomb}} + R_{\text{comb}} + R_x)} \quad (9)$$

In simulations, the recombiner topology has not been used ($D=1$, $R_{\text{recomb}}=0 \Omega$), so the equation for I_{GFPD} shown as Eq. (9) becomes:

$$I_{\text{GFPD}} = I_{\text{leak}} - \frac{I_{\text{mp}} \cdot (C \cdot R_{\text{comb}} + R_x) + I_{\text{leak}} \cdot (R_{\text{comb}} + R_x + R_{\text{GFPD}} + R_{\text{EGC}})}{(R_{\text{GFPD}} + R_{\text{EGC}} + R_{\text{fault}} + R_{\text{comb}} + R_x)} \quad (10)$$

A SPICE model was created with the internal resistance of the conductors and GFPD fusing as shown in Figure 7 in order to investigate ground faults involving the negative CCC. Arrays were simulated with each DC home run cable from the PV to the combiner box totaling 0.25Ω (~80 feet of coated copper 12 American wire gauge cabling at $3.125 \text{ m}\Omega/\text{ft}$) the fault located midway on the cable ($R_x=R_y$). Prior to each string being combined, the positive DC cable is connected to an overcurrent protection device with 0.077Ω resistance (4 A KLKD Littelfuse [2] rated for $1.56 \cdot I_{\text{sc}}$). The combiner box is connected to the inverter through cabling with an impedance of 0.00165Ω (~50 feet of coated copper 400 circular mil (cabling at $0.033 \text{ m}\Omega/\text{foot}$). The ground fault is modeled by a resistor connected from the negative CCC to ground through the 0.041Ω EGC (determined from field measurements [11]). The value of the inverter resistor is set to the MPP of the unfaulted array. The negative inverter connection is connected to ground through the fuse.

To investigate the effect of fuse resistance on fault current, simulations were carried out for fuse resistances of 85.5, 22, 8.16, 0.252, 0.124, and 0.0363Ω (Littelfuse KLKD resistances for 0.1, 0.25, 0.5, 1, 2, and 5 A fuses [2], respectively) with fault resistances of 0.1, 1, and 25Ω . Figure 9 shows the results of the simulations for 1, 2, and 5 A GFPD fuses and fault resistances of 0.1 and 1Ω . Simulations with a 1 A (0.252Ω), 2 A (0.125Ω), and 5 A (0.0363Ω) are shown as red, purple, and orange points, respectively. Triangles indicate a fault resistance of 0.1Ω while circles represent a 1Ω resistance. Solid lines at 1, 2, and 5 A denote the fuse ratings with color corresponding to the fuse trip point. The GFPD current calculated by Eq. (9) is denoted by a dashed line for each set of fuse and fault resistances.

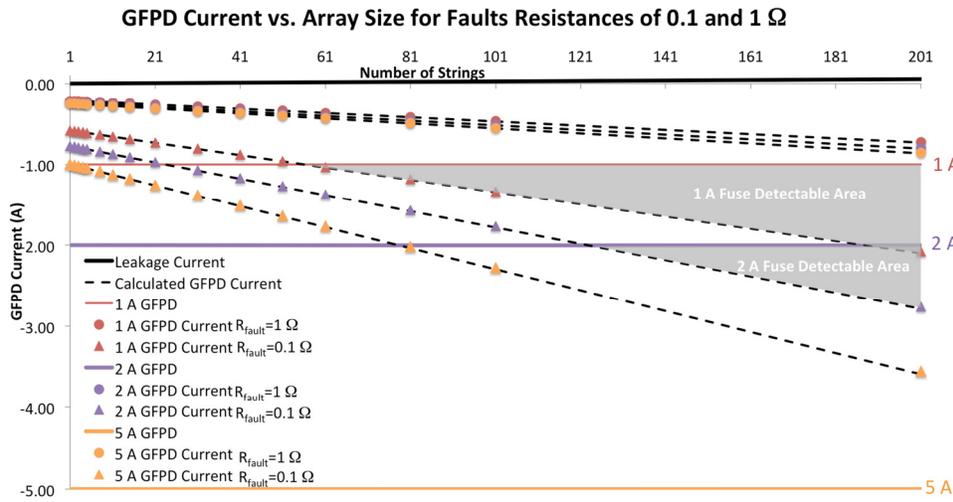


Figure 9: Graph of GFPD current vs. array size for various GFPD and fault resistances. The color of the line indicates GFPD resistance. Red traces denote 1 A (0.252 Ω), while purple and orange traces denote 2 A (0.124 Ω), and 5 A (0.0363 Ω), respectively. Only the 1 A and 2 A fuses are sensitive enough to trip due to the blind spot fault. The region where I_{GFPD} is larger than the trip point is colored in gray.

The GFPD current is linear with number of strings for all fuse ratings and fault resistances. Also, for all arrays up to 201 strings, only the 1 A and 2 A GFPDs (at fault resistance of 0.1 Ω) provide enough GFPD current to trip the fuse (shaded regions denote where $I_{\text{GFPD}} > I_{\text{trip}}$). The 1 A GFPD only detects the ground fault in arrays larger than 56 strings while the 2 A GFPD detects faults in arrays larger than 124 strings. The orange traces do not reach 5 A even for 201 strings, so a 5 A GFPD would never trip for a blind spot ground fault.

It is tempting to believe that decreasing the fuse rating will increase the number of detectable blind spot faults. However, the decrease in trip point is more than offset by the increase GFPD resistance, so fuses with low ratings will detect fewer blind spots. Figure 10 shows the simulation results for 0.1 (green), 0.25 (purple), and 0.5 A (blue) GFPD fuse ratings at R_{fault} of 0.1 and 1 Ω . In each case, due to the increase in fuse resistance, the GFPD current is far too small to trip the fuses.

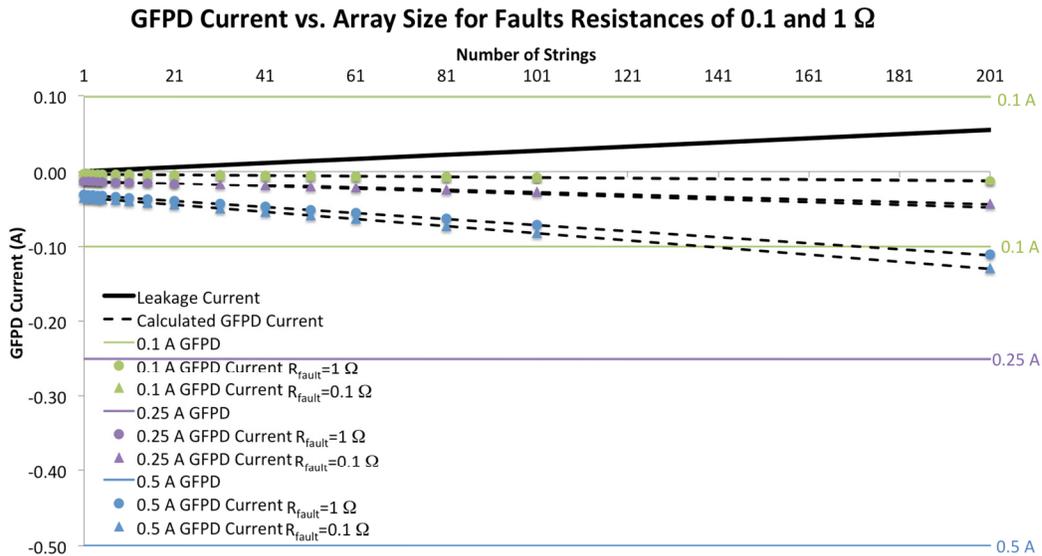


Figure 10: Graph of GFPD current vs. array size for various GFPD and fault resistances. The color of the line indicates GFPD resistance. Green traces denote 0.1 A (85.5 Ω), while purple and blue traces denote 0.25 A (22 Ω), and 0.5 A (8.16 Ω), respectively. Even though the fuses have low trip points, due to the increased fuse resistance, the GFPD current is below the fuse trip point and the blind spot window is increased.

Of the fuse sizes studied (0.1, 0.25, 0.5, 1, 2, and 5 A), only the 1 A and 2 A fuses (at $R_{\text{fault}}=0.1 \Omega$) have the combination of low trip point and low resistance needed to detect the blind spot fault for large array sizes (above 56 and 124 strings, respectively). While, logically, it may be tempting to reduce blind spot faults by decreasing fuse rating, this actually increases the blind spot due to increased fuse resistance. To truly limit the size of the blind spot, fuse rating and fuse resistance must both be considered and optimized and simply replacing one fuse with a lower rated one may actually increase the detection blind spot. Therefore, decreasing the fuse size is not an appropriate solution to the ground fault blind spot and other GFDI devices are necessary.

Residual Current Detection/ Current Sense Monitoring

RCDs and CSMs are included in this section together since they both operate on the principle of detection of stray current flows in the presence of a fault condition. CSMs operate by monitoring (via a current transformer) the current flow through the ground bond. Excessive current flow through the ground bond is assumed to be caused by a ground fault (not array and BOS component leakage) and, if the measured current is above a pre-set threshold, the CSM trips. RCDs operate by monitoring the differential current flow in the positive and negative CCCs. Any current imbalance between the two CCCs above a preset threshold is assumed to be caused by a ground fault and the RCD trips. In non-AC-isolated systems with transformerless inverters, the fault current is fed from the AC side of the system as well, so the RCD can be installed on the AC side of the inverter. Figure 11 shows a circuit schematic detailing the different installation positions of RCD and CSM devices.

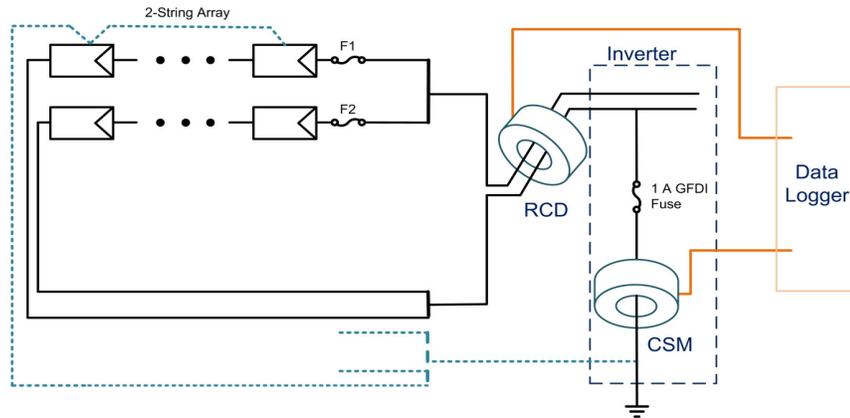


Figure 11: RCD vs. CSM measurements on a PV array.

For both RCD and CSM, the trip threshold is freely selectable and, in either configuration does not modify the conductive pathway being monitored (both CCCs for RCD and between the grounded bus and ground for CSM). Rather, both solutions inductively measure current in the monitored pathway. This approach maintains the inverter certification listing even after retrofit by ensuring that the manufacturer's factory installed ground fault protection system functions exactly as originally evaluated by a Nationally Recognized Testing Laboratory.

The range of detectable ground faults for these solutions depends on the threshold used to define the presence of a fault. If this trip threshold is too low, there will be nuisance trip events resulting from module and BOS component leakage currents; but if the threshold is too high, higher impedance ground faults will go undetected. Both RCD and CSM methods could register array leakage current as a type of fault, therefore the generalized detection threshold must be set above the maximum leakage current in all unfaulted operating conditions (meteorological, topological, and electrical) in the ground fault detector certification standards, e.g. UL 1741 and IEC 62109-2 [19, 20].

Sandia National Labs has worked with a large, utility-scale PV operator to collect the system leakage values of 340 500 kW co-located inverters in a desert environment [21]. The system leakages for each inverter were measured at one-minute intervals for over a year (1 January 2013 to 3 August 2014) using RCDs. In compliance with UL 1741, each inverter has a GFDI fuse rated at 5 A to protect against ground faults. This conservative threshold was chosen to maximize the detection of ground faults while eliminating unwanted tripping events due to electromagnetic interference (EMI), module/inverter leakage, and meteorological events (i.e. lightning).

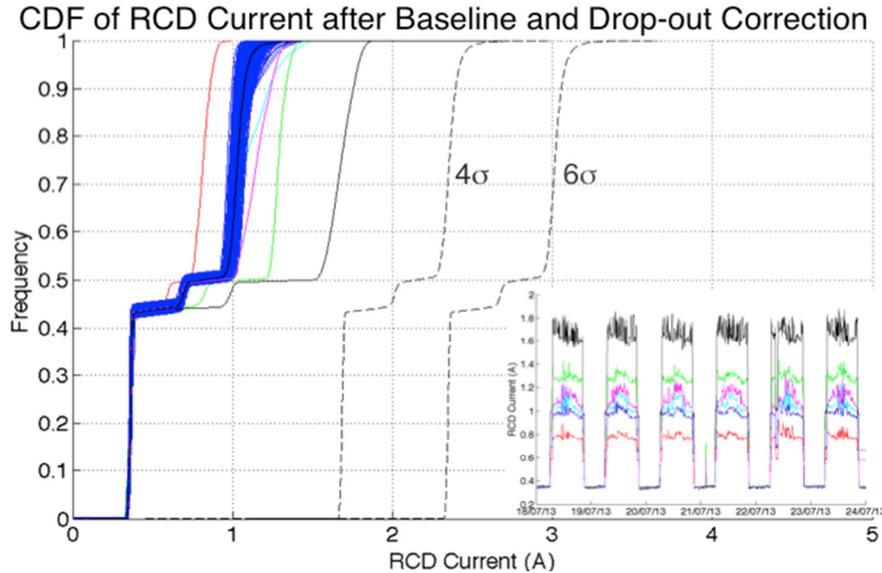


Figure 12: CDFs corrected for baseline and data dropouts. Most of the CDFs are clustered together with a few outlier inverters with higher or lower leakages (shown in inset). Assuming a normal distribution, the $+4\sigma$ and $+6\sigma$ limits of the average CDF are shown as black dashed lines.

Figure 12 shows the cumulative distribution functions (CDFs), corrected for baseline deviations and data dropouts of all 340 RCDs for one year [21]. For a given CDF curve, a shift to the right indicates higher leakages in the inverter possibly due to an incorrect baseline value or a high impedance ground fault. If the effects of data reliability is corrected (which can be done via simple, on-board programming), such as baselining the inverter leakage each night when the inverter is disconnected and eliminating repeated data due to drop-outs, the CDFs of all 340 inverters are surprisingly tightly distributed. All but five of the 340 inverters (colored in blue in Figure 12) lie within a range of 1.14–1.51 A at 99.99% frequency. The five inverters that act as outliers (CDFs are different colors) demonstrate either higher lower leakage values than average. The RCD values over a six-day period of these outlier inverters along with a “typical inverter” (blue) are shown in the inset.

The inverters corresponding to the magenta, green, and black curves show higher measured leakage values during the day while the red curve corresponds to a lower measured leakage value. It should be noted that, although the baseline for each inverter is the same, the turn-off/turn-on shoulder values scale with the daytime leakage of the inverter, indicating that the increased or decreased RCD current may be due to a proportionality (gain) problem in the RCD rather than an actual increase of leakage in the inverter.

The 4σ and 6σ confidence bands of the average CDF of all the inverters (both “normal” and the five outlier inverters) is shown as dashed black lines in Figure 12. Note that these curves represent RCD values that are exceeding rare given the data population: $\Pr(x \geq \mu + 4\sigma) = 0.00317\%$ and $\Pr(x \geq \mu + 6\sigma) = 9.87 \cdot 10^{-8}\%$. These statistical metrics can be used to establish thresholding rules based on the requirements of the inverter manufacturer, O&M company, plant owner, or standards-making panel. For example, there is a 4σ confidence that 99.999% of

measured leakage values are below 3.1994 A and a 6σ confidence that 99.999% of the RCD values are below 3.8616 A (Table I). A set point of 5 A (as currently mandated by UL 1741) corresponds to an eight-9s confidence of the 4σ confidence band.

For the inverter model at this location, the RCD thresholds could be reduced to improve high impedance ground fault sensitivity without additional unwanted tripping events. For the inverters in this installation, the RCD trip point could be lowered from 5 A to as low as 2.5 A with six 9's confidence that any unfaulted RCD current measurement would be lower than the ground fault setpoint. Statistically, this would correspond to 0.5 trips/inverter/year if single, raw 1-minute RCD data were considered. In practice, this number could be reduced even further through more advanced data analysis techniques, such as the proper use of data windowing, averaging, data error correction, or step change analysis.

Table I: High frequency values of the CDFs for the average of all inverters as well as the 4σ and 6σ confidence bands.

Frequency (%)	Average	4σ	6σ
99	1.1825	2.5067	3.1688
99.9	1.6437	2.9679	3.6300
99.99	1.8028	3.1270	3.7892
99.999	1.8752	3.1994	3.8616
99.9999	2.4891	3.8133	4.4754
99.99999	2.8759	4.2001	4.8623
99.999999	3.6827	5.0069	5.6690

In addition to working with array operators, since 2013, Sandia National Laboratories has worked with a major EPC firm to extensively install alternatives to fuse-based GFIDs throughout its fleet of PV systems on commercial rooftop systems [22]. A balance of accuracy, cost, and serviceability led the EPC to decide to install string-level inverters equipped with isolation monitor and RCD technologies on new systems and to retrofit central inverters with CSM devices. Currently, the EPC has retrofitted 331 central inverters, representing 109 MW of inverter capacity, with the CSM technology at an aggressive ground fault trip setting of 100 mA.

Figure 13, reports two days of measured CSM current values for nine healthy PV systems and one system which develops a ground fault. These data were collected from systems deployed using three different manufacturers' inverters—all of which were in the 250 kW to 500 kW capacity range—and three different manufacturers' modules. The measured current values for the healthy systems range from 5 mA, the lower limit for the installed CSM kit, to about 50 mA. Though these measured values include current contributed by the entire dc system, the magnitude of healthy daytime CSM values is largely dependent on the ground current from the inverter.

As illustrated by the black dots in Figure 13, Sandia's SPICE simulation tool can be used to model the fault current for this system and determine proper alarm thresholds for arrays as well as understand array behavior based on a wide variety of fault locations and impedances.

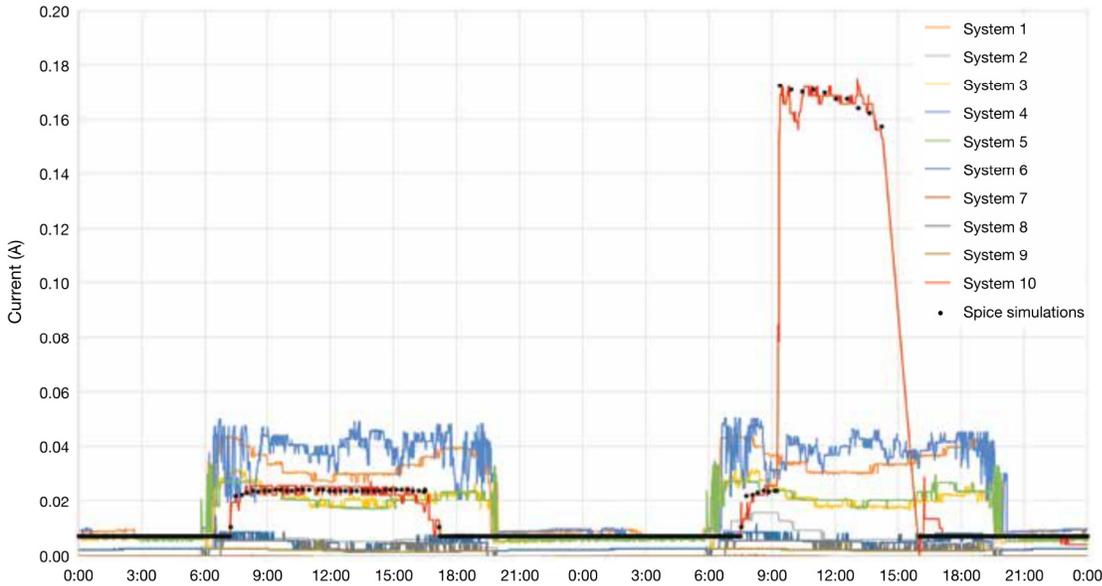


Figure 13: CSM data for 10 different PV systems, one of which (in red) developed a ground fault with a magnitude of approximately 170 mA. The black dots show the results from Sandia’s SPICE model for the ground fault.

Table I summarizes the EPC firm’s experience before and after it implemented CSM equipment on commercial rooftops. Prior to deploying CSM solutions, the EPC experienced nine thermal events in systems protected by traditional fuse-based GFDIs. These fires occurred over a 6-year period and resulted in a range of damage. In the 3 years since the wide-scale rollout of advanced ground fault solutions, the EPC has not experienced a single fire incident in systems protected by one of these solutions. In that same period of time, central inverters equipped with CSM equipment have detected a total of 20 ground faults across the EPC’s fleet which its service personnel were able to identify and repair. Many of these incidents were dangerous, high impedance faults to conductors with low potential to ground that would have persisted indefinitely were fuse-based GFDIs the only fault detection method utilized.

Table I: After retrofitting central inverters on commercial roof-mounted systems with CSM equipment, a major EPC firm was able to increase the detection of latent ground faults and eliminate fire events across its fleet.

	Fuse-based GFDI (6 years)	Post-CSM retrofit (3 years)
Ground-fault detections	--	20
Nuisance Trips	--	9
Fires	9	0

RCD and CSM measurements, especially in the sub-second time period, show that inverter-to-ground leakage component account for a large portion of the overall system leakage when the PV system is exporting power [23]. The exact magnitude and waveform of this inverter-to-ground leakage can vary widely from manufacturer to manufacturer (Figure 14).

CSM leakage data collected at 10 kHz for 0.1 seconds with Tektronix TCP303 current probes is shown in Figure 14 for six residential PV inverters. The CSM measurements are subject to significant inverter switching noise, shown in, which make accurate measurements of the steady-state ground bond current difficult. Interestingly, the noise characteristics from two identical 3 kW inverters (same make/model) with two identical 2.4 kW arrays (two strings of six 200 W mono-Si modules) can produce visually different switching noise—although the RMS current and the mean current were within 4 mA of each other.

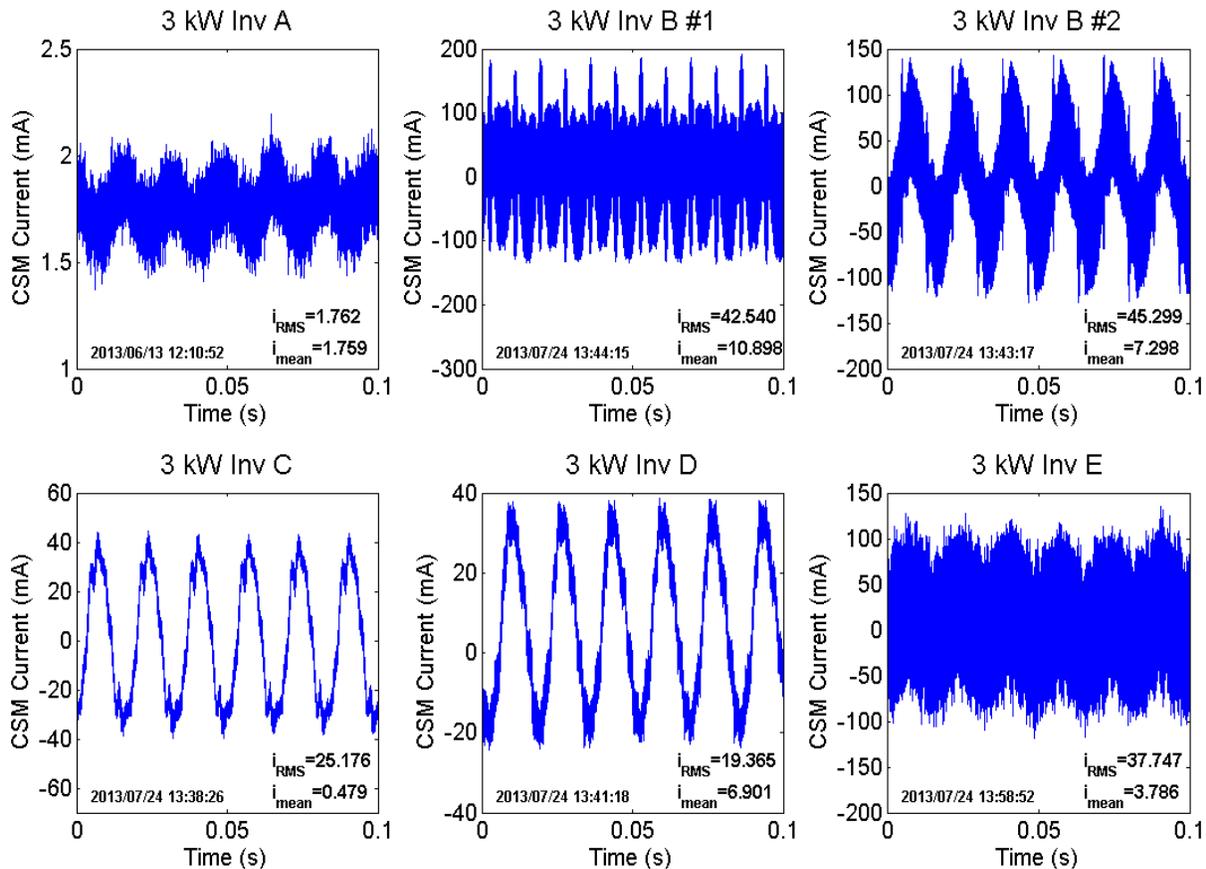


Figure 14: CSM noise from inverter switching.

Although SPICE simulations can successfully predict average leakage and fault current values via CSM, such as those shown in Figure 13, it cannot describe the complicated current waveforms on the ground bond due to inverter switching schemes, which can lead to nuisance tripping events (nine events are identified in Table I). In conjunction with the EPC, the nuisance trip events in their fleet were analyzed and four separate causes of nuisance tripping (thunderstorm events, noise on the ground bond, ac disturbances, and faulty equipment) were identified. The nine nuisance events primarily occurred early in the learning curve with the CSM

equipment, while the EPC was still actively using averaging techniques to investigate proper threshold values.

Lightning and spurious measurements were the primary causes of these unwanted trip events. The EPC was eventually able to eliminate these unwanted trips, a significant source of nuisance trip events, by increasing the CSM unit's trip delay setting from 1 second to 3 seconds, which allows for quick transient currents to pass through the ground bond without tripping the unit. After identifying excessive noise on the ground bond as the cause of unwanted trips at one site, the EPC resolved the problem by using a shielded Current transformer (CT) in place of the standard version. We attribute the remaining unwanted trip events to disturbances on the ac grid and one faulty CSM CT. Since the occurrence frequency of these events is so low, the EPC has yet to implement solutions to these causes.

Isolation Monitoring

In its simplest form (i.e. neglecting array capacitance and noise sources) R_{iso} measurements are carried out on ungrounded systems (or grounded systems which are temporary disconnected from earth ground) by injection of a voltage pulse into one of the two CCCs of the PV system by an external power source. The ground isolation can then be calculated from the current draw on the power source, represented in Eq.(11). If the isolation is measured to be below a certain threshold, the isolation monitor trips.

$$R_{iso} = \frac{V_{applied}}{I(V_{applied}) - I(V_{applied} = 0)} \quad (11)$$

This process is carried out with both positive and negative polarity pulses on one or both CCCs. The pulse polarity and CCC should not affect the measurement of the fault as long as there is sufficient illumination to forward bias the module photodiodes. In low illumination conditions, the pulse will travel through the bypass diodes. One pulse polarity will pass through the bypass diodes and measure the fault, as long as the pulse magnitude ($V_{applied}$) is large enough to overcome the voltage drop of the multiple bypass diodes in the array. The opposite pulse polarity will be blocked by the bypass diodes, possibly leading to anomalous R_{iso} readings. The parasitic resistance of the bypass diodes will add slight position dependence in low-light conditions.

In previous work, the baseline measurements for utility-scale systems were analyzed and compared to ground fault isolation standards [8]. In this paper, we validate the Sandia ground fault SPICE model with experimental R_{iso} measurements of physical faults on two large (750 kW) PV arrays. This, in conjunction with previous [11] validation on ~3 kW arrays is used as a basis to present a theoretical understanding of fault current/power and R_{iso} trip thresholds for safe operation of PV arrays.

The detectable area of R_{iso} measurements depends on the threshold used to define the presence of a fault. Ideal detection thresholding maximizes the balance between system safety and uptime, and is essential to the performance and reliability of the PV array and the safety of those around the system. If this trip threshold is too low, there will be nuisance trip events; but if the threshold is too high, certain ground faults will go undetected. R_{iso} methods register array leakage current (from modules or inverter) as a type of fault; therefore the detection threshold must be set above the maximum leakage current in all conditions (meteorological, configurational, and electrical) while also set low enough to detect the worst-case, lowest current faults possible in the array.

As determined in previous work [9], the array R_{iso} can be calculated in (12) and is a function of module isolation (R_{module}), inverter isolation (R_{inv}), fault resistance (R_{fault}), number of strings in the array (S) and modules in a string (M), as well as the EGC resistance (R_{EGC}).

$$R_{iso} = \frac{1}{\frac{S \cdot M}{R_{module}} + \frac{1}{R_{inv}} + \frac{1}{R_{fault}}} + R_{EGC} \quad (12)$$

Further, the leakage or isolation resistance to ground depends on both PV module and inverter technology [8, 12-15] and can drastically affect the detectable region of the R_{iso} measurements space (Fig 15). At very high values of R_{fault} ($> \sim 100 \text{ k}\Omega$ seen in a healthy systems), the array R_{iso} is dominated by the isolation of the module and other balance-of-system (BOS) components to ground. The size of the array, number of strings in the array (S) and modules in a string (M), and the specific isolation of these components are (R_{module} , R_{inv}) can have a significant effect on fault detectability since, in general, it is not possible to detect the presence of a fault with a larger resistance than the system itself. At very low fault resistances, the R_{iso} measurement is dominated by the series EGC resistance.

Inverter isolation can be a significant contribution to overall system R_{iso} , especially in utility-scale arrays. Previous analysis of large PV arrays [9] have shown that modules can have several hundred $M\Omega$ to $G\Omega$ of isolation per module while inverter isolation values can be as low as tens of $k\Omega$, even when nominally disconnected from ground. These leaky inverter pathways to ground significantly affect baseline R_{iso} readings and therefore, negatively impact the detectability of high-to-moderate impedance faults.

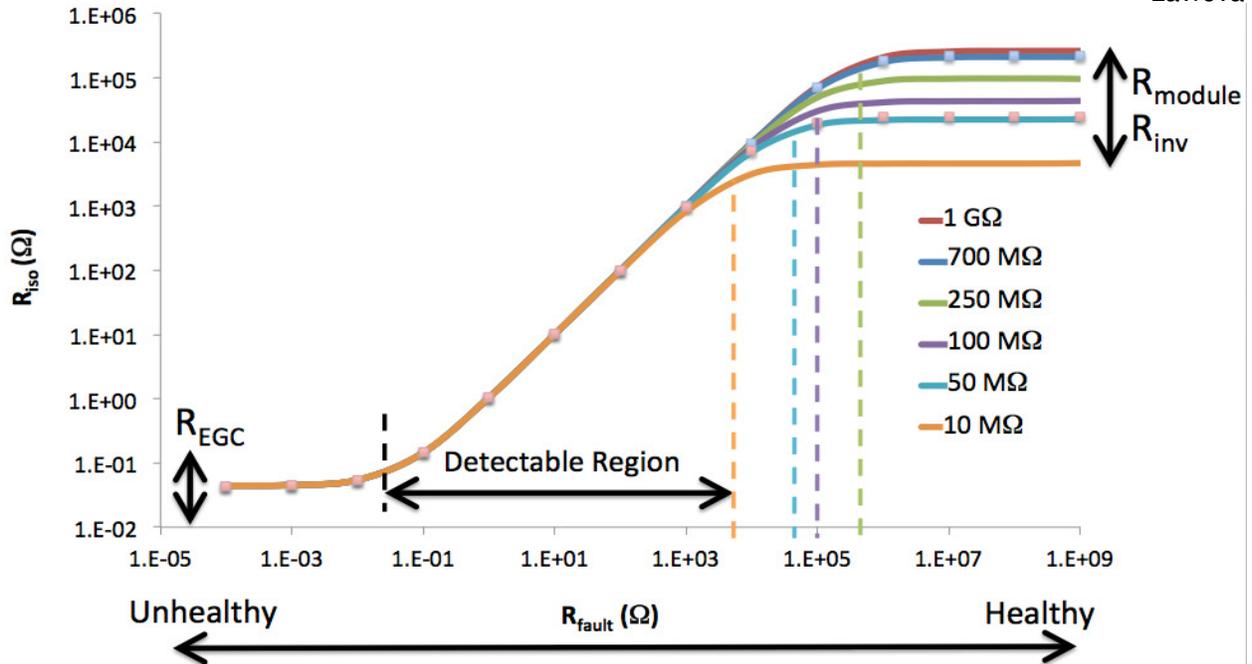


Fig. 155: R_{iso} as a function of R_{fault} for different healthy system isolations to ground. Changes in inverter or module isolation can have significant impacts on the detectability of faults.

Ground faults were induced on two 1000 V, 1.5 MW, positively grounded PV arrays located in Riverside, CA. The arrays consisted of 336 and 408 strings (Array 01 and 02, respectively) of ten E20-435-COM SunPower modules per string. 0.1, 2.6, and 5 k Ω faults were induced at the positive CCC (1+), one module into the array (1-), and five modules into the array (5-) as measured from the nominal positive CCC. After fault initiation, the array was ungrounded and a Bender isoPV-3 unit with coupling box (AGH-PV-3) was used to obtain array R_{iso} . The results of each test are shown in TABLE III.

TABLE III
RESULTS OF FAULT INSTALLATION ON TWO 1.5 MW PV ARRAYS

Time	Fault Location	Fault Impedance (k Ω)	Inverter	isoPV Reading (k Ω)
7:28 AM	1+	5.0	INV02	3.8
8:45 PM	1+	2.6	INV01	2.4
9:05 PM	1-	2.6	INV01	7.2
9:25 PM	5-	2.6	INV01	7.7
Morning	None	None	INV02	19
1:25 PM	1-	0.10	INV01	<0.2
5:30 AM	None	None	INV02	19
5:38 AM	1-	5.0	INV02	8.4
Morning	1-	5.0	INV01	3.9

It should be noted that the morning checks indicated the unfaulted array R_{iso} was low at 19 k Ω . As with previous testing on utility-scale arrays [9], the inverter was found to be a low-impedance pathway to ground, even when nominally disconnected from the ground bond. When the inverter is physically disconnected from the array, Array 01 registered a non-faulted isolation of 769

k Ω (2.6 G Ω /module) while Array 02 had a non-faulted isolation of 126 k Ω (0.5 G Ω /module). In these arrays, the low-impedance pathway to ground through the inverter accounts for 97.6% of Array 01 and 86.5% of Array 02 of the overall R_{iso} value. This poor isolation significantly affects the ground fault protection system.

The results of the experimental data from TABLE II compared to the predicated values from the SPICE simulations are shown in

The measured array R_{iso} does have a significant dependence on location of the fault in the array. The value of R_{iso} matched theory when the fault was on the CCC (1+). However, when the fault is at 1+, the measured value of R_{iso} increases by 300% and 215% for Array 01 and 02, respectively.

Fig. 16. The measured array R_{iso} does have a significant dependence on location of the fault in the array. The value of R_{iso} matched theory when the fault was on the CCC (1+). However, when the fault is at 1+, the measured value of R_{iso} increases by 300% and 215% for Array 01 and 02, respectively. In general, the experimental results match very well with the predicted outcome of the model. Interestingly, although the component of module isolation to R_{iso} differs widely (769 k Ω for Array 01 and 126 k Ω for Array02), the low-impedance pathway to ground through the inverter dominates the entire array R_{iso} and the individual R_{iso} curves for each array are indistinguishable.

This low impedance pathway through the inverter decreases the detectability region when the inverter is connected to the array (and nominally ungrounded). However, it also decreases array-to-array variability and may make determining proper thresholds module insensitive (at least when the inverter is the significant low-impedance path to ground).

The measured array R_{iso} does have a significant dependence on location of the fault in the array. The value of R_{iso} matched theory when the fault was on the CCC (1+). However, when the fault is at 1+, the measured value of R_{iso} increases by 300% and 215% for Array 01 and 02, respectively.

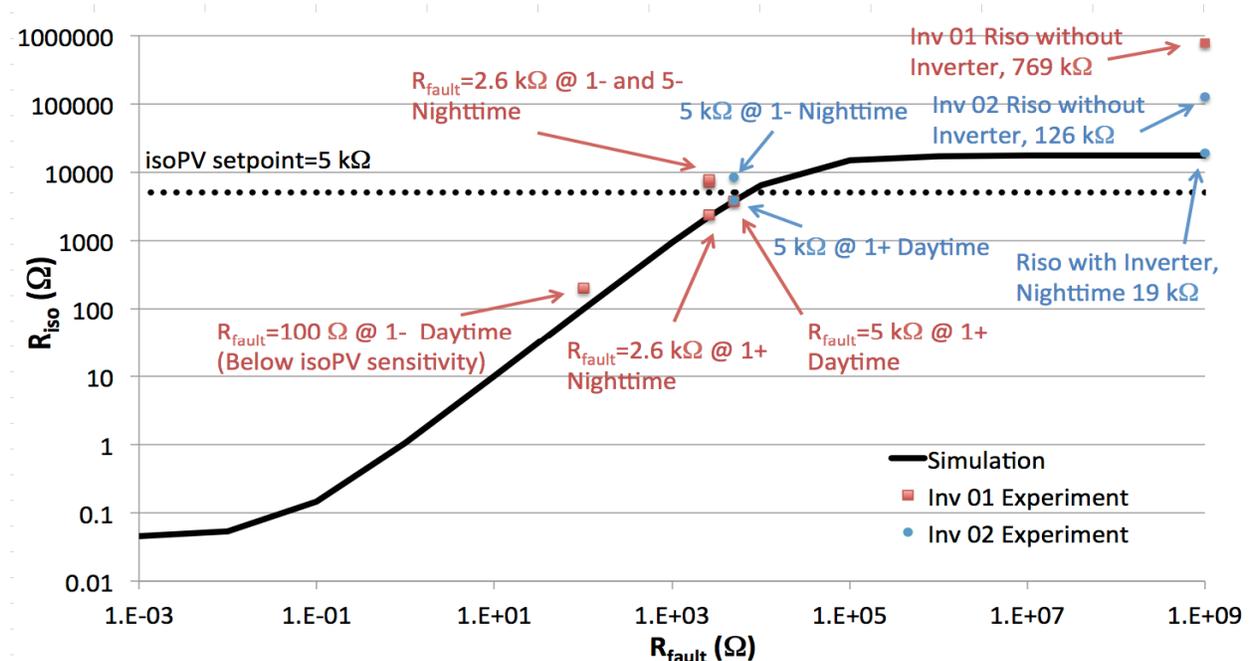


Fig. 16: Experimental data of measured R_{iso} for Array 01 (red) and 01 (blue) compared to simulations (black line). The threshold for this array is set at 5 k Ω and is denoted by the hashed line.

While the presence of the fault on the CCC is sufficient to decrease the measured array R_{iso} below the trip threshold (5 k Ω in this case, shown as a dashed line in Fig. 16), the larger measured R_{iso} for faults internal to the array are actually above the trip threshold and could subsist indefinitely in the array.

Also, interestingly, there is no subsequent increase (just 7% for Array 01) when the fault is moved from 1- to 5-). This dependence of R_{iso} on array location during nighttime R_{iso} measurements is the result of the bypass diodes conducting the voltage pulse.

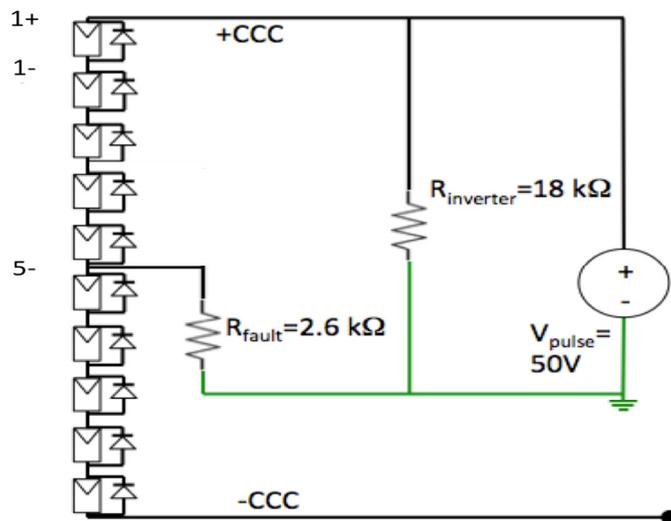


Fig. 17: Schematic of a R_{iso} measurement on the positive CCC.

To measure R_{iso} , the isoPV unit injects a 50 V pulse into one of the CCCs. Fig. 17 shows the pulse injected into the positive CCC, although the measurement unit uses pulses applied to both the positive and negative CCCs for error correction (however the exact nature of the measurement is immaterial as the array is more or less symmetric and either of the CCCs can be used). If the R_{iso} measurement is taken at night, the photodiodes in the modules are not forward biased and cannot conduct the voltage pulse. Therefore, the pulse must travel through the bypass diodes in order to interrogate the fault.

When the fault is at 1+, both the positive and negative pulse polarities give the same value of around 2.27 k Ω (see TABLE) since neither of the pulses have to traverse any bypass diodes. If, however, the fault is internal to the array, the bypass diodes block the positive polarity pulse and the measurement unit will not “see” the fault inside the array. Therefore, the positive pulse will measure R_{iso} to be approximately equal to the inverter isolation (around 18 k Ω) while the positive pulse will measure R_{iso} to the correct value. The isoPV unit then averages the R_{iso} results from the positive and negative pulses to get a final result for array R_{iso} .

When certain pulse polarities are blocked by the bypass diodes, the R_{iso} isolation measurement is (1) increased by several $k\Omega$ when the fault is not on the CCC. This accounts for similar R_{iso} increases when fault is moved from the CCC to 1- or 5-, as the difference between 1- and 5- is only from the small parasitic voltage drop across the bypass diodes.

TABLE IV
THEORETICAL NIGHTTIME R_{iso} RESULTS

Simulation	CCC	Pulse Polarity	+ CCC	1 mod. in	5 mod. in	- CCC
	+	-		2.26 $k\Omega$	2.39 $k\Omega$	2.39 $k\Omega$
+	+		2.27 $k\Omega$	17.5 $k\Omega$	17.6 $k\Omega$	17.9 $k\Omega$
	Average		2.27 $k\Omega$	9.95 $k\Omega$	10.0 $k\Omega$	10.34 $k\Omega$
Experiment			2.4± 0.4 $k\Omega$	7.2± 1.1 $k\Omega$	7.7± 1.2 $k\Omega$	

At night, the bypass diodes block half the polarity pulses from interrogating a fault internal to the array. The R_{iso} measurement unit then incorrectly measures the system isolation. The location dependence of the fault is from the unit averaging the fault resistance (measured with the polarity that can pass the bypass diodes) with the inverter isolation.

Inverter isolation can be a significant contribution to overall system R_{iso} , especially in utility-scale arrays. Previous analysis of large PV arrays [23] have shown that modules can have several hundred $M\Omega$ to $G\Omega$ of isolation per module while inverter isolation values can be as low as tens of $k\Omega$, even when nominally disconnected from ground. These leaky inverter pathways to ground significantly affect baseline R_{iso} readings and therefore, negatively impact the detectability of high-to-moderate impedance faults.

In order to determine the maximum allowable trip thresholds for an array, it is necessary to solve for the fault current and define an allowable fault current/power below which the array can still be considered to exist in a safe condition. In general, the fault current for an arbitrary location in an array is not analytically solvable. However, the worst-case scenario (fault at a current carrying conductor) has an analytical form since the inverter acts as a current divider circuit with impedance R_{inv} .

The fault current through a fault during array operation can be described for an ungrounded array by Eq.13.

$$I_{fault} = \frac{V_{oc}}{2 \cdot (R_{iso} + R_{fault})} \quad (13)$$

For a grounded array, if we assume a ground fault of resistance R_{fault} exists at the ungrounded CCC in parallel with an inverter with impedance, R_{inv} (Fig 18), then current (I) from the array will be split between the fault (I_{fault}) and the inverter ($I-I_{fault}$).

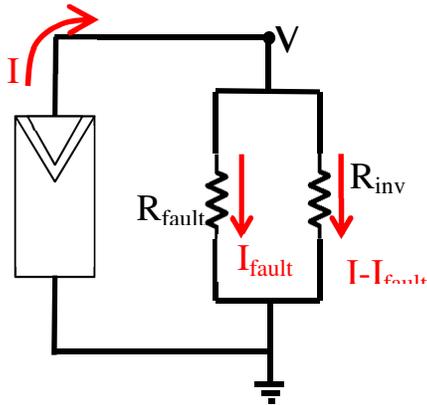


Figure 18: Schematic of ground fault at ungrounded CCC

Using Ohm's Law, the voltage drop across both pathways is equal and can be described by:

$$I_{fault} \cdot R_{fault} = (I - I_{fault}) \cdot R_{inv} \quad (14)$$

Assuming that the MPP does not change with the existence of a fault (an acceptable approximation for utility scale arrays and faults that are greater than $\sim 1 \Omega$), then the supplied current from the array (I) is equal to I_{mp} and the inverter impedance (R_{inv}) is equal to R_{mp} and the fault current can be described by (15).

$$I_{fault} = I_{mp} \left[1 - \frac{R_{fault}}{R_{mp} + R_{fault}} \right] \quad (15)$$

A worst-case approximation for the current through the fault assumes that $R_{fault} \ll R_{inv}$. In this case, (15) reduces to (16). Although the current at V_{oc} is, by definition, equal to zero and these two conditions are mutually exclusive, it gives an added safety margin to assume that the array is in both a high voltage and high current state. Eq. (15) and (16) match well with the results obtained from SPICE simulations (Fig 19).

$$I_{fault} = \frac{V}{R_{fault}} \approx \frac{V_{oc}}{R_{fault}} \quad (16)$$

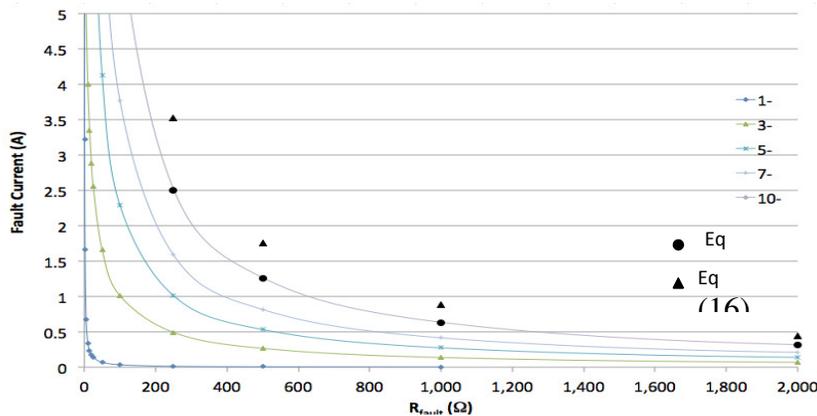


Figure19: SPICE simulations (colored lines) of fault current vs fault impedance for ground faults at different locations of of a 1000 V, 750 kW array compared to analytical equations (black points)

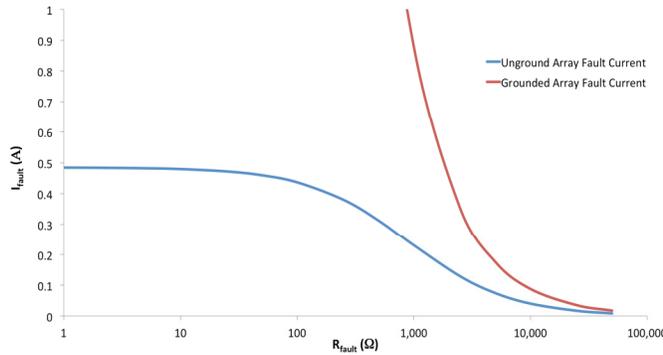


Figure20: Fault current vs. fault resistance for a fault on the CCC for an ungrounded (blue) and grounded (red) array of a 1000V, 1.5 MW array.

It is apparent from the Eq. (15)(13) and (16) and plotted in Figure 20 that grounded arrays provide significantly more fault current than ungrounded arrays. This is due to the “clamping” effect of ungrounded systems, where the available fault current is limited. That is, when a well behaved ($R_{iso} \rightarrow \infty$) ungrounded system develops a fault condition, the array becomes referenced to ground at the point of the fault and it, effectively, turns into a grounded system.

Since grounded systems provide much more available power to the fault, they are *significantly* more dangerous than ungrounded systems. As a matter of safety, the threshold for an array should be set for the worst-case fault: a grounded system faulted at the ungrounded CCC.

From IEC 60364-4-42 [30], the maximum power that can be dissipated safely through an enduring fault without risk of a fire is 70 W instantaneous power or an equivalent energy of 750 J. A maximum allowable energy value of 750 J makes it possible to formulate a trip time vs. fault power curve, as shown in Figure. Assuming a worse case, where the array is at V_{oc} and supplying all the current through the fault (which, as stated before, is impossible in practice, but does give an added safety factor), then the trip-time curve for a current sensing device (i.e. CSM or RCD) would be described by (16)(17), where P_{max_trip} would be 70 W and E_{min_trip} would be 750 J. This equation yields a series of curves that are dependent on array V_{oc} , as in Fig 21.

$$RCD_trip \left\{ \frac{E_{min_trip}}{P_{min_trip}} \leq t < \infty \right\} = \frac{E_{min_trip}}{I_{fault} \cdot V_{oc}} \quad (17)$$

Instead of requiring a trip time as a function of fault current, R_{iso} , has a trip point based on the isolation of the array according to (12). One of the inputs is the fault impedance, which can be found by transforming the fault current into fault impedance using array V_{oc} , as in (16) to give a trip-time vs. fault impedance curve. This curve could finally be transformed into a trip-time vs. R_{iso} curve using (12).

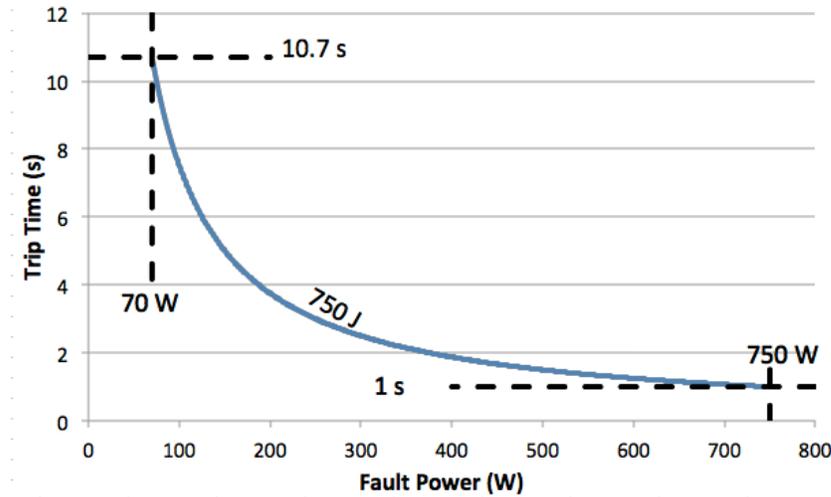


Figure 21: Proposed trip time curve for PV arrays based on 750 J safety limit.

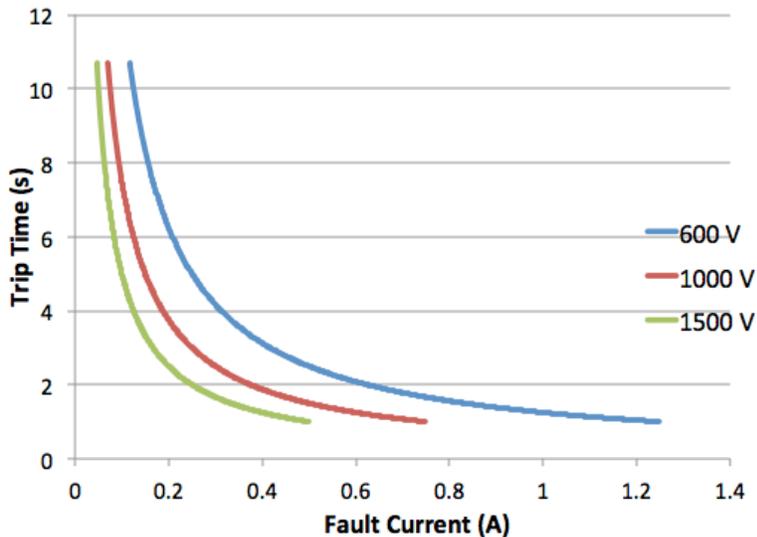


Figure 22: Trip-time vs. Fault Current curves for arrays with different V_{oc} values that would be used for CSM and RCD GFDIs to ensure fault power is below 70 W or 750 J.

As was stated previously, R_{iso} is very slow detection method due to array capacitance and is therefore inappropriate for quick fault mitigation that is more applicable to trip-time curves. R_{iso} is most effectively used to give binary yes/no signal (most likely at morning check). Therefore, the trip setting should only be concerned with the highest R_{fault} value (i.e. the value of R_{fault} that corresponds to a fault power of 70 W). For a 1000 V grounded system, this would correspond to a fault current of 70 mA and would be caused by an R_{fault} value of 14.3 k Ω based on (15)(16). A

system designer, with knowledge of the specific array configuration (S, M), module leakage (R_{module}), and inverter isolation (R_{inv}) could then use (12) to find the proper R_{iso} threshold for the array in question (R_{EGC} is assumed to be zero for thresholding purposes).

Unfortunately, for standards organizations and other bodies such as inverter manufacturers without detailed knowledge of specific array configuration, it is not ideal to describe necessary trip thresholds based on array configuration (S, M). It is possible to remove the array configuration aspects from (12) and completely describe R_{iso} with array electrical information and allowable fault power.

In this case, the number of modules in an array ($S \cdot M$) is a function of the power of the array (P_{inv}), power of a module (P_{mod}), and DC-to-AC ratio ($P_{\text{DC}}/P_{\text{AC}}$) as seen in (18).

$$S \cdot M = \frac{P_{\text{inv}}}{P_{\text{mod}}} \cdot \left(\frac{P_{\text{DC}}}{P_{\text{AC}}} \right) \quad (18)$$

There also exists an implicit assumption in R_{module} on the number of modules (more specifically, in the area of modules present, as module isolation is limited by IEC 61215 [31] to no less than $40 \text{ M}\Omega \cdot \text{m}^2$). The module area (A) is a function of module power (P_{mod}) and module efficiency (η) as shown in (19)(19).

$$A = \frac{P_{\text{mod}}}{1000 \cdot \eta} \quad (19)$$

By inserting (18) and (19) into (12), the value of R_{iso} can be described only in terms of the electrical state of an array (20)(20).

$$R_{\text{iso}} = \frac{1}{\frac{P_{\text{inv}} \cdot \left(\frac{P_{\text{DC}}}{P_{\text{AC}}} \right)}{R_{\text{module}} \cdot 1000 \cdot \eta} + \frac{1}{R_{\text{inv}}} + \frac{P_{\text{fault}}}{V_{\text{oc}}^2}} \quad (20)$$

This equation can be used to determine an array threshold. Let us assume that a standards-making body wants to set a R_{iso} threshold to limit fault power (P_{fault}) to 70 W. A conservative estimation of R_{iso} threshold would be assume a worst-case situation for the array in which large area, leaky modules ($40 \text{ M}\Omega \text{ m}^2$, 10% efficient) with a low inverter impedance to ground (20 k Ω) are installed on an 500 kW, 1000 V system. In this case (shown as the blue curve in Figure) the unfaulted array would have a R_{iso} value of 7.85 k Ω with a trip threshold calculated using (20)(20) to be 4.08 k Ω .

If, however, a system designer installs significantly better modules (1.08 G $\Omega \text{ m}^2$, 20% efficient, $R_{\text{inv}} = 500 \text{ k}\Omega$, red curve in Fig 23), the unfaulted R_{iso} would increase to 230.6 k Ω . This increase would increase the detectability for faults; however, the trip setting calculated for the less efficient modules (4.08 k Ω) would yield a fault power of 193 W, resulting in a hazardous condition where a fault dissipating over 70 W could exist in the system without detection.

Therefore, assuming very poor quality modules as a worst-case condition actually decreases system safety.

Conversely, if it is assumed that high-isolation modules are installed ($R_{\text{module}} \rightarrow \infty$) then the array isolation is only a function of fault impedance (purple line in Fig 23). In this case, the threshold would be set at 14 k Ω . If a system designer installs more leaky modules (blue line in Figure), then there will be nuisance tripping issues as even the R_{iso} of the healthy array case (7.85 k Ω) is below the determined trip threshold.

In general, without some knowledge of the array configuration or module quality, it is impossible to determine a trip threshold that provides safety and prevents unwanted tripping issues. Appropriate R_{iso} trip thresholds *must* be determined on an array-by-array basis with sufficient leeway by system operators to adjust trip threshold settings for their particular usage cases.

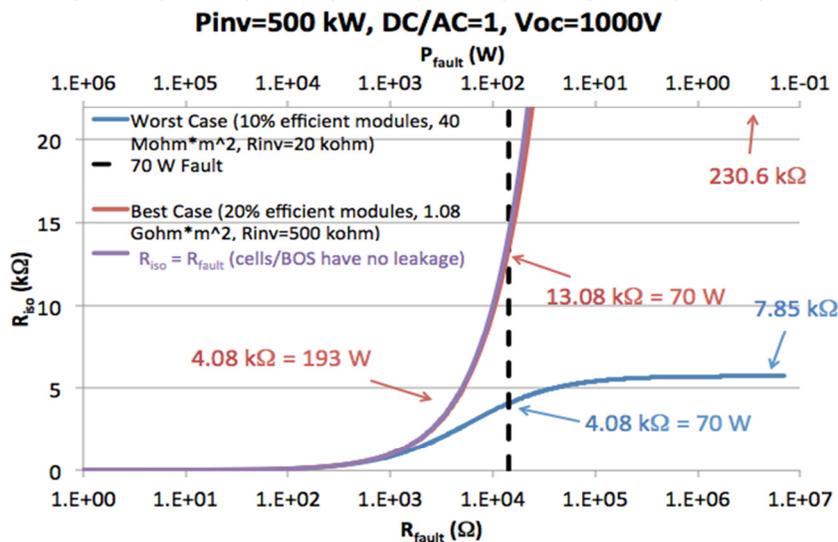


Figure23: R_{iso} vs. R_{fault} for different module technologies based on (17) ranging from very leaky modules (blue line) to slight better modules (red line) to non-leaky modules (purple line). In general, with regard to a priori calculation of R_{iso} trip settings, changes in module efficiencies and isolations result in either safety or unwanted tripping issues.

Although specific, one-size-fits-all R_{iso} trip settings are not possible, standards making bodies can define R_{iso} trip points in a way that is analogous to the advanced inverter functionality testing. Namely, standards could define a minimum allowable set point, a default set point, and a maximum allowable set point that could then be adjusted by a qualified operator to optimize the safety for each individual array. UL or other NRTL nationally recognized testing laboratory certification would correspond to ensuring the accuracy of these set points from the manufacturer.

The basis for the maximum, minimum, and default set points should be based off the R_{iso} equations presented here to ensure any allowed fault power dissipates no more than 70W (for a grounded system, an ungrounded system *can* have higher set points since a first fault will induce much smaller fault currents, but in the interest of defining a single set of numbers we use

$$R_{\min}^{iso} = \frac{1}{\left(\frac{P_{system}}{40 \times 10^6 \cdot 1000 \cdot 0.1} + \frac{1}{20 \times 10^3} + \frac{70}{V_{oc}^2} \right)} \quad (21)$$

grounded systems as a worst case). The minimum allowable set point **Error! Reference source not found.** would be based on the leakiest/lowest efficiency modules/inverter that would realistically be installed in the field (40 MΩm² module isolation, 10% efficiency modules, 20 kΩ inverter isolation).

Since the problem of having too a low a set point is safety, while having too high is only unwanted tripping, the default R_{iso} would be the highest R_{iso} set point that would realistically be used in the field. Therefore, the default set point would be for state-of-the-art modules (1 GΩ m² isolation, 20% efficient, 500 kΩ inverter isolation) and the inverter would be in a “safe” state. A system installer would then alter the set point to deal with unwanted tripping and adjust the R_{iso} down.

$$R_{\text{default}}^{iso} = \frac{1}{\left(\frac{P_{system}}{1 \times 10^9 \cdot 1000 \cdot 0.2} + \frac{1}{500 \times 10^3} + \frac{70}{V_{oc}^2} \right)} \quad (22)$$

For testing/certification of R_{iso} set point accuracy, it is necessary to define a maximum allowable set point as well (23). In this case, we propose the maximum allow set point to be a 50% increase in the difference between the minimum and default set points.

$$R_{\max}^{iso} = R_{\text{default}}^{iso} + 1.5 \times (R_{\text{default}}^{iso} - R_{\min}^{iso}) \quad (23)$$

An example of using these equations to develop minimum, default, and maximum trip points as a function of system size (system size should be calculated to be inverter rating multiplied by maximum DC to AC ratio) for a 1500 V_{oc} system is shown in Table V. The system sizes used in the calculations are the average of system size range for each category (500 kW is used for the highest category). Fig 24 shows how the minimum, defaults (dashed line), and maximum R_{iso} set points compare to current PV standards [19, 20, 32, 33]. The minimum R_{iso} set point matches well with IEC 62548 for utility-scale systems and is more liberal for smaller residential scale systems [33]. The equations presented here are also more liberal than the set points in UL1741 CRD-2012 [32], although much more conservative than the set points in UL1741 CRD-2010 [19].

Table V: R_{iso} minimum, maximum, and default set points as a function of system size for a 1500 V_{oc} system.

System Size (kW)	R _{min} ^{iso} (kΩ)	R _{default} ^{iso} (kΩ)	R _{max} ^{iso} (kΩ)
≤20	12.0	30.2	57.5
> 20 and ≤30	11.4	30.1	58.15
> 30 and ≤50	11.0	30.1	58.75
> 50 and ≤100	10.0	29.9	59.75
> 100 and ≤200	8.4	29.6	61.4
> 200 and ≤400	6.4	29	62.9
> 400 and ≤500	5.2	28.5	63.45
≥500	4.9	28.4	63.65

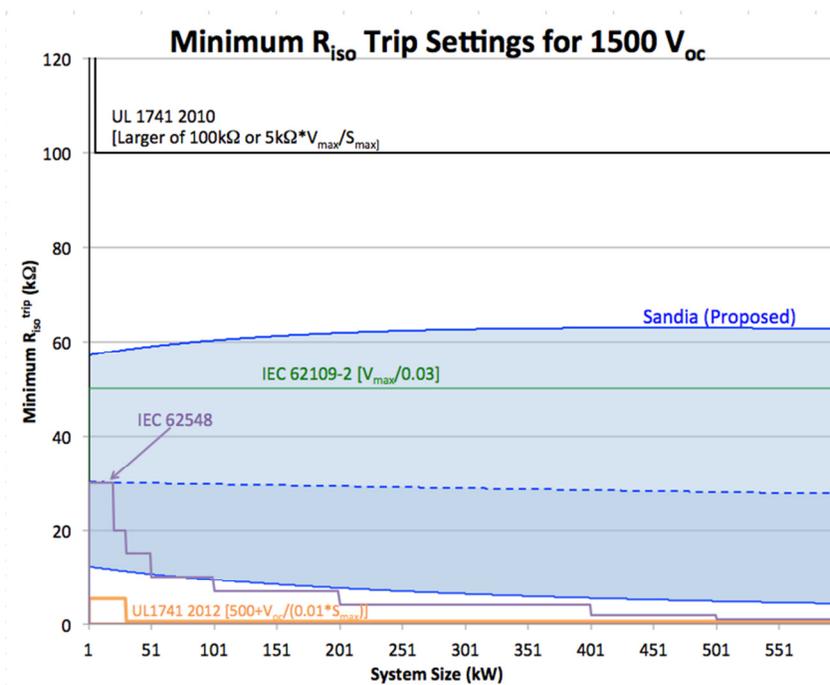


Figure 24: Allowable adjustable Riso range (blue shading) as a function of system size for 1500 V systems. The trip points based on the equations presented in this work (blue) are compared to other PV industry standards for Riso.

Significant Accomplishments and Conclusions: We have examined ground faults in PV arrays and the efficacy of fuse, RCD/CSM, and R_{iso} GFDIs using simulations based on a SPICE ground fault circuit model, experimental ground faults installed on real arrays, and theoretical equations.

SPICE model and analytical results were used to determine trends for various ground fault conditions and to ascertain potential benefits of reducing the fuse ratings in PV systems. Decreasing the GFPD ratings to 1 A would protect against a wider range of ground faults. However, further decreasing the fuse ratings below 1 A does not improve the number of faults that can be detected due to larger internal GFPD resistances and a subsequent decrease in fault current. It is necessary to carefully consider the GFPD rating and resistance to optimize the types of ground faults that can be detected.

To demonstrate the efficacy of CSM/RCD fault detection techniques, Sandia patterned with a major EPC firm for aggressive implementation of advanced ground fault detection equipment that significantly reduced the fire risk in PV systems. Over three years, they have refined the detection thresholds for their systems to minimize unwanted tripping events while maintaining a perfect safety record. Additionally, analysis of one-minute RCD leakage values of 340 co-located inverters found a 5 A trip point to be overly conservative. For these inverters, RCD trip point could be lowered from 5 A to as low as 2.5 A with six 9's confidence that any unfaulted RCD current measurement would be lower than the ground fault setpoint. Statistically, this would correspond to 0.5 trips/year/inverter if single, raw RCD measurement points were

considered. In practice, this number would be drastically reduced through the proper use of data windowing, averaging, or other simple data analysis techniques.

Finally, theoretical equations related to R_{iso} were derived for grounded and ungrounded arrays, which can be used to determine appropriate trip thresholds based on allowed fault power. Equations were also developed to allow the calculation of trip threshold without knowledge of the specific array topology. However, in this case, selection of the default R_{iso} value for leaky modules (low R_{module}/η) leads to potential safety issues if well-isolated modules are installed; while using well-isolated modules to select the default R_{iso} trip threshold leads to possible unwanted tripping issues in systems with leaky modules. Said another way, a default R_{iso} value cannot be determined for a given PV inverter because leaky systems will have unwanted tripping and highly isolated systems will not trip before a fire hazard.

Therefore, it is apparent that any *a priori* calculation of trip threshold cannot mitigate both fire risk and unwanted tripping issues for all possible arrays. Some system knowledge is necessary for the determination of trip points. In general, there is no *one-size-fits-all* solution and standards bodies may have to determine a *range of values* that can be set by array operators based on specific details of the array. Therefore, inverter manufacturers and testing organizations should allow for a range of R_{iso} thresholds that can be determined on a case-by-case basis, most likely as part of array commissioning.

Currently, there are major efforts underway to refine the industry-wide requirements for PV system ground fault protection in U.S. safety standards. The Underwriters Laboratories Standards Technical Panel (STP) for UL 1741 and UL 62109-2 are presently reviewing trip limit proposals for CSM/RCD and isolation monitors. The simulations, experiments, and theoretical questions presented here are being used by the UL STP to justify considerably lower trip limits for PV system ground fault protection than had been required in the past. The updated requirements are being incorporated into UL 62109-2, which will likely be available in 2016. While it is difficult to balance the unwanted tripping with detection sensitivity, one thing is certain: PV systems will be far safer in the future.

Inventions, Patents, Publications, and Other Results:

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