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## Estimation of changes in insulation resistance with various design parameters of interdigitated wire loops

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# **Estimation of changes in insulation resistance with various design parameters of interdigitated wire loops**

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## **Abstract**

In this report we explore the sensitivities of the insulation resistance between two loops of wire embedded in insulating materials with a simple, approximate model. We discuss limitations of the model and ideas for improvements.



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# 1 Introduction

The most basic model of the device to be designed is a capacitor in parallel with a high resistance, *i.e.* two conductors at constant voltage separated by some distance with a small leakage current between them. Physically, the source of the leakage current is possibly due to tunneling and other mechanisms particular to conduction in the polymeric materials. It is minimizing this leakage current that is our primary concern. We define the leakage current as the steady current after capacitive charging and polarization effects have subsided.

To calculate the insulation resistance of the device two equations are needed. First, the electrostatic equation for the electric potential  $\phi$ :

$$\nabla \cdot \epsilon \nabla \phi = 0 \quad (1)$$

where  $\epsilon$  is the dielectric of materials in between and surrounding the conductors and  $\phi$  is fixed on the surface of the metal wires. Second, the current equation for the current density  $\mathbf{i}$

$$\mathbf{i} = \sigma \nabla \phi \quad (2)$$

where  $\sigma$  is the conductivity of the materials external to the conductors. Since the leakage currents are so small we assume there is no coupling between the current and the potential. With the current density field  $\mathbf{i}$  and the difference in potential  $\Delta V$  between the two metal contacts we can calculate the insulation resistance  $R$  as

$$R = \frac{\Delta V}{\int \mathbf{i} \cdot \mathbf{n} dA} \quad (3)$$

*i.e.* the potential difference over the total current,  $I = \int \mathbf{i} \cdot \mathbf{n} dA$ , entering or leaving the metal wires.

Returning to the illustrative example of a parallel plate capacitor such that the plates are large with respect to the plate spacing  $\ell/\sqrt{A} \ll 1$  so that one dimensional solutions to Eqs. (1) and (2) are acceptable. The solution to Eq. (1), in this case, is  $\nabla \phi = \Delta V/\ell$  and hence  $I/A = \sigma \Delta V/\ell$  and so the total insulation resistance is:

$$R \equiv \frac{\Delta V}{I} = \frac{\ell}{\sigma A} \quad (4)$$

which suggests there are three routes to increasing the resistance:

- (a) decrease the intrinsic conductivity of the insulator  $\sigma$ ,
- (b) decrease the (surface) area of the conductors  $A$ , and
- (c) increase the spacing  $\ell$  between the conductors,

in the absence of three dimensional effects and layered materials. For instance, if the area of the conductors is their length  $L$  times a fixed width,  $R$  is inversely proportional to  $L$  due to the fact that the total conductivity of the device will increase with the area of the weakly conductive material between the two plates. Note, when the plates become more like wires in aspect ratio three-dimensional effects will be introduced that will cause deviations to the exact  $R \propto 1/L$  scaling but never to the point that an increase in the area of the conductors will increase the overall resistance.

material	dielectric	resistance [ohm-cm]
copper	–	$10^2$
kapton	3.4	$10^{17}$
acrylic	4.0	$10^{14}$
air	1.0	$\infty$

**Table 1.** Material properties. Note the possibility of significant surface and other resistances in the flexible circuit.

## 2 Application

Flexible, etched circuitry made from copper on a *Kapton* substrate, commonly referred to as *flat-flex*, is utilized for a variety of applications (see Fig. 1). A myriad of manufacturing parameters are specified by the end user of the part, including:

- substrate thickness
- thickness of the copper traces on substrate (also referred to as copper weight)
- width of copper lines after etching
- spacing between copper lines after etching (space or pitch)
- single or double-sided copper traces on substrate, and with double-sided copper: the location of copper traces on the top relative to traces on back side
- total length of the continuous copper trace
- addition of an adhesion layer between copper and substrate (including if this adhesive fully or partially fills the void)
- coverlay applied with adhesive on copper after completed circuitry has been etched and cleaned

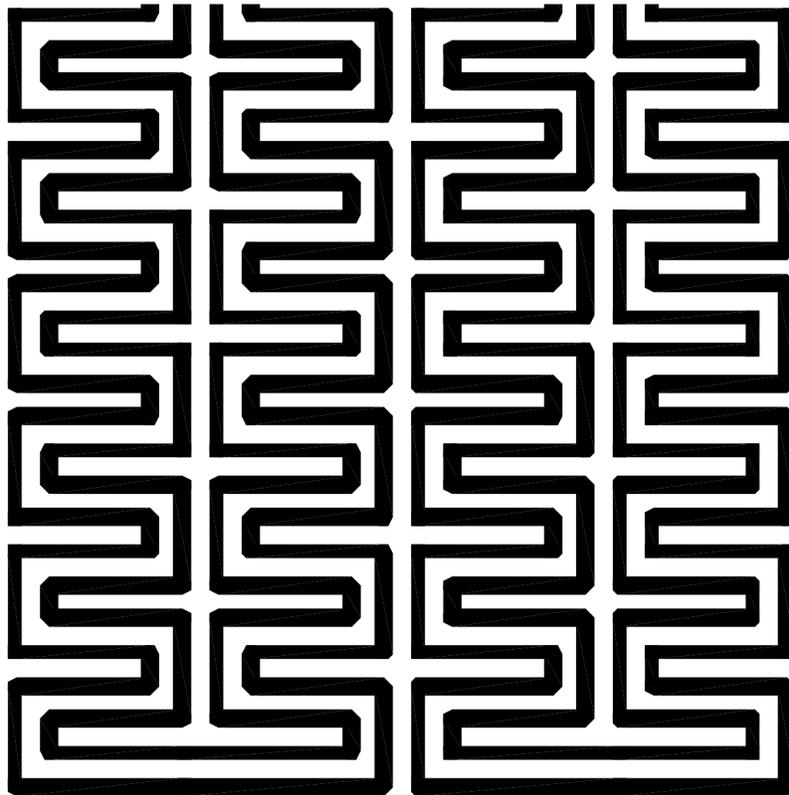
These parameters affect both the physical and electrical properties of the final flexible circuit. As mentioned, the goal of this modeling effort is to develop a model to understand how these parameters specifically affect the insulation resistance,  $R$ , between two parallel copper traces held at a low voltage bias. The key variables required to develop this model include the dielectric constant of the materials, surface and volume resistivities of the substrate, coverlay and any adhesive, and the trace and space of the copper circuitry. The relevant material properties are given in Table 1 and the physical dimensions in Table 2.

dimension	symbol	value [ $\mu\text{m}$ ]
wire width	$t$	150-250
wire height	$h$	18, 36
wire pitch	$s$	150-250
insulation thickness	$k$	50-100
adhesive thickness	$a$	0,65-80

**Table 2.** Physical dimensions. Pitch is also referred to as “space” and what is commonly referred to as 150x150 space-trace with 0.5 oz copper and 4mil insulation corresponds to  $s = t = 150\mu\text{m}$ ,  $h = 18\mu\text{m}$ ,  $k = 100\mu\text{m}$ . Note the AP substrate is “adhesiveless” ( $a = 0$ ) and the LF substrate has  $25\mu\text{m}$  adhesive above and below the copper (thus making a  $k = 50$  LF device equivalent in total thickness to a  $k = 100$  AP device). For this study the nominal dimensions are: AP  $s = t = 150\mu\text{m}$ ,  $h = 36\mu\text{m}$ ,  $k = 100\mu\text{m}$  and LF  $s = t = 150\mu\text{m}$ ,  $h = 36\mu\text{m}$ ,  $k = 50\mu\text{m}$ .

### 3 Model and results

For the flexible circuit, we developed a simple numerical model to understand some of the basic geometric sensitivities. It was expedient to make the model two-dimensional, see Fig. 2a, and only simulate geometric variations that occur in the cross-section of the design, i.e. changes in height and widths, and make the assumption that the details of the complex interdigitation pattern out of this plane would still result in roughly the  $1/L$  scaling predicted by our introductory parallel plate capacitor model. Furthermore, given the number of repeating units in the pattern shown close up in Fig. 1, we assumed a semi-periodic model of the cross-section would be adequate to determine basic trends and sensitivities.



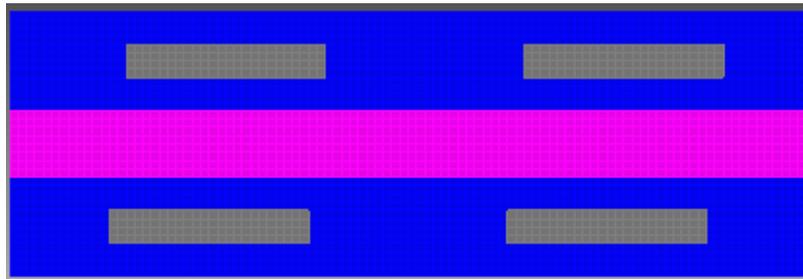
**Figure 1.** Plan view of flat-flex flexible circuitry. Copper trace wires are in black.

## 4 Results

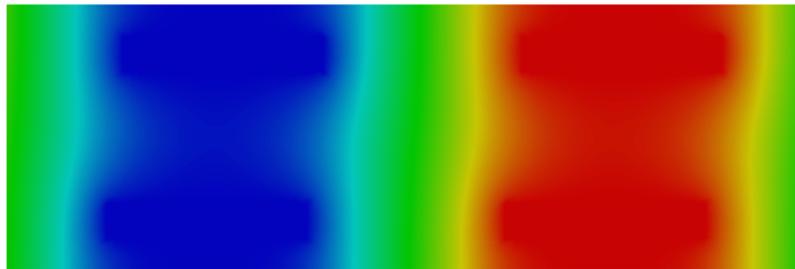
Using the simple two-dimensional circuit model shown in Fig. 2, we can make a few observations:

- Since all dielectric properties (impedance to the electric field) of the materials are on-par the electric field shown in Fig. 2b shows little effect of the substrate. The electric field is largely determined by the alignment of the conductors.
- Given the relative resistance of Kapton substrate and the acrylic adhesive, effectively no current flows across the substrate between the upper and lower loops, refer to Fig. 2c. Essentially all current flows through the adhesive.
- Despite the fact that the Kapton substrate is an effect barrier to current flow, the alignment of the low vs. high potential loops does affect the current since the alignment affects the potential gradients driving current flow through the adhesive. In fact, Fig. 3 shows that the alignment can change the resistance about 60%.
- Fig. 4a shows that by doubling the substrate thickness the resistance can be changed by about 20 %
- From Fig. 4b and Fig. 4c it appears that minimizing the size of the wires is best for insulation resistance, given fixed adhesive and substrate dimensions. (Basically, a smaller fixed potential surface leads to a smaller current, akin to a smaller capacitor having a smaller leakage current.)
- Fig. 4d shows that increasing the pitch relative to the width of the wires increases the resistance but only minimally. Also, for the nominal configuration of the flexible circuitry in Fig. 2a, Fig. 4c shows that the resistance increase with increased pitch does not overcome resistance decreases with increased wire size.
- Most of the trends over the ranges given are fairly linear and can be summarized by the sensitivities given in Table 3, with changes in height being the strongest influences on total resistance.

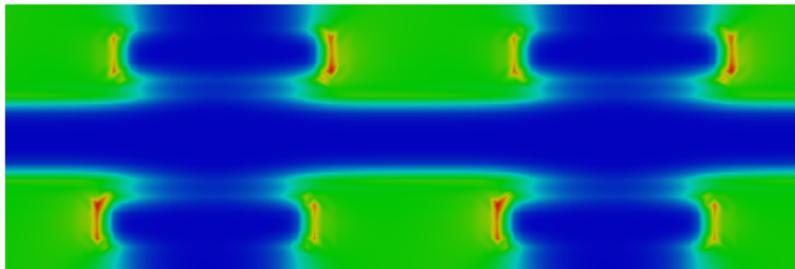
Note that all the (per-length, per-repeating cell) resistances predicted by the model have been normalized for comparison.



(a) mesh

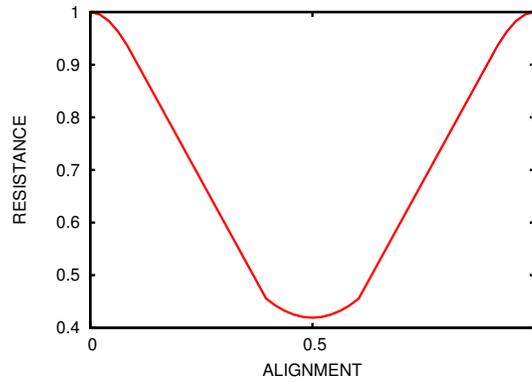


(b) potential



(c) current

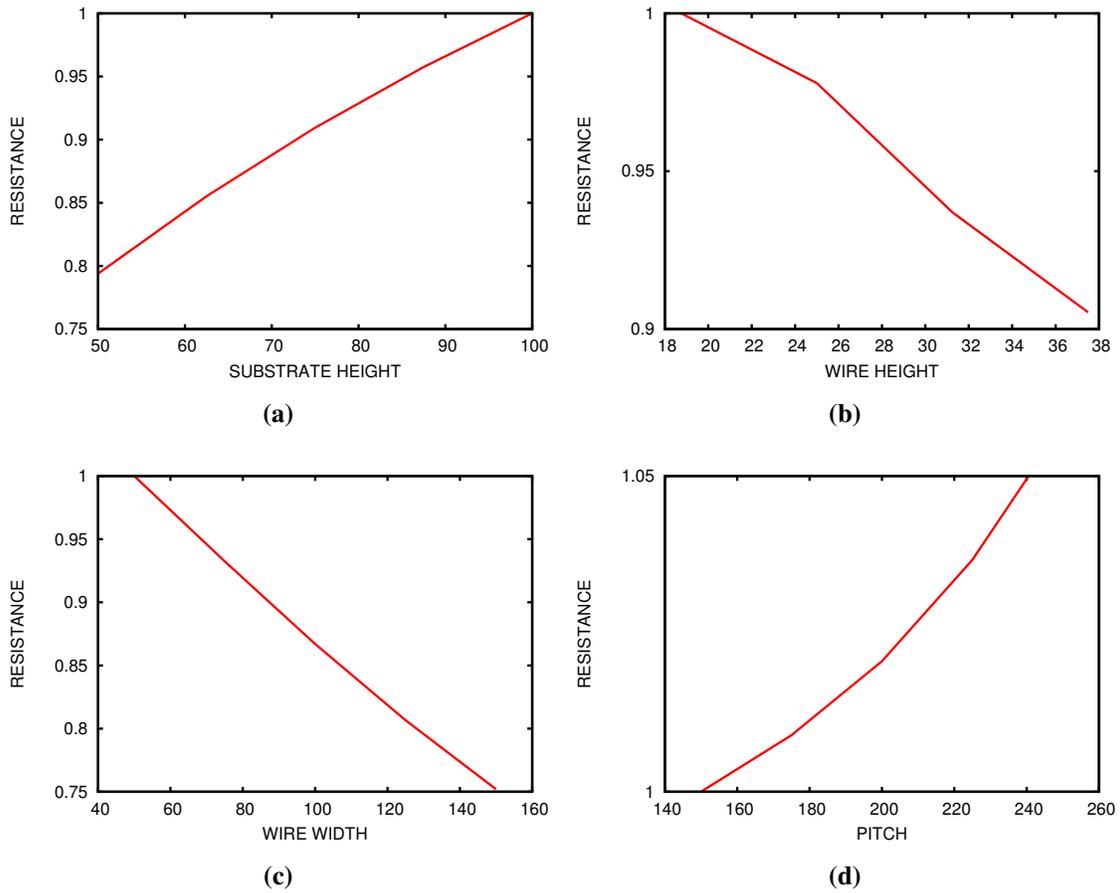
**Figure 2.** Through thickness two-dimensional model of flat flex repeating unit (LF design). (a) mesh, (b) potential, and (c) current magnitude for a typical configuration. In (a) copper wires are gray, The substrate (Kapton) is magenta and adhesive, which fully fills the space not occupied by the wires above and below the substrate, is blue. In (b) potential and (c) current field plots hotter colors designate higher values, with the loop with low potential on the left and that with high potential on the right.



**Figure 3.** Resistance as a function of: alignment, where 0 on the x-axis is loop A over A and 1/2 is A over B,

sensitivity	parameter
-0.52	wire height
0.41	substrate height
-0.25	wire width and pitch
0.06	pitch with fixed wire width

**Table 3.** Sensitivities to various geometric changes in percent change in resistance per  $\mu\text{m}$  change in the given dimension obtained from the slopes of the resistance curves in Fig. 4. Negative values indicate a decrease in resistance with increase of the particular parameter.



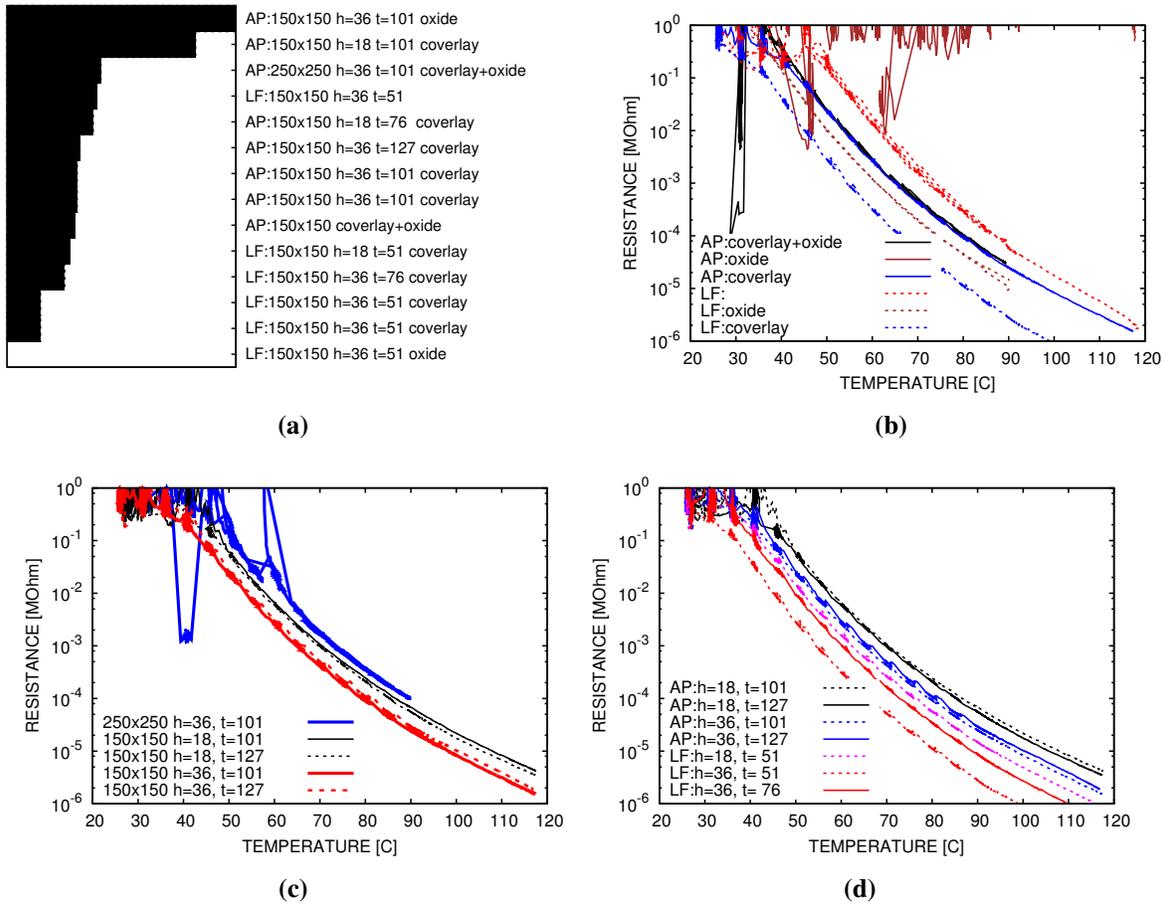
**Figure 4.** Resistance as a function of: (a) substrate thickness, (b) wire height keeping the other dimensions fixed. (c) wire width with the pitch equal to twice the wire width (d) pitch with fixed wire width

## 5 Experimental data

A number of electrical resistance measurements have been made on actual flexible circuitry configurations. Although the results shown in Fig. 5a are primarily focussed on temperature dependence, the fact that the trends are fairly uniform across devices allows us to rank the configurations (see Fig. 5b). (Note the only dataset that does not conform to the quasi-exponential decay with temperature “AP: 150x150 oxide” exceeded the measurement capacity of the available lab equipment and likely follows the same trend as the other datasets.) Observations:

- The configuration with the least adhesive has the highest resistance by orders of magnitude. In fact the superiority of AP vs. LF devices is largely due to the amount of adhesive, less due to the thicker insulation.
- The insulating oxide on the wires increases resistance but only marginally compared to removing contact of the wires with the adhesive
- Increasing the wire width and spacing appears to substantially increase the resistance of circuitry – in contrast with the predictions of the two-dimensional model.
- Increasing wire dimensions decreases resistance to leakage, as predicted. and more so than decreasing insulation The larger sensitivity to wire size (surface area) vs. insulation thickness is also apparent in the data.

Lastly, insensitivity to alignment in measured data (not shown) is likely due to the flexible circuit having fairly random alignment given any particular A & B wires in the overall pattern.



**Figure 5.** (a) Ranking for all tested configurations of flat-flex at 70 C. Note in (a) the horizontal bars denoting resistance are on a log scale. Resistance vs. temperature for (b) material changes (all 150x150  $\mu\text{m}$  space-trace, h=36  $\mu\text{m}$ , AP: k=100  $\mu\text{m}$ , LF k=50  $\mu\text{m}$ ), (c) geometry variations (all AP), and (d) manufacturer (all s=t=150). The datasets are labelled according to their manufacturer, spacing and wire width, insulation thickness, wire dimensions, and whether they had an insulating coverlay and/or an insulating oxide on the wires. Note the AP: 150x150 oxide, LF 150x150 and LF 150x150 devices lack the standard coverlay (all dimensions in  $\mu\text{m}$ ).

## 6 Conclusions

Looking at ranked configurations (Fig. 5a), clearly the resistivity of the acrylic adhesive is the determining property. Design changes that address this issue will likely be the most effective. So, if possible, remove all contact of the wires with the adhesive. If it is not feasible to remove the adhesive, insulate the wire from adhesive. An air gap would be most effective. A thick oxide should reduce potential gradients due its high dielectric and also reduce current directly due to its added resistance in the current path from one wire to another. The idea of obtaining less adhesive contact by using taller wires is a trade-off between reliable decrease in resistance due to increase in conductor surface area and an unreliable increase in resistance from potentially less adhesive contacting the sides of the wire traces.

In addition to an investigation of how to insulate the wires from any necessary adhesive, a number of other ideas for useful future work are: modeling the effects of (a) corners of the wires due to the interdigitated pattern (b) wires at edges of strip which are not surrounded by the complete interdigitated pattern, which will perhaps necessitate a fully three-dimension model and hopefully corroborate the experimental finding that increased spacing (pitch) can increase resistance substantially. A three-dimensional model will also be able to refine our estimate of the scaling of resistance total wire length. It should be possible to optimize the resistance given a fixed copper coverage constraint.

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