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Superconductive Silicon Nanowires Using Gallium Beam Lithography

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LDRD 159300 : Superconductive Silicon Nanowires Using Gallium Beam Lithography

M. David Henry and Robert Jarecki - MESAFab Operations

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Abstract

This work was an early career LDRD investigating the idea of using a focused ion beam (FIB) to implant Ga into silicon to create embedded nanowires and/or fully suspended nanowires. The embedded Ga nanowires demonstrated electrical resistivity of 5 mΩ-cm, conductivity down to 4 K, and acts as an Ohmic silicon contact. The suspended nanowires achieved dimensions down to 20 nm x 30 nm x 10 μm with large sensitivity to pressure. These structures then performed well as Pirani gauges. Sputtered niobium was also developed in this research for use as a superconductive coating on the nanowire. Oxidation characteristics of Nb were detailed and a technique to place the Nb under tensile stress resulted in the Nb resisting bulk atmospheric oxidation for up to years.

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NOMENCLATURE

MESA	micro electro
DOE	Department of Energy
SNL	Sandia National Laboratories
Ga	gallium
Si	silicon
NW	nanowire
SC	superconductivity
ICP	inductively coupled plasma
RIE	reactive ion etcher
RTA	rapid thermal anneal
LHe	liquid helium
FIB	focused ion beam
T_c	critical temperature
SCE	superconductive electronics
SOI	silicon on insulator
BOX	buried oxide
q	charge of an electron
SPA	semiconductor parameter analyzer
MPMS	magnetic property measurement system

1. INTRODUCTION

The research performed in this LDRD was to investigate effects of superconductivity (SC) in nanowires (NW) using gallium implantation in silicon using a focused ion beam (FIB). Two paths were taken to achieve this objective: 1) implantation of Ga followed by rapid thermal anneal (RTA) to create an embedded superconductive line in Si, and 2) implantation of Ga in Si, followed by an inductively coupled plasma reactive ion etch (ICP RIE) to define the suspended NW, and finished with deposition of a sputtered niobium film.

1.1. Project Goals

The goal of the LDRD was fundamentally simple, create a method to achieve superconductive nanowires and understand the technical problems limiting fabrication of said devices. Primarily the path was to utilize recent results from a 2010 and 2011 applied physics letter [1], [2] in which Ga was implanted at 100 kV into silicon, annealed and demonstrated superconductivity at 7 K. This result was to be combined with another 2010 paper from Nanotechnology [3] in which Ga was implanted in silicon and then an ICP RIE was used to etch nanoscale features. This LDRD combined both methods but deviated by focusing on using a lower implantation voltage of 30 kV of a FEI tools FIB. Since this tool has a very small beam waist, down to 4 nm, very small features could rapidly be written in silicon and either method pursued. The reward for pursuit of this technology would be a method to either have an extremely simple method for creating SC Ga NW and/or silicon NW writable using a FIB.

Implanted Ga Nanowires Embedded in Silicon: This method for fabricating SC NW was largely based on the work of Skrotzki et al.[1], [2] in which Ga was implanted into silicon at 100kV though a thin oxide layer. After implantation, a rapid thermal anneal would drive the overdosed Ga layer up to the oxide-silicon interface. The layer would be under enough compressive stress that the Ga would demonstrate superconductivity at 7 K. This LDRD was structured such that a FIB could implant the Ga layer and an RTA could anneal out the Ga to the interface. A unique feature of this LDRD would be to implement this effect using the FIB and that a FIB could create implantation length scales down to the tens of nanometers. The major risk of this method was that Ga implantation was not a confirmed result by anyone outside of the German research group nor was it understood that it would be feasible at lower implantation voltages using the FEI FIB.

Suspended Ga-Si Nanowires with Niobium Coatings: The second method was to utilize a dry lithography technique where the FIB again implanted a Ga layer into the silicon in the shape of a nanowire. However, this method would use a highly selective and accurate etch to define the nanowire and suspend it in one step as demonstrated by Henry et al.[3], [4] Then with a suspended nanowire, a SC metal such as niobium could be sputter deposited leaving a SC coated NW. Pursuit of NW using this method had a fair amount of technical risk involved. A fabrication sequence would need to be developed for both the etch and the sputter deposition. At the start of the LDRD, there was no superconductive depositions available in the μFab nor was there an etch as sensitive as to what was required for this project. Further, the SC film would need to be thin and superconductivity is greatly altered based on film thickness. This film thickness could be altered in very different ways. It was also very unclear, at the start of this,

what the effect of suspending SC would be and how a SC NW made in this fashion would behave.

2. GA LITHOGRAPHY IN SILICON FOR SUPERCONDUCTING NANOWIRES

This chapter details the method of lithographically defining Ga structures in silicon using the collimated FIB. This method is distinct from standard FIB oblation or milling where Ga is implanted into a material above the solid solubility and material is sputtered away defining a structure. In this method, areal doses around 10^{16} to 10^{17} cm^{-2} are implanted into silicon by rastering a collimated FIB in a defined pattern. With a 30 kV beam, Ga is implanted into silicon approximately 25 nm, with a 10 nm straggle defining a total thickness of approximately 20 nm. Using Ga focused down to beam waists of 4 nm, structures down to 20 nm can be defined. At this point two different routes can then be taken. In the first method, a rapid thermal anneal drives the Ga to a silicon oxide interface where the Ga piles up. This creates a thin embedded Ga structure in the silicon. A second method utilizes an ICP RIE to selectively and anisotropically etch the silicon away leaving only the Ga, and silicon under the implanted Ga, remaining. By then tuning the etch to become isotropic, the structure can be released leaving a fully suspended structure. This technique follows that of Henry et al.[3]

2.1 FIB Implantation Into Silicon

This work utilized a FEI Nova 600 dual beam (SEM and Ga beam) FIB. If the structure was desired to be embedded into the silicon, a thin thermal silicon dioxide was grown with variable thickness (typically less than 30 nm). If the structure was desired to be suspended, no oxide was grown. Although the tool could handle a full 150 mm (6”) wafer, smaller pieces were utilized which were typically cleaved into 1 cm x 1 cm samples. These samples were mounted on a SEM stub using copper tape and if oxide was present on the silicon, better imaging was achieved by rolling the end of the copper tape onto the top corner of the silicon sample. This greatly reduced charging by providing a path for charge to dissipate. The sample was loaded into the SEM and eucentric height was determined; typically at a stage height of 5 mm and 52.5 degrees, the electron beam and the Ga beam could be focused on the same location on the sample. At the edge of the sample, the beams could be turned on and focused; the Ga beam should be turned off after focusing so the sample would not get inadvertently dosed.

A FIB typically has multiple implantation voltages and beam currents available. Beam voltage directly controls implantation depth, straggle, skewness and kurtosis, [Fig 1]. Beam current controls implantation rate and beam waist. For this work, 30 kV beam voltages were used to achieve the thickest Ga layer possible. Beam current was varied based on the implantation size. If the structure was large, such as the 50 μm contact pad, the beam current was typically set to 6.5 nA or 20 nA (a 143 nm beam waist) which had a large beam waist but permitted patterning of the micron scaled structures with reasonable implantation times. For the smaller nanowire structures, 260 pA beam current was typically used which had a 15 nm beam waist. Lower beam currents available on this tool could achieve beam waists down to 4 nm. The effect of ion beam parameters could be simulated, with accurate results, using the Stopping Range of Ions in Matter (SRIM) by Ziegler et al., [Fig 2].

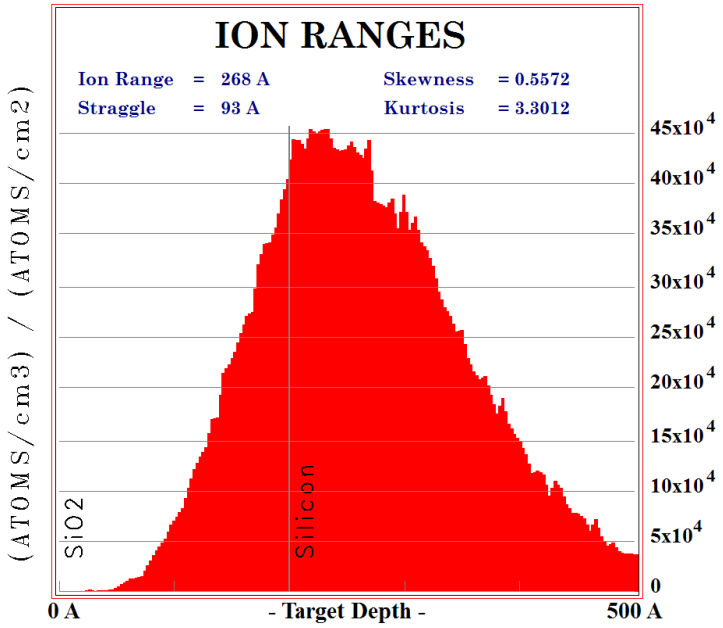

Figure 1. TRIM simulations for implanting 30kV Ga through 20 nm of SiO_2 and into Si. The graph provides a method to convert areal dose to volumetric dose. The implantation depth is 26.8 nm and thickness of the Ga layer is 18.6 nm.

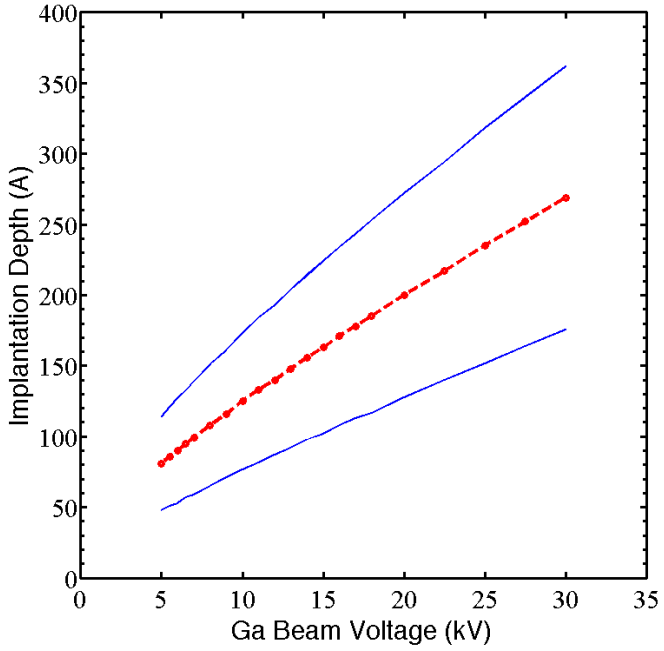

Figure 2. SRIM simulations for implanting 5-30kV Ga into Si. The center line (red dash) indicates the mean implantation depth, the outer lines (blue solid) indicate the straggle length.

By controlling the implantation time (t), area and beam current (BC) the areal implantation dose could be controlled. The following equation illustrates this relationship:

$$Dose = \frac{BC * t}{10^4 * q * (LxW)} \tag{1}$$

In this equation, q is the charge of an electron, L and W are the length and width of the structure to be defined. The areal dose calculated in eqn. (1) can then be related to the implantation dose by Fig 1. To understand how much Ga should be implanted, it should be related to the solid solubility of Ga in Si, which is about 0.1 at. %. This equates to about $5x10^{19}$ cm^{-3} Ga in Si, or an areal dose of $1x10^{14}$ cm^{-2} before the Ga begins to precipitate out of the Si substrate. Taking Si to have $5x10^{22}$ atoms / cm^3, if the Ga starts to approach this dose Si should begin to sputter out. This places an upper limit of $1x10^{17}$ cm^{-2} areal dose for implantation. In the work presented here, areal doses ranged between 10^{16} to 10^{17} cm^{-2}; this value was based on achieving reported results of both superconductivity and etch masking. These dose values, when combined with the desired area permitted a relation between BC and t. Although BC is greatly determined by length of write time, other subtle factors include ion channeling and charge dissipation rates distorting the implanted structure fidelity. [Fig 3] is a SEM of an example implantation of Ga into silicon through an Al contact pad. The nanowires were defined using a 26 pA beam current at 30 kV. All nanowire lengths were 30 um and the dose was scaled such that 1 second would give a 100 nm NW a dose of 0.5 x 10^{16} cm^{-2}. The write times were 8, 6.2, 4, 3.1, and 2.2 seconds for the 200, 150, 100, 75, and 50 nm NW widths.

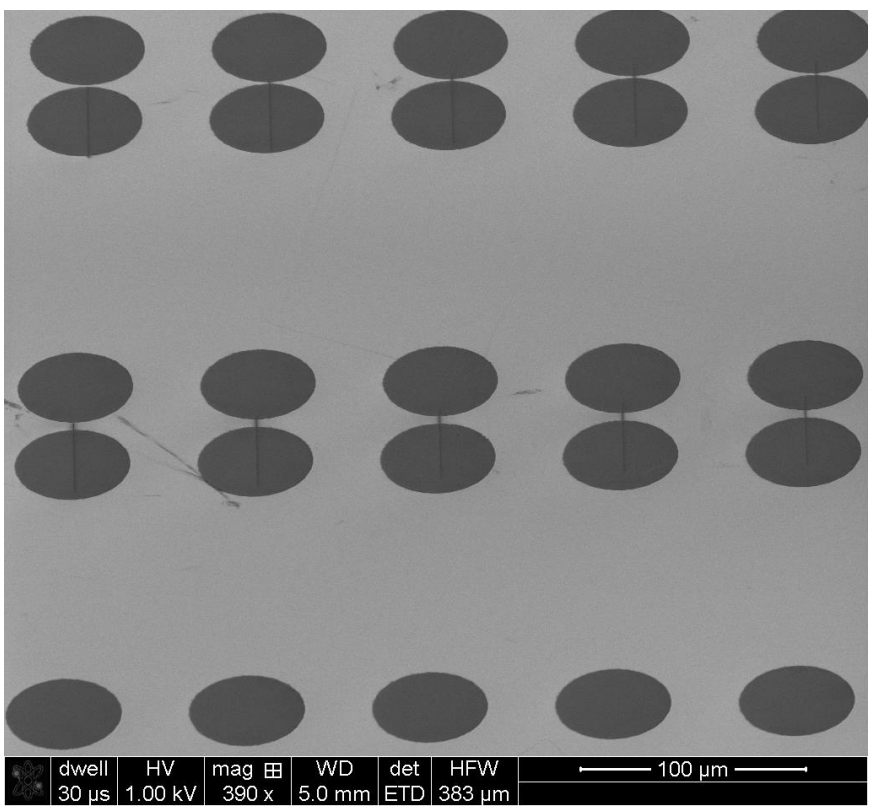

Figure 3. SEM of 50 um diameter Al contact pads with implanted Ga nanowires connecting the two pads. The width of the wires are 200. 150, 100, 75, and 50 nm. The lengths of the wires were varied by 10, 5, 2.5, 2, 1.5, 1 um.

At this junction, the samples can be either plasma etched to suspend the nanowire or annealed to drive the Ga to the silicon-oxide interface. In what follows, the etching parameters are first described, followed by understanding how implantation dose affects the etching properties, followed by a brief description of the RTA.

The etches were performed in a Plasma Therm ICP RIE using a Bosch like process (nicknamed pseudo bosch) which defined the structure. An isotropic etch was then used to release the nanowire. Since the starting wafer was typically SOI with ½ um device layer, the etch was fairly short landing hard on the BOX layer. Typical etch parameters for the tool are as follows:

- SF_6/C_4F_8 - 50 / 90-110 sccm
- ICP / Fwd - 900/20 Watts
- Pressure - 10 mTorr
- HeBacking- 4 Torr

This etch was typically performed for 60 to 90 seconds with an approximate etch rate of 400 nm per minute. Once the etch step completed, the etch tool would automatically shift to zero flow of C_4F_8 and an increase of ICP power to 1000 W with no Fwd power applied. These conditions defined the release step; typically 11 seconds long. It should be noted that the release step could be omitted if the release of the structures was undesired. The maximum etch depth achievable is determined by the areal implantation dose. To demonstrate this concept, a dose matrix was constructed to determine how long a given implantation dose could hold out. It is assumed that unless a dose was greater than the 10^{17} cm^{-2} areal dose, the majority of the Ga should be contained within a 20 nm band approximately 25 nm below the surface of the silicon. This assumption is based on TRIM simulations described earlier. How long the implantation mask holds out against the plasma etch will be determined by the rate of sputtering of the Ga layer. If the layer is highly dense, a GaF or GaO_x will form from the etch chemistry, and the nonvolatile layer will only be subjected to mechanical milling. If the volatile etch rate of the silicon (about 400 nm/min) can exceed the mill rate of the thin Ga layer (~5 nm/min) then a high selectivity can be achieved. To describe this selectivity more quantitatively, squares of identical sizes were implanted with different doses. Then multiple etch times were run on identical samples. By measuring the overall etch height, a set of curves can be established to understand the minimum required dose for achieving the etch height of the structure, [Fig 4].

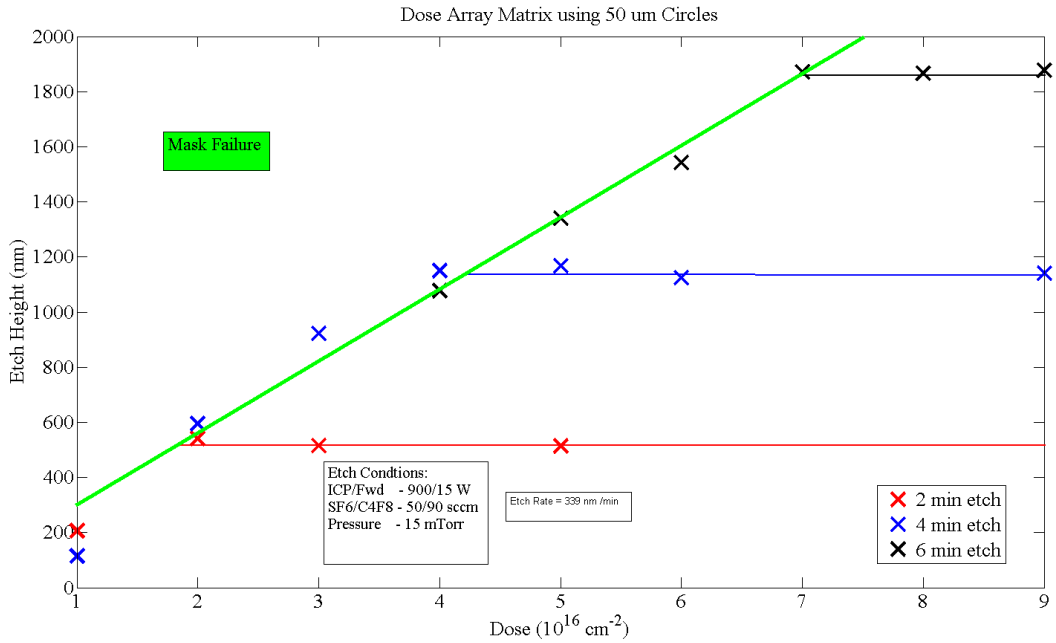

Figure 4. Established dose array for using implanted Ga as an etch mask. By implanting the appropriate dose to stay to the right of the diagonal curve, the expected fidelity of the etch mask can be achieved for the required etch depth.

By understanding the dose required for the given etch depth, a minimum required dose is established with the upper dose still being that of not milling the structure away. Another effect dose can play on the physical aspect of the structure is to change the physical dimensions of the structure being etched. To understand this effect, recall that the Ga beam is approximated as a Gaussian beam where the beam waist describes the full width half max. Compounded to that distribution, a perfect delta function beam impacting the silicon has a dose distribution described by the straggle. These two factors combined result in a Gaussian distribution of dose in the silicon. The pattern is created by rastering the beam to have 50% overlap as defined by the beam waist and not by the combination of beam straggle times the beam waist. The convolution of the two Gaussian beams then, results in another Gaussian beam for the final dosing profile, which defines the final lithography of the structure. But the final etched structure also relies on the etch selectivity as seen in figure 4. Although a 20 nm structure is desired, the final result is a slightly larger structure than that desired. Although the dosing profile is approximated as Gaussian and the dose profile is linear, the combined effect becomes difficult to calculate and predict.

A more practical approach was taken to characterize what the resulting structure fidelity is after etch. A set of squares were implanted creating an array such that in the column dimension the areal dose was varied in 1 x 10^{16} cm^{-2} increments from 1 to 8 and in the row dimension the size of the square was varied to have the following sides: 20, 30, 40, 50, 60, 80 and 100 nm. The structure was then etched for 500 nm, [Fig 5]. Measurement of the difference between the desired structure and the actual pattern, referred to here as fidelity, indicates that pattern transfer reaches optimum at ~4-5 x 10^{16} cm^{-2} areal dose, [Fig 6].

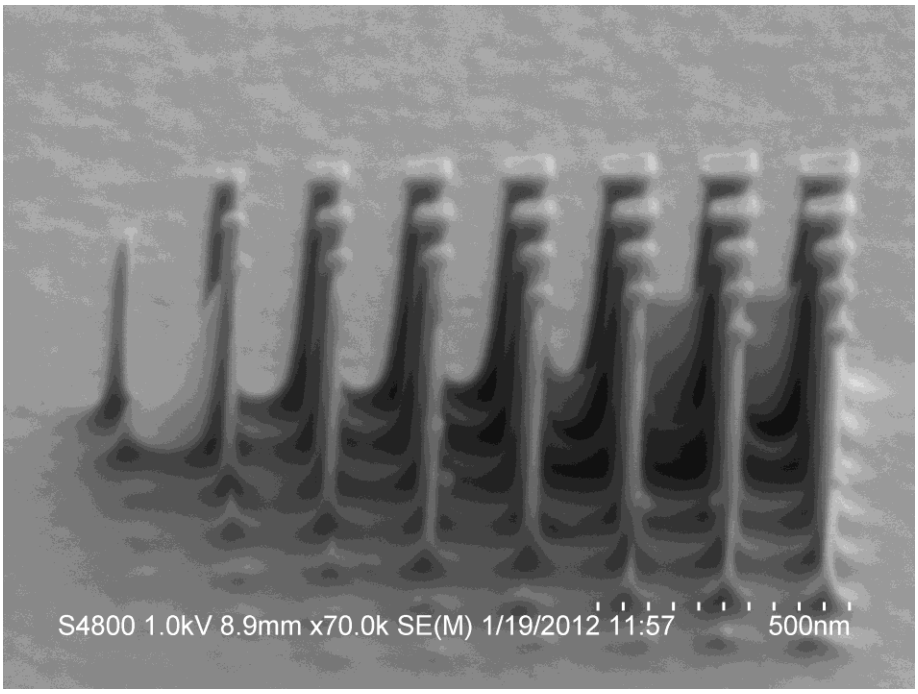

Figure 5. Etch matrix to establish the relationship with implantation dose, varied from 1-8 x 1016 cm-2 in the columns, and sizes of 100, 80, 60, 50 , 40, 30, 20 nm in the rows.

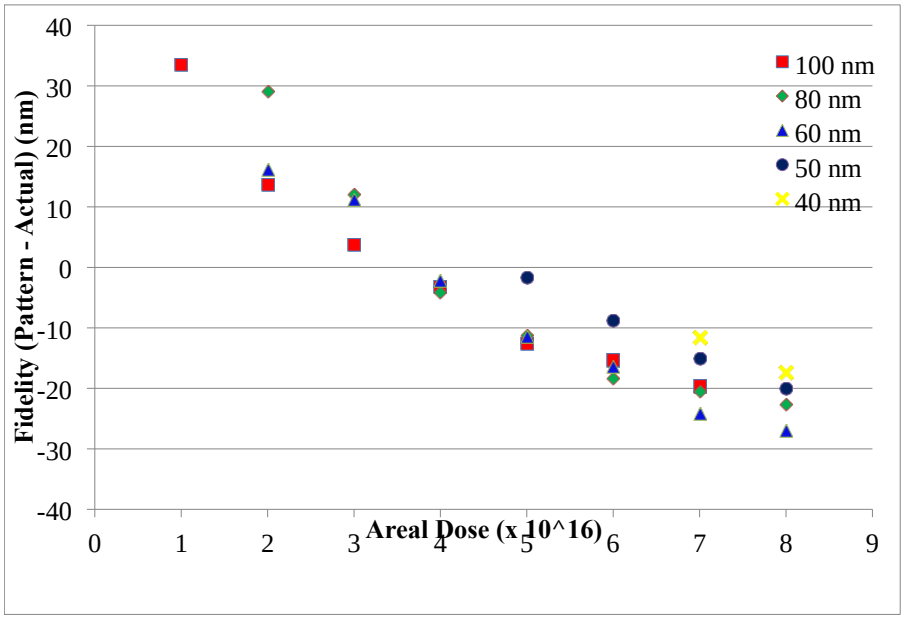

Figure 6. Fidelity of desired structure after implant and etch. A negative value indicates that the structure is larger than desired. Note the tops of pillars are larger than the structures, this graph describes the etch masks on top.

The fidelity array also demonstrated that as the structures were reduced in size, the higher doses were needed to adequately mask the structures for the ½ micron etch. Note that the 30 and 20 nm structures existed at one point during the etch, but the mask did not hold for the entire thickness. With the dose array and fidelity array complete, lateral structures could be fabricated.

Two sets of example structures were made. Similar to that seen in [Fig 3], two 5 um diameter circles were connected with rectangles 5 um long and variable widths. The smaller contact pads were used to significantly decrease FIB write time. These structures were first etched with the pseudo bosch etch and imaged to verify that the etch profile was acceptable. An example etch is seen in [Fig 7] and [Fig 8]. The etch profile was good enough to generate a structures ½ micron tall with widths below 40 nm implying that the etch did not undercut 20 nm on both sides. By taking the arctangent of 20/500, the sidewall profile was better than 88 degrees vertical with no undercut detectable.

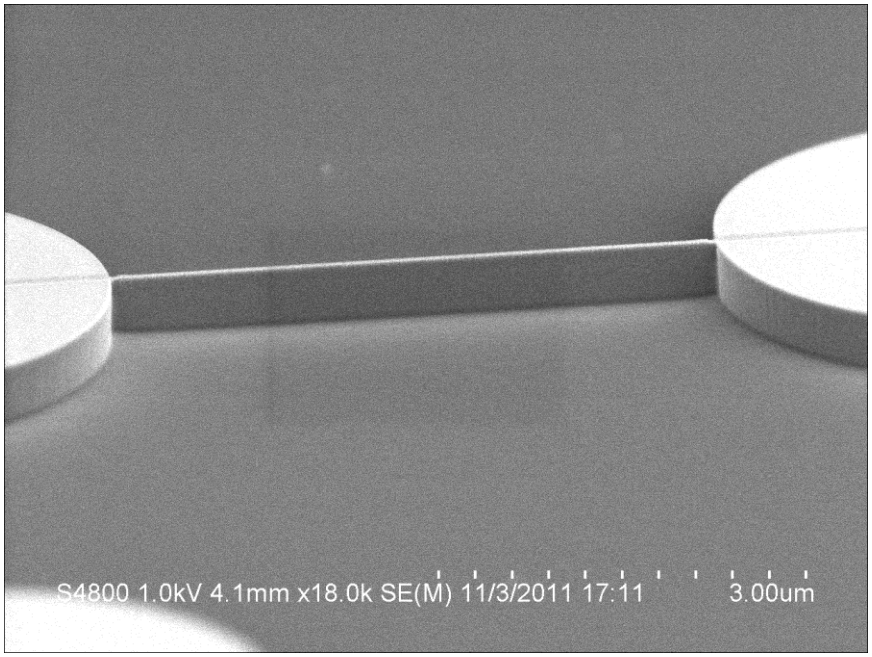

Figure 7 SEM of ridge etched ½ micron into silicon. Circles are 5um in diameter and ridge is 5 um long. Release etch has not been performed.

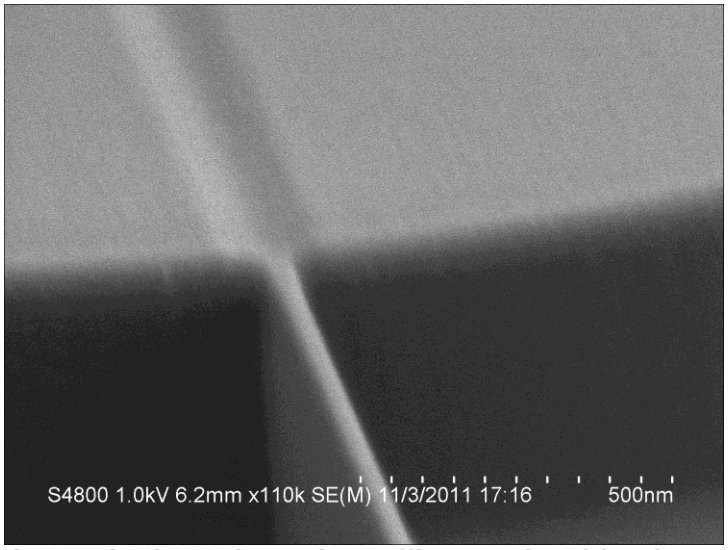

Figure 8 SEM of ridge etched ½ micron into silicon. The ridge is approximately 40 nm wide by 500 nm tall indicating that the etch was calibrated vertical to better than 88 degrees.

With the etch calibrated, the release etch was then performed. This was achieved by changing from a pseudo bosch etch to an isotropic release etch. The result was that the silicon under the Ga implant was etched away leaving a nanowire fully suspended, [Fig 9] and [Fig 10]. Although the 5 um pad was also etched, it was left mostly intact as the silicon under the wire was seen to be completely removed.

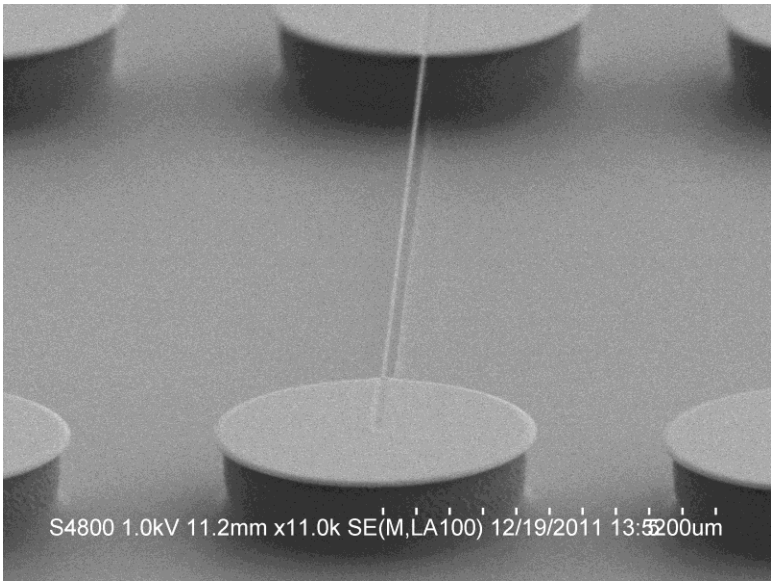

Figure 9 SEM of fully suspended nanowire.

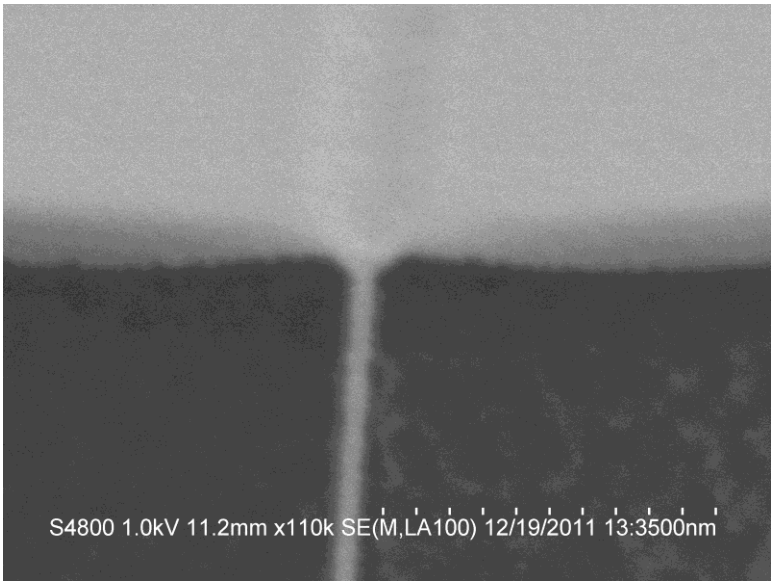

Figure 10 SEM of fully suspended nanowire with dimensions down to 30 nm wide and 5 um long. Indentation in the circle can be seen due to having been twice implanted from the circle write and the rectangle write.

The structures fabricated were not limited to the simple suspended structure. As a demonstration of what could be achieved, two other structures were fabricated. The first structure was similar

to the suspended nanowire, but the additions of 3 more circular pads were pattered with nanowires connected to the main nanowire, [Fig 11]. This would provide a structure such that if a current were injected into the wire, a voltage along the length of the wire could be measured in Kelvin resistance measurement. The second structure fabricated was the generated using a .bmp file of the Sandia National Labs thunderbird logo, [Fig 12]. By adjusting the magnification and specification of the write area, the resulting pixel size was 25 nm patterned the thunderbird.

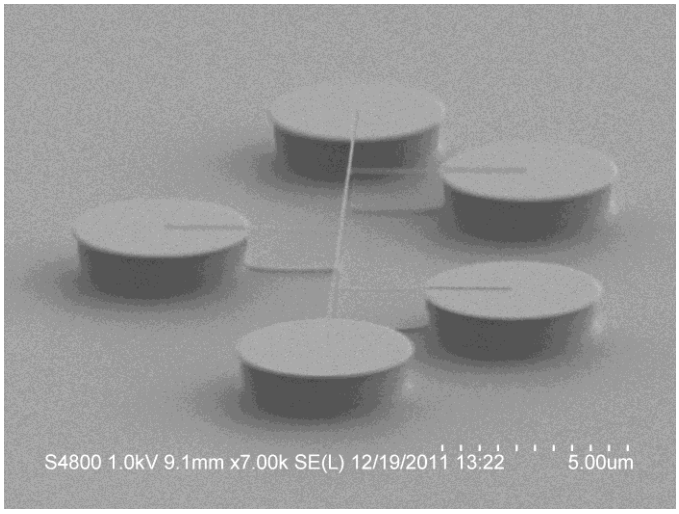

Figure 11 SEM of fully suspended nanowire with dimensions down to 30 nm wide and 5 um long. Indentation in the circle can be seen due to having been twice implanted from the circle write and the rectangle write.

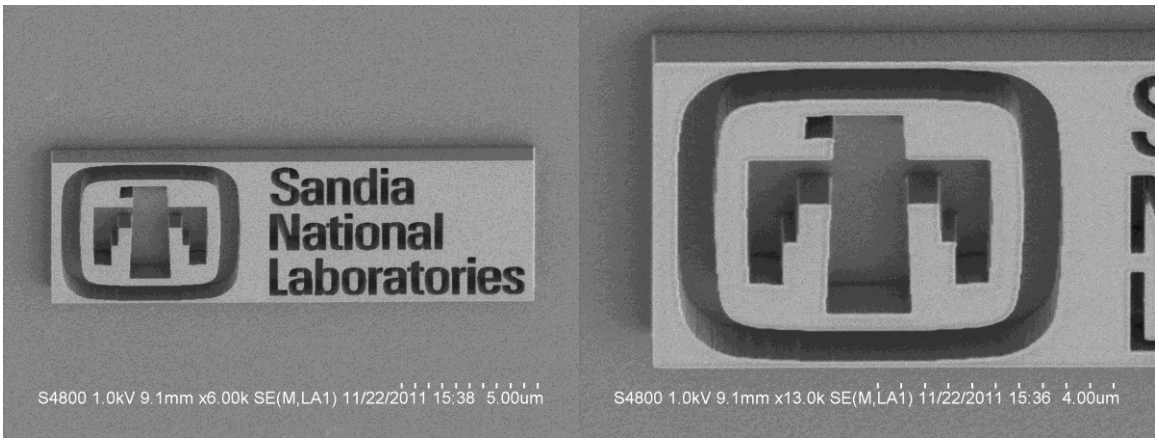

Figure 12 SEM of fully suspended nanowire with dimensions down to 30 nm wide and 5 um long. Indentation in the circle can be seen due to having been twice implanted from the circle write and the rectangle write.

2.2 Electrical Measurement of Ga Implanted Si

Before cryogenic or vacuum measurements of the nanowires could be made, an understanding of how the conductivity of Ga implanted silicon was required for a bulk material. Particular questions which required understanding included: contact resistance of tungsten probe tips to the

Ga layer which resided about 20 nm below the surface of the silicon, would that contact be Ohmic, what is the resistivity of the Ga implanted silicon, and how did the silicon behave in the LHe temperatures.

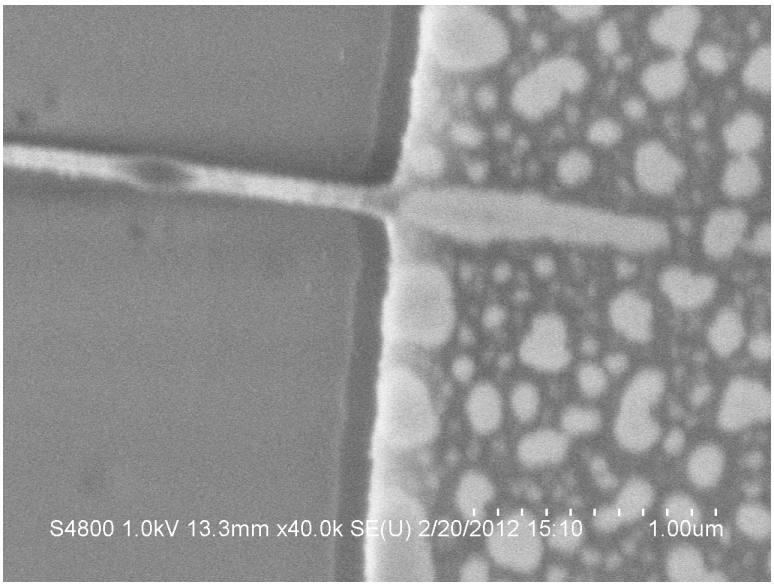

Figure 13 SEM of etched nanowire and pad. In both structures, light areas are observed to be Ga segregated out of the silicon due to over dosing during implantation.

Since Ga is in the periodic table under column III, it is expected that if it activates and becomes bound in the silicon matrix, it would perform similar to boron in that it would donate a hole at a mobility 2-10 times less measured by Tsai et. al.[5] With implantation levels so high, the implanted area would be expected to act as a P+ region. However, all of the doping will not activate and that amount of Ga not activating will locate itself interstitially between grain boundaries and aggregating into substantial collections. This second feature was observed in some of the structures etched when implantation dose was high, [Fig 13]. From a conductivity standpoint, this interstitial Ga should still improve the electrical conductivity. Together, the higher dosing and higher conductivity made an Ohmic contact when a tungsten probe tip is placed on the implanted silicon. This contrasts markedly different to a tungsten probe tip contacting silicon, making a Schottky contact. More information on Ga in silicon can be found here, [5]–[9].

Both of these contacting effects were measured on a probe station using a Keithley 2400 multimeter controlled by Matlab via a GPIB-USB controller from National Instruments. This method of testing permitted running I-V sweeps of different integration times and at different rates. Measurements were performed by contacting a tungsten probe tip to the silicon or implanted area, [Fig 14]. The W-Si contact demonstrated a Schottky diode with turn on voltage around 0.2 V and an I_o of 4.3×10^{-7} A. When the W tip contacted the implanted Ga, albeit only 20 nm thick, a very different IV curve emerged. By implanting Ga, the contact became very Ohmic. Moreover, as the implant areal dose increased, the resistivity of the contact decreased.

A very subtle 'S' shape in the curve around V=0 also emerges; a behavior that is described by thermionic-field emission theory. This theory requires a barrier height low enough that electrons can thermally jump over it and thin enough that electrons can also tunnel through. A W-Si contact itself does not permit either of the two conditions to be met; the depletion region for $5x10^{15}$ cm^{-3} is 381 nm wide given a W-Si (p-type) barrier height approximately 0.67 eV. By implanting the Ga to 20 nm thick and approximately to $1x10^{20}$ cm^{-3} dose, the barrier height gets reduced from 0.64 eV to 0.03 eV using the following equation:

$$\Delta\phi_{Bp} \sim \frac{q}{\epsilon_{Si}}\sqrt{\frac{N_{Ga} * t_{Ga}}{4\pi}}$$

Here, N_{Ga} is the doping level achieved by implantation and $\Delta\phi_{Bp}$ is the barrier height reduction. Since both the barrier height and barrier thickness become reduced, the charge carriers can now be described by thermionic field tunneling.

$$Rc = \frac{V_{th}\sqrt{V_{oo}}Cosh\left[{V_{oo}}/{V_{th}}\right]Coth\left[{V_{oo}}/{V_{th}}\right]}{A^{**}T^2\sqrt{\pi\left(\phi_{Bp}-\phi_p\right)}} * Exp\left[\frac{\phi_{Bp}-\phi_p}{V_{oo} * Coth\left[{V_{oo}}/{V_{th}}\right]} - \frac{\phi_p}{V_{th}}\right]$$

where V_{th} is 0.02582 V, T is temperature, A** is the Richardson Constant, and

$$V_{oo} = \frac{\hbar}{2} * \sqrt{\frac{N_{Ga}}{m * \epsilon_{Si}}}$$

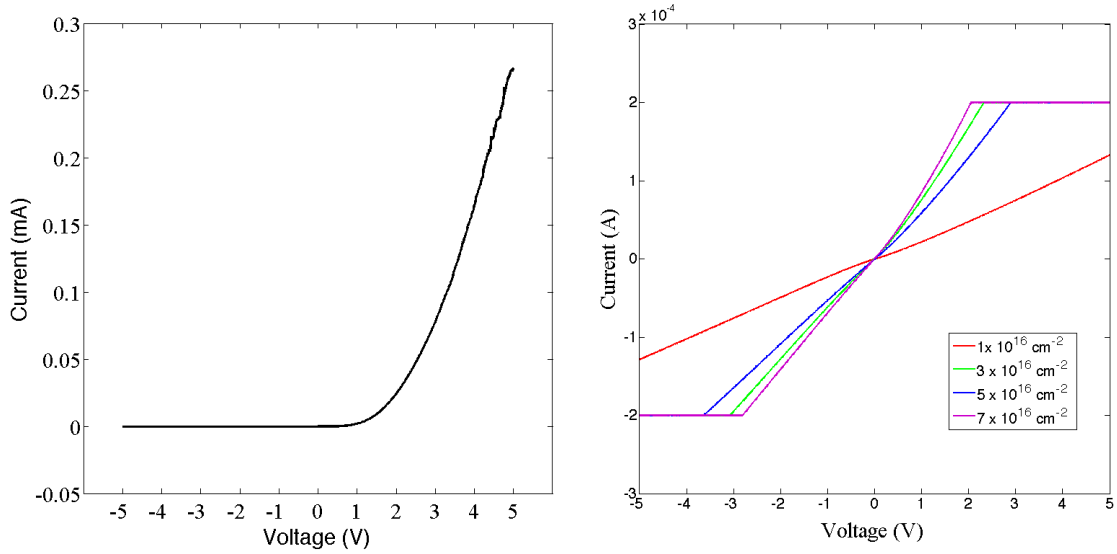

Figure 14 I-V curves of tungsten probe tip contacting silicon creating a Schottky diode-contact (left) and the tungsten probe tip contacting the un-annealed implanted Ga creating Ohmic contacts of reducing resistivity as dose increases (right).

The contact resistance equation explains the slight 'S' curvature of an otherwise straight resistance line. From the I-V curves, the contact resistance could be calculated from the derivative of the measured I-V curve at V=0.

$$R_c = A * \left(\frac{dI}{dV_{V=0}}^{-1} - R_{Spread} \right)$$

$$R_{spread} = \frac{\rho}{2\pi r} * (\tan^{-1} \frac{2\,h}{r})$$

Here, A is the implant contact area (pi*25^2 um^2), R_{spread} is the resistance of the current traversing through the wafer thickness from a contact (approximately 990 ohms for 675 um thick 10 Ω-cm resistivity silicon), ρ is the wafer resistivity and h is the wafer thickness. For implantations above 2 x10^{16} cm^{-2}, the contact resistance was about 0.3 Ω-$cm^{2,}$ [Fig 15]. This value supports the I-V results suggesting that the contact is a combination of carriers tunneling and thermally excited over the barrier. This work follows that of Henry 2010 [10].

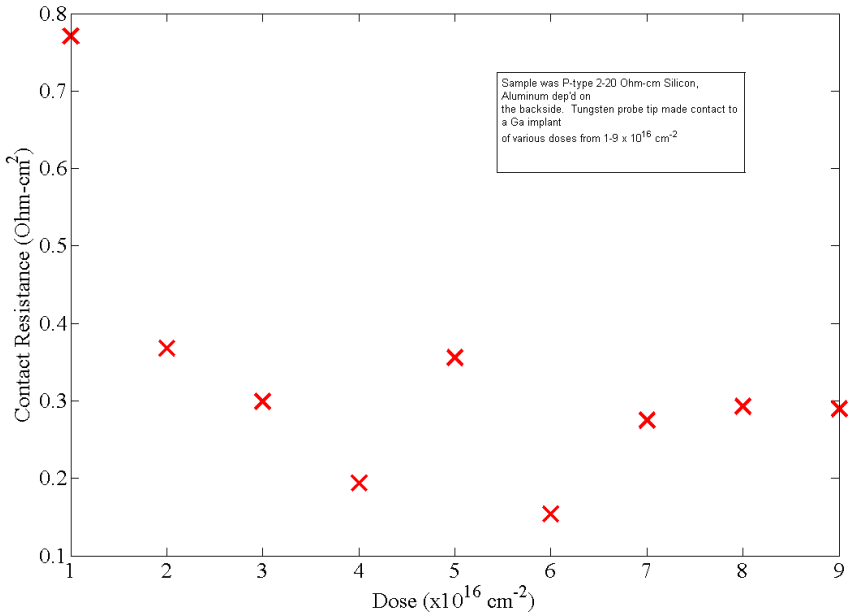

Figure 15 Contact resistance of 50 um diameter circles implanted with Ga for 1-9 x10^{16} cm^{-2} areal dose in P type silicon.

Although the data suggests a good Ohmic contact, previous research has suggested that annealing using RTA could reduce the contact resistance by almost a factor of 10 for anneal temperatures around 450 C, Langfischer et. al,[7] and 600 C, Mogul et. al.[8], [9] For temperatures too low or too high the resulting effect of annealing was an increase in the contact resistance from that 'as implanted'. Since the future state of the implanted Ga was needing an RTA to establish the correct conditions for superconductivity, understanding what annealing did to the devices was a critical measurement. Two RTAs were performed on the devices. The first was performed at 400 C for 30 seconds under an argon purges chamber and the second was performed at 650 C for 60 seconds; also in an argon environment. For the 400 C anneal, the resistance of the contacts increased, albeit only slightly. Once the 650 C anneal was performed, the contact resistance decreased by a factor of 10; a very similar result to that described by Mogul et. al, [Fig 16].

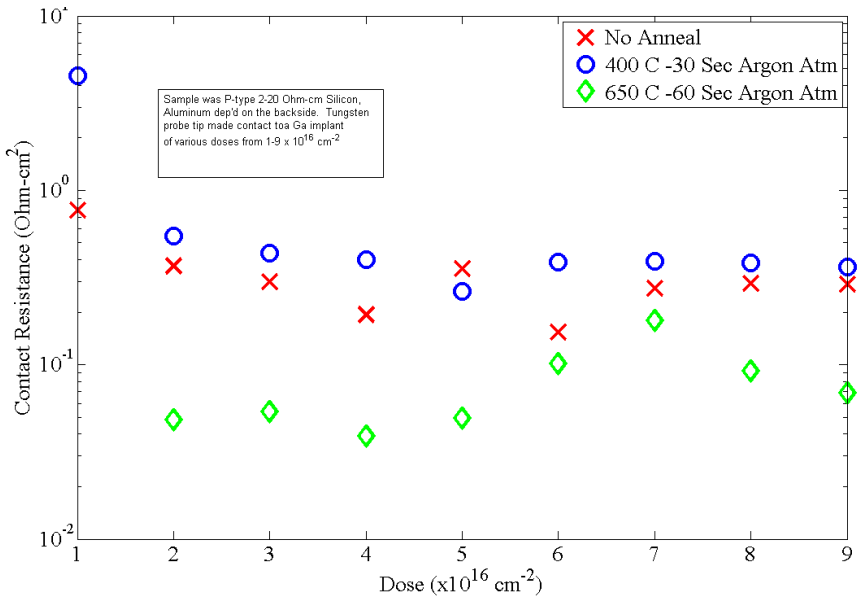

Figure 16 Contact resistance of 50 um diameter circles implanted with Ga for 1-9 x10^{16} cm^{-2} areal dose in P type silicon then annealed at 400 C followed by 650 C.

2.3 Electrical Measurement of Ga Implanted Si Nanowires

With a thorough understanding of how the implanted Ga electrically behaved in silicon, devices could be created using this method with a reasonable understanding of how to electrically test them. The electrical testing was critical to the research goal of creating a superconducting nanowire. The next challenge was to confirm that nanowires could be contacted using the W probe tip and that they would be able to be tested under cryogenic and vacuum conditions. During this testing, the physical model used to describe the nanowires was constantly evolving. As testing progressed, factors where demonstrated to be important which were not first considered significant. One such parameter was the changing resistivity of unannealed samples; as I-V sweeps were conducted the resistivity of the devices decreased. Other parameters, which changed during testing, were pressure induced resistivity variations, stage temperature induced resistivity changes, and light induced carrier injection. This section will briefly discuss the results of the testing and what conclusions could be brought based on the data.

The first set of nanowires tested were devices created by using the implant lithography and etch technique described in section 2.1. One particular set of devices fabricated were implanted to a dose of 4.2 x 10^{16} cm^{-2} and with dimensions of 10 um long, 20 nm thick and 80,100, and 140 nm wide. The samples were submounted to a chuck in a lakeshore cryostat and contacted with W probe tip to an Agilent semiconductor parameter analyzer 4156C. Probe tips were touched down on 50 um diameter pads which connected across the nanowire. Atmospheric and room temperature I-V measurements were first taken to verify a linear, Ohmic relationship [Fig 17]. The data confirmed the relationship with the additional 'S' curve. Although the previous section demonstrated that part of the curvature was related to the W-P^+-P-type silicon contact, it is also likely that device physics of nanoscale structures also influences the I-V relationship. A second obvious relationship of increasing resistance (inverse of the I-V slope) with a reduction in nanowire width was observed. The slopes past 1 volt yielded resistance values of 108.7 MΩ,

62.2 MΩ, and 41.9 MΩ for the 80, 100 and 140 nm width nanowires respectively. The resistivity is then calculated to 1.7, 1.24, and 1.17 Ω-cm respectively, generally consistent across the wire dimensions. This indicated that suspended structures could be electrically operational.

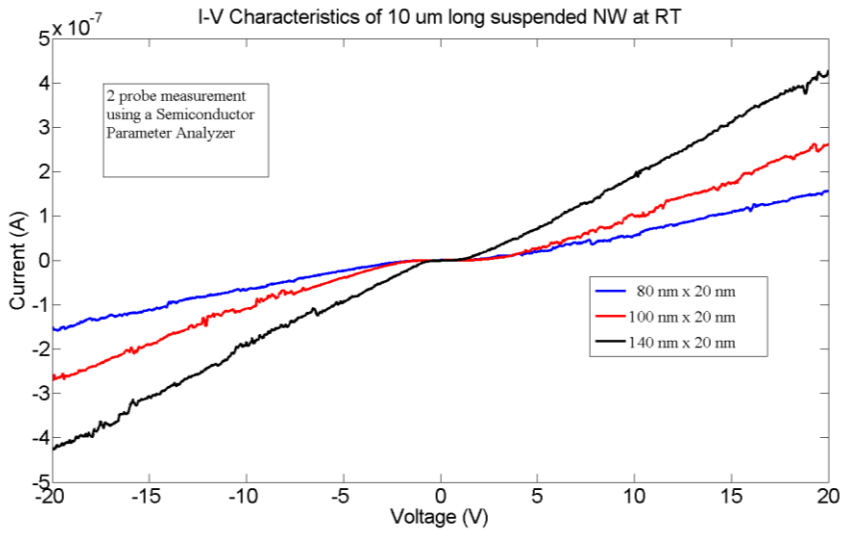

Figure 17 Two-probe I-V measurements of suspended nanowires 80, 100, and 140 nm wide by 10 um long using a SPA.

The next logical progression was to test the nanowires under cryogenic operation to verify normal (as compared to superconductive) conduction. Since the nanowire is a hybrid of P^+ silicon with interstitial and segregated Ga metal, it was expected that as the suspended wire was cryogenically cooled down, carrier freeze out would occur. This idea was confirmed in the Lakeshore cryogenic station. A suspended 128 nm wide, 20 nm thick, 10 um long nanowire was placed on the cryo-stage and the chamber pumped to a 10^{-4} Torr vacuum level. The cryo-stage is an open LHe flow and is controlled by throttling LHe flow and using a stage heater. The stage temperature was measured and controlled using a Lakeshore 331 temperature controller. A slow cool down rate could then be managed such that resistance measurements using the Agilent could be made. By knowing the dimensions of the nanowire and with the measured 2-probe resistance measurements, resistivity dependence on temperature could be determined [Fig 18]. A very clear transition from carrier saturation to carrier freeze out begins to occur around 200 K.

$$\rho = \frac{1}{e * \mu_p(T) * p(T)}$$

$$p = ni * Exp(\frac{E_i - E_f}{kT})$$

Here ρ is the resistivity of the acceptor silicon, μ_p is the mobility of the silicon, E_i is the intrinsic silicon Fermi level, E_f is the Ga doped Fermi level, k is Boltzmann's constant and T is the semiconductor temperature. As the silicon is cooled, the resistivity begins to increase since the thermal excitation of carriers begins to reduce. Although the Fermi level also changes, the dominant source of carriers is from the Ga ions donating holes so E_f-E_i is mostly constant. Mobility improves initially due to phonons beginning to freeze out, which reduces hole

scattering, but then mobility then begins to be limited by the impurity ions causing an electric potential scattering. The overall effect is a further increase in resistivity. Since the Ga implanted silicon is closer to degenerately doped silicon with interstitial Ga, it is expected that the silicon would continue to conduct at cryogenic temperatures.

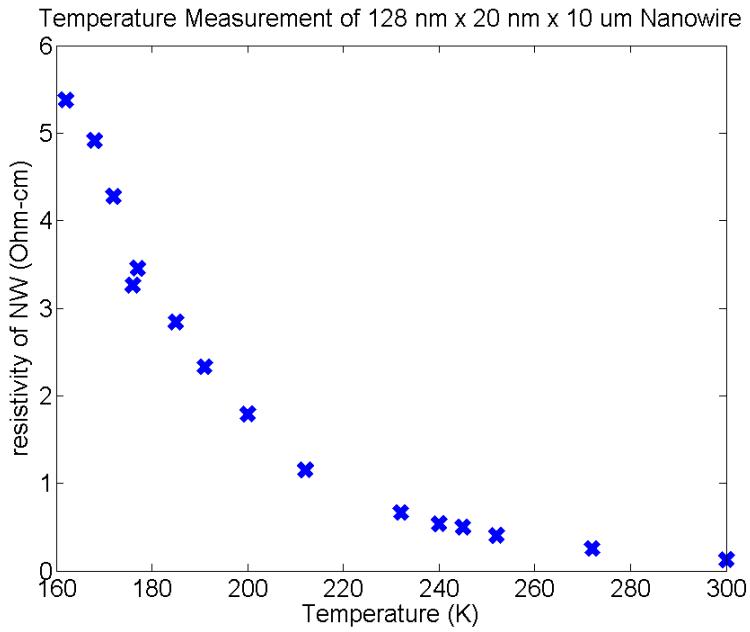

Figure 18 Two-probe I-V measurements of suspended nanowires 128 nm wide by 10 um long while cooling the stage using LHe.

Cryogenic testing proved effective, but a considerable amount of oscillation in resistance occurred based on pumping of the cryostat. This effect is exemplified during resistance measurements of a 175 nm wide by 20 nm thick by 10 um long suspended nanowire mounted in the cryostat stage and held at room temperature. As the chamber was pumped down the resistance was observed to decrease. To better measure this effect, a bleed valve was installed on the chamber and opened while a gate valve to the pump was throttled. For every resistance measurement, the pump throttle valve was adjusted and chamber pressure allowed to stabilize as measured using a micro-pirani gauge. This measurement provided data to establish a clear relationship of resistance to chamber pressure for suspended nanowires.

This effect was determined to be due a Pirani effect. At atmospheric pressure, a voltage applied to the nanowire is measured by applying a given current. As the current passes through the wire, Joule heating occurs as described by Fourier's heat equation. The heating then causes the resistivity of the silicon to decrease. This reduces the measured voltage of the nanowire and hence the measured resistance. As vacuum is pulled in the chamber, the number of atoms, which collide with the nanowire and carry away heat, is reduced. This forces the amount of heat generated in the nanowire to increase, which again reduced the resistivity. The combined effect indicates two very important consequences. First the nanowire is highly sensitive to chamber pressure implying that this makes a very good Pirani gauge. The second is that there is a temperature distribution in the nanowire during normal conduction. The first effect was recognized to be a very good solution to create silicon nanowire Pirani gauges and was explored

in more detail in the next chapter. The second effect established that a very real problem existed for suspended silicon superconductive nanowires. This aspect of suspended silicon nanowires will be discussed in the next section, but this route towards suspended silicon nanowires was abandoned at this point.

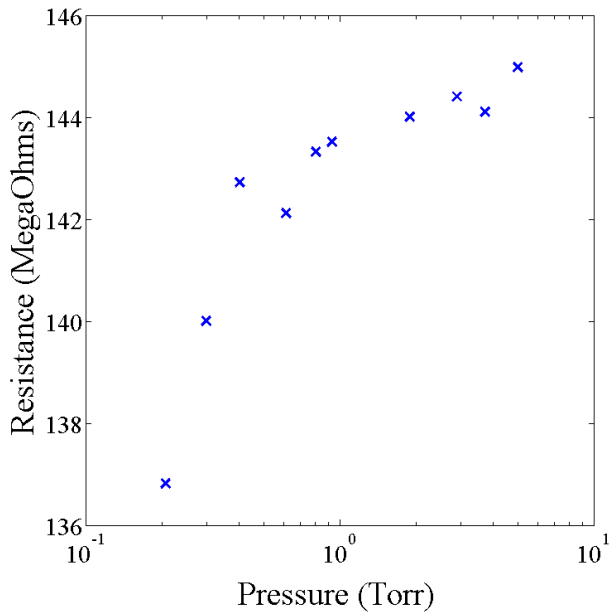

Figure 19 Two-probe resistance measurements of a 175 nm wide, 20 nm thick, 10 um long suspended nanowire as pressure is reduced in the chamber.

During the experiments at cryogenic temperatures, it was noted that electrical conduction in silicon substrate was completely frozen out. This observation implies that if the nanowire were to be tested after implant, and not suspending it with plasma etch, conductivity would still be exclusively through the implanted region with no stray charge through the substrate when the substrate was cooled below 200 K. Hence stopping the fabrication after implantation, [Fig 3], would eliminate the Pirani effect problem observed since every part of the wire would be at the same temperature as the substrate. This route, in the end, proved most effective. However a new problem was observed. Since the cryostat had an optical window for a microscope objective to look through, light was able to impinge on the silicon substrate. The impinging photons onto the silicon substrate generated charge carriers. Since the substrate temperature was around 4 K, the carrier recombination processes had a significant rate reduction; the carrier lifetime was significantly increased.

To quantify the photo-generation effect, a lamp source with 5 different settings (in addition to off) illuminated a 1/3 x 1 mm Ga implanted rectangle with a dose of 4.2 x 10^{16} cm^{-2}. Two tungsten probe tips contacted the surface of the implant and sourced 100 nA. Measuring the voltage permitted resistance to be calculated out. With the window covered, resistance was measured at 50 kΩ. As the light intensity increased, the resistance decreased and was eventually nulled out. This implies that the silicon behaved as a current source generating enough current to offset the injected current driving the voltage drop across the implanted region down to zero. A

linear extrapolation permits a response of the silicon to approximately 30.3 nA per unit of LI (which could be measured by looking at the power output of the bulb).

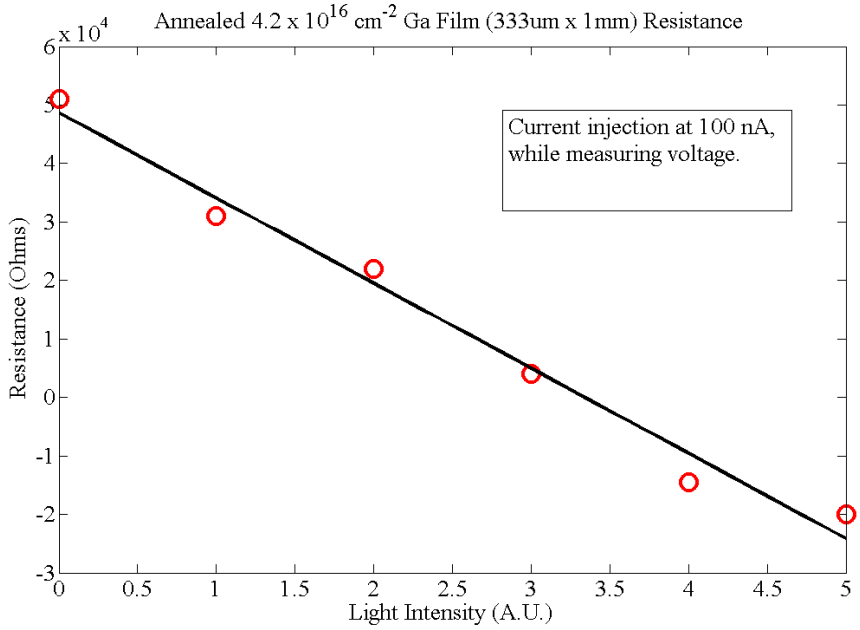

Figure 20 Two-probe I-V measurements of 1/3 mm x1 mm field implanted Ga annealed at 650 C while varying the stage light intensity with stage temperature of 4.2 K.

2.4 Superconductivity of Ga Implanted Si

The objective of this work was to attempt to make a Ga implanted suspended silicon nanowire go superconductive with an objective backup-path-forward of having made a suspended silicon nanowire coated with sputtered niobium. From the electrical testing it was clear that the Ga implanted layer was the primary conduction path, resistivity was low, and connection using W probe tips was successful and nanoscale structures achievable. The measured Pirani effect on the nanowire demonstrated that a suspended structure would not be adequate for accurate superconductive measurements; especially if transition temperature variations, which were expected, could be attributed to multiple effects. One should expect heating from resistive losses, even from superconductive films, but especially from superconductive nanowires. The first reason is that even a pure LTS has electrons comprising of a combination of normal current and super current unless being measured at 0 K. The second reason is that a superconductive nanowire is expected to have a Josephson like oscillation current (AC); even for superconductors, AC current is lossy. So given the calculated 3 K temperature distribution across a typical nanowire, the superconductivity measurement seemed unlikely.

In an attempt to utilize the nanostructures fabricated, given that making nanoscale structures is inherently difficult, the alternative of using a sputtered superconductor on the suspended structure was explored. The created nanowires were first imaged after Nb sputter deposition to ensure dimensions, similar to seen in [Fig 20]. Devices were then measured by sweeping voltage and measuring current (I-V) using the Agilent SPA and calculating resistance. This

measurement was repeated as the stage was cooled. At 220 K, the nanowire measured a resistivity of 228 nΩ-m; a value consistent with having most of the current flow through the Nb film only [Fig 21]. The flatness of the measurements as voltage was swept indicated that the two probe measurement was completely resistive. The inflection in the curve as V=0 was due to the SPA calculating V/I as I was reduced to zero, resulting in an infinity. During further measurements taken as the nanowire continued to cool, a superconductive transition was observed. However, the transition temperature continued to shift from cool down to cool down. This became problematic for understanding if the Pirani effect was why the T_c was shifting, if the Nb is oxidizing and changing the T_c, or if the nanoscale dimensionality was changing. It would be unlikely that heating or dimensionally would alter the measurements from cool down to cool down. For this reason, an extensive effort was put into understanding the oxidation of niobium as described in section 4. The result of those investigations indicated that indeed, the Nb oxidized on the nanowire, greatly changing the transition temperature. Unfortunately, the project's lifetime expired before non-oxidizing Nb was deposited on the nanowires.

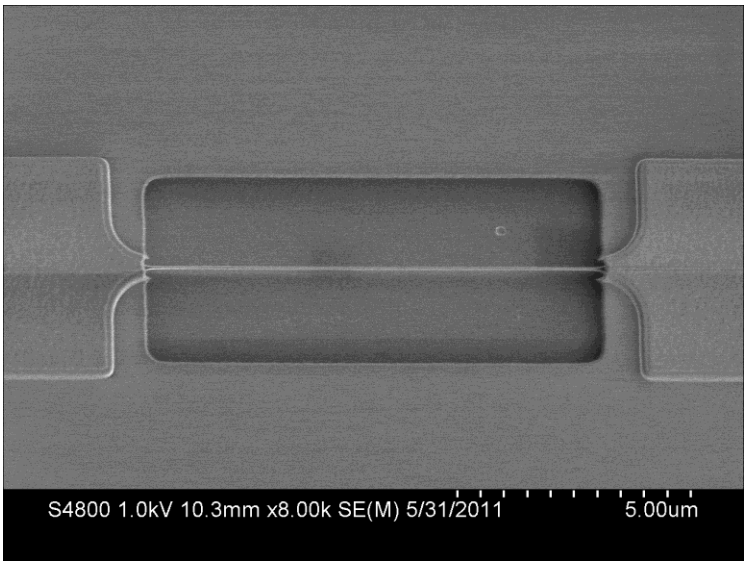

Figure 20 SEM of a fabricated suspended NW with sputtered Nb coating the surface of the wire.

Given the difficulties with the suspended nanowires (both Ga and Nb coated), efforts were also placed into understanding how the implanted Ga behaved. To study this, both resistance and Meissner measurements were performed on implanted sheets. Ga was implanted to 4.2 x 10^{16} cm^{-2} and annealed over a range of temperatures, 600, 650, and 700 C. The films were then placed in the Lakeshore cryostat and cooled while film resistance was intermittently measured, [Fig 22]. It was expected to see a transition to superconductivity around 7 K. From the graph, no such transition was observed although conductivity was still reasonable for a P^+ silicon film.

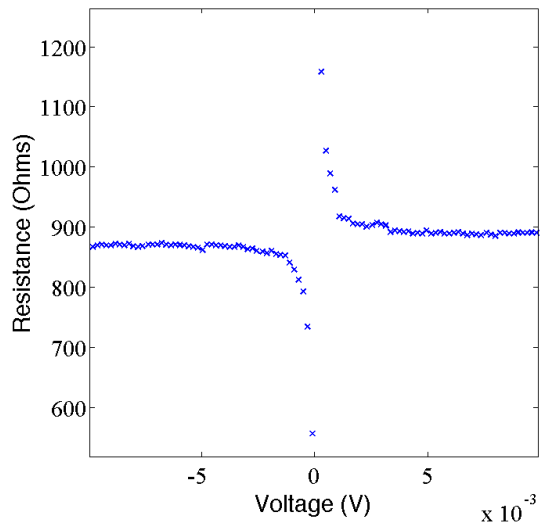

Figure 21 Resistance measurement of a Nb coated suspended nanowire measured at 220 K.

A more conclusive test of superconductivity could be performed using a magnetic property measurement system. This tool utilizes a sensitive SQUID, superconducting quantum interference device, as a magnetometer as low magnetic fields are passed through the sample. If the film is cooled passed a superconducting transition the magnetic field becomes rejected and the detector can accurately pick up this change. This effect is known as the Meissner effect and is generally the best test for determining superconductivity.

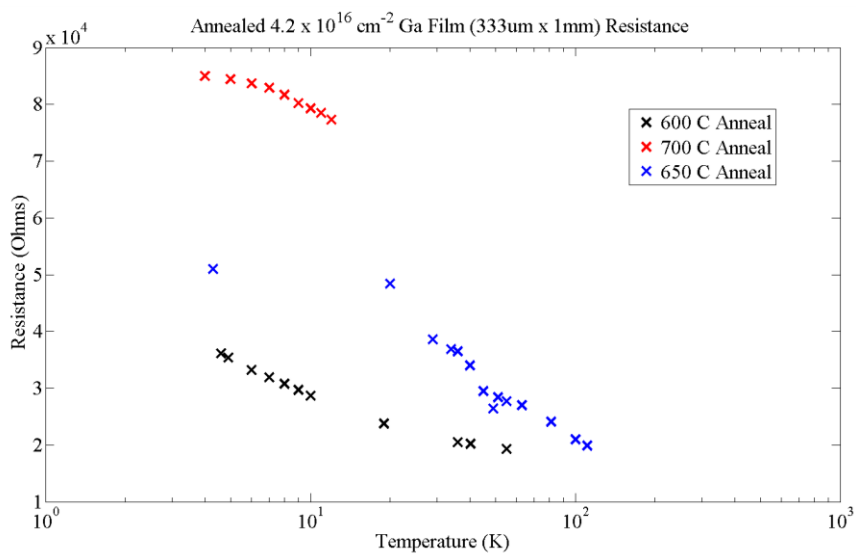

Figure 22 Two-probe I-V measurements of 1/3 mm x1 mm field implanted Ga annealed under various conditions with no observation of a superconductive transition.

As a magnetic field enters a superconductor, the super current begins to flow in a manner to create an opposite current. If too strong of a field is applied, the superconductivity breaks and the film reverts to a normal conductor. This feature prevents the application of too strong of a magnetic field to test the superconducting film. Moreover, the amount of magnetic field which

penetrates the superconductor decays in an exponential function with the decay length known as the London penetration depth. The Ga films created in this work were typically 15-20 nm thick. Based on previous research on superconducting Ga, the London penetration depths were expected to be around 1 um. These two aspects imply that making the Meissner measurement would require low fields and would be very difficult to make.

A MPMS measurement is performed by first cooling the sample to 2 K with the magnetic field off, then turning on the magnetic field as the sample is warmed slowly. All the while the SQUID is measuring the amount of magnetic field going through the sample. This is referred to as zero field cooling, ZFC. The field is then left on as the sample cools back to 2 K, FC. If the sample is superconducting, the ZFC measurement would show an inflection in measured magnetic moment and the FC would not due to the magnetic field preventing superconductivity. This experiment was performed over various annealed samples, with various applied magnetic fields.

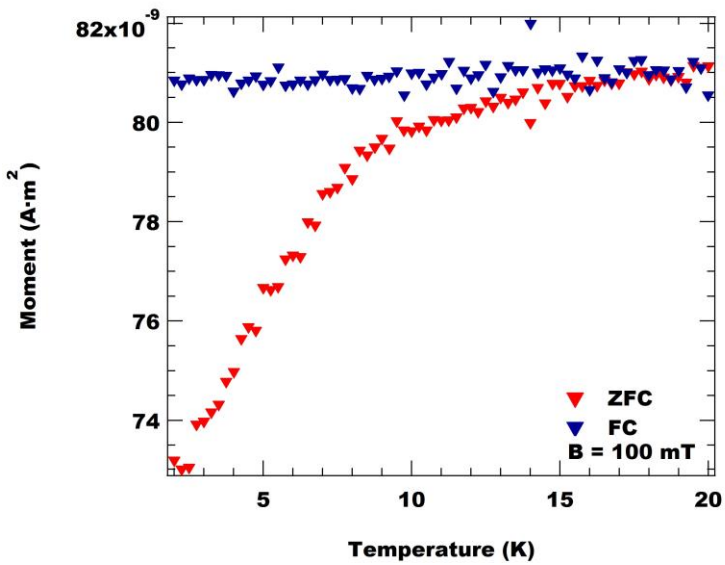

Figure 23 MPMS measurement of a Ga implanted sample annealed at 600 C and with an applied magnetic field of 100 mT.

With the magnetic field set to 100 mT, three samples annealed at 600, 500 and 440 C all demonstrated an inflection in the ZFC curve with little to no inflection in FC curve [Fig 23], [Fig24], and [Fig 25]. This result at first glance, would imply that a superconductive transition occurred at 10 K. This is unlikely as Ga is expected to transition at 7 K. It was confirmed correct operation of the tool using a solid Nb slug with perfect transition at 9.2 K; the tool was operating correctly. More measurements were performed at lower fields, 10 mT [Fig 26] and 1mT [Fig 27]. The results of these measurement indicated that the sensitivity of the detector was not sufficient to accurately resolve the Meissner effect occurring in such a thin film. Correct interpretation of the inflections of the ZFC fields is currently not understood but it is not likely that Ga was superconducting at such a high magnetic field and at such a high temperature.

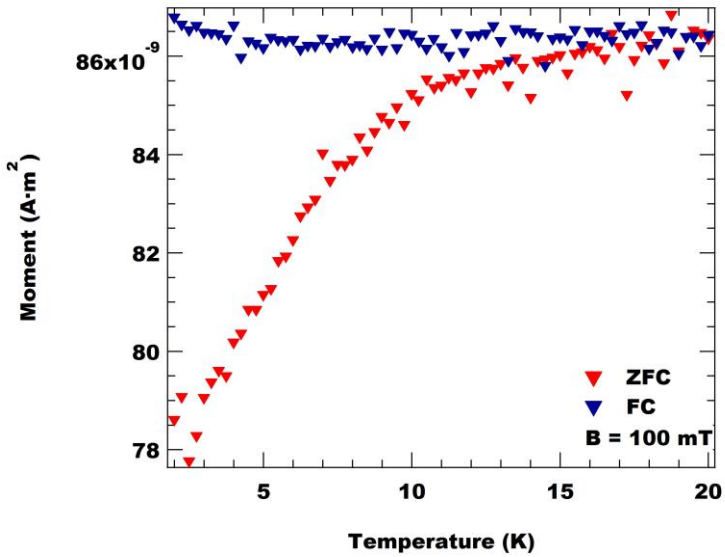

Figure 24 MPMS measurement of a Ga implanted sample annealed at 500 C and with an applied magnetic field of 100 mT.

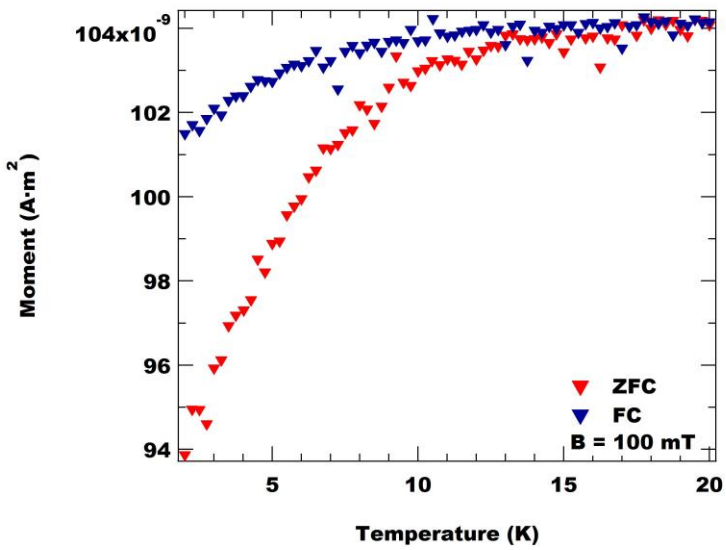

Figure 25 MPMS measurement of a Ga implanted sample annealed at 440 C and with an applied magnetic field of 100 mT.

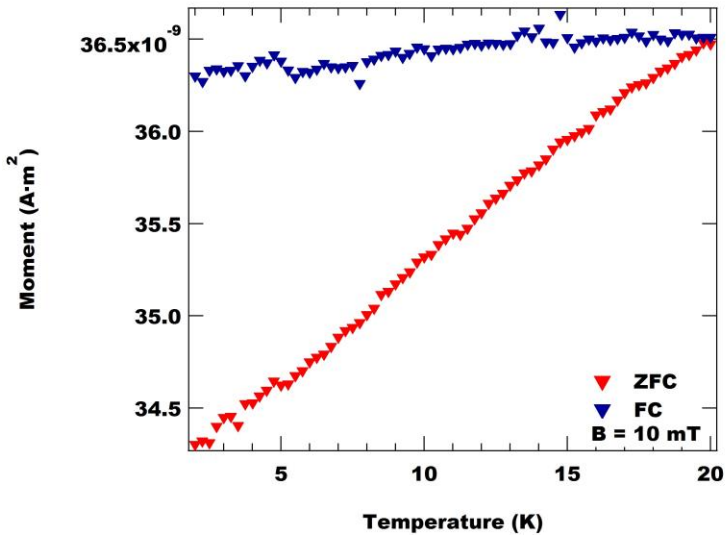

Figure 26 MPMS measurement of a Ga implanted sample annealed at 500 C and with an applied magnetic field of 10 mT.

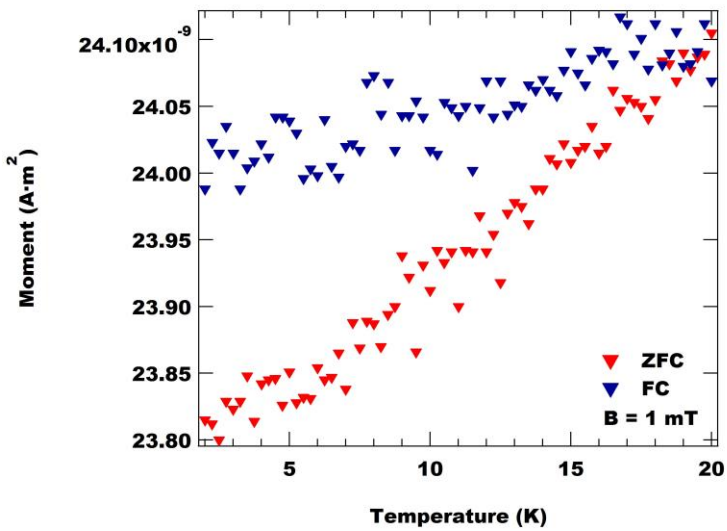

Figure 27 MPMS measurement of a Ga implanted sample annealed at 500 C and with an applied magnetic field of 1 mT.

In conclusion, superconducting nanowires were achieved using Nb deposited on suspended Ga lithographic nanowires. Anecdotal evidence suggested that Ga could indeed go superconducting but the results were not reproducible nor conclusive; transitions were observed at 7 K for Ga films but the transition rapidly decayed to lower, non-repeatable transitions. The project was terminated before further study could be performed. It is likely that Ga implanted in silicon does go superconducting but requires finding the 'magic' anneal temperature appropriate for the implantation voltage.

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3. GA-SI SUSPENDED NANOWIRE PIRANI GAUGES

Since the fabricated suspended nanowire's resistance demonstrated a very high dependence on pressure, a logical application of using the wire as a Pirani sensor was explored [11], [12]. A focused ion beam again was used to implant a Ga layer 20 nm thick into silicon using the plasma etch to define and release the nanowire. Nanowires were created in the range of widths from 30 nm to 130 nm with suspended lengths up to 10 um connected to the 50 um diameter contact pads. Electrical measurements confirmed the Ohmic contact to the silicon through the Ga layer and resistance measurements performed over temperature yield the temperature coefficient of resistivity around 33.5 Ohm-cm/K [Fig 18]. Initial resistance measurements performed over varied pressure demonstrate the expected Pirani effect [Fig 19]. This method benefits over standard Pirani integration schemes with decreased fabrication complexity, decreased thermal conductivity of amorphous silicon (from implantation) and increased electrical conductivity of Ga doping to reduce device area and fabrication complexity of a Pirani gauge.

The Pirani effect can be understood as a temperature dependence of resistivity where the temperature is moderated by gas molecules removing heat from the suspended nanowire [11]–[13] . As a vacuum is created around the nanowire, the amount of heat being removed by the gas molecules for a given current is reduced. The increased amount of heat changes the resistivity of the nanowire; in the case of silicon, the resistance of the nanowire is reduced due to thermal injection of charge carriers from the silicon. Nanowires such as those created here, offer an increased surface to volume ratio enabling more of the heat generated in the wire to make it to the surface for ease of removal by gas molecules.

These devices utilized a FIB at 30 KeV to implant areal doses from 1 to 10^{16} cm^{-2} into silicon substrates. Control over the beam current determined the beam width of the patterning resolution; typically <15 nm for this work. This patterning method implants about 25 nm deep into the silicon with a layer thickness approximately 20 nm thick. A SF_6 / C_4F_8 mixed mode silicon etch (ICP 900 W, Bias 15 W, Pressure 10 mT) then etches the un-implanted silicon with a typical selectivity better than 30:1 over that of the silicon implanted with Ga. Actual selectivity can be controlled based on the implantation dose. However, implantation dose also increases the electrical conductivity.

Patterning arbitrary shapes and figures is easily programmable in the FEI FIB tool. In this work we pattern 50 um circles and connect them with rectangles, which range in width and length, on SOI with the device silicon layer of crystal silicon and amorphous CVD silicon. This implanted pattern is then etched in a Plasma Therm DRIE to define the structure down to the BOX. The etch chemistry is then shifted to an isotropic etch which etches under the rectangle structure to release the nanowire. For the work described here, nanowires of 10 um length, 20 nm thickness, and 130 nm wide were characterized, [Fig 18, Fig 28, Fig 29].

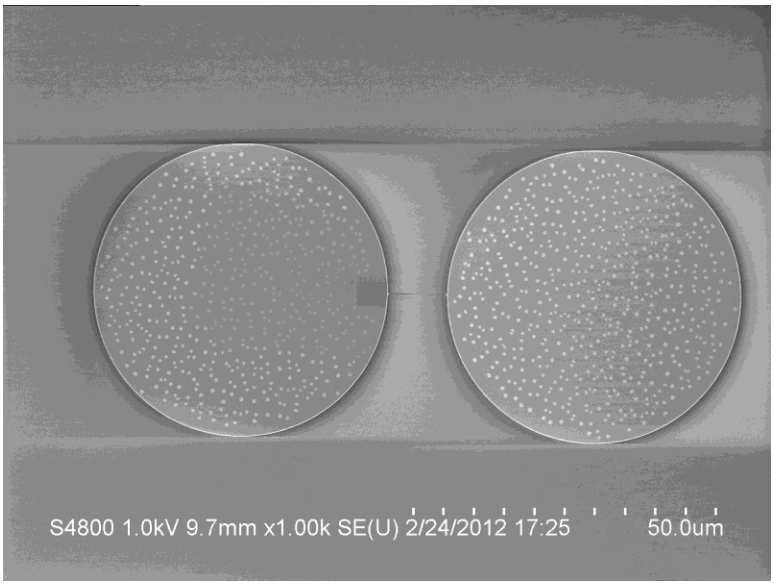

Figure 28 SEM of a 10 um long Pirani nanowire connected to two 50 um contacts on a SOI substrate.

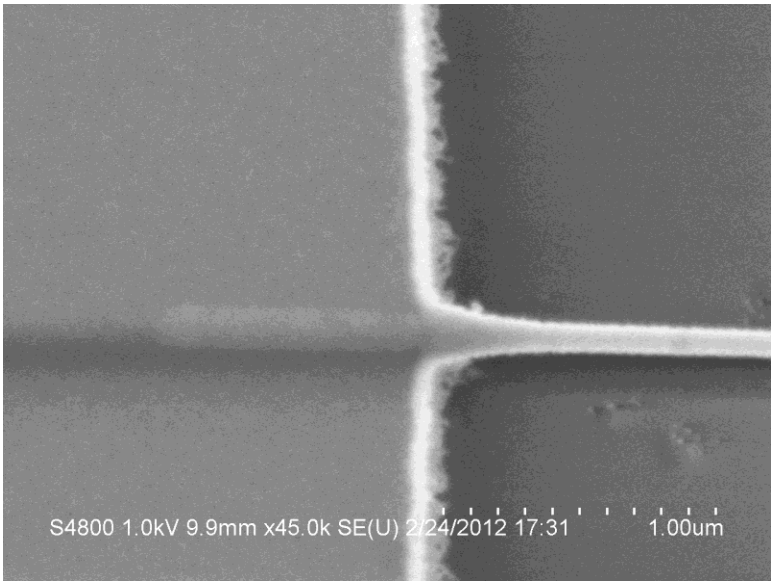

Figure 29 Increased magnification SEM of a 10 um long Pirani nanowire connected to two 50 um contacts on a SOI substrate.

Two electronic measurements were performed. The first measurement was to determine the I-V characteristics of the implanted Ga layer when probed using a tungsten probe tip [Fig 17]. Using an Agilent 4156C, a W probe tip contacting the 50 um implantation measured the implant region to have good Ohmic contact resistance [Fig 15]. For contrast, the W tip also measured bare silicon on the same crystal silicon sample which demonstrated an expected Schottky contact. This measurement confirmed that contacting the nanowire using the 50 um pads would provide low contact resistance. Placing a sample in a Lakeshore Cryostat, where stage temperature could be controlled while making 2 probe resistance measurements of nanowires, a second measurement was performed. The first of these measurements provided a thermal coefficient of

resistivity value of 33.5 Ohm-cm/K [Fig 18]. Other measurements held the substrate at 300 K while throttling a gate valve to the chamber pump while monitoring a calibrated chamber pressure gauge. Once the valve was throttled, the chamber was allowed to reached a pressure equilibrium, usually taking 2-5 minutes; when the pressure stabilized, a two probe resistance measurement was performed. This measurement was typically performed by utilizing a Matlab/GPIB controlled Keithley multimeter applying a voltage while measuring current although verification measurements of injecting current while measuring voltage were also used to confirm results; however current injection for measurement was least desirable due to reduction of measurement sensitivity.

One of the main problems in application of a voltage while measuring a current is the feedback loop which arises from the physical properties of the silicon. If a voltage is applied to the nanowire, the starting resistance of the nanowire induces a current. This current induces a Joule heating on the wire according to Fourier's heat equation. The heat reduces the resistivity of the nanowire by creating excess charge carriers. Since the voltage is constant, but the resistance reduced, the current injected increases causing more heating. This feedback loop continues. However, since the heat equation creates a cosine like heat distribution along the wire, the affected length undergoing a significant resistance change is relatively minor, [Fig 30]. The feedback loop becomes stabilized and voltage measurements allow for a more accurate current measurement.

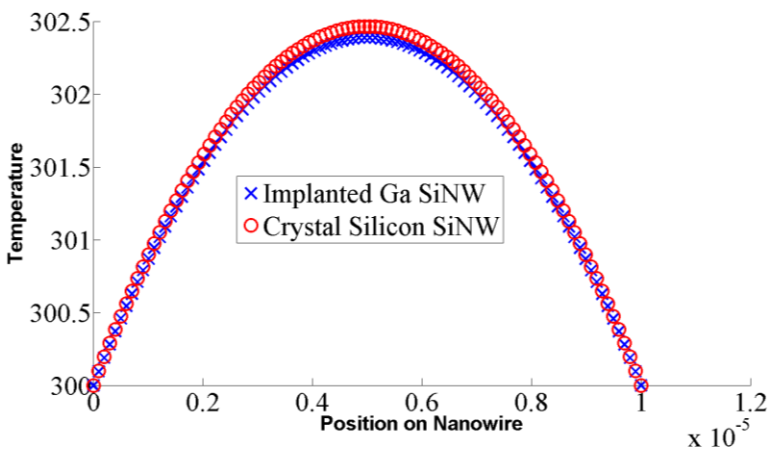

Figure 28 Calculation of Joule heating along a 130 nm x 20 nm nanowire, 10 um long. The two curves compare the effect of thermal conductivity of amorphous, doped silicon to crystalline silicon with the probe pads thermally connected to 300 K.

Suspended nanowires were first measured at 1 volt bias as the pressure was varied; a power low enough such that the Joule heating would not induce annealing effects in the nanowire. For this first experiment, a short but thinner nanowire was used with dimensions of 100 nm by 20 nm by 2 um. The chosen dimensions permitted a nanowire resistance of 10 MΩ to be achieved. The nanowire demonstrated sensitivity in the 1 to 100 Torr range, with resistance changes around 7.5% of the total resistance, [Fig 31]. This is a very strong resistance dependence on pressure.

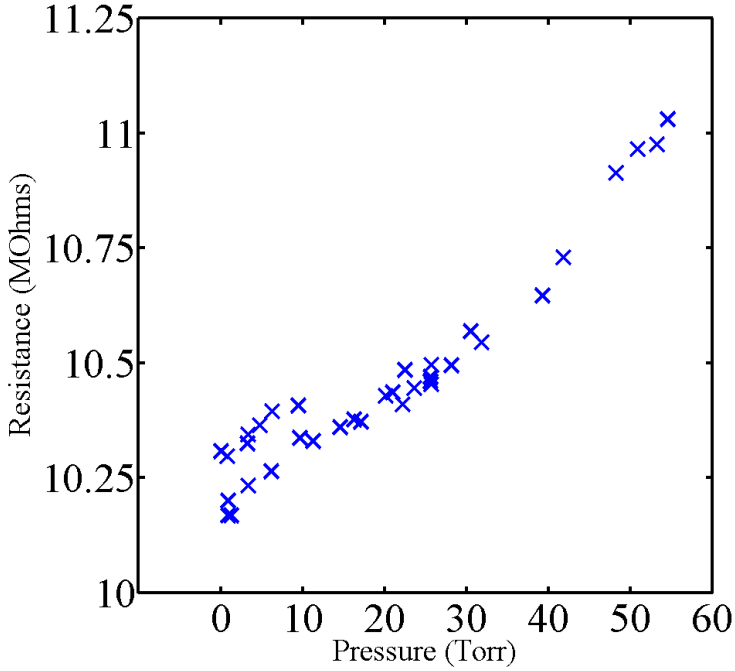

Figure 31 Pressure dependence for a suspended 100 nm x 20 nm x 2 um nanowire at 1V bias. Implanted dose is 8 x 10^{16} cm^{-2}.

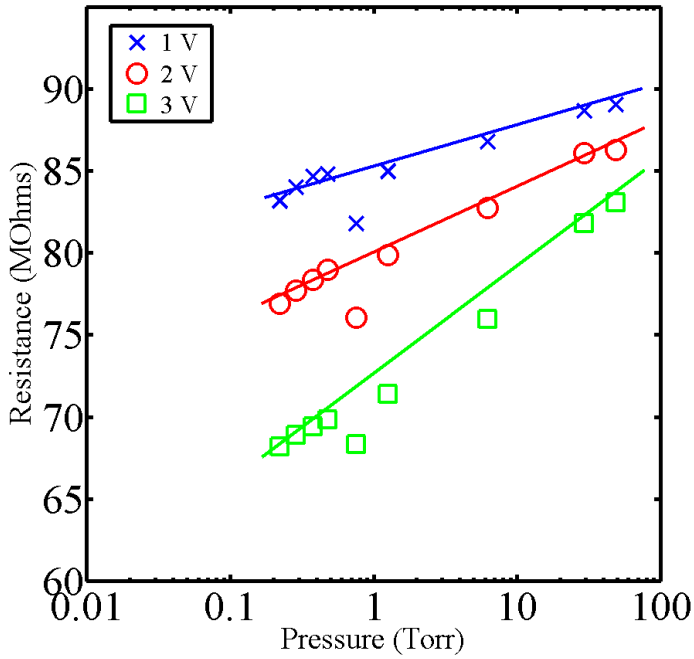

Figure 29 Pressure dependence for a suspended 130 nm x 20 nm x 10 um nanowire at 1, 2 and 3V bias. Implanted dose is 5x 10^{16} cm^{-2}.

A second nanowire was tested with a much longer length, 10 um, which drove the resistance value much higher, around 80 MΩ. The dimensions of this device demonstrated pressure

sensitivity over 3 orders of magnitude, 100 mTorr to 100 Torr. During this experiment, the applied voltage was varied 1 to 3 volts. The increased voltage, increased the Joule heating of the device improving the strength of the effect on the nanowire: for 1 volt bias, the range of the Pirani gauge was 8.2% of it's total resistance, the 2 volt bias had a 13.3% range, and the 3 volt bias had 27.7% range. This equates to a 3 fold increase in sensitivity over the same range of pressure, [Fig 32].

Although this LDRD did not focus on the Pirani effect, it helped to understand the physical background behind the pressure dependence. Beginning with the steady state Fourier's Heat Equation (Poisson Equation), the nanowire was modeled by adding a resistive heat source and heat removal from molecular gas flow to the equation:

$$d_x{}^2 U(x) = -\frac{J^2\,\rho_o}{k_{nw}} - \frac{J^2\,\rho_o\,\alpha\,U(x)}{k_{nw}} + \frac{\eta\,k_c\left(\frac{P/P_o}{1+P/P_o}\right)U(x)}{k_{nw}\,t\,z}$$

where,

$$\rho(x) = \rho_o(1 + \alpha\,U(x))$$

Here J is the current density, ρ is the resistivity, k_{nw} is the thermal conductivity of the nanowire material, t is the thickness of the nanowire, z is the height the nanowire is suspended above the substrate, U is the difference of the nanowire temperature (T) to the substrate temperature sink (T_o), P is the pressure, P_o is the point at which the gas goes from viscous to molecular flow, and α is the temperature coefficient of resistivity. Solution to this equation, which can be solved closed form, yields a heat profile across the wire accounting for the change in resistivity as a function of temperature, assuming that the ends of the nanowires assuming the ends of the wires are connected thermally to the substrate at T_o.

$$T(x) = T_o + \frac{\delta}{\epsilon}\left(1 - \frac{\cosh(\sqrt{\epsilon}(x - L/2))}{\cosh(\sqrt{\epsilon}\,L/2)}\right)$$

The heat distribution, and subsequent change in resistivity across the nanowires is then integrated and averaged. The total resistivity and resistance of the nanowire can be determined.

$$R = \frac{\rho\,L}{t\,w}\left(1 + \frac{\alpha\,\delta}{\epsilon}\left(1 - \frac{\tanh(\sqrt{\epsilon}\,L/2)}{\sqrt{\epsilon}\,L/2}\right)\right)$$

This equation is useful as it can significantly guide design of the nanowires for use a Pirani gauges. Although much has been understood from this research, a significant amount of engineering is required to be performed to move this work to product realization.

This section has demonstrated the technique of Ga lithography implanted using a FIB, and using this implantation layer as a highly selective etch mask to create silicon nanowire Pirani gauges. The fully suspended nanowires are fabricated in the device layer of SOI for electrical isolation and demonstrate an Ohmic contact to tungsten. When placed in a vacuum, the nanowires demonstrate 3 orders of magnitude of response to pressure changes making them an interesting technology for Pirani sensors in MEM packaging situations.

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4. OXIDATION OF SPUTTERED NIOBIUM

We report on the suppression of room temperature oxidation of DC sputtered niobium films and the effects upon the superconductive transition temperature, Tc. Niobium was sputter deposited on silicon dioxide coated 150 mm wafers and permitted to oxidize at room temperature for up to two years. Resistivity and stress measurements indicated tensile films greater than 400 MPa greatly resisted bulk oxidation with measurements using TEM, EDS, XPS, and SIMS confirming this result. Although a surface oxide, Nb2O5, consumed the top 6-10 nm, we measured less than 1 at. % oxygen and nitrogen in the bulk of the films. Tc measurements using a SQUID magnetometer indicate the tensile films maintained a Tc approaching the dirty superconductive limit of 8.4 K after 2 years of oxidation with transitions approaching 5 K for the most compressive films.

4.1. Introduction

Niobium continues to be one of the more important elemental low temperature superconductors (LTS) due to the inherent mechanical stability and a transition temperature reachable using He-4. A significant amount of research has been invested into its properties so that it can be utilized in various superconducting fields such as planar waveguides and resonators, superconducting electronics (SCE), and quantum qubit computers. With rare exception, achieving the best superconductive properties such as small London penetration depths, high mean free paths, and large coherence lengths are seen in crystalline Nb. Crystalline Nb is, however, difficult to support for fabrication of SCE circuits so other niobium films are utilized. Such films can be created using techniques including evaporation and sputter deposition. That these deposition methods cause an immediate reduction in film quality is shown by imperfect crystalline formation and inclusion of impurities such as hydrogen, oxygen and nitrogen during deposition. Bulk energy gap values are seen to drop from 1.6 meV to 1.45 meV corresponding to critical temperature reductions of 9.25 K to 8.45 K. This reduction can be directly attributed to a significant reduction in the mean free paths of electrons and a reduction in the coherence length of paired electrons. Associated with this reduction based on structure of the films, is a further reduction in the superconductive properties due to inclusion of impurities such as nitrogen or oxygen in the niobium films during deposition. After deposition, niobium films continue to deteriorate due to oxidation in atmosphere. This effect begins immediately on exposure of the newly deposited film to atmosphere with the creation of a surface oxide and continues with bulk oxidation over time.

Sputter deposition then becomes problematic for creating good superconductive niobium films. Since the deposition temperature is usually quite low, films are typically more amorphous with grain sizes around 10 nm. Further, in order to sputter the Nb, Ar gas is typically used which creates inclusions in the film; although Ar does have the advantage that an electronic interaction with niobium's superconductive d-electrons are not expected. The great advantage to sputter deposition is the high deposition rates and high control over stress and film formation. By tuning of parameters such as Ar, pressure and deposition power, films can be deposited with strains

ranging from compressive to tensile with deposition rates around 10-20 nm per minute. For the majority of these films, the mean free paths are typically short enough that the niobium falls under the London impure limit where the mean free paths are much shorter than that of the intrinsic coherence length. In this so-called 'dirty limit', ideal critical transition temperatures are expected around 8.45 K. Even with the most ideal sputtered film using Ar, oxidation of the niobium begins immediately once the film is removed from the deposition chamber.

This creates a problem with fabrication of SCE circuits since wafer scale fabrication times can be long, up to 6 months or more depending on complexity, and the wafers can be exposed to atmosphere during that time frame. In this work we detail how control over the DC-sputtering conditions of niobium influence the properties of the film and can help reduce the bulk oxidation in the film. In this report, thermally oxidized 150 mm silicon wafers with DC-sputter deposited niobium films were characterized, then permitted to oxidize at room temperature for up to two years. During this oxidation period, measurements including film stress and resistivity, TEM, EDS, XPS, and SIMS were used to quantify the effect of oxygen diffusion in the films. The effect of the oxygen on the superconductive properties was then quantified using a SQUID magnetometer tool by Quantum Designs to measure the critical transition temperature. The outline of this report is broken into four sections. In section II, the details of how the niobium was sputtered will be discussed along with the initial stress and resistivity measurements. Section III describes measurements taken on the oxidation of the niobium films, and section IV details the effects of the oxidation on the superconductivity. Section V discusses the profile of oxygen through the films followed by concluding remarks.

4.2 Experimental

Niobium was sputter deposited in a Denton Discovery 550 sputter deposition tool on 150 mm silicon wafers. Prior to deposition, the clean silicon wafers were thermally oxidized for a 200 nm thick SiO2 layer to facilitate room temperature sheet resistivity measurements. The sputter chamber was pumped down to pressures in the low 10-7 Torr vacuum levels before deposition. Deposition conditions were varied using Ar flow, DC power, and time in the range of 15 to 30 sccm, 150 to 300 watts, and 400 to 700 seconds respectively, as the pressure was held around 4 mTorr. Some variation in chamber pressure was observed and ranged from 3.7 to 5.5, linearly dependent on the Ar flow rate. These deposition conditions, thicknesses, and sputtering times are reported in table I. Although the specific thickness was not directly controlled, the deposition time was targeted such that the Nb film would be thick enough that a 1/d suppression in Tc would not significantly contribute [14]. This suppression was expected to occur for films less than approximately 80 nm thick. Actual thickness was measured by profilometer measurement on a thickness monitor at the edge of the wafer and reaffirmed using TEM and SIMS during the course of this work. Upon completion of the depositions, the deposited film stress was measured using a Flexus 2320-S thin film stress measurement tool and the sheet resistance measured using a VersaProbe VP10 4 probe resistivity measurement system. The Flexus operates by taking pre and post measurements of wafer curvature, where concave down is compressive and concave up is tensile, and calculates the wafer stress using Stoney's equation. The VersaProbe takes multiple four probe measurements at 9 sites on the wafer where this work reports the mean of the measurements.

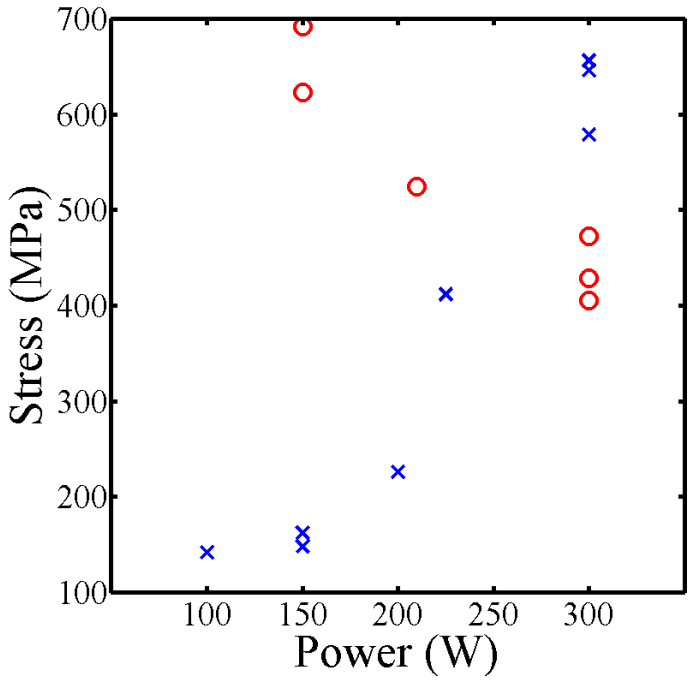

Figure 30. Effect on sputtered Nb film stress as DC Power is changed for 15 sccm Ar flow (o) and 30 sccm Ar flow (x).

As expected, the Ar flow and the bias power directly influenced the stress of the film [15]–[17]. As power increased for the 30 sccm flow rate, the stress was measured to transition from compressive to tensile [Fig. 1]. As the Ar flow increased the stress, in general, moved from tensile to compressive. We note that although the data shown all have varied thickness, which should also modulate stress, the effect of power and Ar pressure was observed to dominate in our thickness regime. As example, the samples deposited at 300 W power and 30 sccm Ar show a range of stress from 579 MPa to 657 MPa for a variation in thickness of 149 nm to 229 nm but a decrease to 200 W power lowered the stress to 226 MPa. A second observation was that a reduction in Ar flow from 30 to 15 sccm, significantly increased the stress to more tensile. It is likely that this mechanism is due to having less Ar entrained in the metal during the deposition process. The most significant observation was that as the stress became more compressive, the resistivity greatly increased, [Fig. 2]. Several interesting trends emerged: films with tensile stress greater than 400 MPa had measured resistivity closest to the ideal bulk of 152 n□-m and for films with stress less than 400 MPa the resistivity increased with decreasing (more tensile to compressive) stress. A linear least squares fit to the changing region gives a slope of -2.7 n□-m per MPa of stress.

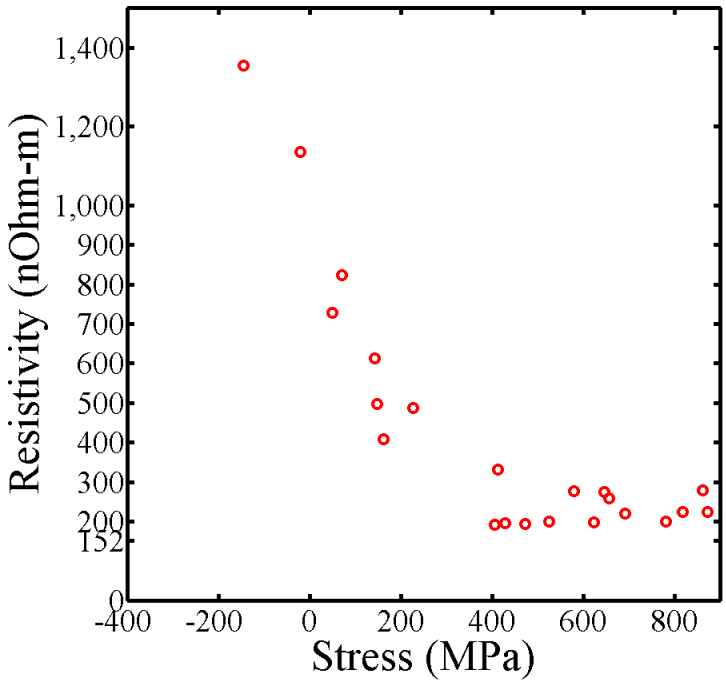

Figure 31 Measured effect of Nb film resistivity as the measured sputtered flim stress is changed by changing power and Ar flow rate, measured within a week of deposition. Compressive wafer stress is indicated here as negative and tensile wafer stress is indicated as positive.

4.3 Oxidation Of Sputtered Niobium Films

After these initial measurements were performed, the samples were allowed to oxidize in a class 10 cleanroom at room temperature and pressure. Based on previous work, it was expected that a Cabrera-Mott potential oxidation of the surface would occur [18], [19]. As oxygen is absorbed by the Nb, a Nb2O5 is formed at a rate of approximately ln(t), where t is time. This Nb2O5 oxide is predicted to terminate around 6 nm for crystalline films after approximately 5000 minutes (3.4 days) as the driving potential decreases, reducing the oxygen drive across the surface oxide. Nb conduction electrons being bound by the absorbed O build up a Mott potential, creating the drive for the ionized O atoms. Eventually the surface oxide terminates when the tunneling probability diminishes. The oxidation then continues as oxygen diffuses into the niobium film creating a NbO metallic oxide which is still conductive but since the d-electrons become bound a notable reduction in the transition temperature occurs. The oxidation is expected to continue with the newly converted NbO transitioning into a final state of NbO0.2. Through the creation of these oxides, the niobium film resistivity increases and with a corresponding reduction in superconducting performance and Tc. For further extensive discussion see Halbritter [19].

Since the Nb2O5 is significantly more resistive, as compared to the niobium film, we expected to see an increase in the resistivity of our sputtered films over time. We note that the oxidation sequence described above is for bulk films whereas the films deposited here were expected to be

more amorphous or polycrystalline. A subset of the sputtered films resistivity was re-measured using the same VP10 tool; wafers were selected to span the range of stresses previously measured. The first re-measurement was performed at 9 months and then a second measurement at 17 months, [Fig. 3]. At 9 months the resistivity of the films increased up to 170% from the original (as sputtered) resistivity for films less than ~ 450 MPa tensile. As the films became more compressive, the change in resistivity increased. Although the samples' resistivity further increased at 17 months, the change was not as severe. The most compressive sample increased in resistivity another 30%. For the films tensile between 450 and 800 MPa, the films' resistivity decreased at 9 months and slightly again at 17 months, [Fig. 4]. This decaying increase in resistivity suggests that the film is oxidizing but does not offer an apparent reason for such dramatic changes based on stress. To better clarify the oxidation, the wafers were cleaved and samples were viewed in a transmission electron microscope and oxygen content looked into using EDS measurements at 17 months of room temperature oxidation.

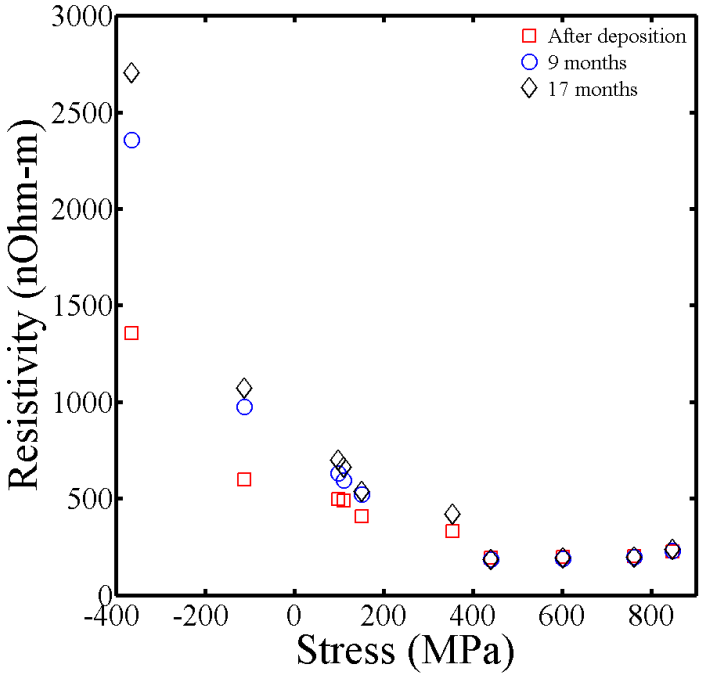

Figure 35 Measured change in resistivity as the sputtered Nb films are permitted to oxidize at room temperature and pressure. The first measurement (square) was made within a week of deposition, the second measurement (circle) was made after 9 months of oxidation, and the third measurement (diamond) was made after 17 months of oxidation. The stress was only measured within the first week of deposition.

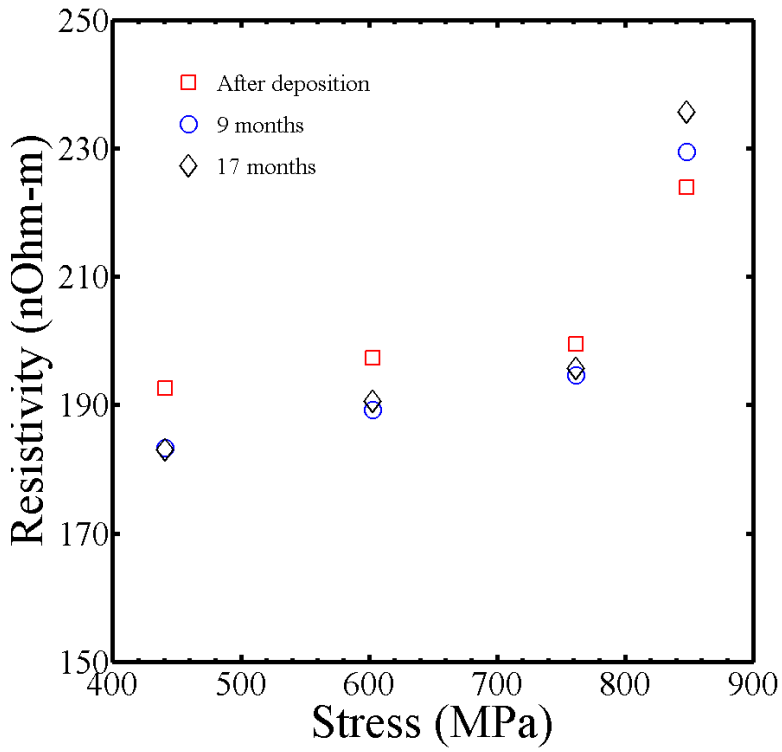

Figure 36 Zoomed in measurement change in resistivity, for the tensile Nb films, as the sputtered Nb films are permitted to oxidize.

A subset of those measured for resistivity were imaged using a scanning transmission electron microscope (S/TEM); the samples original stress values are as follows: -366, -113, 150, 441, 603, 848 MPa. The TEM utilized was an FEI Titan S/TEM with a Cs probe corrector operated at 200 kV. The images were taken in scanning mode with a bright field detector. The EDS scans were taken at a magnification of 320 kX and collected for 1200 seconds. Results were scaled according to the signal strength to normalize effects of thickness variations between samples. Oxygen content was determined by comparison of the relative oxygen-KA and niobium-LA transitions. The dark regions at the bottom of the micrographs are the silicon dioxide layers and the lighter areas denote the niobium films, [Fig. 5.a-5f]. The highly compressive structures indicate columnar grain growth with strain at the oxide interface. The dark regions in the film indicate a large separation of the grains; either by oxide formation or voids in the film. As the samples become more tensile, the grain growth becomes less columnar and more polycrystalline with less surface roughness and fewer voids. EDS measurements show oxygen dispersed throughout the niobium film indicating oxidation in the bulk of the film, [Fig. 6.a-6.f]. Oxygen distributions in the compressive samples were heterogeneously distributed whereas the tensile films became more homogeneously distributed. Further, the tensile samples had a distinctive 5-10 nm oxide layer at the surface; this is consistent with an Nb2O5 Cabrera-Mott oxidation on the surface at 300K . There was no indication of an oxygen gradient at the silicon dioxide – niobium interface suggesting that oxidation from silicon dioxide supplying the oxygen is not occurring. The EDS measurement permitted a relative O:Nb ratio to be calculated with the most compressive film normalized to a value of 1. As the sample stress moved towards more tensile, the relative ratio continued to decrease to 0.39; this information is displayed in table II.

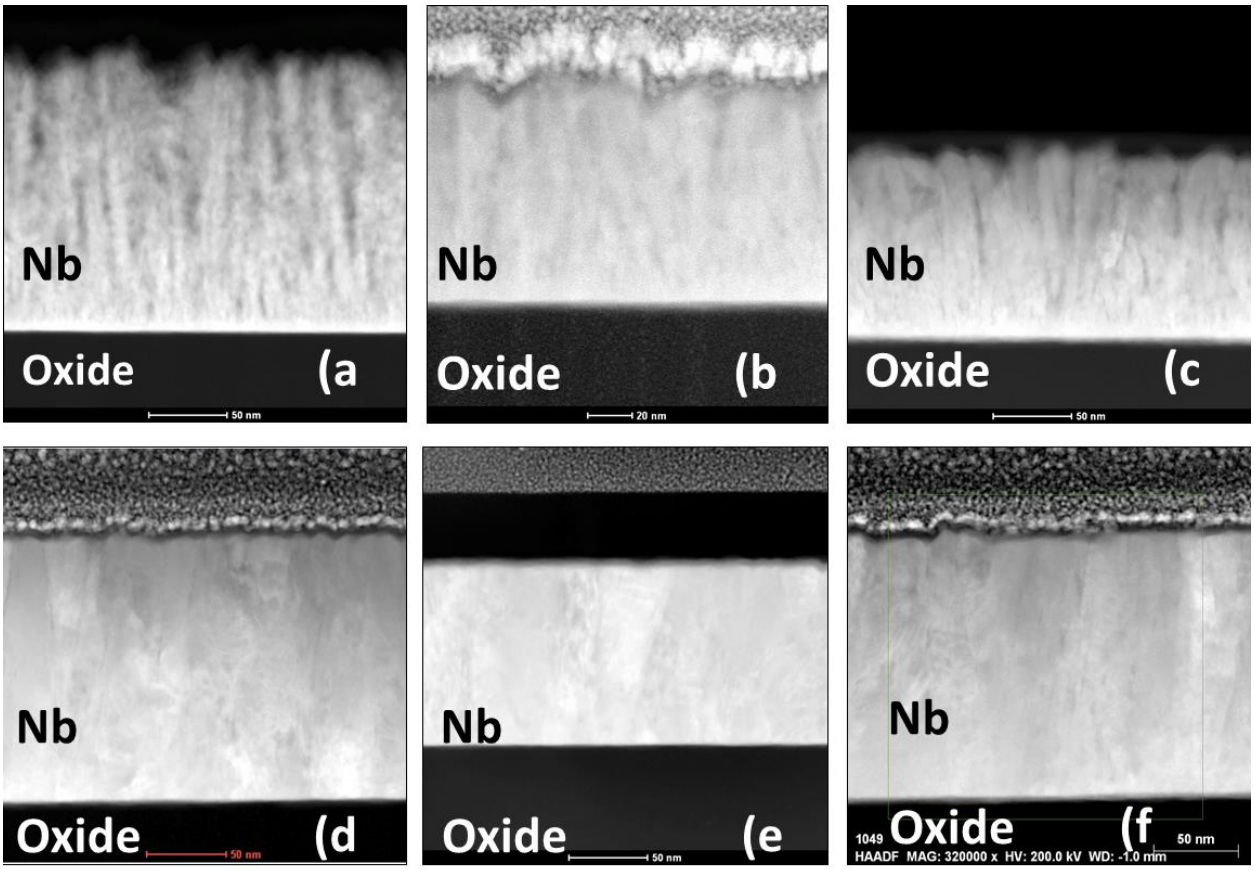

Figure 32 Transmission electron cross-section micrographs of sputtered Nb films on thermal silicon oxide. These samples were imaged after 17 months of oxidation at room temperature and pressure. Scale bars for sample a, c, d, e, and f are 50 nm and sample b has a 20 nm scale bar. The sample numbers and corresponding starting stress are: a) Sample 12, -366 MPa, b) Sample 8, -113 MPa, c) Sample A3, 150 MPa, d) Sample G6, 441 MPa, e) Sample C6, 603 MPa, f) Sample B2, 848 MPa.

From the TEM and EDS measurements the compressive samples appear to have a tight bundling of the columnar growth at the oxide-niobium interface. The grains then greatly disperse at the surface. This type of structure clearly has a natural expansion at the top of the film as compared to the base of the film giving a mechanism to the compressive wafer bow measured. This type of growth also permits a larger fractional area of the sputtered film to be exposed to atmosphere and an oxygen source. EDS measurements further support this idea with large streaks of oxygen going into the bulk; this is likely a surface oxide rather than bulk oxide occurring in the bulk of the film. This oxidation scheme for the compressive samples would permit a much more rapid oxidation of the Nb film since Nb2O5 oxide occurs at a significantly faster rate than NbO. The relatively faster rate of resistivity increase for compressive samples compliments this idea.

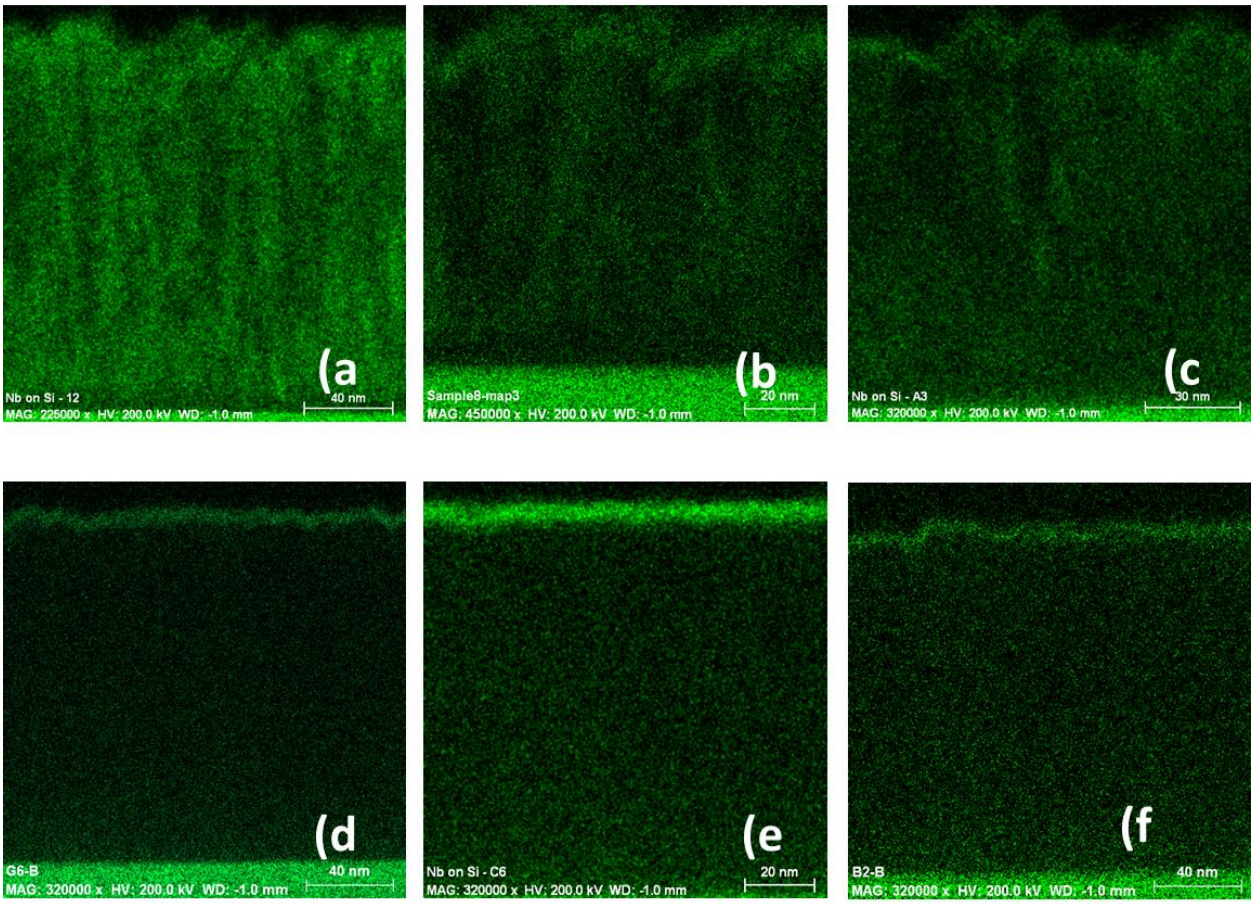

Figure 33 EDS measurements of the oxygen concentration in the transmission electron cross-section micrographs of figure 5 a-f. These samples were imaged after 17 months of oxidation at room temperature and pressure. The sample numbers and corresponding starting stress and scale bars are: a) Sample 12, -366 MPa, 40nm,. b) Sample 8, -113 MPa, 20nm, c) Sample A3, 150 MPa, 30nm, d) Sample G6, 441 MPa, 40nm e) Sample C6, 603 MPa, 20nm f) Sample B2, 848 MPa, 40nm.

As the samples' stresses tend towards tensile, a very clear surface oxide becomes apparent. The heterogeneous oxygen distribution also changes into a more homogeneous oxygen distribution in the bulk suggesting a diffusion-based process creating NbO. This transition in oxygen distribution is very distinct in the compressive samples and becomes non-observable as the samples go past 441 MPa. The observation that films with tensile stress greater than ~ 400 MPa did not have a significant shift in the resistivity measurements over time suggests a much slower oxygen uptake scheme.

4.4 Superconductive Performance Of Oxidized Sputtered Niobium Films

Reduction of the superconductive properties of sputtered niobium is typically controlled by a few major factors: thickness of the sputtered film, film quality, and impurities in the film. The superconductive properties are generally inferred by observation of the film's critical temperature, Tc, and the penetration depth, □. These parameters are reflective of the combined

effects of phonon stiffness, electron-phonon interactions and reduction of the density of electronic states. Minhaj et al.[14] and Gubin et al.[20] have described the effect of reduction in film thickness with increasing penetration depths for films below 50 nm. This effect set our work's minimum film thickness requirements to be greater than 50 nm. Film quality also has significant effects which are typically reflected in resistivity (residual) values or residual resistivity ratio. Mayadas et al.[21] has shown that the mean free path (l) can describe the amount of disorder and corresponding reduction in the penetration depth. Holding the coherence length constant, penetration depth is expected to decrease roughly as l -1/2. From the resistivity measurements, a mean free path can be inferred from the intrinsic value of □□□ l = 3.72 x 10-7 n□-m2, as displayed in [Fig. 7]. For our samples more compressive than 400 MPa, the sputtered films are clearly in the dirty superconducting limit with l below 26 A.

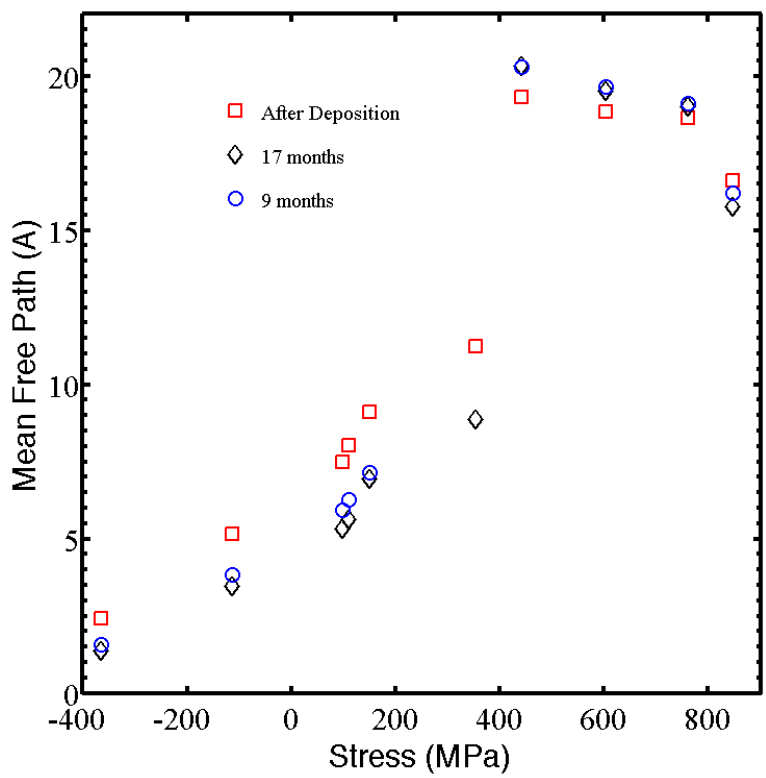

Figure 34 Mean free path of sputtered Nb films, calculated from initial (square), 9 month (circle), and 17 month (diamond) resistivity measurements. For films with stress less than 400 MPa, the Nb films are likely in the dirty superconductor limit.

Previous work by DeSorbo[22], and then later by Koch et al.[23], demonstrated a significant reduction of niobium's critical temperature and an increase in electrical resistivity as dissolved oxygen atomic % increased. Their results suggested that critical temperature falls linearly by 0.93 – 0.96 K per O at. %. For this work we then expected that as the samples oxidized the critical temperature would also reduce. Since the sputtered films were likely to be mostly in the dirty superconducting limit we did not expect to measure critical temperatures reaching 9.25 K. For dirty thin Nb films, Minhaj et al.[14] calculated a theoretical limit for Tc0 to be 8.4 K using the Ebisawa-Fukuyama-Maekawa model[24].

After 24 months of room temperature and pressure oxidation, the samples were measured in a Quantum Design magnetic properties measurement system (MPMS) SQUID magnetometer. Samples were cleaved into approximately 3-4 mm squares and placed in a plastic transport tube. Both zero field cooled (ZFC) and field cooled (FC) measurements were performed with only the ZFC results reported in [Fig. 8]. A DC field of 10 Oe was utilized for a temperature sweep from 2 to 15 K. The critical temperatures were determined by taking the midpoint between 10% and 90% of magnetic moment curve. These critical temperatures, reported in Table II, were compared against original stress and plotted in [Fig 9]. From this plot, a clear trend occurs in which the highly tensile films maintained a Tc close to the 8.4 K prediction after 24 months of room temperature oxidation. As the sputtered films move towards compressive, a sudden change occurs and Tc begins to rapidly drop off below 400 MPa. This stepped trend is also seen from the resistivity-stress curves, where resistivity began a marked increase as stress became more compressive than 400 MPa.

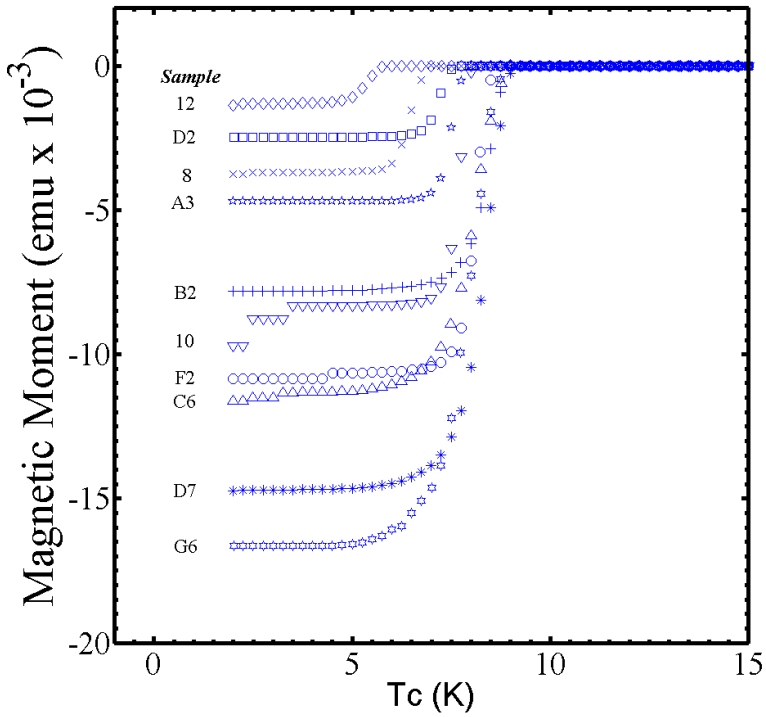

Figure 35 Magnetization measurements of sputtered Nb films measured using a magnetics property measurement system. The samples, labeled to the left of the curves were measured using a 10 Oe DC field. Samples were measured after 24 months of oxidation at room temperature and pressure.

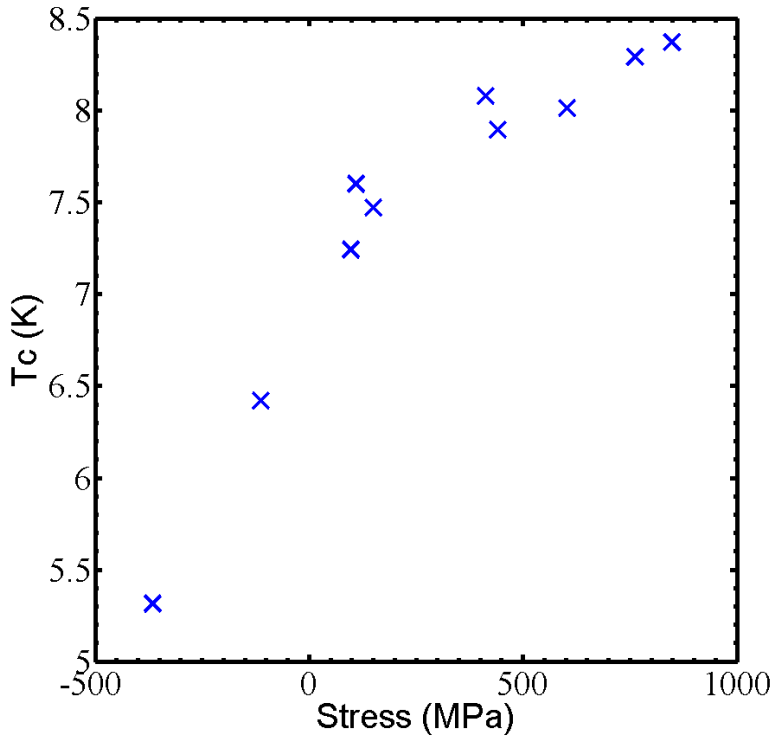

Figure 41 Effect on critical temperature (Tc) as the sputtered Nb films were varied in stress. Tc was determined by taking the midpoint between 0.1 and 0.9 of the MPMS measurements.

When Tc is compared with original resistivity taken at 300 K, [Fig. 10], a clear linear decrease is evident with an intercept approaching that of the dirty limit. The linear decrease is only slightly less than that reported by Minhaj et al.[14] taken at 10 K, supporting the assumption that the films were in the dirty, weakly localized regimes[24], [25].

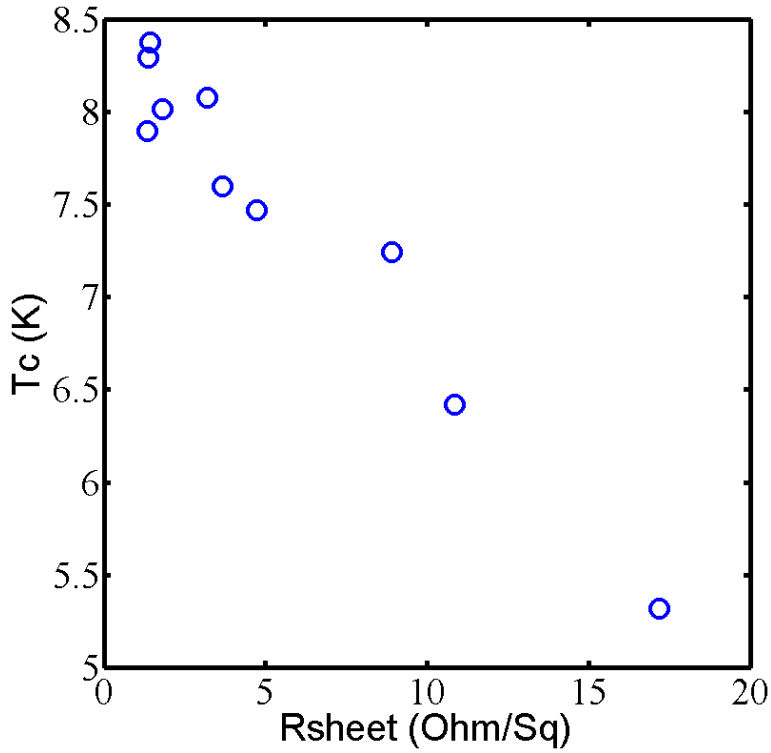

Figure 36 The superconducting critical temperature (Tc) as a function of sheet resistance (taken at 17 months of oxidation).

One particular difficulty with measuring the films using EDS is that the oxygen content can only be compared on a relative basis. For this work, the oxygen content was normalized with the most compressive sample, #12. Utilizing the relationship established by DeSorbo, Tc measurements were converted to relative oxygen content using [O] at. % = (9.25 – Tc) / 0.93 and then normalized using sample 12. These two methods of determining oxygen content in the sample, as a function of stress, is seen in [Fig. 11]. Reasonable trending between the two methods is observed with some discrepancy at the lower oxygen contents. The high correlation between these two methods indicates that oxygen bonding with niobium is the likely cause of Tc reduction and the niobium film stress controls the amount of oxidation. However, the measurements also indicated a much more interesting problem with the oxygen and Tc. The compressive Nb samples with their heterogeneous oxygen distribution, low Tc, higher resistivity, and resistivity change with time, suggest oxidation throughout the bulk of the film which is likely a surface Nb2O5 oxide. The tensile Nb samples which displayed a surface oxide with homogenous bulk oxygen, Tc approaching the dirty superconductive limit, lower resistivity, and lower resistivity change with time suggests that a surface oxide forms with a much slower oxygen penetration into the bulk. Further, both regimes also suggest that a direct comparison of this work to DeSorbo and Kock et al. is incomplete since their samples were homogeneous distributions of oxygen in niobium, likely NbO, and there is a clear distribution of oxygen in the samples presented here suggesting Nb2O5, [Fig. 12]. Observation of the MPMS data shows that the strength of the diamagnetic moment is not only a function of thickness but also a function of sputtered film quality as described by the critical temperature.

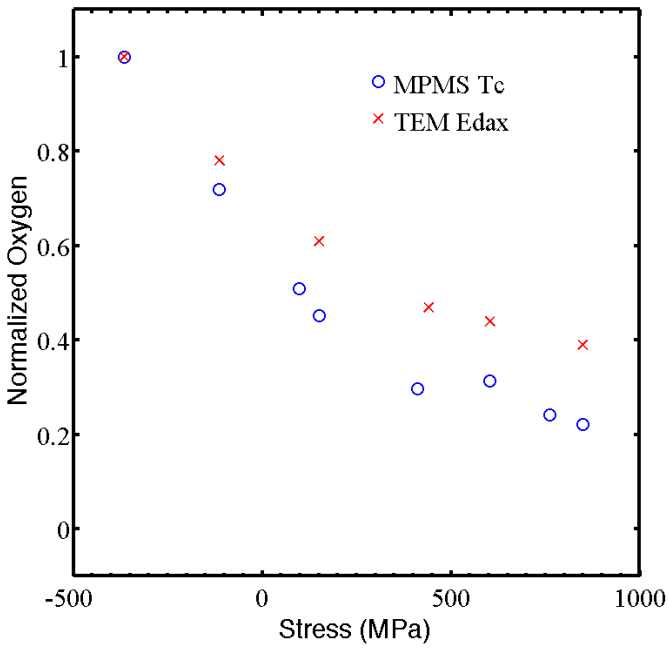

Figure 43 Comparison of oxygen uptake of the sputtered Nb films as a function of stress measured at the time of deposition. Oxygen at. % measured by TEM EDS (x) is normalized to the most compressive sample. Theoretical oxygen at. % is calculated from the critical temperature (o) is normalized to the same compressive sample.

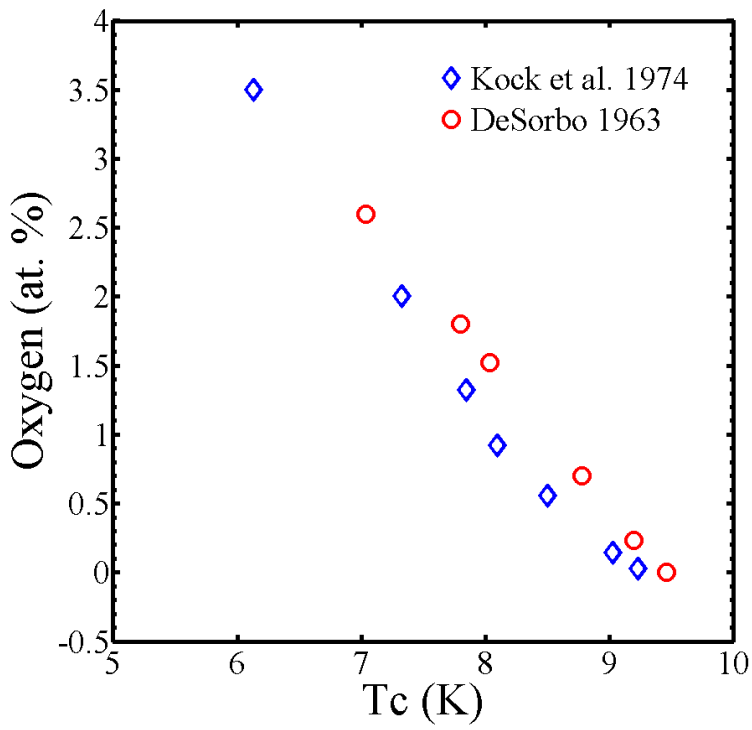

Figure 37 Data from DeSorbo and Kock et al. where oxygen dissolved in niobium was tested for the critical transition temperature. Both groups achieved a relation in which oxygen reduced the critical temperature around 0.93 K / at. % O.

4.5 Oxygen Profile In Sputtered Niobium Films

To better understand the oxygen profile in the film, and hence the superconductive quality, secondary ion mass spectrometry (SIMS) was performed on the niobium films after 24 months of room temperature oxidation. For this technique oxygen, silicon, niobium, and nitrogen were measured. Since the oxygen concentration was approximately that of the niobium, the SIMS data required calibration for the higher oxygen concentrations. This calibration was performed on three different samples using x-ray photoelectric spectroscopy (XPS). The three samples used were sample 12, (-366 MPa), sample 8 (-113 MPa), and sample D2 (98 MPa) chosen due to their relatively high oxygen concentration [Fig. 13]. For the XPS measurement, all of the samples displayed a surface oxygen concentration of 72 at. %; consistent with a surface oxide of Nb2O5. The oxygen concentration then decays down with a minimum just above the silicon dioxide interface. We note that the sharp increase at that oxide boundary is consistent with the measured film thickness, annotated with vertical lines. Although the oxygen content was significantly higher than estimated using Tc, the correlation of increasing oxygen content to reduction in critical temperature remained consistent with sample 12, 8, and D2 having Tc measured at 5.3 K, 6.4 K, and 7.2 K respectively. With oxygen percentages below 50%, it is clear that the entire Nb film was not oxidized to NbO; although various compounds of NbOx (x<1) are probable. These measurements in the 10, 20, and 30 at. % ranges were then compared with the SIMS results and used to calibrate the SIMS measurements.

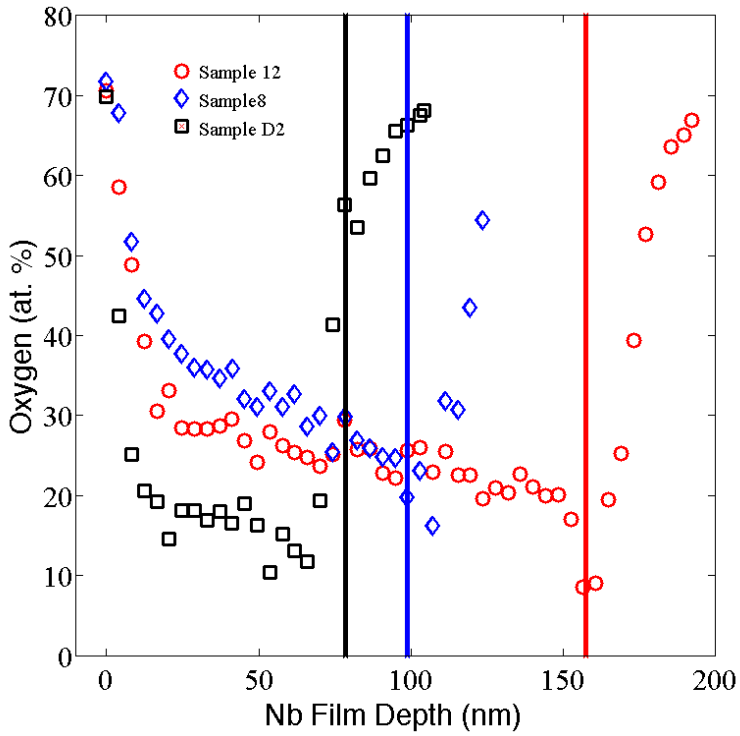

Figure 38 XPS measurements of sample 12 (circle), sample 8 (diamond), and sample D2 (square) used to calibrate the SIMS measurement. The vertical lines at 157.5 nm, 99 nm, and 78.4 nm are the measured sputtered niobium film thicknesses as measured after sputtering.

SIMS measurements were performed on the same subset of samples as those measured for resistivity and MPMS, with sample G6 as an exception [Fig. 14]. In all cases, measurements indicated high oxygen content at the surface of the Nb film, consistent with the Nb2O5 surface oxide. As with XPS, the oxygen content then decayed to a minimum at the silicon dioxide interface. For all samples, two oxygen concentrations decay rates were observed: a very fast decay in the first 10 nm, then a much slower decay through the bulk of the material to the oxide interface. For most films between compressive and 400 MPa tensile, the curves displayed a slow decay starting with oxygen concentrations ranging from 40 to 10 at. % oxygen and decaying to a minimum around 10 to 1 at. % at the interface. For samples C6, D7 and B2 the oxygen content approached very low values below 1 at. %. Their corresponding critical temperatures were also consistent with DeSorbo's results[22] of 1 at. % dissolved oxygen resulting in a critical temperature of 8 K, [Fig. 12]. Nitrogen was also measured for all the samples and was consistently less than 1 at. % throughout the thickness of the niobium films.

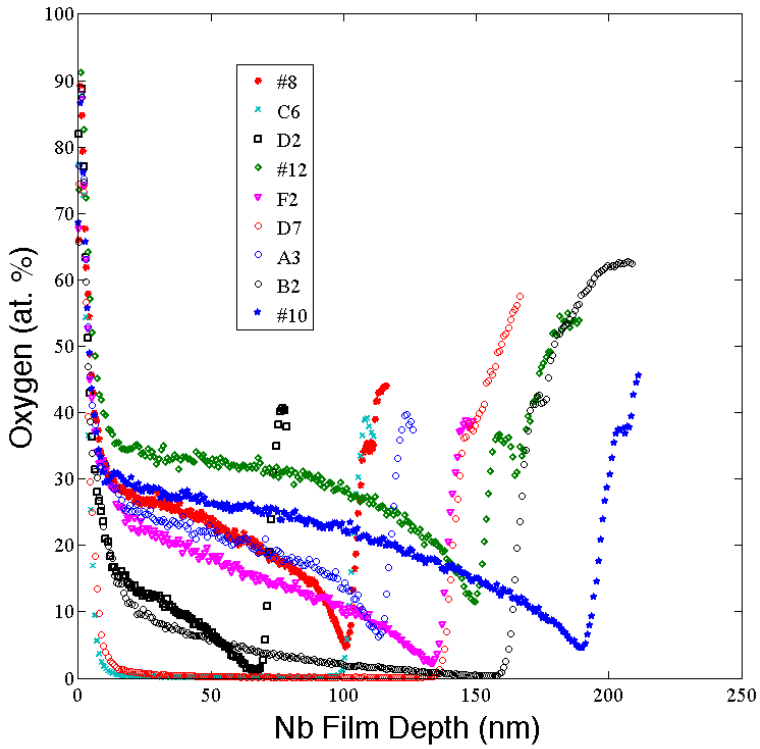

Figure 39 SIMS measurements for oxygen concentration in the sputtered Nb films plotted as a function of depth. The sharp uptake in oxygen in the depth of the film is the interface between the niobium and silicon dioxide interface. The samples with the lowest oxygen content (ie. Samples C6 and D7) also had the highest measured Tc after 2 years of oxidation.

The critical temperatures of the sputtered niobium films generally followed predictions of [Fig. 12] based on the measured SIMS oxygen minimums. However it is clear that graded oxygen content implies a graded reduction of superconductivity as well. The binding of niobium with oxygen greatly reduces the density of states for the conduction electrons and so it should be expected that the SIMS profiles are indicative of the effective superconductive layer. This

effective reduction of a superconductive layer is further supported in the observation of different magnetic moments measured using MPMS, which cannot be fully explained by thickness alone.

4.6 Conclusion

This work has studied the effect of sputtered niobium film stress on atmospheric oxidation and superconductivity of niobium over a 2-year period. By varying the DC power and Ar flow during sputtering, the film could be made to go from compressive to tensile while depositing on clean silicon dioxide. Resistivity measurements made after deposition indicated a transition from low resistivity to increased resistivity as film stress became more compressive than 400 MPa tensile. TEM and EDS measurements indicated that films in this range heterogeneously oxidized whereas films more tensile than 400 MPa tended to develop a Nb2O5 surface oxide with little bulk oxidation, NbO. Resistivity of the films tended to increase as the oxidation occurred with little to no increase in resistivity for the tensile Nb films. The superconductive properties were measured using a MPMS tool operating on the Meissner effect. Results indicated that niobium films better than 400 MPa tensile had a Tc close to the dirty superconductive limit of 8.45 K. As the films transitioned to compressive, the Tc decreased significantly. To confirm that oxidation was responsible for the Tc reduction, SIMS and XPS was performed on the films. These results indicated an expected Nb2O5 surface oxide and then a diffusion process of oxygen into the bulk of the films. It also indicated that the very tensile films could resist bulk oxidation more effectively and maintain an oxygen concentrations below 1 at %.

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5. CONCLUSIONS

This LDRD has discovered much interesting science during characterization down the path of fabrication of these NW. Electrical characterization of the Ga NW embedded in silicon was performed with characterization spanning, size, implantation dose, and temperature. NWs created this method offer excellent resistivity of 1 mΩ-cm at room temperature, excellent resistivity at 4 K (although only anecdotal evidence of superconductivity was observed), and act as a very Ohmic contact between silicon and tungsten (probe tips). I-V behavior was measured at 10 K and 4 K; however, the extent of the physics of this behavior was not greatly studied due to time limitations.

Ga-Si NW were also successfully fabricated using FIB implantation and highly selective etching in an ICP RIE. Suspended NW with dimensions down to 20 nm x 30 nm x 10 μm were fabricated and electrically tested. These devices demonstrated an exceptional sensitivity to vacuum according the Pirani effect (heat removal by molecular flow of gas particles affected the resistivity of the wire). This effect was measured and experimentally characterized as well as mathematically derived using the heat equation. From this set of work, nanoscale Pirani gauges were designed and tested. A second note from this lithographic technique is that it can also be utilized to make very small features (other than NW) in silicon. This was demonstrated by printing of the Sandia thunderbird logo at 4 um widths with pixel resolution down to 25 nm.

Finally, but most importantly, sputtered niobium was developed and characterized for the μFab. Niobium is a SC extensively utilized due to its property of having a critical temperature (T_c) around 9.2 for crystalline layers and 8.4 for sputtered thin films. By deposition of this film on suspended NWs and measuring the T_c, significantly lower than expected SC transitions were observed. To conclusively rule out effects other than dimensionality, thin film investigations were performed. It was found that Nb oxides quite rapidly in atmosphere, as described in literature, and was more likely the cause of our transition suppression in the NW. A surprising result was that we determined that increasing the stress, towards tensile, of the sputtered Nb film could retard bulk oxidation up to two years. This result helps drive the use of Nb as a superconductive film for manufacturability of SCE circuits.

In general, the SC effect of the Ga thin film was not conclusively observed. Strange electrical behavior at 4 K of the embedded NW was measured but the underlying physics of the devices remains a very intriguing mystery; worthy of future LDRD efforts. Some Meissner SC measurements of the Ga films suggested that a possible transition was occurring but due to the thin nature of the films, measurements are not conclusive. Efforts to measure superconductivity of Nb on suspended NW were indeed successful, but oxidation of the Nb confounded nanoscales effects of SC. The sputtered Nb we characterize in this report would be sufficient, in addition to accounting for the reduced thickness effect, for creating suspended SC NW. In this regime, care would be needed to account for the Pirani effect forcing the NW to leave the SC regime mid measurements.

In summary 3 types of devices were created and two fabrication techniques developed. Device 1 is a suspended silicon nanowire Pirani gauge with good sensitivity in the 100 mTorr to 100 Torr range with measurements suggesting future work. Device 2 was embedded high conductivity Ga

nanowires in silicon; these devices offer good thermal contact to the substrate eliminating nanowire Joule heating and potentially superconductivity. Device 3 are Nb coated suspended silicon nanowires; under the newly established conditions it is likely that nanoscale investigations can be performed without the threat of oxidation confounding the measurements. The first fabrication technique developed was the ability to use Ga lithography for repeatable nanowire creation in silicon; this technique offers the advantage of rapid prototyping and 3-D architecture in silicon. The second fabrication technique developed was a superconducting sputtered niobium with the ability to resist oxidation; this technique will prove valuable to future superconducting electronics efforts.

This LDRD work generated the following publications:

- Henry, M.D., Shaner, E.A., Jarecki, R., "Silicon Nanowire Pirani Sensor Fabricated Using FIB Lithography", IEEE DRC 71st Annual, 2013.
- Patent Application – SD 12277 - "Silicon Nanowire Pirani Gauge Fabricated Using FIB Lithography".
- Henry MD, Wolfley S, Monson T, Clark BG, Shaner EA, Jarecki R, "Stress dependent oxidation of sputtered niobium and effects on superconductivity", accepted for publication in Jour Appl Phys, 2014.

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