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Accelerating Development of Advanced Inverters: Evaluation of Anti-Islanding Schemes with Grid Support Functions and Preliminary Laboratory Demonstration

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Accelerating Development of Advanced Inverters: Evaluation of Anti-Islanding Schemes with Grid Support Functions and Preliminary Laboratory Demonstration

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Abstract

The high penetration of utility interconnected photovoltaic (PV) systems is causing heightened concern over the effect that variable renewable generation will have on the electrical power system (EPS). These concerns have initiated the need to amend the utility interconnection standard to allow advanced inverter control functionalities that provide: (1) reactive power control for voltage support, (2) real power control for frequency support and (3) better tolerance of grid disturbances. These capabilities are aimed at minimizing the negative impact distributed PV systems may have on EPS voltage and frequency. Unfortunately, these advanced control functions may interfere with island detection schemes, and further development of advanced inverter functions requires a study of the effect of advanced functions on the efficacy of anti-islanding schemes employed in industry. This report summarizes the analytical, simulation and experimental work to study interactions between advanced inverter functions and anti-islanding schemes being employed in distributed PV systems.

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NOMENCLATURE

AC	Alternating Current
AI	Anti-Islanding
dB	decibel
DC	Direct Current
DER	Distributed Energy Resource
DETL	Distributed Energy Technology Lab
DOE	Department of Energy
DUT	Device Under Test
EPS	Electrical Power System
GSF	Grid Support Function
MPPT	Maximum Power Point Tracking
NPPT	Northern Plains Power Technologies
OUF	Over or Under Frequency
OUV	Over or Under Voltage
PLL	Phase-Locked Loop
PV	Photovoltaic or Photovoltaics
RLC load	A load containing a resistor, an inductor and a capacitor
ROT	Run-On Time
SFS	Sandia Frequency Shift
SNL	Sandia National Laboratories
VAr	Volt-Amps reactive
W	Watts

1. INTRODUCTION

In this chapter essential background is provided as well as information on the structure of the project, layout of this report and outcomes of the research.

1.1. Background

1.1.1. *The Emerging Role of PV*

Historically, PV power plants were relatively small, and their numbers on utility circuits were low enough such that any impacts of the PV plants tended to be lost in the variability of the load. For this reason, and because most of these plants were connected to distribution circuits, utilities tended to regard PV basically as a negative load. The only special requirements were that PV not support an island for longer than 2 sec, that the quality of power being delivered be in compliance, and that the PV source stop delivering power if the voltage or frequency deviated outside of narrowly-defined windows.

Today, this situation is changing rapidly. PV plants as large as 5 MW have appeared on distribution feeders, larger plants are appearing on sub-transmission systems, and some regions have seen enough PV deployed on feeders that at times portions of the distribution system are sourcing power back to the transmission system. The “negative load” treatment is clearly not appropriate in this case. In fact, as more distributed renewable generation is incorporated into the grid, well-regulated conventional generation will be displaced by stochastic energy sources, which are likely to contribute to voltage and frequency regulation difficulties [1]-[3]. In response, utilities are becoming increasingly interested in requiring that PV plants act more like generation assets, meaning that they should participate in voltage and frequency regulation, grid stability maintenance, and other protective and security protocols. To that end, inverter manufacturers have been incorporating functions collectively known as “grid support functions”, “advanced inverter functions”, or “smart inverter functions”. The term “grid support functions” (GSFs) will be used here as it is less generic than the others. GSFs will allow PV to play a more active role in the grid and thus increase the value of PV, but there is also a concern that GSFs will impede the ability of distribution-connected inverters to detect and prevent unintentional islanding. This concern arises because most active anti-islanding functions rely on exacerbating abnormal grid conditions, whereas GSFs are designed to reduce the impact of abnormal grid conditions. For example, if a low frequency is detected, it is difficult for the inverter to determine whether the low frequency indicates a system-level condition that should be ridden through, or a local condition that indicates an island and necessitates a shutdown.

1.1.2. *Grid Support Functions*

To improve grid performance, new control functions are being investigated for use in distributed PV converters. Two grid support functions have been proposed: volt-var and frequency-watt [1],[2]. The main parameters for the volt-var control that can be set are the four voltages V_1 , V_2 , V_3 and V_4 and corresponding four reactive power quantities Q_1 , Q_2 , Q_3 and Q_4 . A plot of the volt-var characteristic used to control the inverter’s reactive power is shown in Figure 1 for the expected operating condition $Q_2=Q_3=0$ and $Q_{max}=Q_1=-Q_4$ volt-var. Depending on the irradiance

conditions, Q_{max} may be limited ($Q_{max} < Q_I$) by the reactive power capability of the inverter. In other words, Q_{max} would be whatever capability the inverter has “left over” after the real power has been taken into account, and is given by:

$$Q_{max}(t_k) = \sqrt{S_{rated}^2 - (P(t_k))^2} \quad (1)$$

where S_{rated} is the inverter’s rated apparent power capability and $P(t_k)$ is the real power being produced at the k^{th} discrete time interval. Bear in mind that Q_{max} is not constant when defined in this way. What is described here is VV11 (watt priority function and is not the case for the VV12 (VAr priority function)

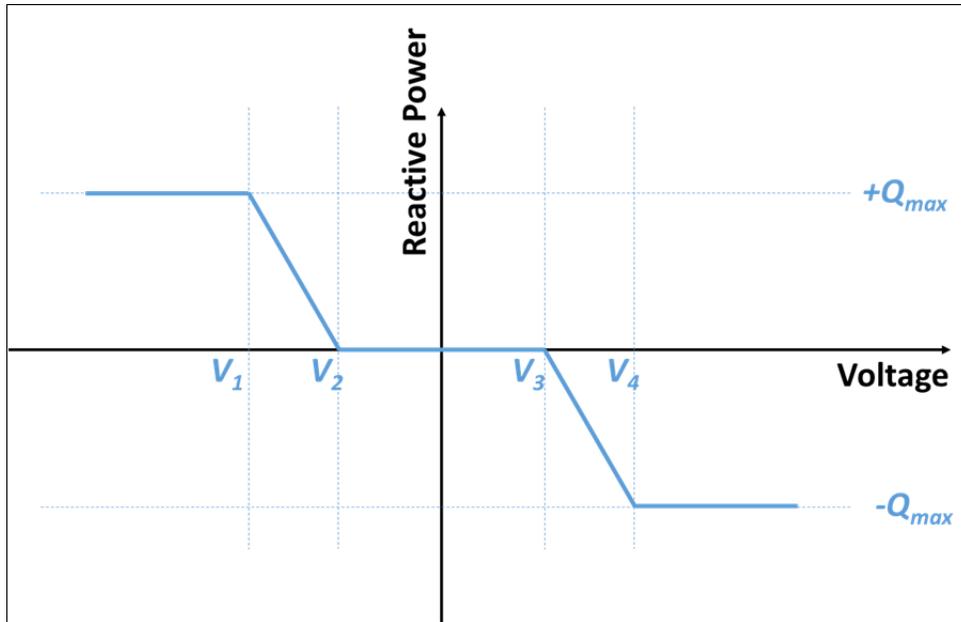


Figure 1. Plot of the volt-var characteristic used in this work

A plot of the frequency-watt characteristic used to control the inverter’s output power is shown in

Figure 2. This is a general characteristic that covers both upward and downward frequency support. It is noted that upward frequency support requires the inverter to source additional power in response to a sagging grid frequency, which requires either that the PV plant be operated below its maximum power point, or that the plant include energy storage.

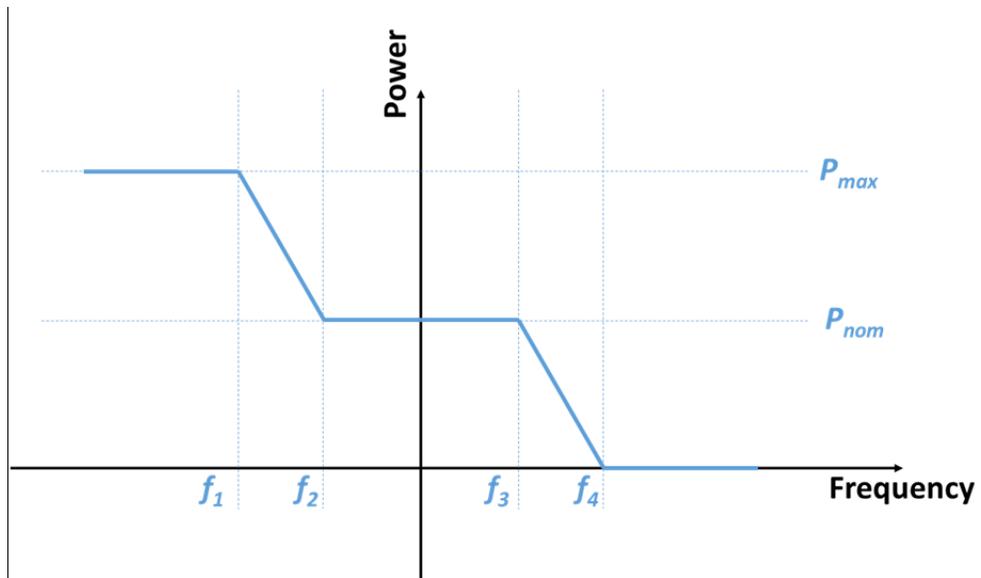


Figure 2. Plot of the frequency-watt characteristic used in this work

1.1.3. The IEEE 1547.1 Anti-Islanding Test

Most modern PV inverters are designed to pass the IEEE 1547.1 anti-islanding test, and are certified as being able to pass that test under UL-1741. This test is a single-inverter test using a resonant RLC load with quality factor of 1.0, and the standard requires that under these circumstances the inverter be able to detect and cease to energize an unintentional island within 2 sec [1]. In fact, included in the test is the matched-load case, wherein generation matches load power at rated voltage; in this case, the voltage measured at the point of common coupling does not change when disconnected from the utility. Thus, it might be expected that an unintentional island containing a single PV inverter and lasting longer than 2 sec would be extremely unlikely.

However, in the real world, many deviations from the conditions of this anti-islanding test are encountered. One increasingly common deviation is that islands in the field would rarely contain only a single inverter. Most PV installations will contain more than one inverter (in fact, for AC arrays or plants using string inverters, there may be hundreds of inverters), and a distribution feeder with a high penetration of PV may be hosting many inverters from several different manufacturers. That last variable is of particular concern, because in the US the means by which manufacturers detect and prevent unintentional islands are not standardized; manufacturers typically use proprietary means of passing the IEEE 1547.1 test. Note that IEEE 1547 requires that a distributed generator detect and cease to energize an island within 2 sec under all circumstances, regardless of the number of distributed generators or the loading conditions. There is a concern that, if several manufacturers' products are contained within an island, these proprietary means of safely de-energizing the island may be incompatible with each other; that is, the 2 second maximum time to de-energize would not be reliably met for all loading conditions and all combinations of distributed generators.

1.2. R&D Approach

1.2.1 Project Narrative

The project was structured as follows. During FY13, Sandia National Laboratories (SNL) and Northern Plains Power Technologies (NPPT) worked on developing detailed, manufacturer-specific models of residential-scale, single-phase photovoltaic (PV) inverters to be used in an investigation on the impact of having multiple inverters in an island as well as having multiple manufacturers' products contained in an island. In parallel with the model development work, Sandia investigators in the Distributed Energy Technologies Laboratory (DETL) acquired units of the inverters being modeled and performed characterization experiments on these units, to be used for model validation purposes and to improve fundamental understanding of multiple inverter behavior. The team designed a set of experiments using single and multiple inverters in the 10-node inverter testbed at the DETL, and these data were to be analyzed and compared against model results. Once validated, the models would be used to extend the experimental results, seeking additional validation for specific cases as appropriate.

As part of this work, a procedure was to be developed and adopted for ensuring that the quality factor Q of the resonant RLC circuit used in anti-islanding studies was kept constant during multiple inverter tests. This is important because it is well known that increasing Q will cause run-on times to rise, and this effect would mask the impact of the multiple inverters. During this same time period, NPPT and SNL investigators collaborated with NEDO and Kandenko in Japan regarding Japan's new anti-islanding technology and standard, and its potential applicability in the US [1].

Finally, starting in the summer of 2013, additional experimental, modeling and theoretical work was begun to characterize the potential interactions between grid support functions and anti-islanding. The goal of this work was to be able to make at least preliminary determinations regarding the magnitude of this potential problem, and gather insights regarding its solution.

1.2.2 Report Layout

In Chapter 2, a procedure for conducting multi-inverter anti-islanding experiments both in hardware and simulation is described. Therein, detailed models of the DETL 10-node inverter testbed and four commercial PV inverter systems are developed, a method for maintaining unity quality factor for non-unity power factor operation is described and the results of multi-inverter experiments attained in simulation are compared to those attained in the laboratory in terms of run-on time (ROTs) following grid disconnection. These experiments are done without GSFs employed and are intended to assess the software models. In Chapter 3, the software models are augmented to include GSFs and then undergo exhaustive simulation study to characterize their performance subject to different permutations of power level and interconnectivity. In Chapter 4, theoretical analysis is employed to explain some of the anticipated interactions between GSFs and anti-islanding schemes. In Chapter 5, efforts to integrate volt-var functionality onto a commercial PV inverter are described, and the successful laboratory test results are provided. Conclusions are provided in Chapter 6.

2. BASELINE MULTIPLE INVERTER TESTING

2.1. System Modeling and Experimentation

In Task 1 of this project, the performance of multiple-inverter systems was evaluated in simulation and hardware experiment. The specific deliverable items were:

- Documentation describing the impacts on run-on time (ROT) of multiple inverters from different manufacturers;
- A procedure for maintaining unity quality factor for non-unity power factor operation;
- Documentation of responses to the additional support required by Sandia.

2.1.1. Procedure

To conduct the evaluation, inverter hardware was attained from four different manufacturers, detailed system models were developed for each through collaboration with vendors, and the 10-node inverter testbed at the Distributed Energy Technology Lab (DETL) at Sandia National Laboratories (SNL) was modeled. Multiple inverters were then interconnected via the testbed for selected cases, both in hardware and in simulation.

In particular, simulations were conducted to examine the concerns associated with multi-inverter systems having several different types of active anti-islanding. The focus was on the two most commonly-used islanding detection means:

- Sandia Frequency Shift (SFS), in which the inverters' output current phase is shifted as a function of the voltage frequency error.
- Impedance detection, in which an output pulse in either W or VAR is used to periodically check for a suspicious change in the impedance of the grid as seen from the inverters.

These simulations were to be coordinated with tests to be conducted on commercially-available inverters in the 10-node inverter testbed in the Distributed Energy Technologies Laboratory (DETL) at Sandia.

2.1.2. The DETL 10-Node Inverter Testbed and Model

The purpose of the 10-node inverter testbed is to allow the interconnection of several (up to 10) commercial inverters onto a single bus, with shared load, for anti-islanding testing. A photo of the 10-node inverter testbed is shown in Figure 3. To ensure proper representation of the system in the simulations, a detailed model of the 10-node testbed was developed. The model schematic is shown in Figure 4. The utility source is at the upper left, and the ten inverter connection points are in the yellow blocks across the bottom of the schematic. Transformer and conductor impedances are included in the model. The transformer impedances were computed from the

transformer nameplate information, and the conductor impedances were calculated based on conductor types and lengths supplied by DETL investigators.



Figure 3. 10-node Inverter Testbed at the Distributed Energy Technology Lab (DETL).

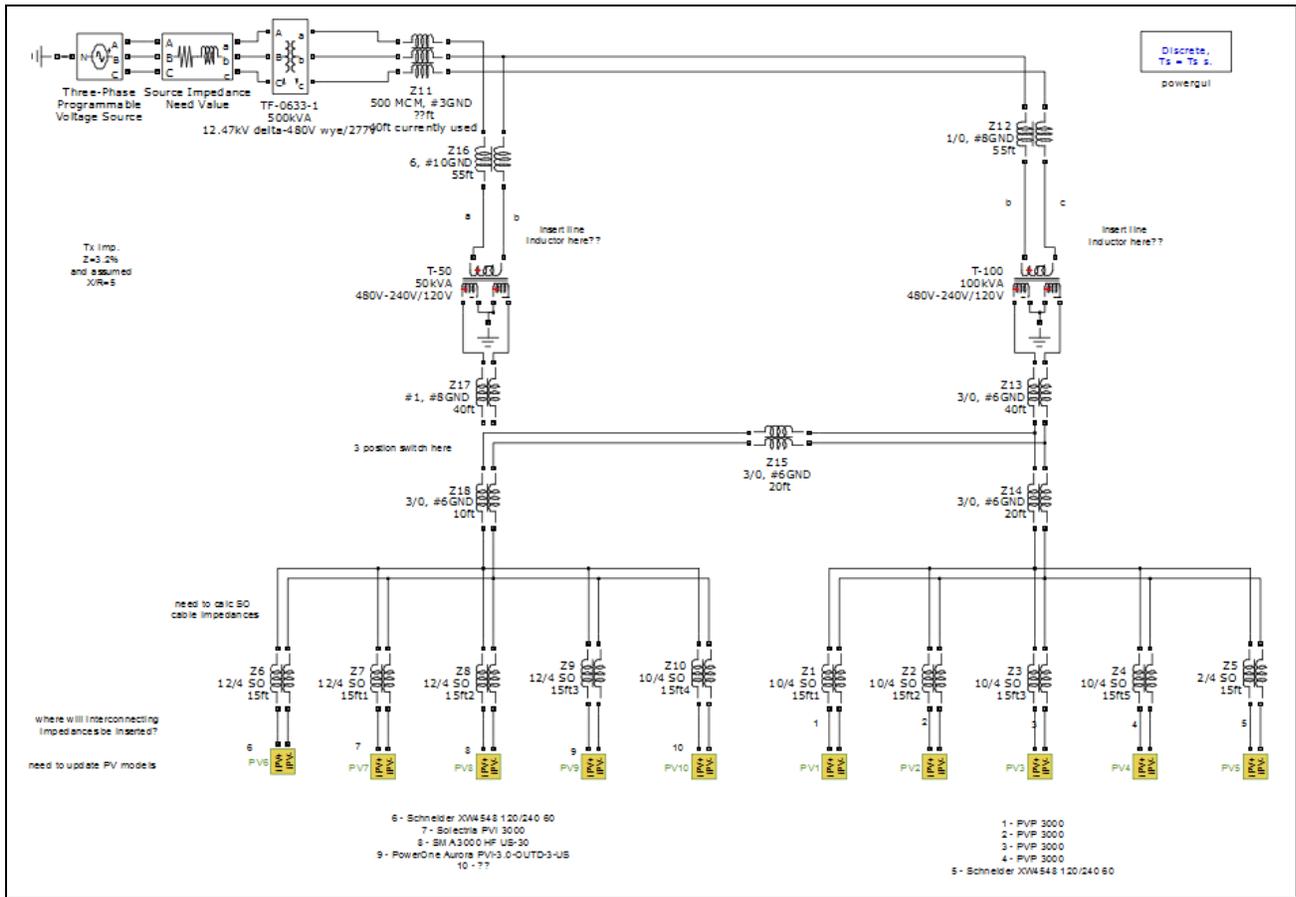


Figure 4. MATLAB/Simulink model of the DETL 10-node inverter testbed.

2.1.3. Inverter Model Development

The second step was the development of a set of manufacturer-specific inverter models. A conceptual diagram illustrating the structure of these models is shown in Figure 5.

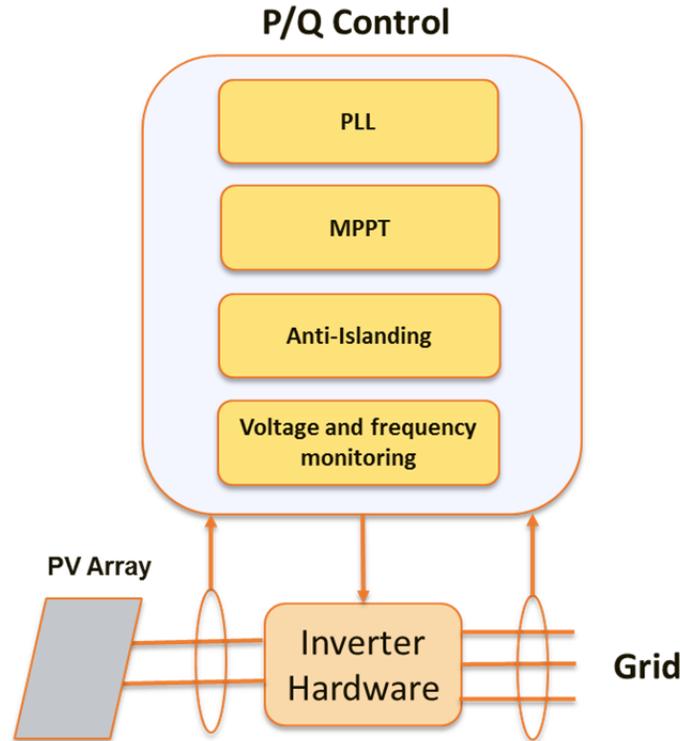


Figure 5. Conceptual diagram of MATLAB/Simulink Inverter model (without advanced functions)

At the time of this report, models exist for four manufacturers' products, denoted herein as Inverters A, B, C and D. All are switch-averaged models and include detailed representations of the anti-islanding schemes, grid synchronization (i.e. phase-locked loops (PLL)) and current wave shaping controls, over/under voltage and over/under frequency detection, and the hardware filters. Some include maximum power point tracking (MPPT) while others do not. These inverters represent four distinctly different but commercially common anti-islanding approaches, as listed in Table 1. To develop the models, nondisclosure agreements were first executed with all four manufacturers, and the A, B, C, D designations are used to maintain anonymity.

Table 1. Inverters and anti-islanding methods

Inverter designation	Anti-islanding method used
A	SFS, implemented using phase or frequency shifting
B	SFS combined with impedance detection using a reactive power pulse
C	Impedance detection based on a real power pulse, coupled with a voltage-current correlation detection scheme
D	Impedance detection

Inverter data sets with sufficient detail to support the production of high-fidelity manufacturer-specific models were developed. These data were used to construct the MATLAB/Simulink inverter models. In parallel with the model construction, inverter testing was performed in the DETL, and these test data were used to check the validity of the models.

It is noted that, for intellectual property security reasons, manufacturers are often unable to share certain details of their inverters' operation. Unfortunately, these details often pertain to aspects of the inverter that are critical to precisely matching modeled and measured performance. This problem was circumvented via one of three means: a) persuading manufacturers to provide needed information; b) obtaining as much data as the manufacturers could provide, and then using those together with DETL-gathered experimental data and the experience of the Sandia team to develop in-house models of missing components based on a knowledge of the required behavior and laboratory data; or c) obtaining a "black-box" model from the manufacturer in which the sensitive data were encrypted and not visible to the end user. This process met with considerable success, but was time-consuming; the process from first contact to a working model took, on average, six to nine months to complete. Though time-consuming, this process was anticipated.

However, an issue arose that was not anticipated. There were often differences between the inverters' conceptual design and actual implementation that, while very subtle, could have significant impacts on an inverter's ability to detect an unintentional island. These differences themselves were not surprising; such differences often arise in the final steps of commercial product development. What was surprising was the sensitivity of the anti-islanding behavior to very subtle variations in control software. The team has been working with the manufacturers to uncover the differences and either explain or correct them; this process has been more time consuming than the process of developing the models, and it has put a greater burden on the manufacturers. Based on the work done to date, it appears that the mechanism most often responsible for this problem lies in differences between the modeled and as-implemented phase-locked loops (PLLs). Considerable progress has been made in harmonizing the models and laboratory results, but additional work remains.

2.2. Maintaining quality factor of 1.0 for non-unity power factor operation

The goal of this task was to develop a procedure that enables an experimenter to conduct tests in both the "AC array" and "solar subdivision" configurations that isolate the impact of multiple inverters from the impact of increasing resonant circuit quality factor Q . The quality factor Q is often designated as a circuit's *tendency to oscillate* at a particular frequency. It is well-known that active anti-islanding methods have more difficulty detecting an island when Q is higher because a higher Q circuit has a greater tendency to maintain a given frequency (e.g. 60 Hz) regardless of frequency manipulation schemes employed by the inverter(s).

When conducting tests for multiple-inverter islands, in which the goal is to determine the impact on ROT of the number of inverters in the island, it is desirable to be able to eliminate the

influence of changing Q on these results. Thus, the goal of this subtask is to allow decoupling of the number of inverters from the quality factor.

2.2.1 Tuning the Load for an Islanding Test

The quality factor Q of a parallel RLC circuit with resistance R , capacitance C and inductance L , assuming the series resistances of the L and C are negligible, is given by:

$$Q = R\sqrt{\frac{C}{L}} \quad (2)$$

The load's resonant frequency ω_0 in rad/sec is:

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (3)$$

In an anti-islanding test, the resistance is set to match the inverter real power, so if P is the PV inverter's real power output and V is the nominal terminal voltage in V_{rms} , then R is determined by:

$$R = \frac{V^2}{P} \quad (4)$$

The values V , P , Q and ω_0 are all known, so this constitutes a set of three equations in the three variables R , L and C . The load resistance R is given by (3); setting $Q = 1$, equations (2)-(4) give the following:

$$C = \frac{1}{R\omega_0} = \frac{P}{V^2\omega_0} \quad (5)$$

$$L = \frac{R}{\omega_0} = \frac{V^2}{P\omega_0} \quad (6)$$

Typically, when performing an anti-islanding test, an experimenter will compute the load resistance such that the net real power flow from the island is zero and make the initial adjustment. This would automatically satisfy the load resistance determination, assuming that losses in the C and L of the test apparatus are negligible. Next, the experimenter calculates the required values of C and L , and adjusts the experimental apparatus accordingly. In practice, additional adjustments will be necessary; due to stray reactances in the conductors and transformers as well as losses in the inductors and capacitors and other parasitic effects, the experimenter will generally need to readjust R , L and C to properly tune the circuit and match the load. For adjusting Q , it is generally preferable to adjust L , because the parasitic C in the island test apparatus should be very small, so most of the parasitic impedance is inductive.

2.2.2 Tuning the Load with Multiple Inverters

The primary challenge in applying this method occurs when trying to use it in the multi-inverter case with deliberately-added interconnecting impedances to simulate a higher level of electrical distance between the inverters. In that case, equation (2) is no longer strictly valid because the circuit may no longer be reasonably represented by parallel RLC components, and one must revisit the definition of quality factor:

$$Q = 2\pi \times \frac{\text{energy stored per cycle}}{\text{energy dissipated per cycle}} \quad (7)$$

The energy dissipated is easily obtained as it must be equal to the total real power injected into the circuit. The energy stored will be given by:

$$W_{\text{stored}} = W_{\text{stored},L} + W_{\text{stored},C} + \sum_{n=1}^N W_{L,\text{int},n} \quad (8)$$

where $W_{\text{stored},L}$ and $W_{\text{stored},C}$ are the energy stored in the RLC load inductors and capacitors, respectively, and $W_{L,\text{int},n}$ is the energy stored in each of the N interconnecting inductors. The energies stored in the capacitors and inductors are given by (9), (10) and (11) respectively.

$$W_{\text{stored},C} = \frac{1}{2} CV^2 \quad (9)$$

$$W_{\text{stored},L} = \frac{1}{2} LI^2 \quad (10)$$

$$W_{L,\text{int},n} = \frac{1}{2} L_{\text{int},n} i_{\text{int},n}^2 \quad (11)$$

2.3. Results of Simulation and Laboratory Experimentation

Due to different levels of effort from manufacturers, varying levels of discrepancy between the as-described and as-implemented inverter controls, and certain other logistical factors, the accuracy of the inverter models in terms of how well they predict laboratory results varies from one to another. For example, Figure 6 shows a comparison of simulated and measured data for Inverter B. Inverter B uses a combination of impedance detection and positive feedback, the so-called “quasi-SFS” method in which the positive feedback is applied to the output impedance detection pulse. The simulated data came from the sixth iteration of the manufacturer’s black-box model, but as can be seen in Figure 6, the model’s predictions of inverter performance can be quite accurate. The overall trend is the same in the lab and modeled results, and the difference in run-on times is generally around 2.5 line cycles or less. Figure 7 shows results of a model vs. lab comparison for the phase-shift version of Inverter A.

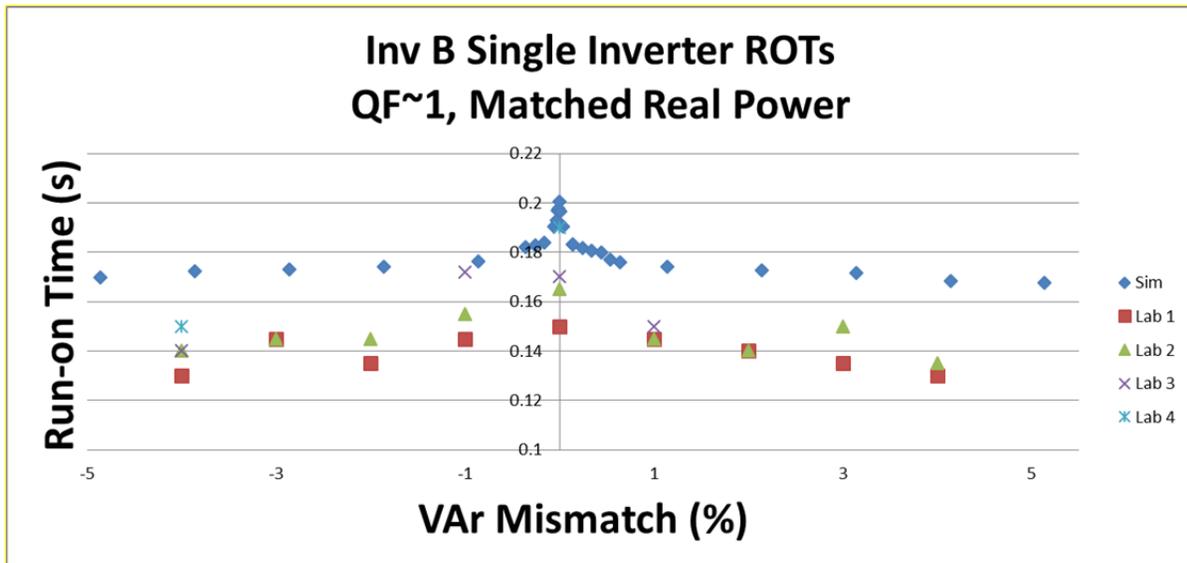


Figure 6. Simulated and measured run-on times for Inverter B, in the single-inverter case.

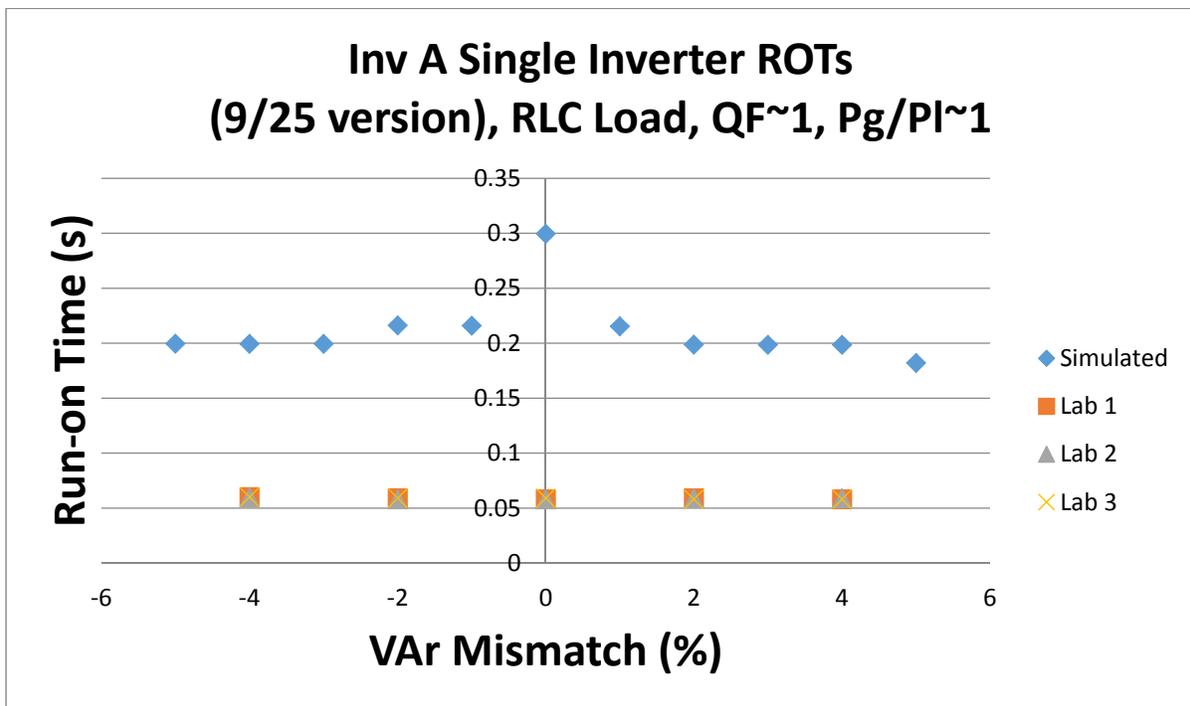


Figure 7. Simulated and measured run-on times for the phase-shift version of Inverter A, in the single-inverter case.

As noted in Table 1, Inverter A uses the Sandia Frequency Shift (SFS) method in which the output current of the inverter is adjusted using positive feedback on the voltage frequency error, without any impedance detection pulse. Either the phase or the frequency of the output current can be adjusted, and models of Inverter A using both methods have been produced. In this case, the matching between predicted and measured run-on times is reasonable except for the precisely matched case (zero VAr mismatch), where the model predicts run-on times on the order of twice

as long as those measured in the lab. However, a detailed comparison of the voltage and current data from the simulations and experiments indicated that, although the agreement was fairly good, the behavior of the modeled inverter in the island did not match the lab observations particularly well. In other words, the relatively good matching in the ROTs was somewhat coincidental. After considerable effort by the Sandia team and the manufacturer, it was determined that the reason for this discrepancy stems in part from a difference in the way the phase-locked loop (PLL) is implemented in the inverter, relative to how the manufacturer intended for the PLL to be implemented. This difference in PLL implementation led to a higher degree of instability than was intended, and it also appears to be causing the inverter to make an erroneous frequency measurement, so that the inverter “thinks” the frequency is different than it actually is. These behaviors caused the ROTs in the matched case to be shorter than expected. The Sandia team is currently working with the manufacturer to adjust the model accordingly.

Figure 8 shows a model-to-experiment comparison for a manufacturer-supplied “black box” model of Inverter C. This inverter uses two anti-islanding methods in concert: an active method based on “classical” impedance detection using a real power pulse, and a passive method in which the correlation between voltage and frequency is monitored by checking whether the signs of ΔV and ΔI at the inverter terminals are the same over three consecutive monitoring periods. The passive method amounts to another form of impedance detection: if the grid is still present, it and the loads will control the inverter’s terminal voltage, so that there should be little correlation between ΔV and ΔI . If an island has been formed, the inverter’s terminal voltage is the Ohm’s Law response of the load to the inverter’s output current, and ΔV and ΔI should be well-correlated, at least over short time intervals. In this case, neither the ROTs nor the inverter behavior match the experimental results well. For mismatched cases the predictions and measurements are similar, but for matched cases there is a significant and important discrepancy as the model predicts considerably longer run-on times and much greater island stability than is observed in the lab. The model’s prediction is much more in line with physical expectations than are the laboratory results, and once again it appears that the reason can be traced to the simulated PLL being more ideal than the actually-implemented PLL, which causes the real-world inverter to be considerably less stable than the conceptual one. In the laboratory, the impedance-detection pulses create considerable oscillation in the inverter output because of this instability, and when the grid is not present that oscillation triggers the passive anti-islanding method. Note that as long as the instability does not negatively impact the inverter’s output power quality when the grid is connected, the instability is not necessarily undesirable. In this case also, the Sandia team is continuing to work with the manufacturer to improve the fidelity of the model.

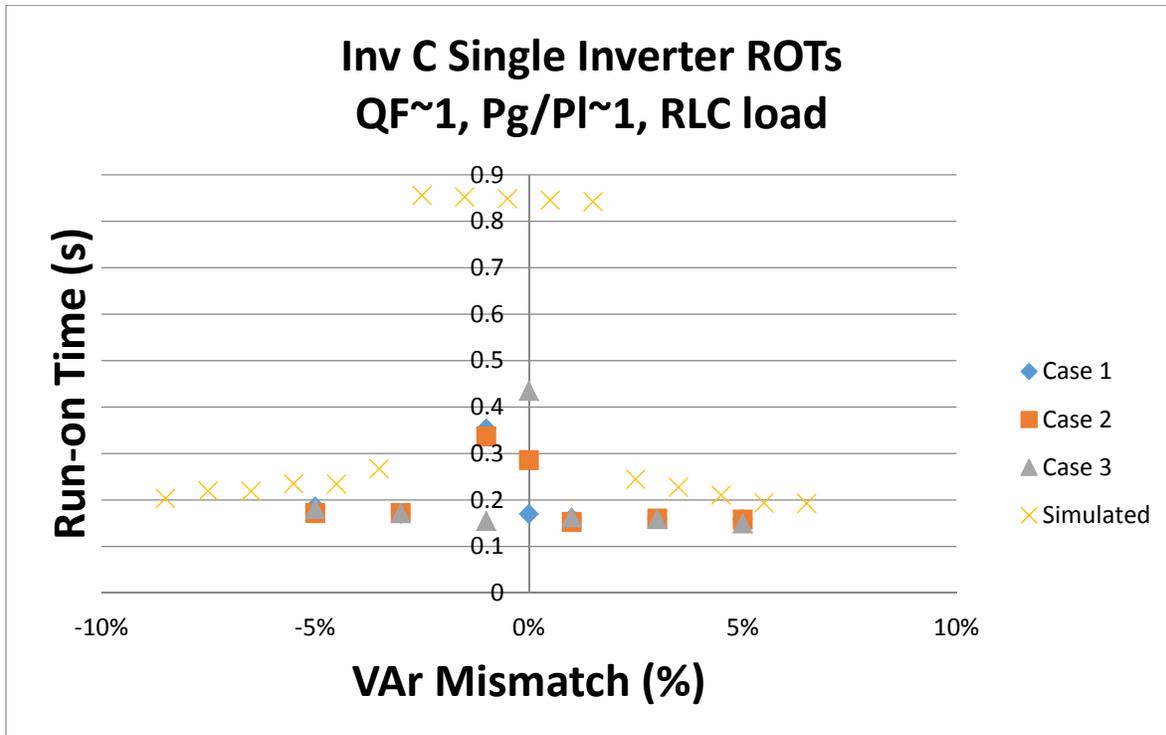


Figure 8. Simulated and measured ROTs for the “black box” version of inverter C, in the single-inverter case.

These models have been used to evaluate multi-inverter interactions, and also interactions between different manufacturers’ products, within the simulated 10-node testbed shown in Figure 4. The island is configured in the “AC array” configuration in which there is a local RLC load associated with each inverter. Figure 9 shows simulated run-on times for Inverter A as a function of VAr mismatch, for cases involving 1, 2, 3, 5, and 10 inverters of the same type. Figure 9 shows results for the phase-shift version. The maximum ROT is observed for a closely-matched case, which is as expected, but that maximum run-on time decreases as the number of inverters increases. This suggests that for the phase-shift based SFS method, it is not expected that ROTs will lengthen significantly as the number of inverters increases, when all inverters are from the same manufacturer. In fact, it appears that the presence of multiple inverters actually *improves* the effectiveness of SFS because the overall stability of the island decreases.

This multi-inverter experiment was repeated using an “in-house” version of the model of Inverter C. Figure 10 shows the results. Unlike the results in Figure 9, Figure 10 indicates that this island detection method strongly deteriorates as the number of inverters increases, because the impedance detection pulses are not synchronized and tend to “average out” over larger numbers of inverters. The situation could be improved by increasing the size of the pulse or by adjusting detection thresholds, but it cannot be eliminated entirely.

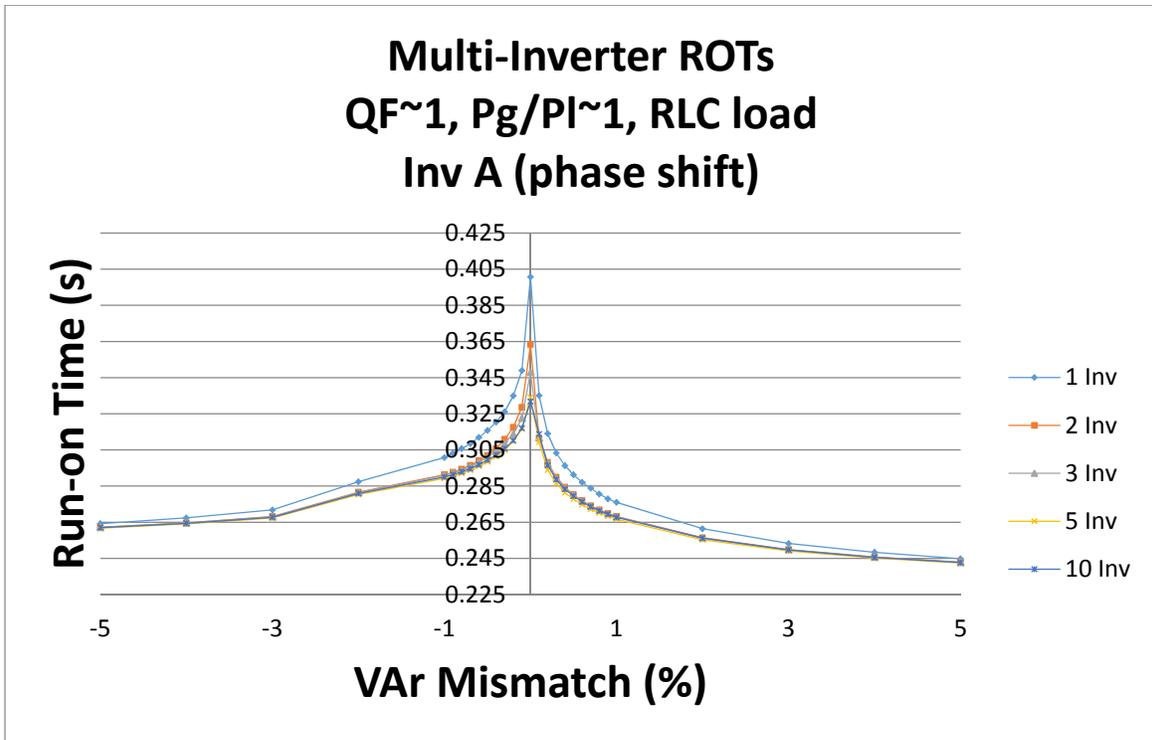


Figure 9. Simulated run-on time (ROT) vs. VAr mismatch for the phase-shift version of Inverter A. Curves are shown for islands with 1, 2, 3, 5, and 10 inverters.

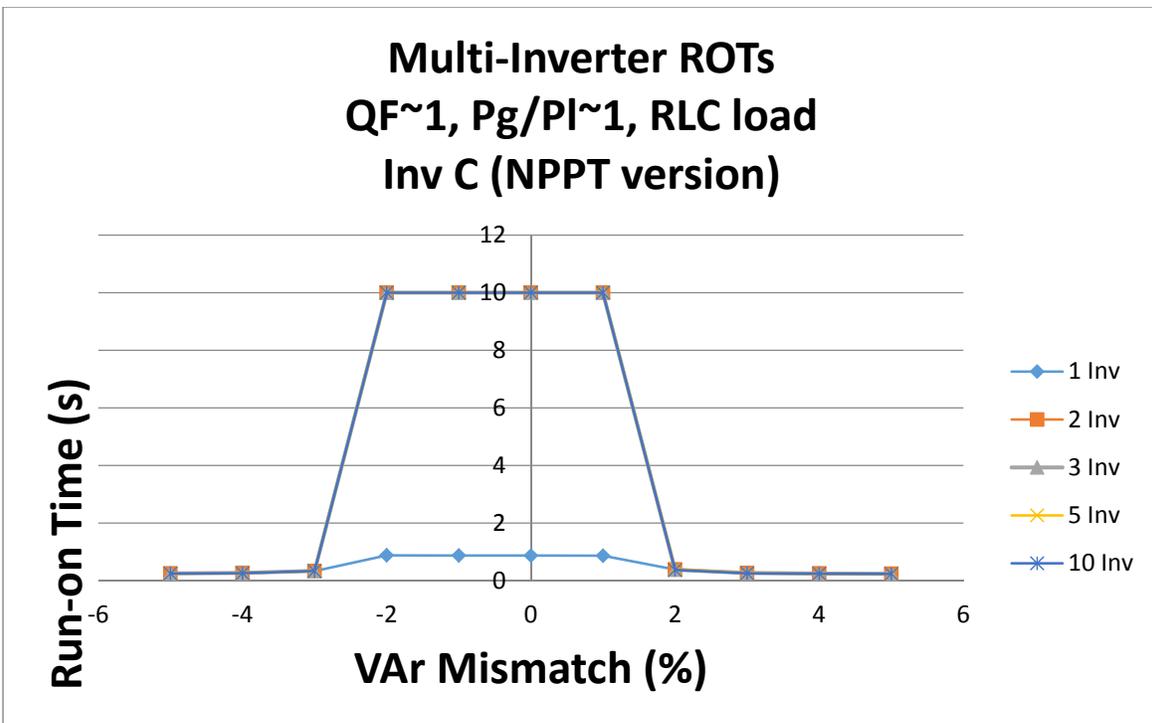


Figure 10. Simulated run-on time (ROT) vs. VAr mismatch for the in-house model of Inverter C. Curves are shown for islands with 1, 2, 3, 5, and 10 inverters.

It is clear that there is a significant difference in the behavior of these two methods, and thus it is of interest to see whether they may interact with one another in any unfavorable way. Figure 11 shows the results of simulations designed to investigate this possibility. In these simulations, the 10-node testbed is simulated with ten inverters present in each simulation.

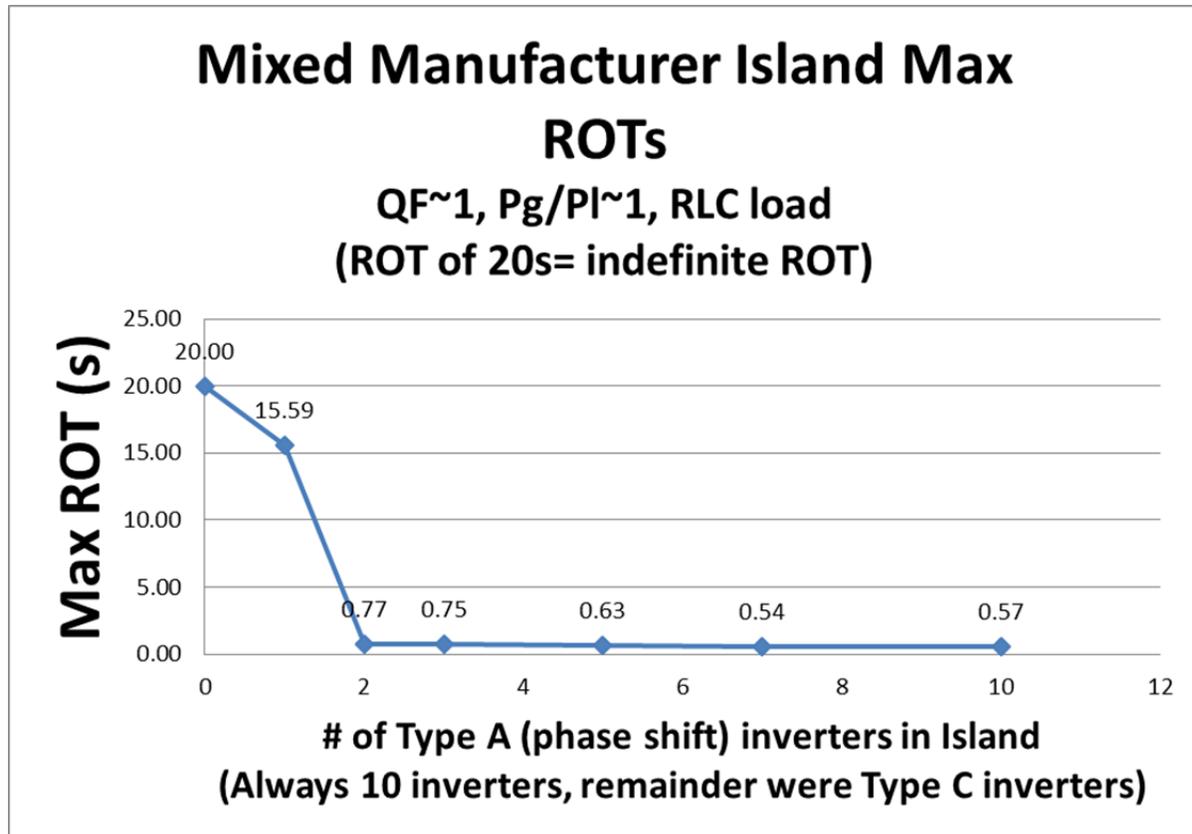


Figure 11. ROTs for an island containing ten inverters, in which some use impedance detection and some use phase shift-based SFS. The x-axis value is the number of SFS inverters, so the number of Z-detection inverters at each data point is $10 - x$.

The simulation starts with ten inverters all using impedance detection, and no inverters using SFS. Then, one by one, the impedance detection inverters are replaced with SFS inverters, until all ten inverters are SFS inverters. The run-on time as a function of the number of SFS inverters in the island is plotted in Figure 11. If the anti-islanding methods did not interact unfavorably with one another, it is expected that the plot would be monotonically increasing or decreasing. However, if there is an unfavorable interaction, one would expect a maximum in the plot somewhere in the middle. In this case, Figure 11 shows a decreasing trend from left to right, indicating that these two anti-islanding methods do *not* interact unfavorably with one another, and an island containing inverters of both types would not run on longer than an island containing only one type or the other.

Figure 12 shows the run-on times for a two-manufacturer test involving the frequency-injection version of inverter A, and the same inverter C as in Figure 11. The results in Figure 12 are similar; no interaction between the inverters is detected.

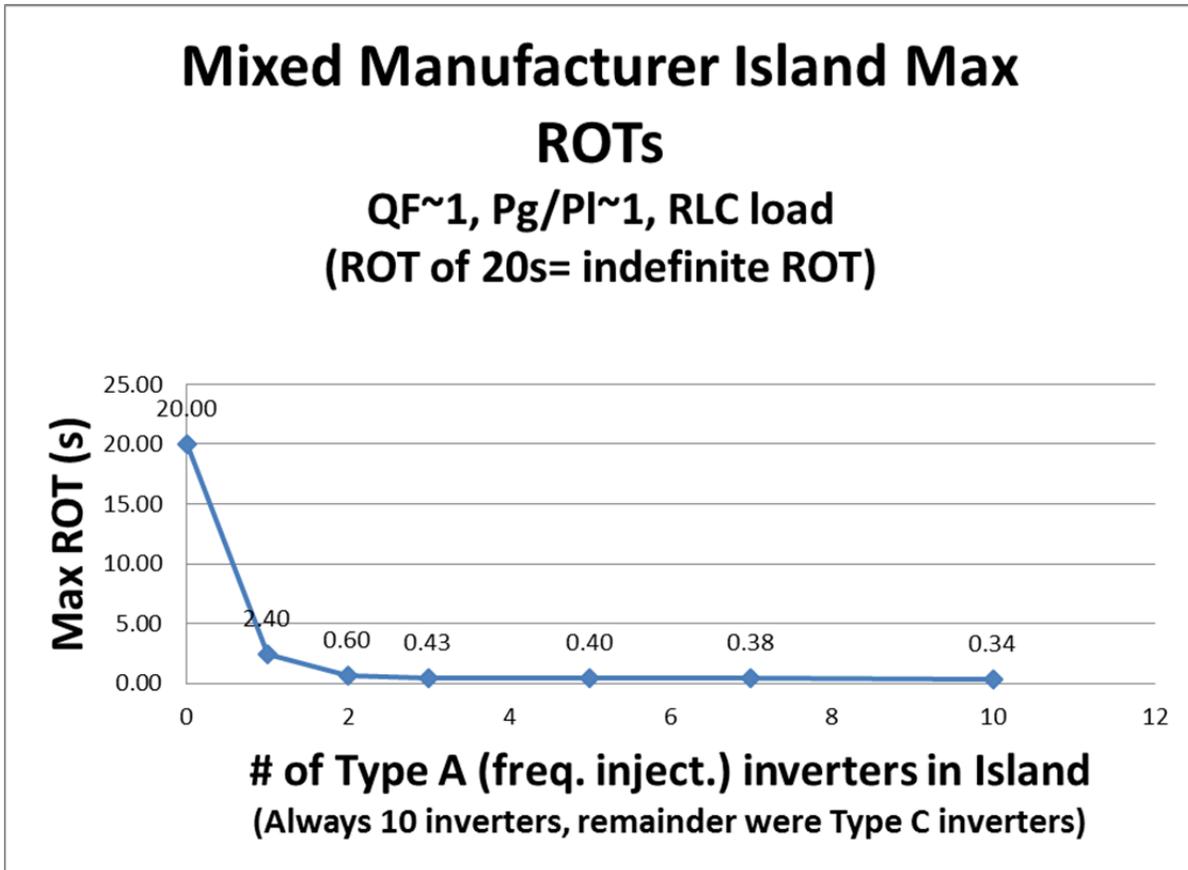


Figure 12. ROTs for an island containing ten inverters, in which some use impedance detection and some use frequency injection-based SFS. The x-axis value is the number of SFS inverters, so the number of Z-detection inverters at each data point is 10 – x.

2.4. Summary

The results of this section may be summed up as follows.

- During this first period of the work, most of the team’s time was consumed by developing the manufacturer-specific models. This process was expected to be long, but it has turned out to be longer than anticipated due to subtle differences between the fielded inverters and the design documentation provided by the manufacturers. The key issue appears to be the stability of real-world PLLs vs. the more idealized PLLs used in simulation. The team continues to work on this issue.
- Operational models have been produced that utilize two different variants of SFS (phase shift and frequency injection). In addition, another model that uses impedance detection coupled with a passive voltage-current correlation technique is working.
- Preliminary indications are that the positive-feedback based SFS method continues to work well in the multi-inverter case, but classical impedance detection methods perform poorly in the multiple inverter case.
- Preliminary indications suggest that for SFS and impedance detection, there is no adverse interaction between inverters using these two anti-islanding techniques.

3. IMPACT OF GRID SUPPORT FUNCTIONS ON ISLAND DETECTION EFFECTIVENESS

In Task 2, simulations and theoretical considerations were used to develop a better understanding of the potential impact of GSFs on the effectiveness of passive and active anti-islanding techniques. The grid support functions studied included:

- Low-voltage ride-through (LVRT)
- Low-frequency ride-through (LFRT)
- Voltage support via volt-var controls
- Frequency support via frequency-watt controls

Other advanced functions such as ramp rate control have not yet been considered. To study these impacts, the conceptual inverter model structure must be modified to add the volt-var and frequency-watt controls as well as updated voltage and frequency bounds; see Figure 13.

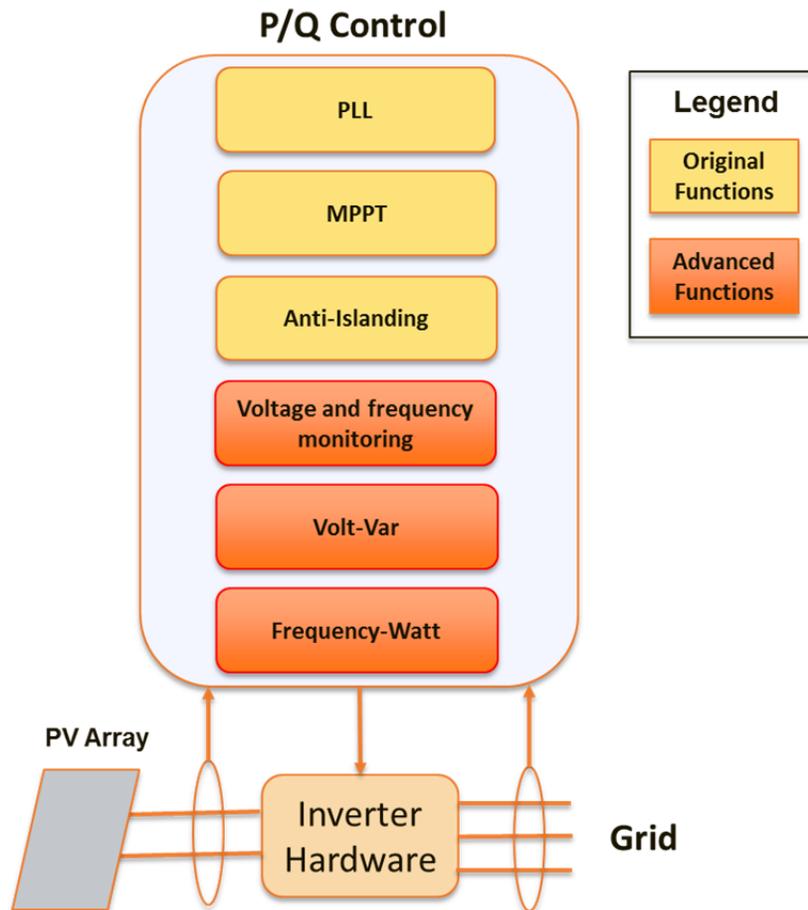


Figure 13. Conceptual diagram of MATLAB/Simulink Inverter model with advanced functions

Two paths were followed to evaluate the potential for adverse interaction between active anti-islanding and GSFs. The first was to look at a manufacturer-specific implementation of anti-islanding and GSFs and conduct risk-of-islanding studies with and without the GSF functions

enabled. A second more theoretical approach, supported using generic models, is discussed in Chapter 4 of this report.

3.1. Procedure

3.1.1. System Description

The inverter used for this work is a detailed manufacturer-specific model of a 500 kW inverter, used with the manufacturer’s permission. This is a switch-averaged model and includes highly detailed representations of all inverter controls, the PLL, the current regulators, the maximum power point tracker, and all DC and AC filters. The anti-islanding used is a phase shift-based SFS with a relatively high gain. For this part of the work, the inverter is programmed with the default IEEE 1547 voltage and frequency trips shown in Table 2. In addition to the default IEEE 1547 trips, this inverter includes a very fast overvoltage trip activated by instantaneous and not RMS voltage. This is a self-protection feature but it also helps prevent transient overvoltage, and most commercial inverters include a trip similar to this. All of the voltage trips are applied on a per-phase basis (if the voltage limits are violated on any one phase, the time-to-trip applies). This model was used partly because of availability, and partly because it has GSFs on-board. It seems more likely that GSFs will be implemented in the near future in inverters of this size than in the single-phase residential-scale inverters used in the preceding work. This model has been validated against laboratory data obtained by the manufacturer at NREL.

Table 2. Voltage and frequency trip setpoints used in this portion of the work.

Parameter and value	Time to trip
$0.5 \text{ pu} < V_{\text{rms}} \leq 0.88 \text{ pu}$	2 sec
$V_{\text{rms}} \leq 0.5 \text{ pu}$	160 msec
$1.1 \text{ pu} \leq V_{\text{rms}} < 1.2 \text{ pu}$	1 sec
$V_{\text{rms}} \geq 1.2 \text{ pu}$	160 msec
$V_{\text{inst}} \geq 1.2 \text{ pu}$	500 μ sec
$f \leq 59.3 \text{ Hz}$	160 msec
$f \geq 60.5 \text{ Hz}$	160 msec

The values for V_1 , V_2 , V_3 and V_4 used in this work are given in Table 3, and a block diagram of the implementation of the volt-var controller is shown in Figure 14. This controller was tested using rectangular voltage disturbances (upward and downward steps) and was found to perform as expected.

Table 3. Parameter settings for the volt-var controller.

Parameter	Value (per unit)
V_1	0.95
V_2	0.98
V_3	1.02
V_4	1.05

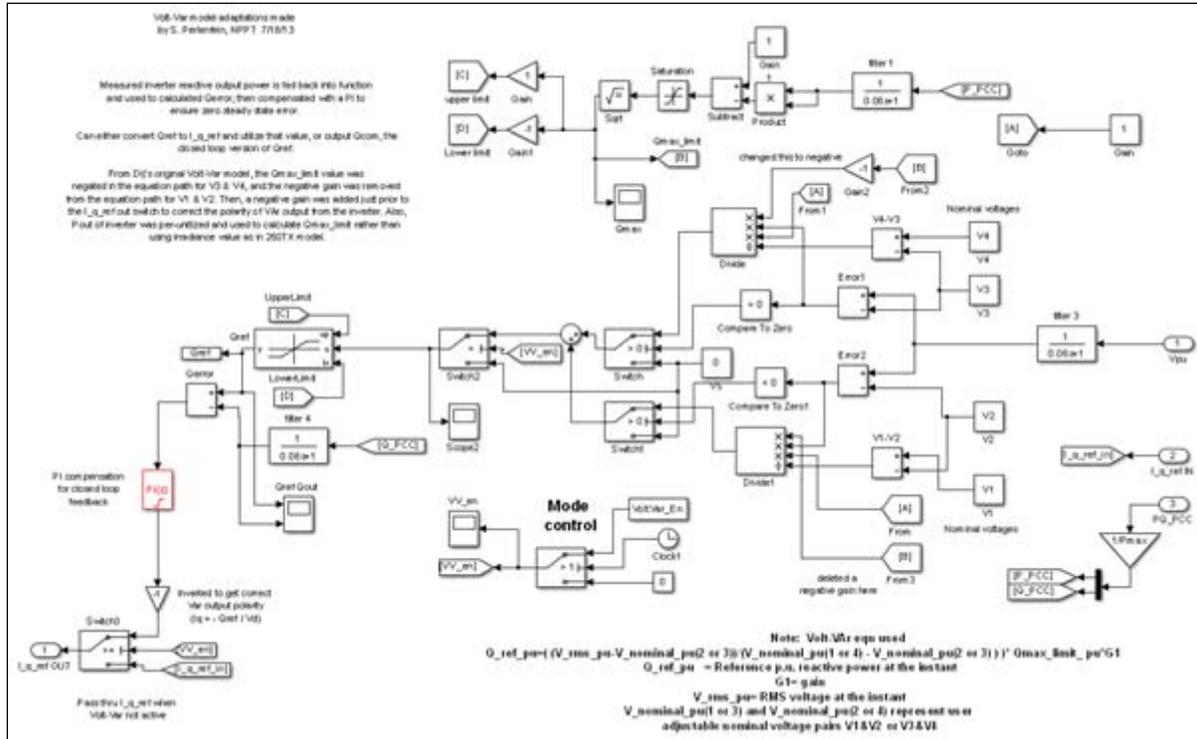


Figure 14. Block diagram of the volt-var controller used here.

Since energy storage is not included in the work described here, so $P_{max} = P_{nom}$, and f_1 and f_2 have no effect and are not used. The PV inverter only adjusts its power as a function of frequency for positive frequency deviations. The values for parameters f_3 and f_4 are given in Table 4, and a block diagram of the implementation of the frequency-watt controller is shown in Figure 15. This controller was tested using rectangular frequency disturbances (upward and downward steps) and was found to perform as expected.

The model specified in Table 4 and Figure 15 was used to quantify the impact of volt-var and frequency-watt controls on the effectiveness of active anti-islanding by performing a large series of simulations in which the inverter was islanded with an RLC load, with and without the GSFs active, for different irradiance levels and different values of RLC load parameters. In each simulation, the inverter's run-on time was recorded. By comparing the run-on times with and without the GSFs, the impact of GSFs on anti-islanding can be ascertained.

Table 4. Parameter settings for the frequency-watt controller.

Parameter	Value (Hz)
f_3	60.2
f_4	61

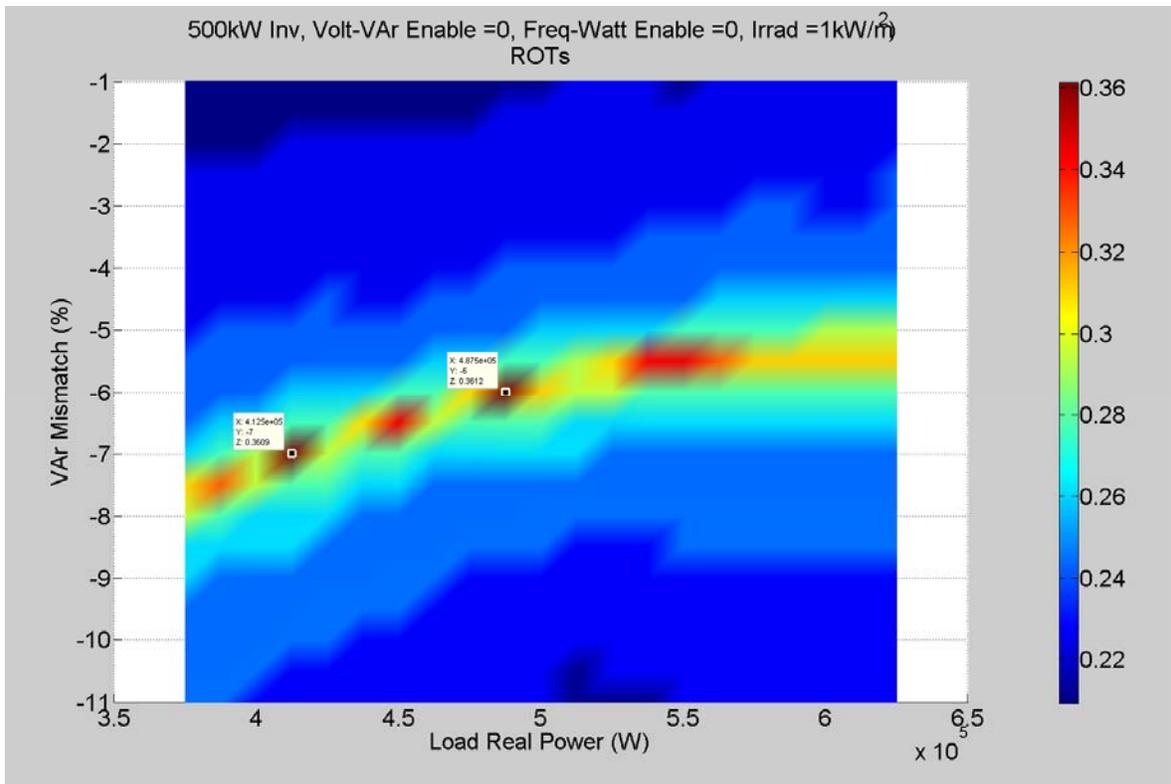


Figure 16. Run-on times for a single 500 kW inverter using SFS with no volt-var or frequency-watt controls (baseline case), under full irradiance.

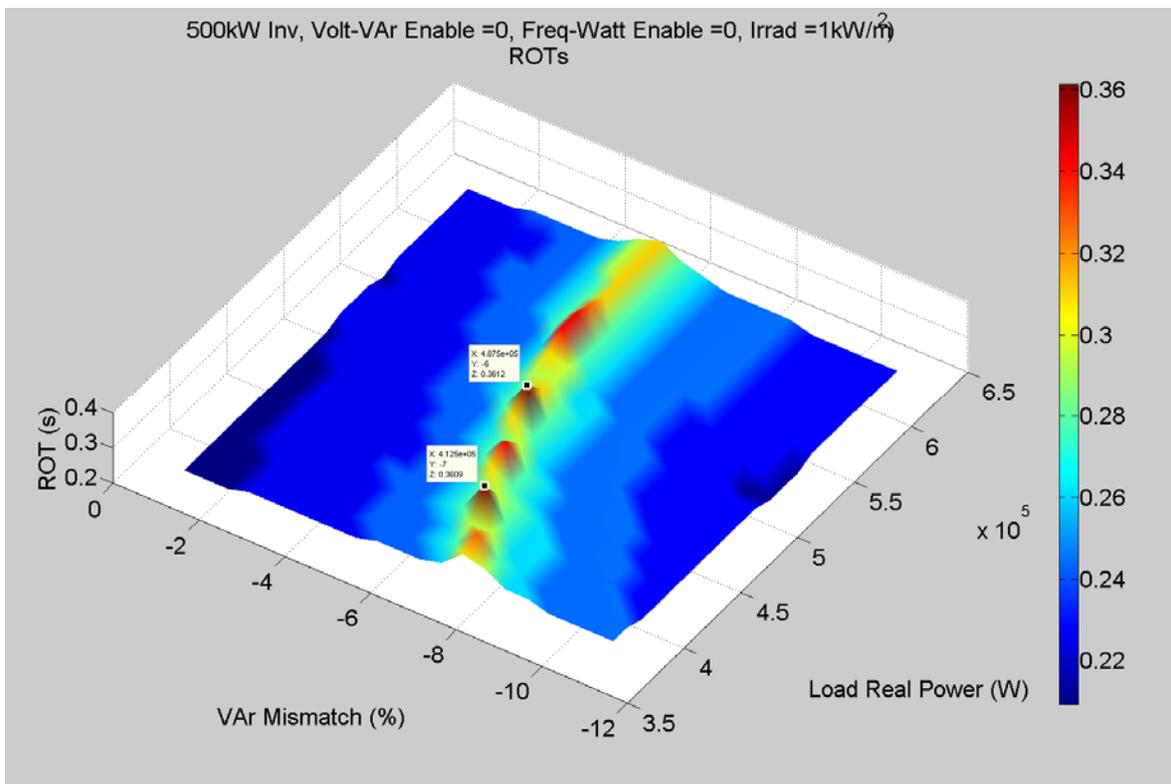


Figure 17. Perspective view of Figure 16.

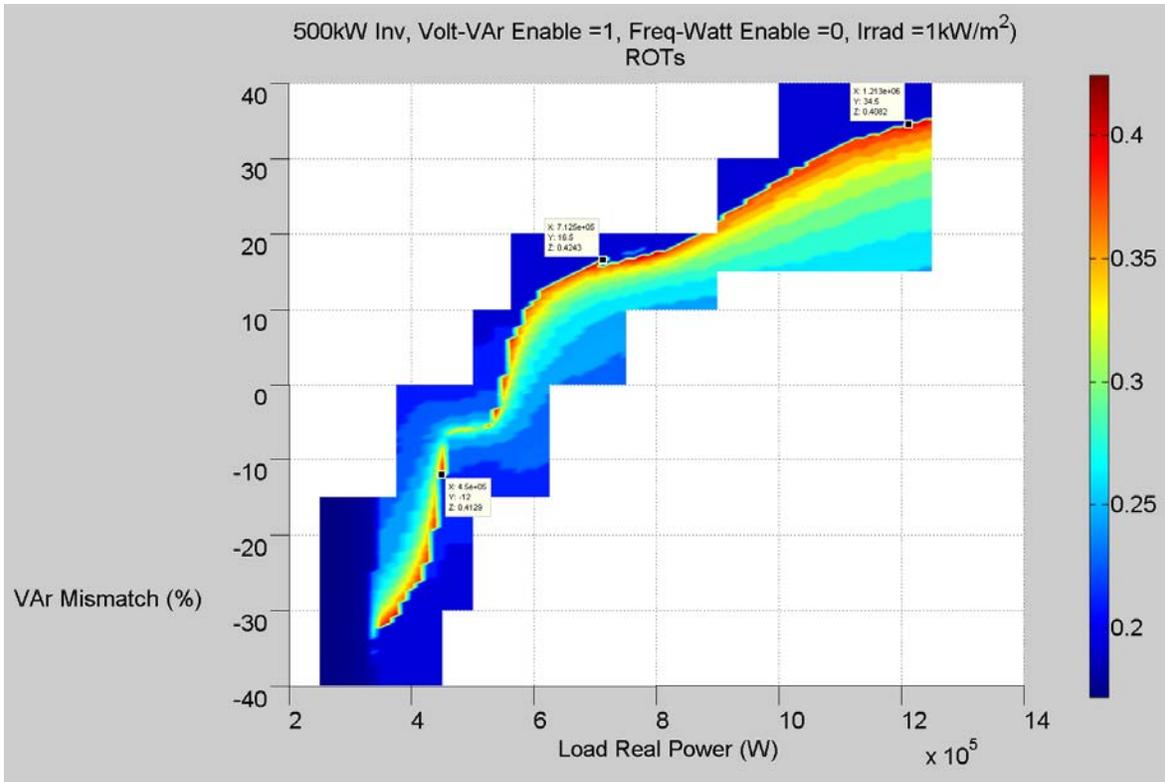


Figure 18. Run-on times for a single 500 kW inverter using SFS with volt-var enabled but frequency-watt disabled, under full irradiance.

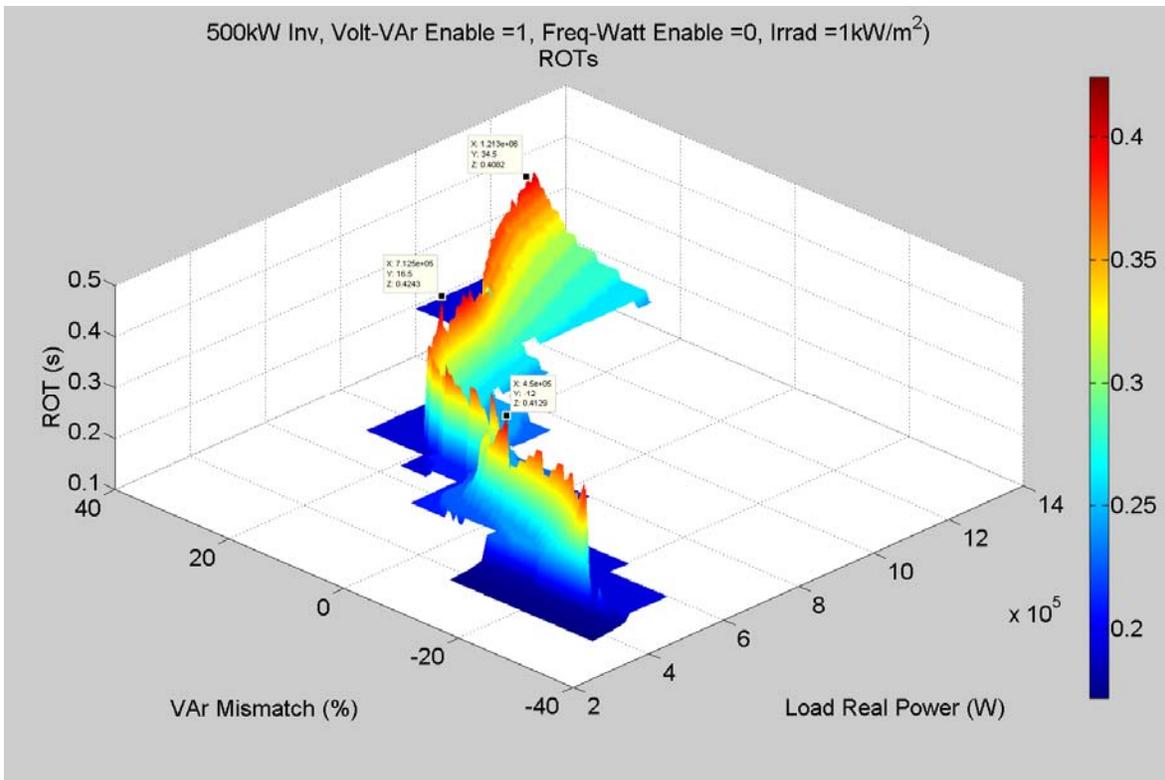


Figure 19. Perspective view of Figure 18.

Figure 20 shows the run-on times as a function of real and reactive loading, for full irradiance, using IEEE 1547 voltage and frequency trips, and with both volt-var and frequency-watt controls active. Figure 21 and Figure 22 show two different perspective views of Figure 20. These plots show an interesting “V”-shaped ridge of elevated run-on times. This shape of ridge is usually an indication that different factors dominate in different regions. The width of the ridge in the VAR direction has increased again, and the maximum run-on times have now risen to slightly less than twice what they were without any GSFs. The conclusion is that adding the frequency support controls has further degraded the inverter’s ability to detect an unintentional island, but it also remains true that no run-on approaches 2 sec, so no IEEE 1547 violation has occurred (recalling that the voltage and frequency trips are as shown in Table 2).

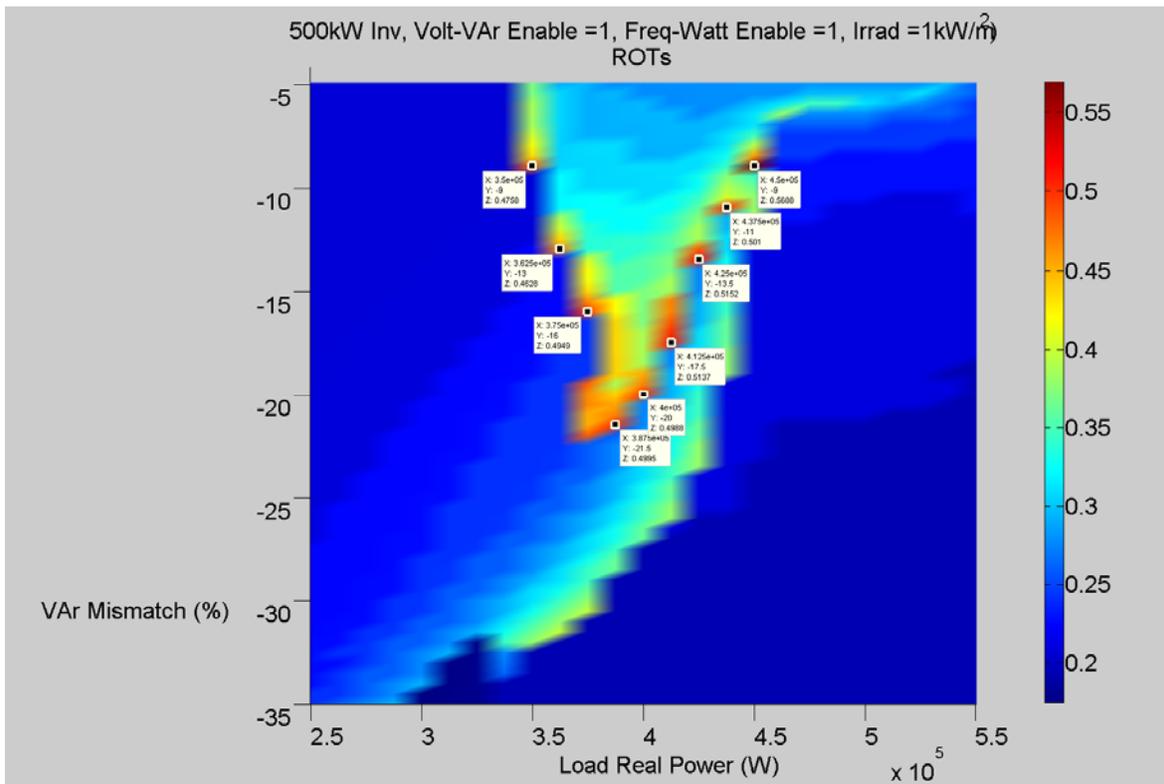


Figure 20. Run-on times of a single 500 kW inverter using SFS, with both volt-var and frequency-watt controls enabled, under full irradiance.

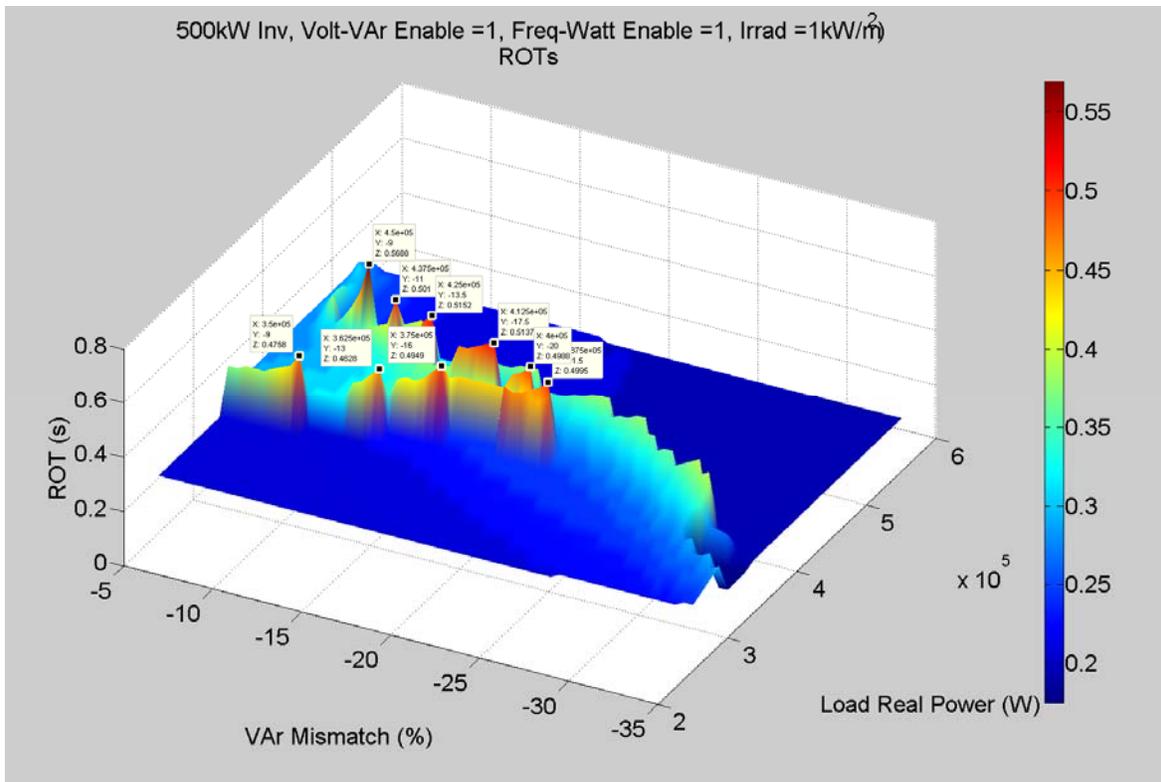


Figure 21. Perspective view of Figure 20.

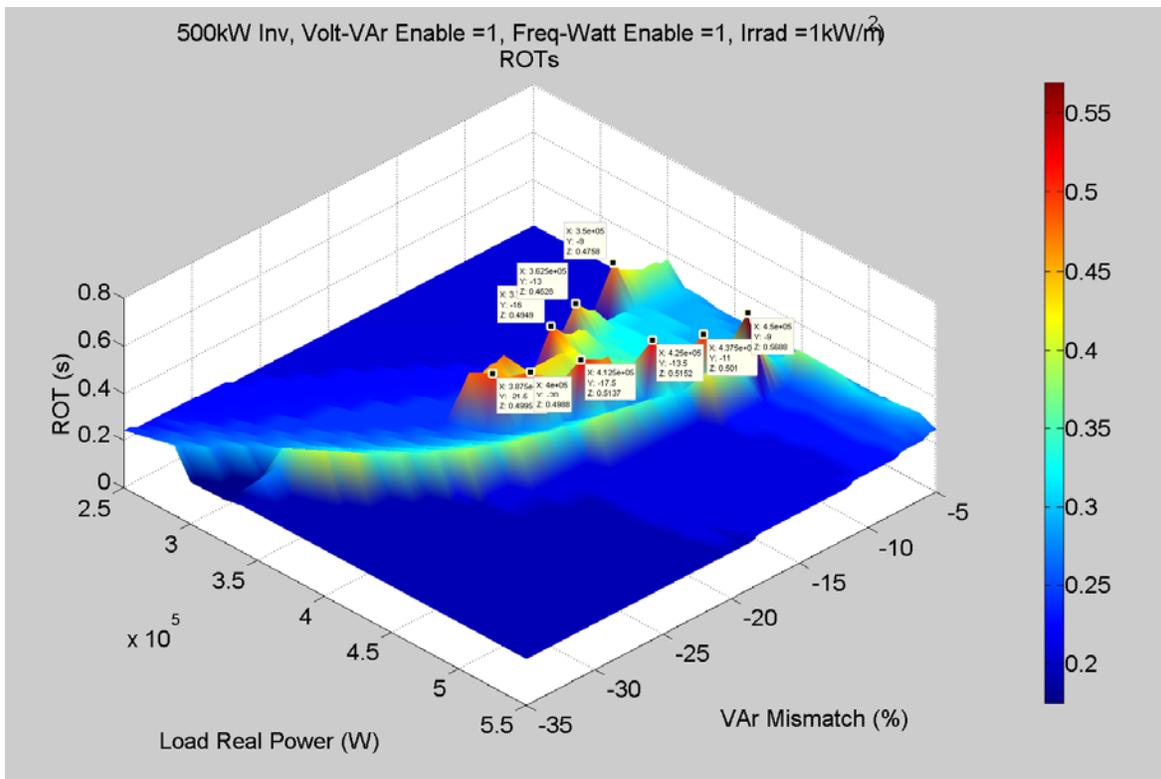


Figure 22. Another perspective view of Figure 20.

3.2.2. Results under 66% irradiance with IEEE 1547 trip setpoints

The next set of figures shows surface plots of ROTs vs. loading conditions for the 500 kW inverter with the trip setpoints shown in Table 2, but with the irradiance reduced to 66%. The primary impact of reducing the irradiance is that the parameter Q_{max} in (1) will be much larger; so the inverter will have more capability to “push” voltage via VArS.

Figure 23 shows the baseline case with no GSFs active. In general, the maximum run-on times are around 260 msec which is similar to the 100% irradiance case, except for one point at the far right of Figure 23 that is an outlier and not indicative of the general trend. Figure 24 shows a 3-D perspective view of Figure 23.

In Figure 25, the volt-var controls have been added, again with IEEE 1547 trips and at 66% irradiance, and the change is noteworthy. The typical maximum run-on times have increased by about 25%, similar to what was seen in the 100% irradiance case, but the extent of the region of elevated ROTs has become extremely large, covering a huge range of VAr mismatch values. Figure 26 shows a perspective view of Figure 25. Note that there is a set of relatively high peaks in the lower-left portion of Figure 25.

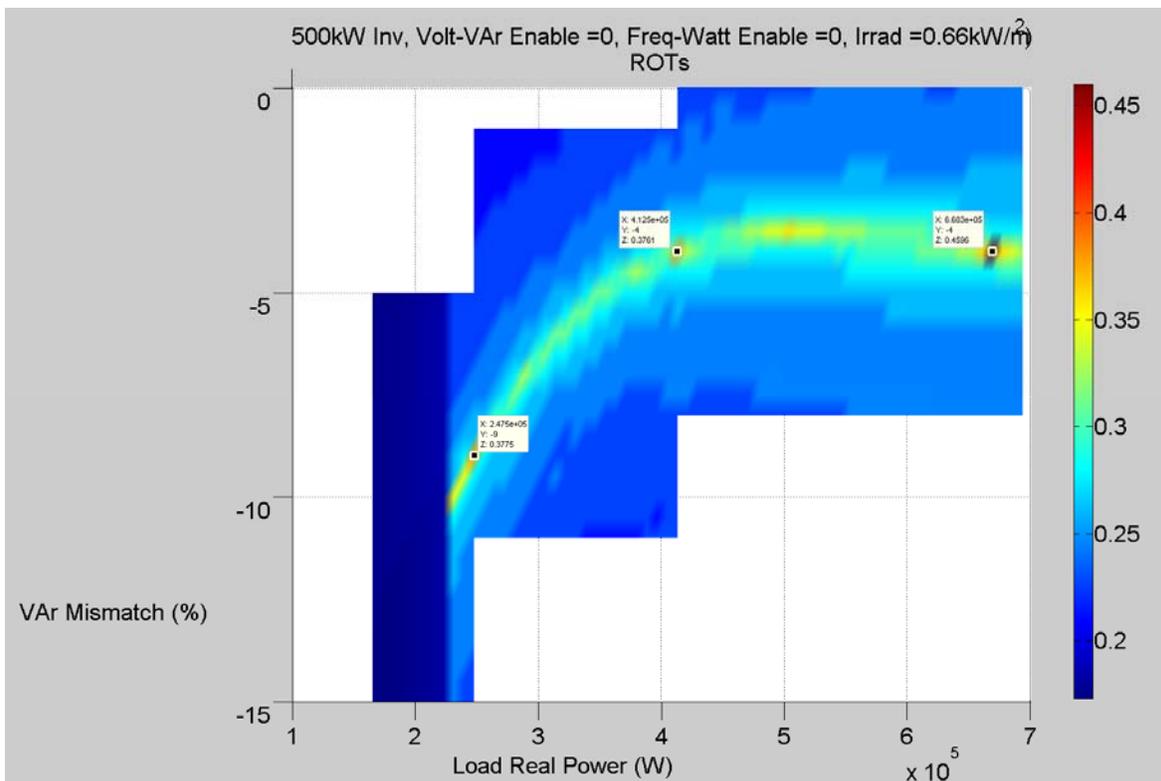


Figure 23. Run-on times of a single 500 kW inverter using SFS, without volt-var or frequency-watt controls (baseline case), under 66% irradiance.

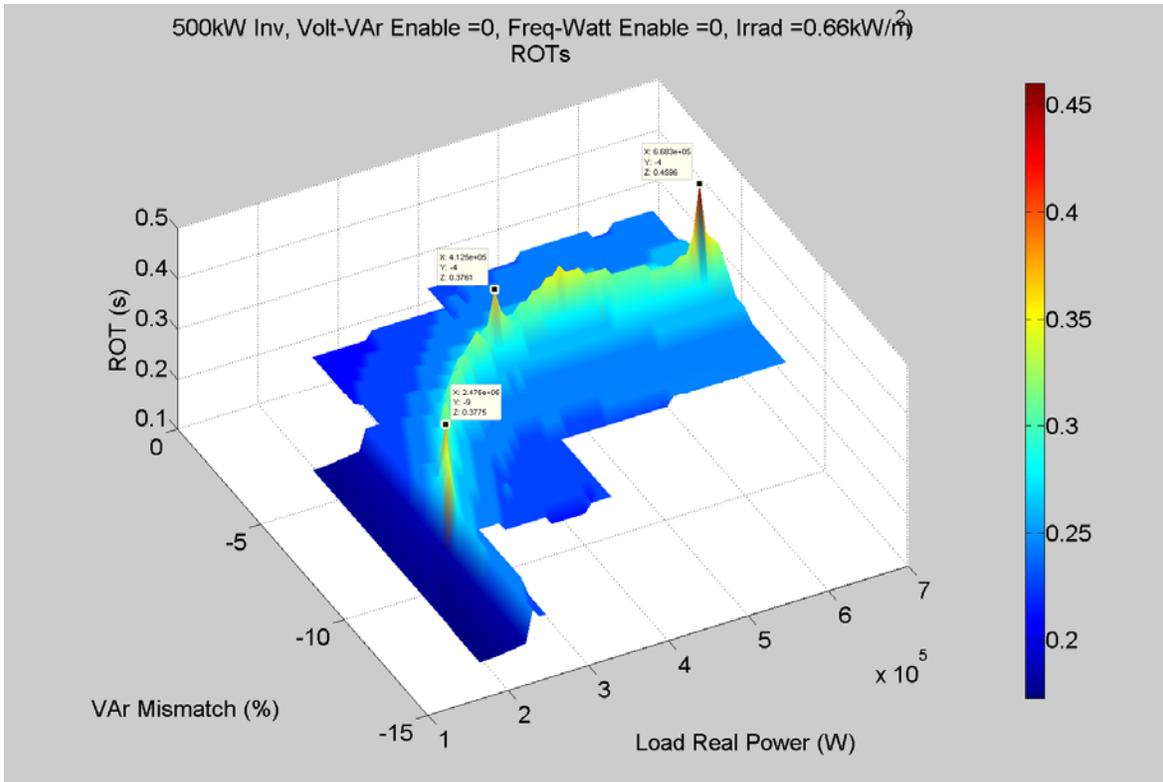


Figure 24. Perspective view of Figure 23

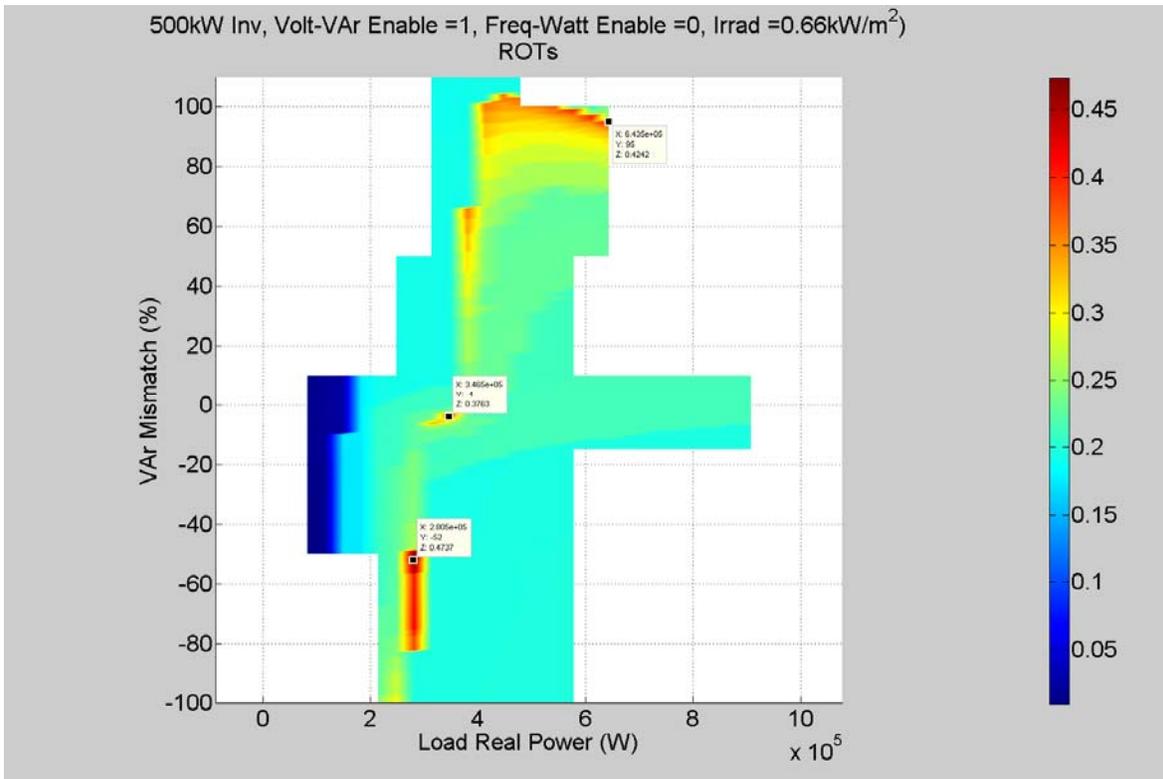


Figure 25. Run-on times of a single 500 kW inverter using SFS, with volt-var but without frequency-watt controls, under 66% irradiance.

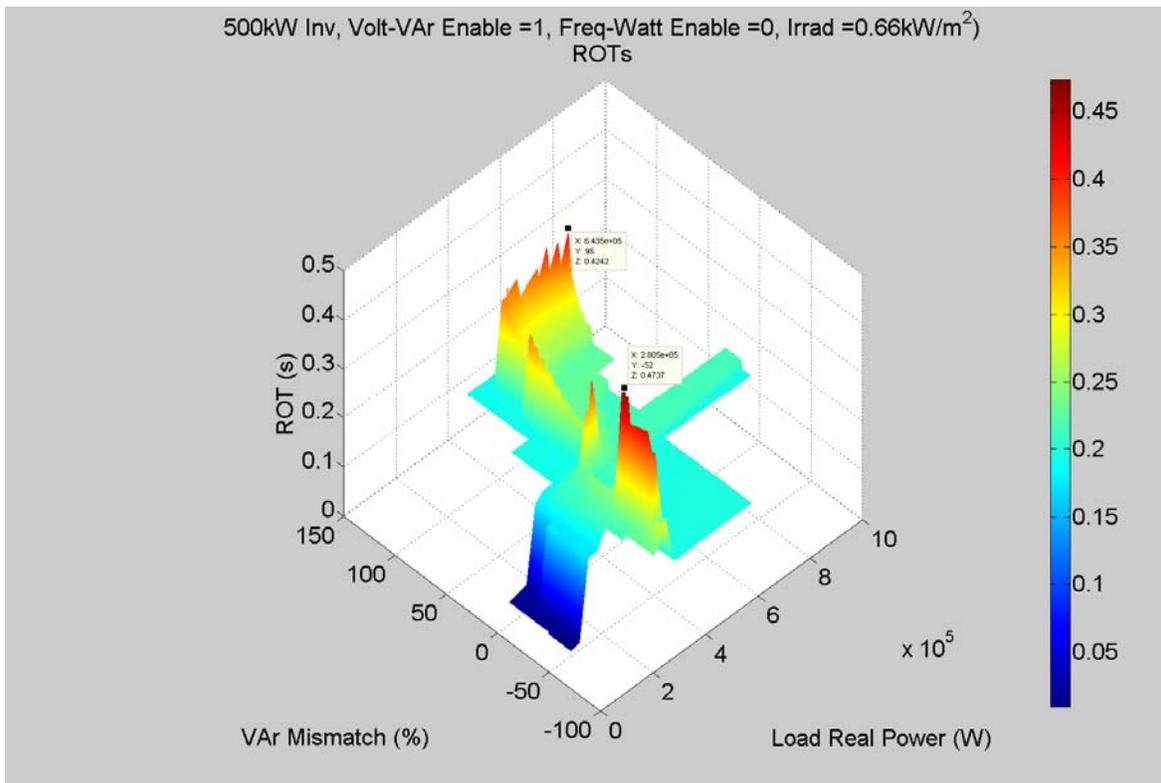


Figure 26. Perspective view of Figure 25.

The effects of volt-var controls were investigated further by running a batch of simulations at higher resolution, and the results are shown in Figure 27, with a perspective view in Figure 28. The higher-resolution plot shows a single point at which the run-on times are over 0.7 sec.

To understand what is causing this extended run-on, the inverter's internal anti-islanding command (phase shift in radians) and its reactive power output command (in pu) are plotted in Figure 29, and the frequency is plotted in Figure 30. These plots are telling as they clearly show that each time the active anti-islanding attempts to shift the inverter's phase in response to the detected frequency deviation, the volt-var controller issues a conflicting command. The result is that the inverter reactive power output command and phase shift command appear to oscillate greatly for nearly a second before finally de-energizing following an under frequency trip. As shown in Figure 30, the reason for the extended run-on is clear; the conflict between the anti-islanding and the volt-var controls causes the system to take longer to reach the frequency trip setpoint.

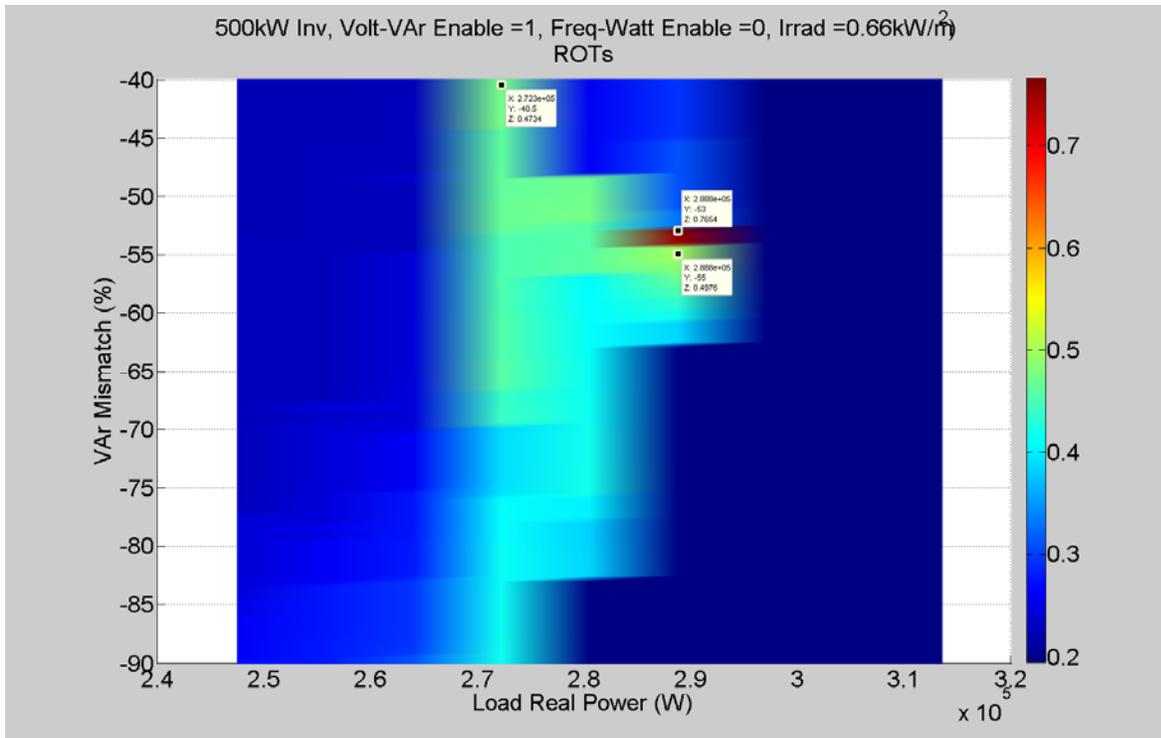


Figure 27. Zoomed in and higher-resolution view of the area of elevated run-on times in the lower left portion of Figure 25.

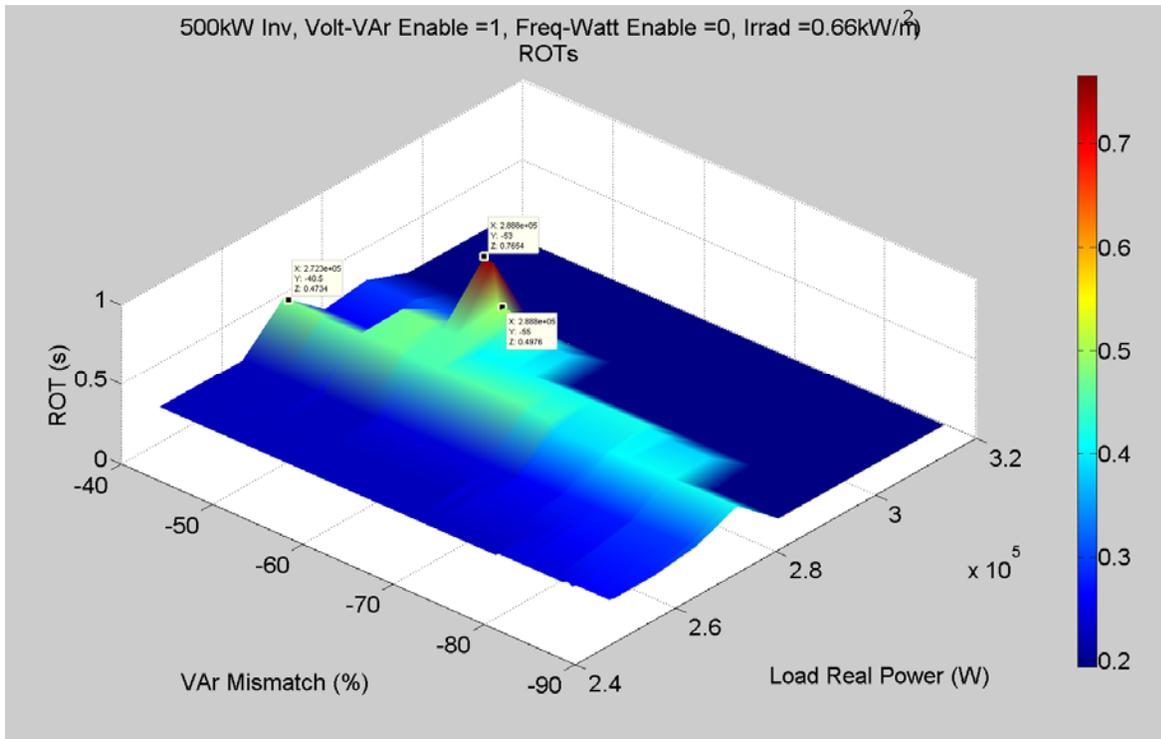


Figure 28. Perspective view of Figure 27.

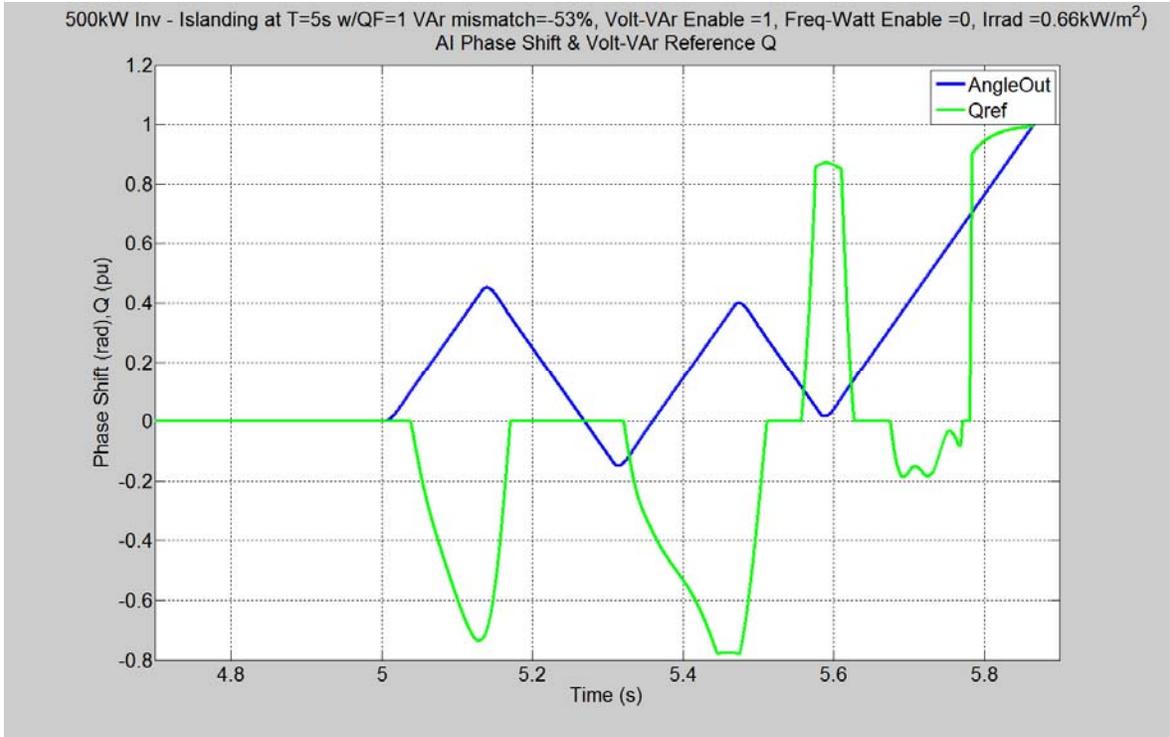


Figure 29. Anti-islanding command (“AngleOut”) and commanded reactive power (“Qref”) during the longest-lasting island event in Figure 27.

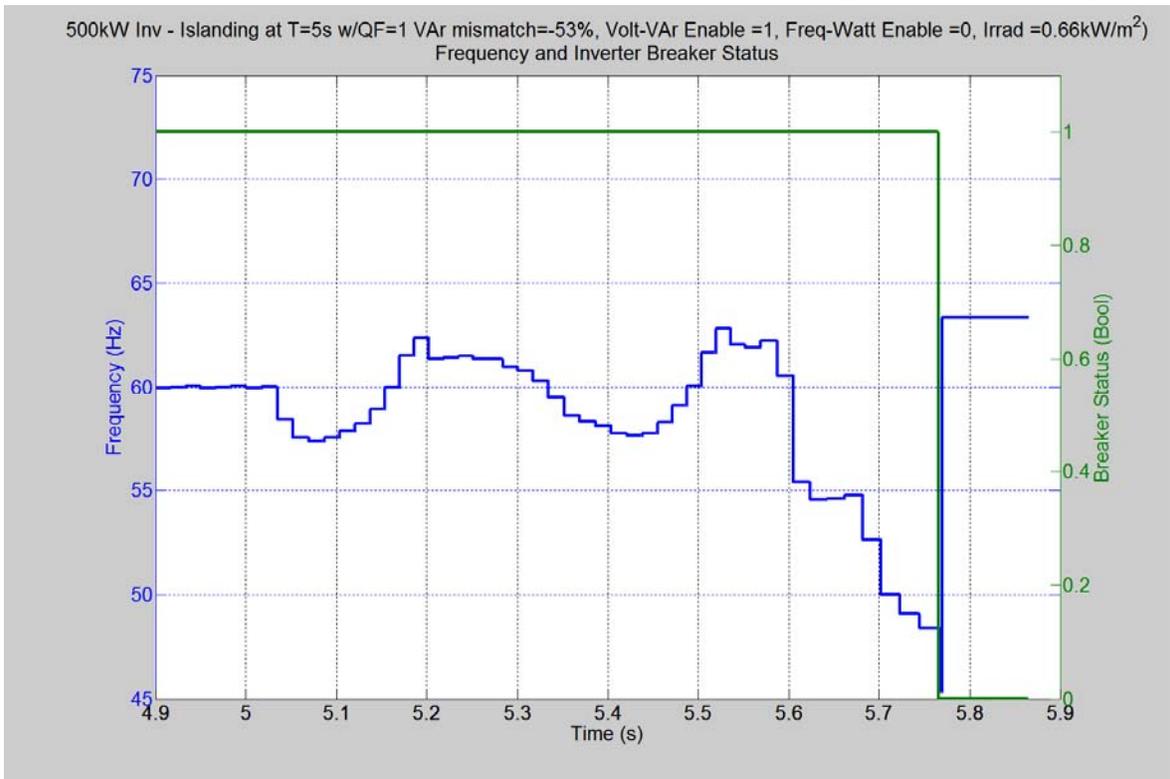


Figure 30. Frequency measured by the inverter during the longest-lasting run-on in Figure 27.

In Figure 31, both volt-var and frequency-watt controls are active, and the result is that typical run-on times rise to over 0.5 sec (again nearly double the baseline case) over a loading range that is similar in extent to that seen in Figure 25. Figure 32 shows a 3-D perspective view of Figure 31, and Figure 33 shows a narrower-range, higher-resolution version of Figure 31. These results clearly illustrate that the inverter's ability to detect an island is impeded by the GSFs over a wide range of load conditions, but again note that in no case does the ROT approach 2 sec.

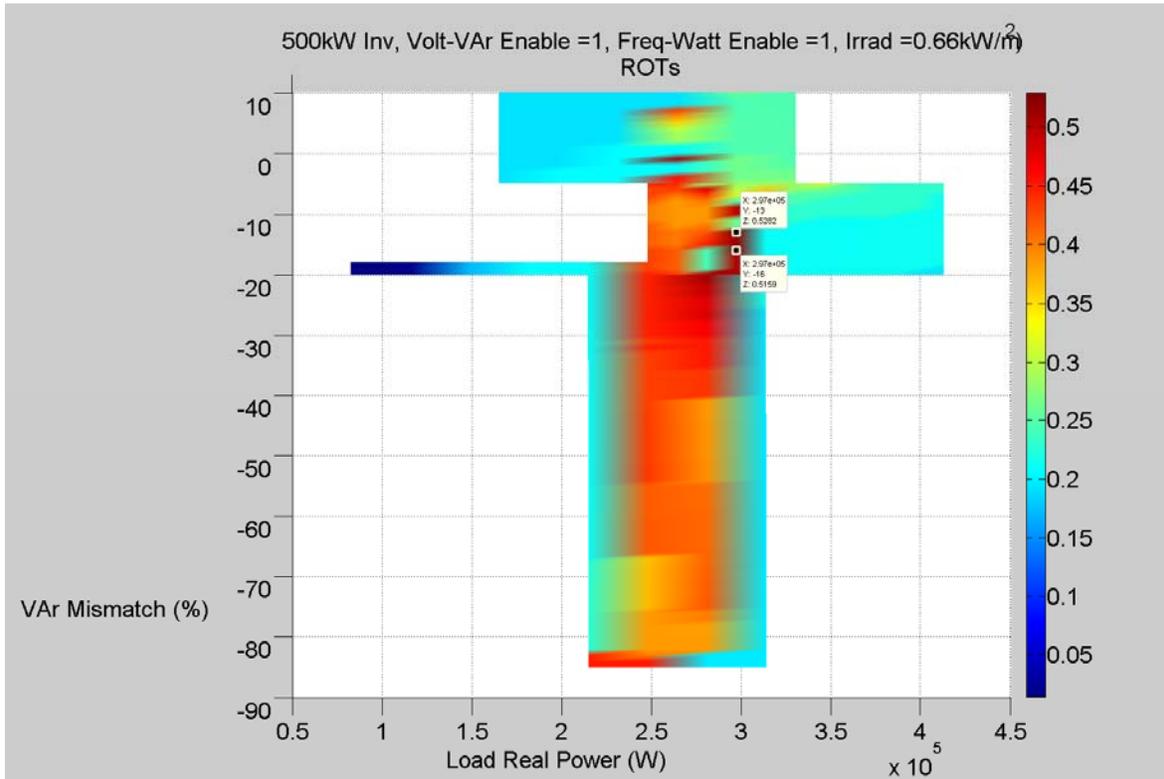


Figure 31. Run-on times of a single 500 kW inverter using SFS, with both volt-var and frequency-watt controls enabled, under 66% irradiance.

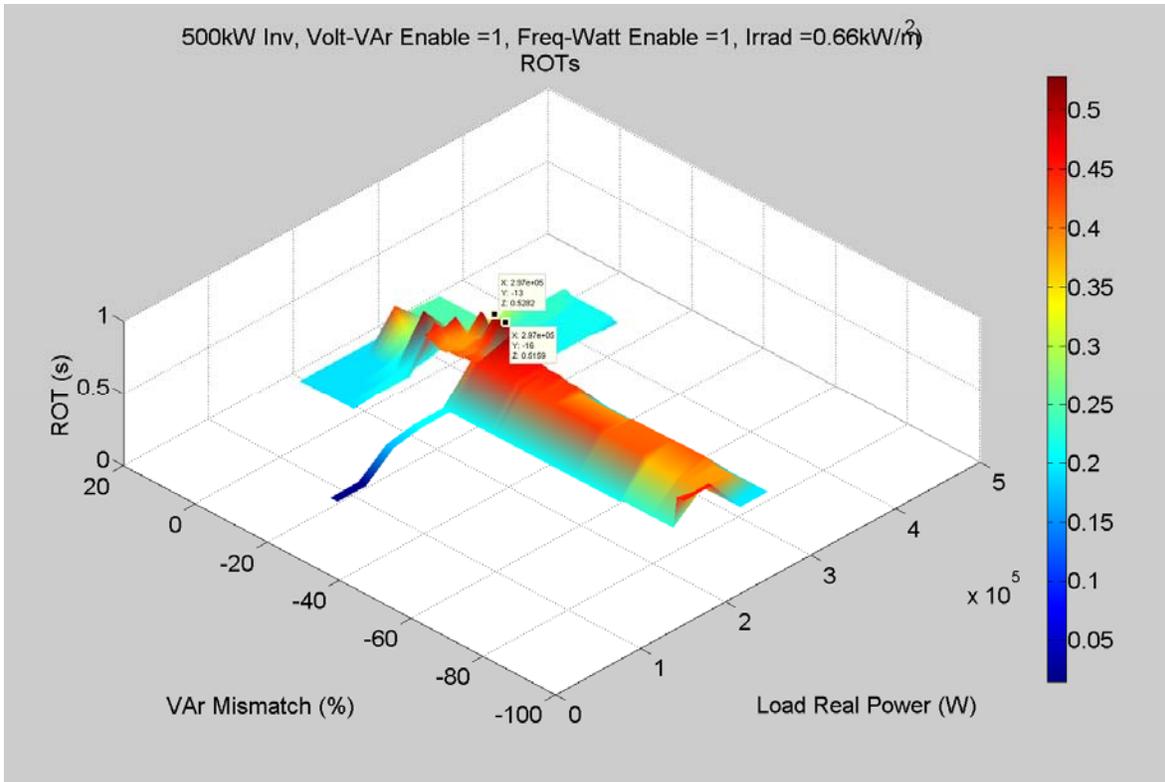


Figure 32. Perspective view of Figure 31.

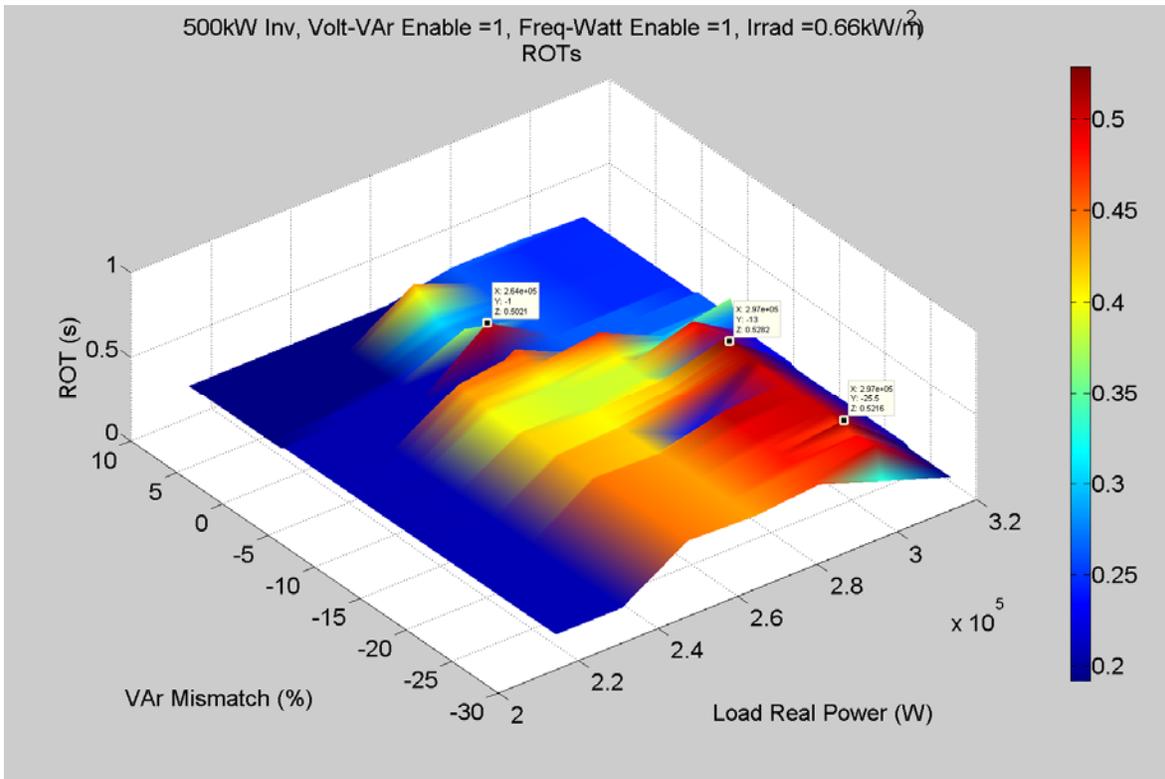


Figure 33. Higher-resolution, narrower-range view of the surface in Figure 32.

3.2.3. Results with 1547a setpoints

The next set of figures shows surface plots of ROTs vs. loading conditions for the 500 kW inverter with the trip setpoints shown in Table 5. Figure 34 shows the run-on time as a function of loading condition for the SFS-equipped 500 kW inverter, with volt-var controls active but frequency-watt controls disabled, under 100% irradiance, and with the voltage and frequency trip setpoints widened to match the IEEE 1547a recommendations. Comparing Figure 34 with Figure 18 (same conditions but with narrower IEEE 1547 trips), it is clear that the widening of the trip setpoints has had the expected effect: the ridge of elevated ROTs becomes wider, and the peak run-on times increase by roughly 75%. Thus, the widening of the trip setpoints did degrade the inverter’s ability to detect an island; although, it is noted that none of the run-on times is near the 2 sec threshold. Figure 35 shows a 3-D perspective view of Figure 34.

Table 5. 1547a Settings Used for Grid Support Function Batching

Parameter and value	Time to trip
$V_{rms} \leq 0.45$	160 msec
$0.45 \text{ pu} < V_{rms} \leq 0.6 \text{ pu}$	1 sec
$0.6 < V_{rms} \leq 0.88$	2 sec
$1.1 \text{ pu} \leq V_{rms} < 1.2 \text{ pu}$	1 sec
$1.2 \text{ pu} \leq V_{rms} < 1.6 \text{ pu}$	160 msec
$V_{inst} \geq 1.6 \text{ pu}$	500 μ sec
$f \leq 57 \text{ Hz}$	160 msec
$57 \text{ Hz} < f \leq 59.5 \text{ Hz}$	20 sec
$60.5 \leq f < 62 \text{ Hz}$	20 sec
$F \geq 62 \text{ Hz}$	160 msec

Figure 36 shows the run-on times as a function of loading condition for the 500 kW inverter with volt-var and frequency-watt controls enabled and a 1 kW/m² irradiance, but with the voltage and frequency trip setpoints made wider in accordance with the recommendations in the most recent draft of IEEE 1547a. One might expect that widening of the trip setpoints would cause run-on times to increase somewhat. Comparing Figure 36 with Figure 20, one sees that this is the case; the run-on times have increased. The new maximum run-on times are just under 0.8 sec, which represents a roughly 33% increase in ROTs. However, it is noted that the locations of these higher run-on times are *not* as expected. Instead of the “V”-shaped ridge in Figure 20 becoming slightly higher, which is what might be intuitively expected, Figure 36 shows a new line of higher run-on time peaks has appeared to the right of the “V”. A 3-D perspective view is shown in Figure 37.

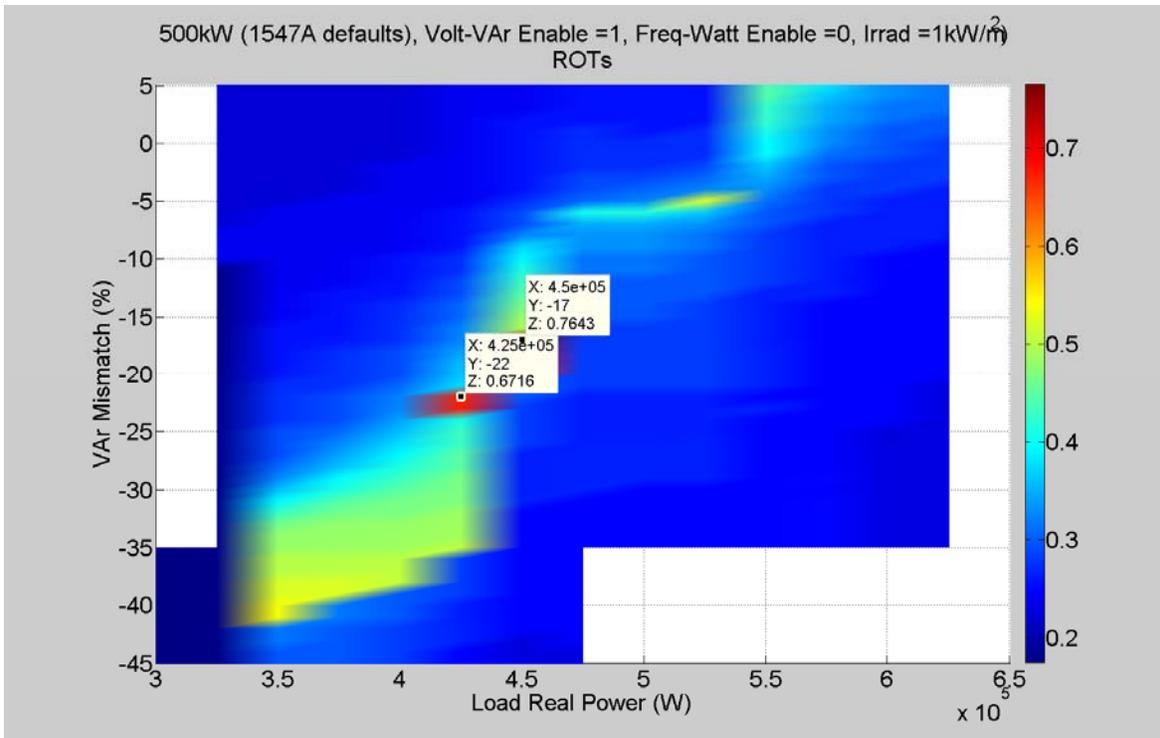


Figure 34. Run-on times vs. load power and VAr mismatch for a 500 kW inverter with volt-var controls but without frequency-watt controls, 100% irradiance, and wider IEEE 1547a trip setpoints.

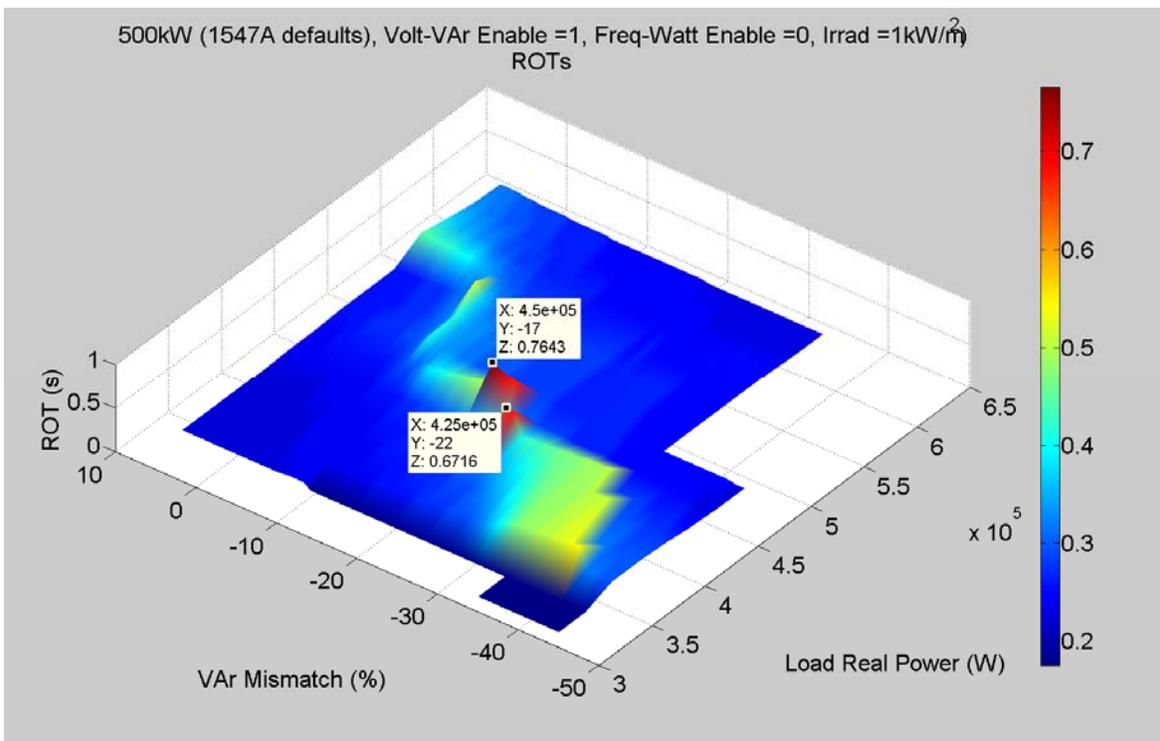


Figure 35. Perspective view of Figure 34.

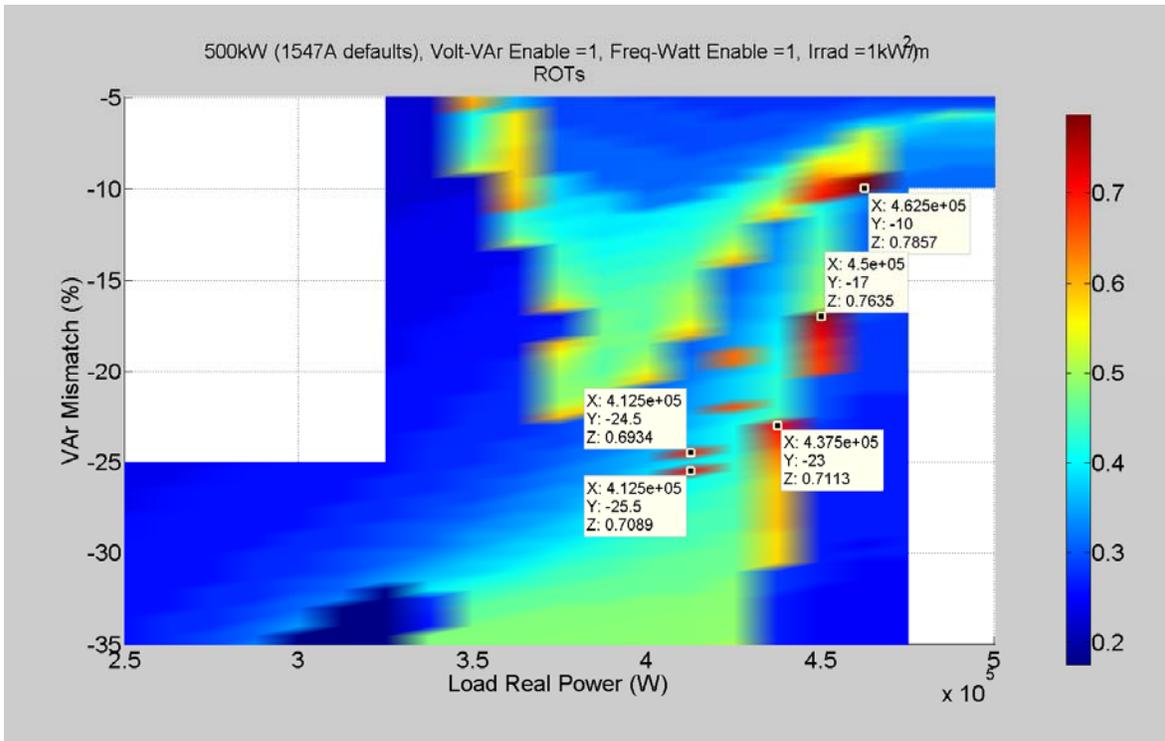


Figure 36. Run-on times vs. load power and VAr mismatch for a 500 kW inverter with volt-var and frequency-watt controls enabled, 100% irradiance, and wider IEEE 1547a trip setpoints.

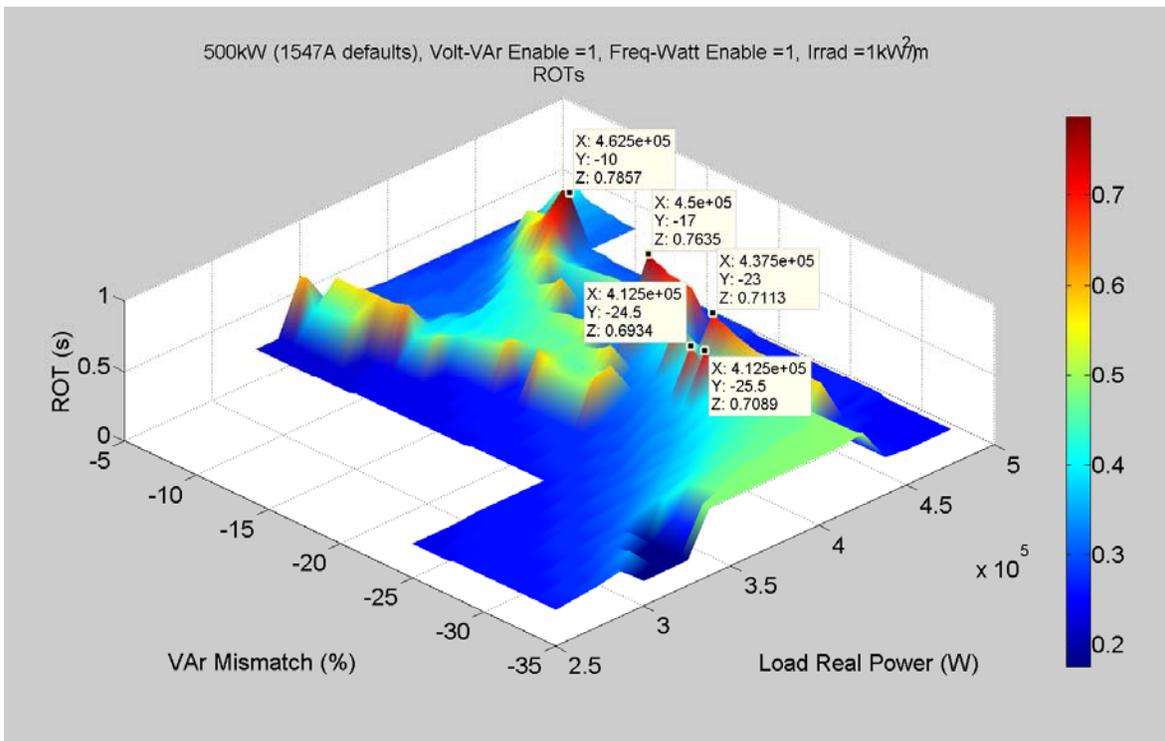


Figure 37. Perspective view of Figure 36.

Further understanding for the reason for the extended run-on in Figure 36 can be gained from Figure 38, which is a plot of the inverter’s commanded SFS anti-islanding phase shift (“AngleOut”) and the commanded output reactive power (“Qref”). The conflict between the two is apparent; as soon as the anti-islanding commands a phase shift in one direction, the volt-var function is triggered and produces a conflicting command.

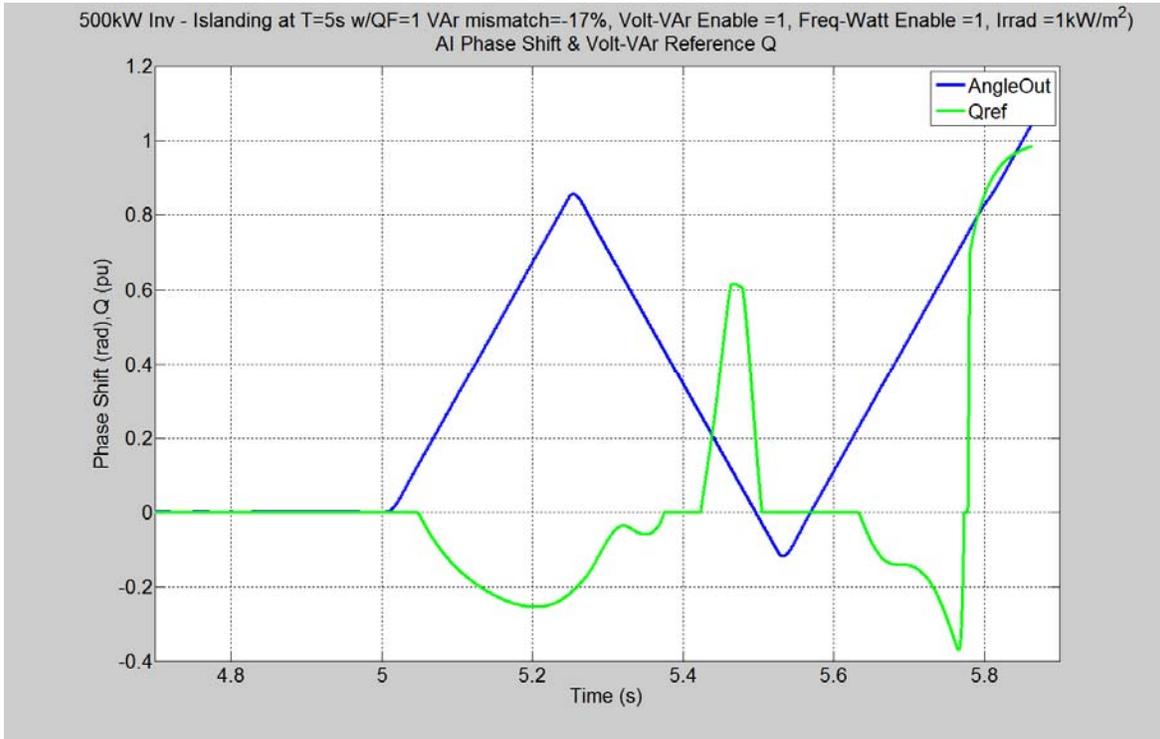


Figure 38. Inverter anti-islanding phase shift command (“AngleOut”) and commanded reactive power (“Qref”) during the longest-lasting island in Figure 36.

Figure 39 shows run-on times vs. loading conditions for the 500 kW SFS-equipped inverter, with volt-var but without frequency-watt controls, with IEEE 1547a trips, and under 66% irradiance. This figure is compared with Figure 27. Here, the wider trip setpoints have made little difference, and the reason can be seen in Figure 30: when the frequency does finally drop, it drops quickly through 59.3 Hz and below 57 Hz, so that both trip points are surpassed at basically the same time.

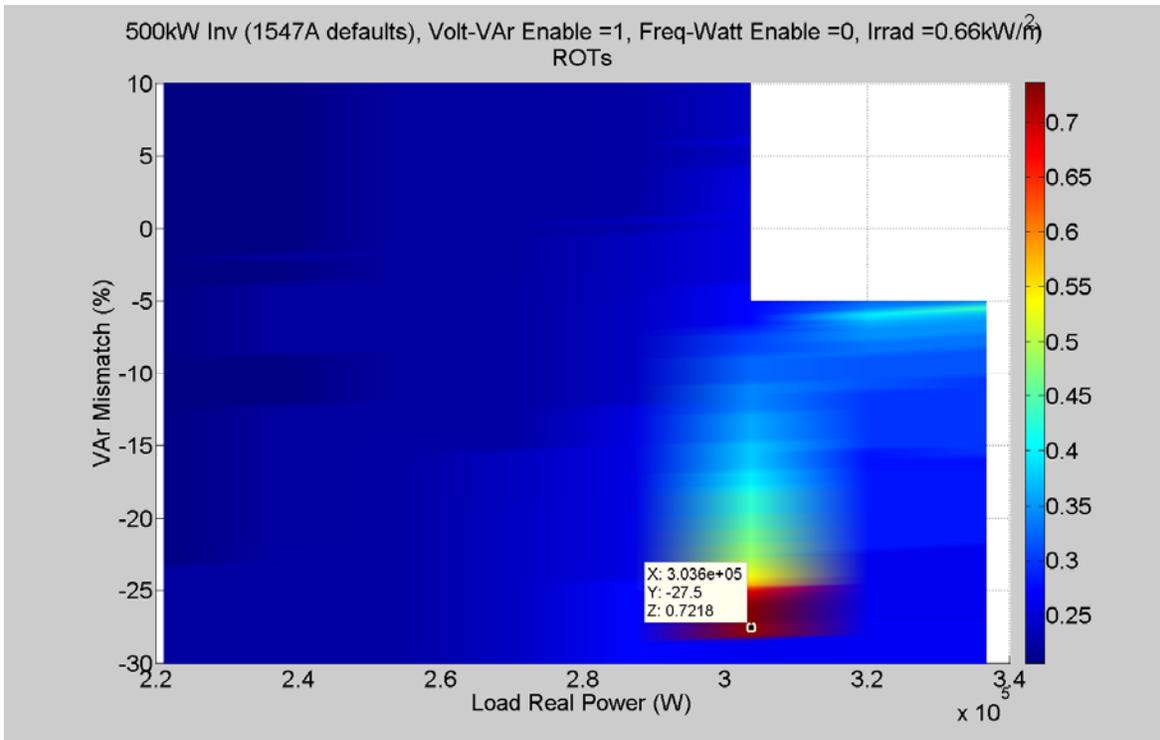


Figure 39. Run-on times vs. loading conditions for the 500 kW SFS equipped inverter with volt-var but without frequency-watt controls, with wider 1547a trip setpoints, and under 66% irradiance.

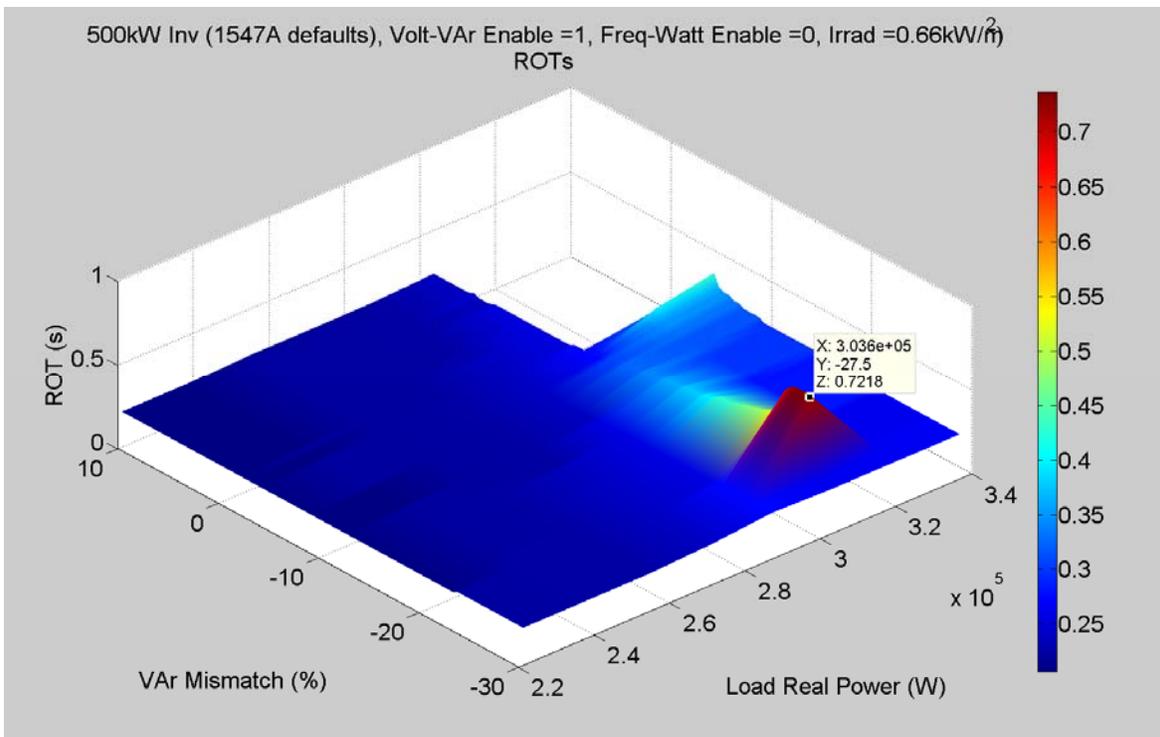


Figure 40. Perspective view of Figure 39.

3.3. Summary

It is clear from the results presented here that there is an adverse reaction between GSFs and SFS-based islanding detection, and that this interaction becomes worse when the wider voltage and frequency trip setpoints in IEEE 1547a are applied. The GSFs themselves do not necessarily cause a compliant system to become noncompliant, but the complexity of the behavior seen is concerning because it makes it very difficult to predict what will happen in multi-inverter cases, or what might happen if inverters and rotating machines are islanded together. These results are a strong incentive to move toward anti-islanding means that do not rely on creating abnormal voltages or frequencies. Because communications-based methods would decouple islanding prevention from GSFs, they would appear to be good candidates.

4. DYNAMIC CONSIDERATIONS FOR INVERTERS WITH GRID SUPPORT FUNCTIONS

Several methods exist to prevent an islanding condition, including passive and active methods [2]-[6]. Each method operates by sensing and differentiating inverter dynamics when grid-connected versus when in an islanded condition. However, since new advanced inverter functions are intended to emulate generator control [4], a grid disconnection may be more difficult to detect with these in operation. Two examples involving passive detection methods and one example involving an active method, Sandia frequency shift, are discussed analytically.

4.1. Modeling Inverter Dynamics with Grid Support Functions

Two generic inverter models were developed for this investigation. These models are separate from those provided by industry and were developed to provide greater flexibility for investigating the interdependencies of the control and system/circuit parameters.

The first model considers the inverter as an ideal source of real and reactive power that has been configured for anti-islanding test, with RLC load having phase inductance L , phase capacitance C and (for a three-phase inverter) phase resistance $R = 3V_{rated}^2 / P_{rated}$ for rated power and voltage; see Figure 41 [10]. This figure is intended to be illustrative and consistent for either single or three phase implementations; V is the RMS phase voltage of the load.

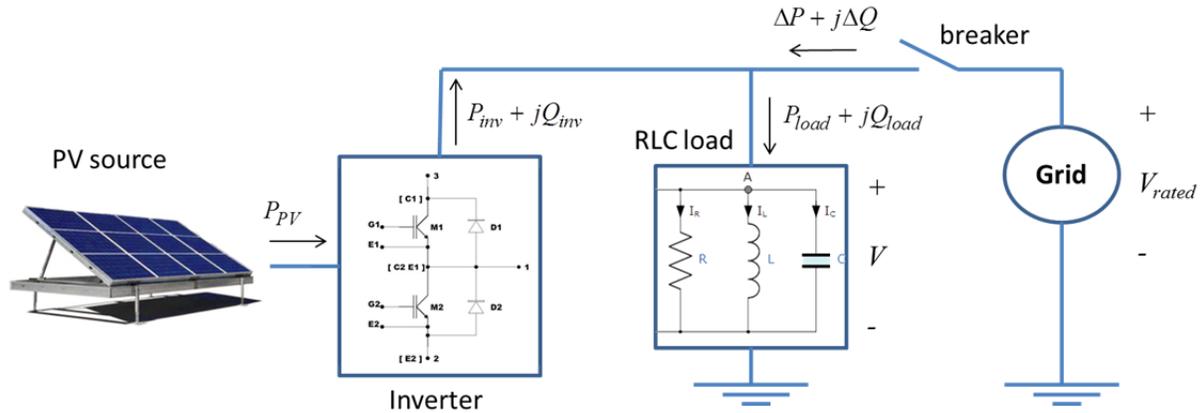


Figure 41. PV converter connected to grid and RLC load for islanding test

When the inverter is connected to the grid and the grid is at rated voltage, $V = V_{rated}$, $P_{load} = P_{rated} = P_{inv} + \Delta P$, $Q_{load} = Q_{inv} + \Delta Q$ and frequency is matched with the grid. When the grid is disconnected, $P_{load} = P_{inv}$, $Q_{load} = Q_{inv}$ and the load voltage and frequency seek an equilibrium given (for a three-phase inverter) by equations (12) and (13) [10].

$$V(P_{inv}) = V_{rated} \sqrt{\frac{P_{inv}}{P_{rated}}} \quad (12)$$

$$f(Q_{inv}, V) = \frac{-\frac{Q_{inv}}{3CV^2} + \sqrt{\left(\frac{Q_{inv}}{3CV^2}\right)^2 + \frac{4}{LC}}}{4\pi} \quad (13)$$

Combining the grid support functions shown in Figure 1 and Figure 2 with equations (12) and (13), it can be shown that a closed-loop system is realized. Without grid support functions, the frequency and voltage will change following a grid disconnect based upon the real and reactive power mismatch as quantified by ΔP and ΔQ . When grid support functions are then incorporated that respond to voltage and frequency measured at the PCC by generating new commanded real and reactive power P_{inv}^* and Q_{inv}^* , the voltage and frequency response will be dependent upon ΔP and ΔQ in addition to the control coefficients that define the GSFs.

4.1.1. Simplified Generic Inverter Model with GSFs

To simulate this dynamic response, a simple model was developed that assumes commanded real and reactive power can each be realized by the inverter with some fixed control lag (time constant τ). A system diagram is shown in Figure 42.

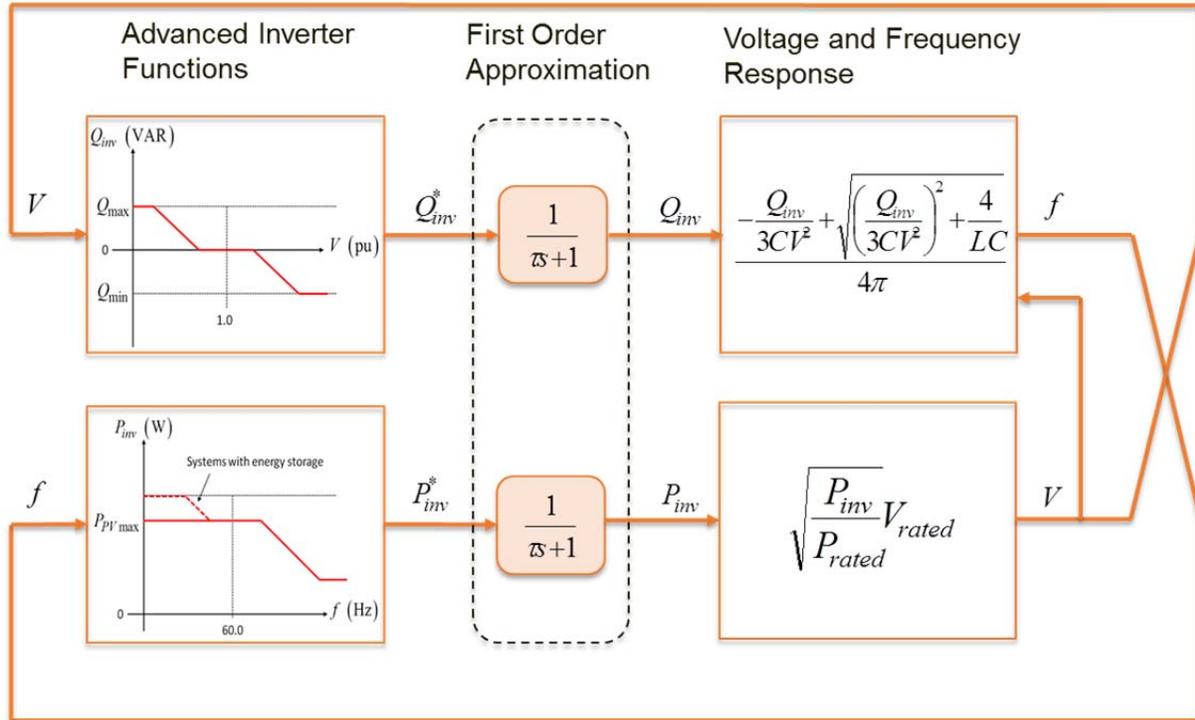


Figure 42. Dynamical Representation of Inverter Dynamics with Grid Support Functions

If the volt-var and frequency-Watt functions are represented as $Q_{inv}^* = g_{VV}(V)$ and $P_{inv}^* = g_{FW}(f)$ respectively, appropriate substitution of equations (12) and (13) allow the inverter to be expressed as a second order nonlinear system with the states $x = [Q_{inv} \quad P_{inv}]^T$ and the trajectories given by

$$\begin{aligned} \frac{dQ_{inv}}{dt} &= \frac{1}{\tau} (Q_{inv}^* - Q_{inv}) \\ &= \frac{1}{\tau} (g_{VV}(V) - Q_{inv}) \\ &= \frac{1}{\tau} \left(g_{VV} \left(V_{rated} \sqrt{\frac{P_{inv}}{P_{rated}}} \right) - Q_{inv} \right) \end{aligned} \quad (14)$$

$$\begin{aligned} \frac{dP_{inv}}{dt} &= \frac{1}{\tau} (P_{inv}^* - P_{inv}) \\ &= \frac{1}{\tau} (g_{FW}(f(Q_{inv}, V)) - P_{inv}) \\ &= \frac{1}{\tau} \left(g_{FW} \left(\frac{1}{4\pi} \left(-\frac{Q_{inv} P_{rated}}{3CV_{rated}^2 P_{inv}} + \sqrt{\left(\frac{Q_{inv} P_{rated}}{3CV_{rated}^2 P_{inv}} \right)^2 + \frac{4}{LC}} \right) \right) - P_{inv} \right) \end{aligned} \quad (15)$$

where the evolution of the state dx/dt depends on the system state x and system parameter constants. It is noted that $g_{VV}(V)$ and $g_{FW}(f)$ are both non-increasing functions in V and f respectively and given by

$$g_{VV}(V) = -K_v(V - V_0) \quad (16)$$

$$g_{FW}(f) = P_{PV \max} - K_f(f - f_0) \quad (17)$$

where V_0 and f_0 are the nominal voltage and frequency and $K_v, K_f \geq 0$ are the function slopes with units VAr/V and Watt/Hz respectively; it is noted that K_v is piecewise constant between the values of V_1, V_2, V_3 and V_4 as is K_f piecewise constant between values of f_1, f_2, f_3 and f_4 .

4.1.2. Detailed Generic Inverter Model with GSFs

In addition to the simplified generic model, a switch-averaged waveform model was developed in Matlab to represent a 3-phase commercial inverter and photovoltaic source. The system model includes a detailed PV panel model, dc link capacitor, 6-switch converter stage with conduction losses and switching losses modeled, output LC filter, isolation transformer and RLC load. The converter controls include a phase locked loop (PLL), qd-axis current control and maximum

power point tracking on the PV panel. Frequency was measured using zero crossings. A schematic of the generic inverter is shown in Figure 43.

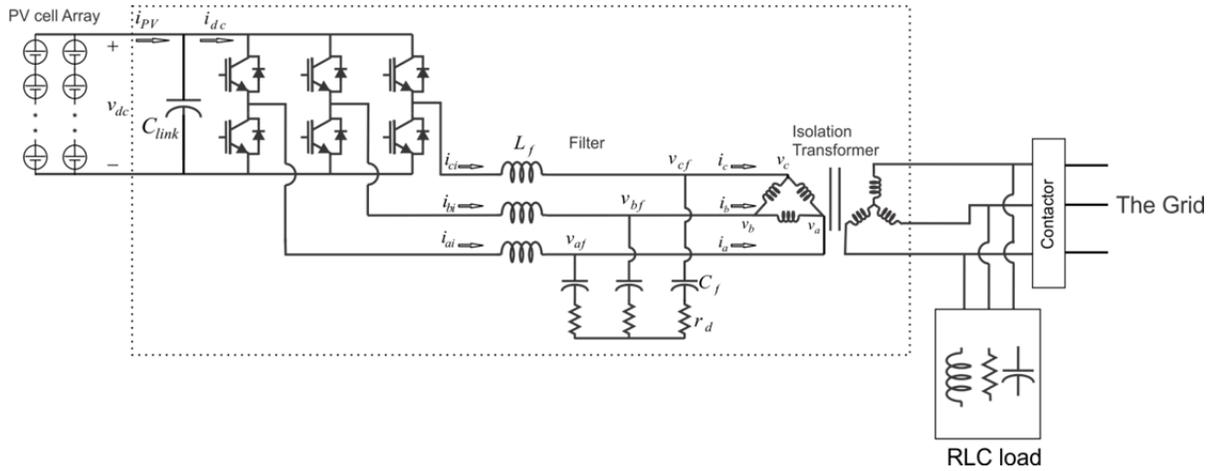


Figure 43. Schematic representation of 3-phase PV inverter with RLC load for Islanding test

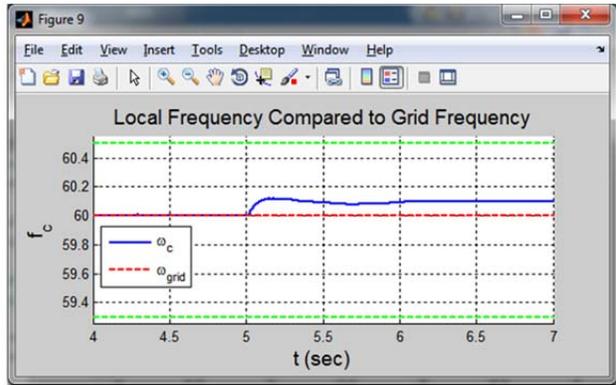
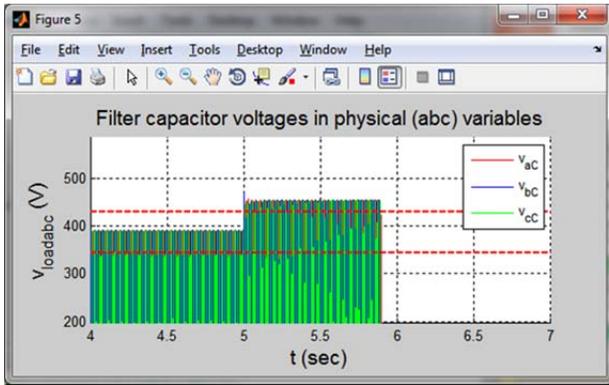
To enable future studies with multiple detailed generic models connected to a single bus, Sandia worked with PC Krause and Associates to package the Matlab detailed generic model into a custom Simulink library [13]. The details of this library are provided in the Appendix.

4.2. Passive and Active Anti-Islanding and Grid Support Functions

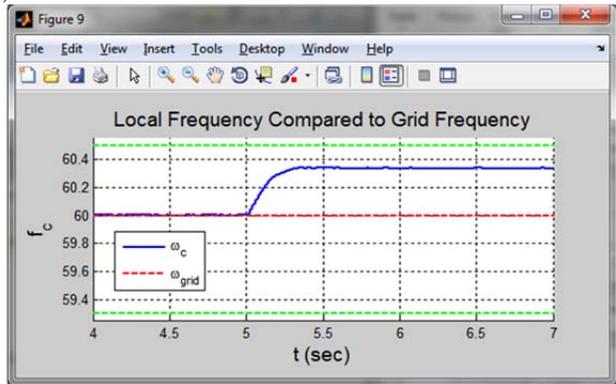
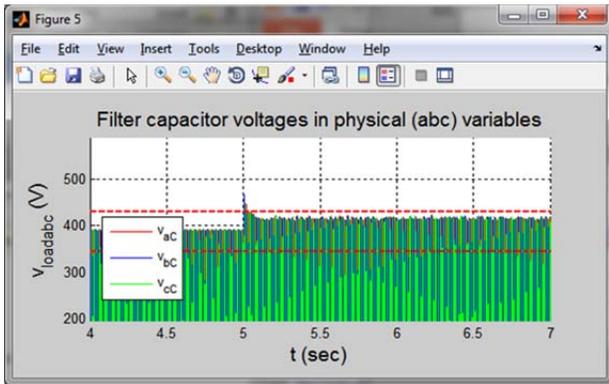
4.2.1. Over/Under Voltage (OUV) and Over/Under Frequency (OUF) with GSFs

Herein, we illustrate the effect of advanced inverter functions by looking first at the effect on the over-under voltage (OUV) and over-under frequency (OUF) detection, which is “...one of the oldest methods adopted for distribution system protection” [12].

The implementation of grid support functions is found to have the potential for limiting the efficacy of OUV and OUF methods for anti-islanding. Specifically, the GSF can stabilize the real and reactive power response such that the voltage and frequency stay within the OUV and OUF limits despite a VAR or Watt mismatch of the load that would normally warrant a shutdown. Two examples are presented to illustrate the effect. In the first example, the inverter produces 50 kW and 0 VAR though the load resistance is such that it consumes 37.5 kW and 100 VAR ($\Delta P = -12.5 \text{ kW}, \Delta Q = 100 \text{ VAR}$) at nominal voltage. No active anti-islanding is employed. At $t=5$ seconds, the grid is disconnected, the voltage swells above 110% and the frequency rises to 60.1 Hz. See Figure 44 and Figure 45; voltage and frequency limits are denoted using red dashed lines. Without GSFs, the inverter detects an overvoltage and ceases to deliver power at approximately $t=5.9$ sec. When voltage and frequency support is added in this scenario, with $K_f = 30 \text{ kW/Hz}$ and $K_v = 50 \text{ VAR/V}$, the voltage and frequency limits are now both maintained within limits, and the inverter runs on for greater than 2 seconds.

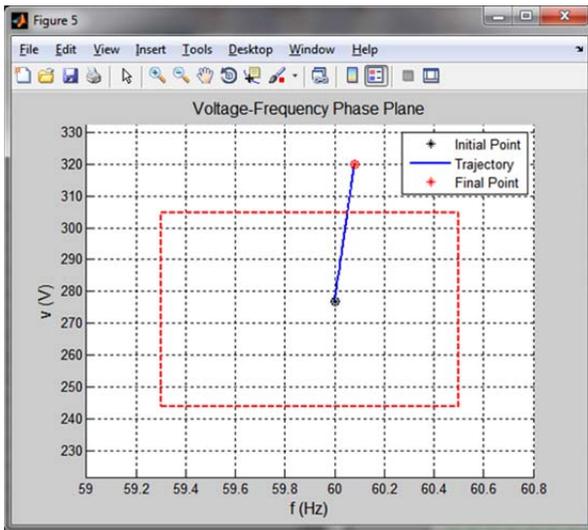


(a)

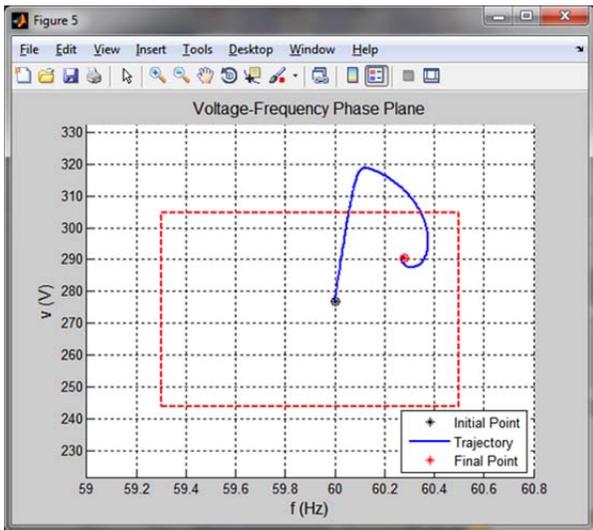


(b)

Figure 44. Detailed model simulation indicates (a) an over voltage trip without GSFs and (b) with GSFs interfering with overvoltage trip



(a)



(b)

Figure 45. Simplified model simulation shown in v - f phase plane for (a) an over voltage trip without GSF and (b) GSF interfering with overvoltage trip

4.2.2. Sandia Frequency Shift with GSFs

The Sandia Frequency shift (SFS) algorithm operates by continuously perturbing the frequency of the output current of the inverter and applying positive feedback to the output frequency error. To shift the output current frequency, a “chopping fraction” cf is applied to the current waveform or an angular shift is applied to the commanded qd -axis currents; see equation (18) [12]. The term cf_0 is an offset that alternates positive and negative from cycle to cycle, and K_{sfs} is the SFS gain.

$$cf = cf_0 + K_{sfs}(f - f_0) \quad (18)$$

When the grid is disconnected, the frequency deviation of the current causes the frequency of the voltage (measured at the PCC) to deviate; with positive feedback, this deviation continues until an over or under frequency condition is encountered and the inverter shuts down. An exemplary response is shown in Figure 46. Therein, the output current frequency is shifted up and then down from cycle to cycle, but the voltage frequency remains steady as the inverter output is connected to the grid. At $t=1$ second, the grid disconnects, the frequency of the measured output voltage shifts down, and the result of positive feedback brings the frequency further down to an under-frequency condition.

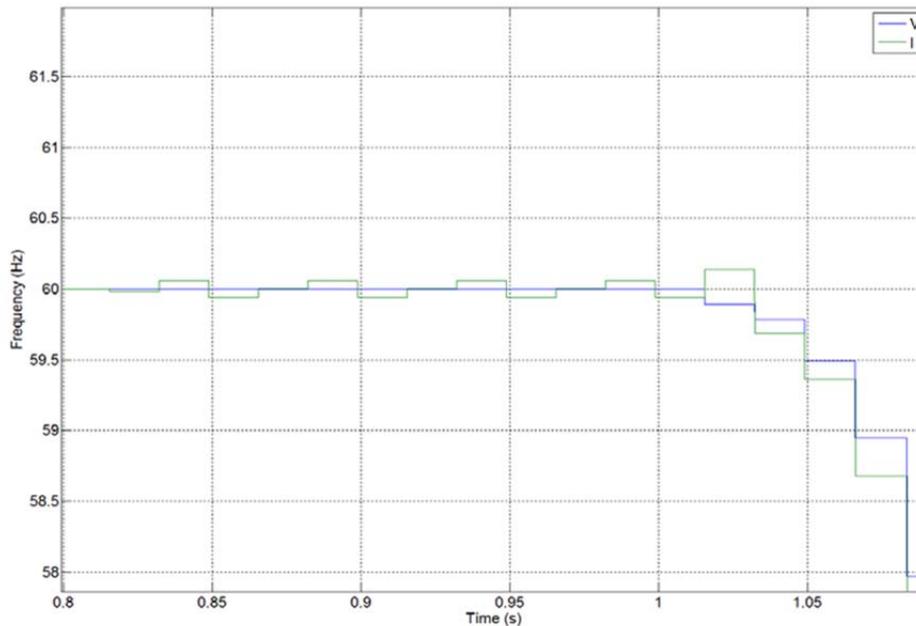


Figure 46. Illustration of Inverter Frequency Response using Sandia Frequency Shift; grid disconnects at $t=1$ sec

Unfortunately, when GSFs are connected, the negative feedback realized by (16) and (17) interferes with the positive feedback indicated by equation (18). This interference with the positive feedback can result in extended run-on times as indicated in the next example.

In this example, the inverter produces 50 kW and 100 VAR with load adjusted such that $\Delta P = 0$ W, $\Delta Q = 100$ VAR at nominal voltage. In addition, the inverter is implementing phase-

shift SFS anti-islanding with $cf_0 = 0.01$ and $K_{sfs} = 0.01$. At $t=5$ seconds, the grid is disconnected. See Figure 47; again, voltage and frequency limits are denoted using red dashed lines. In the first case, without GSFs, the voltage does not change noticeably, but the frequency increases exponentially due to the SFS control. The inverter controls detect an over frequency condition and the inverter ceases to deliver power at approximately $t=5.6$ sec. When voltage and frequency support is added in this scenario, with $K_f = 30$ kW/Hz and $K_v = 1000$ VAr/V, the voltage and frequency response appears erratic, but both are maintained within limits, and the inverter runs on for greater than 2 seconds. In this scenario, the inverter would fail the anti-islanding test with GSFs enabled.

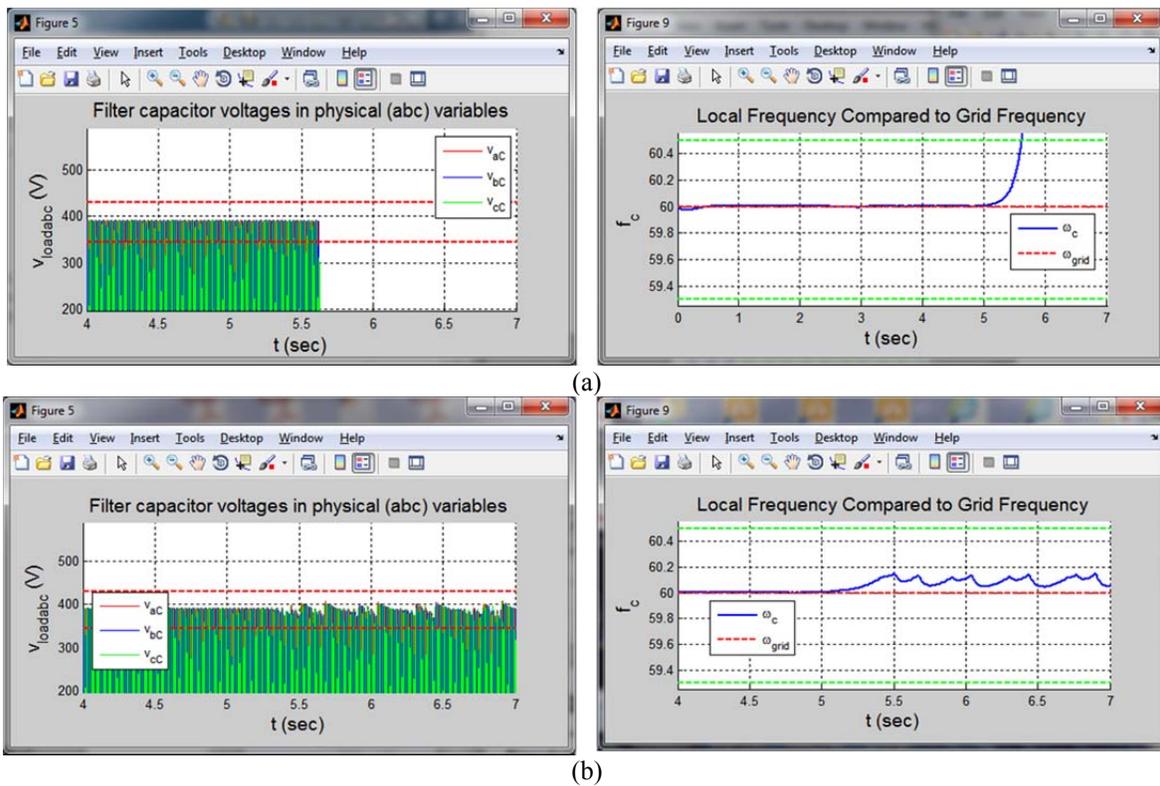


Figure 47. Simulation indicates (a) over frequency trip resulting from SFS and (b) GSF interfering with SFS

4.3. Summary

In this section, an attempt was made to explain some of the mechanisms affecting the interoperability of anti-islanding (specifically passive OUV/OUF and SFS) with volt-var and frequency-Watt functions. A simplified model was developed to clarify the resulting closed-loop system realized by the GSF feedback. Considering first the passive system, the additional feedback results in a new system with steady-state active and reactive power values that are different from the standard system described in [10], resulting in different steady-state voltage and frequency characteristics and thus a different “non-detection zone”. With the SFS algorithm, island detection relies on positive feedback of the frequency error; since GSFs provide a negative feedback, the efficacy of SFS is diminished.

5. VOLT-VAR INTEGRATION ON COMMERCIAL INVERTER

Sandia National Laboratories Distributed Energy Technologies Laboratory (DETL) has developed a facility that is well suited to investigate operational capabilities of utility interconnected distributed energy resource (DER) devices. The DETL utilizes laboratory equipment capable of simulating programmable dc and ac resources necessary to evaluate the performance of the device under test (DUT). The dc source is capable of simulating PV module characteristics at different irradiance and module temperature conditions. The ac simulator is a regenerative arbitrary waveform generator that provides a high quality ac voltage with programmable voltage and/or frequency anomalies that are consistent with LVRT curves proposed by different agencies. To evaluate an inverter's advanced inverter function capabilities, the inverter is configured to operate with the simulated utility as shown in Figure 48.

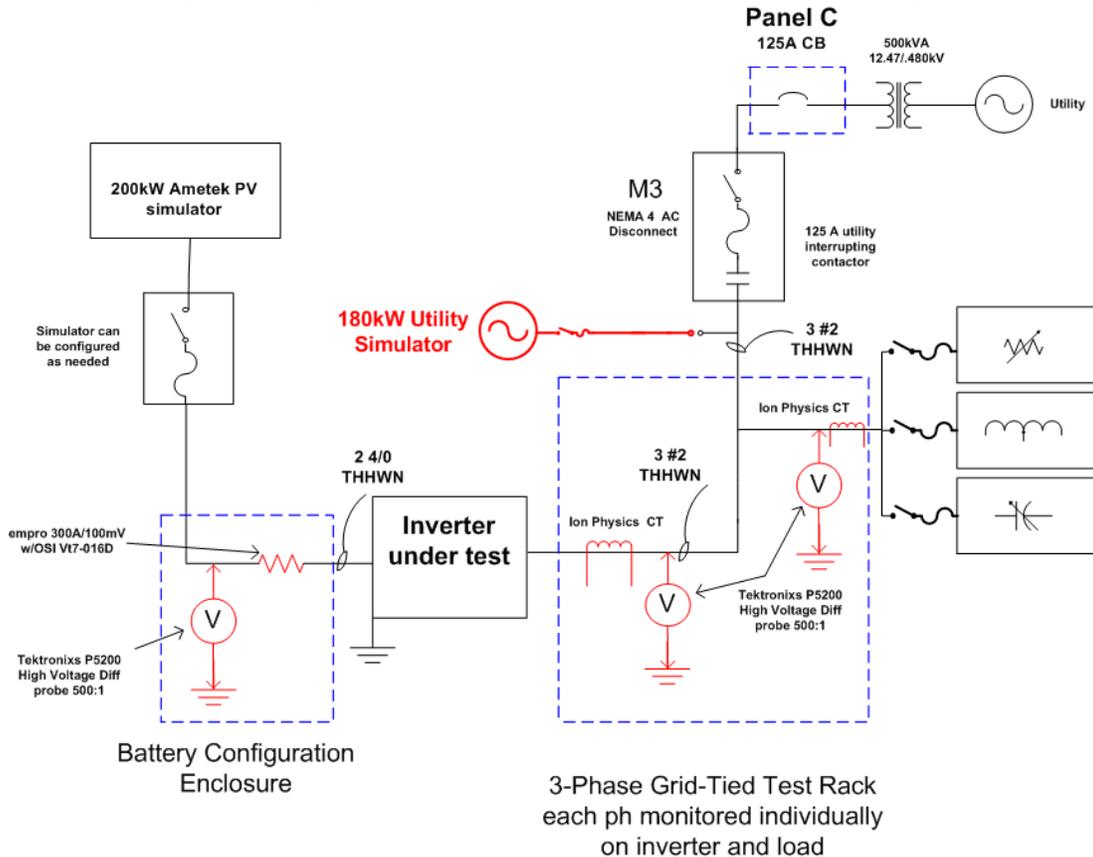


Figure 48. DETL 3-phase test bed

Evaluating an inverter with advanced inverter capabilities requires the ability to change the line voltage to levels that initiate the DUT to deliver reactive power. Adjusting the line voltage beyond the pre-programmed dead-band voltage initiates the volt/VAR function to be implemented and the DUT will deliver reactive power in an effort to assist the utility in meeting its voltage regulation requirements.

A draft SNL Interoperability Test Protocol has been developed for the evaluation of industry products with advanced inverter functionality [14]. The test protocol has been designed to incorporate utility controlled advanced function implementations as well as autonomous

implementation of the advanced functions. Table 6 and Table 7 show the function capability for determining the mode of volt-var to be implemented and if delays and/or ramp rates apply to the power adjustments.

5.1 Parameters and Function Capability Table (FCT)

The DUT’s capabilities should be listed in the function capability table (FCT), which includes four possible volt/VAr modes (VV11, VV12, VV13, VV14) and three optional parameters (random time window to initiate, ramp rate to change output, timeout period for the command.) The FCT indicates which tests are specified for each VV mode. If the DUT can act on any of the optional parameters, then additional tests of those capabilities shall be performed, as indicated in the FCT.

Mode and Optional Parameters	Yes/ No?	Action
VV11 – available VAr support with no impact on watts (watt priority)		Parameters as specified in A61.1; Tests specified in Table A6-4
VV12 – maximum VAr support without exceeding maximum watts (VAr priority)		Parameters as specified in A61.2; Tests specified in Table A6-5
VV13 – static settings		Parameters as specified in A61.3; Tests specified in Table A6-6
VV14 – No VArS		Default setting; output returns to unity power factor
Time window (optional parameter)	No	-
	Yes	Additional tests using procedures in Appendix 17; Typical value 60 seconds
Ramp Rate (optional parameter)	No	-
	Yes	Additional tests using procedures in Appendix 18
Timeout period (optional parameter)	No	-
	Yes	Additional tests using procedures in Appendix 19

Table 6. Volt-Var parameters

Depending on the volt-var curve chosen from Table 7, the voltage setpoints are described by the following:

- V1- upper voltage set point where maximum available VArS are available
- V2- upper voltage set point where dead-band ends
- V3- lower voltage set point where dead-band ends
- V4- lower voltage set point where maximum available VArS are available

See also Figure 1.

5.2 VV11 Volt-Var Example

This test is conducted by varying the AC line voltage beyond the percentage of nominal voltage and these percentages are shown in the table below. An AC utility simulator is used to provide the stimulus for the inverter to supply the reactive power; as the voltage increases or decreases the available VArS are delivered to the pre-prescribed levels. This allows the volt-var capabilities of the inverter to be characterized. Recording the AC line voltage and current as well as apparent, active and reactive power levels allows the capabilities of the inverter to be documented.

DUT Initial Operating State	Volt/Var Initiation	Volt/Var [V,Q] Array				Requested Ramp Time (% VARaval/s)	Time Window (seconds)	Timeout Period (seconds)
50% rated power, unity power factor	Binary, 1	V1	94	Q1	1000	-	-	-
		V2	97	Q2	0			
		V3	103	Q3	0			
		V4	106	Q4	-1000			

Table 7. Programmed Volt-Var Settings

5.3 Volt-Var Laboratory Results

SNL has been collaborating with an industry partner to implement the advanced inverter functions and assess the capabilities in a pre-commercial product. The VV11 volt-var function has been programmed into an inverter and the test was conducted to document the response of the inverter when the voltage exceeded the pre-prescribed voltage settings. The program settings are shown in Table 7, which is a subset of the SNL interoperability test protocol volt-var test matrix. The results of conducting the volt-var test are shown in Figure 49. For this test, the inverter is set to operate at 50% of rated power. This allows sufficient current to be available for reactive power as the voltage is varied from nominal. The inverter controls the voltage at the PCC and responds accordingly to supply reactive power as the voltage sags or swells. Figure 49 shows the inverter response to a voltage sag and swell. The results indicate successful implementation of volt-var control.

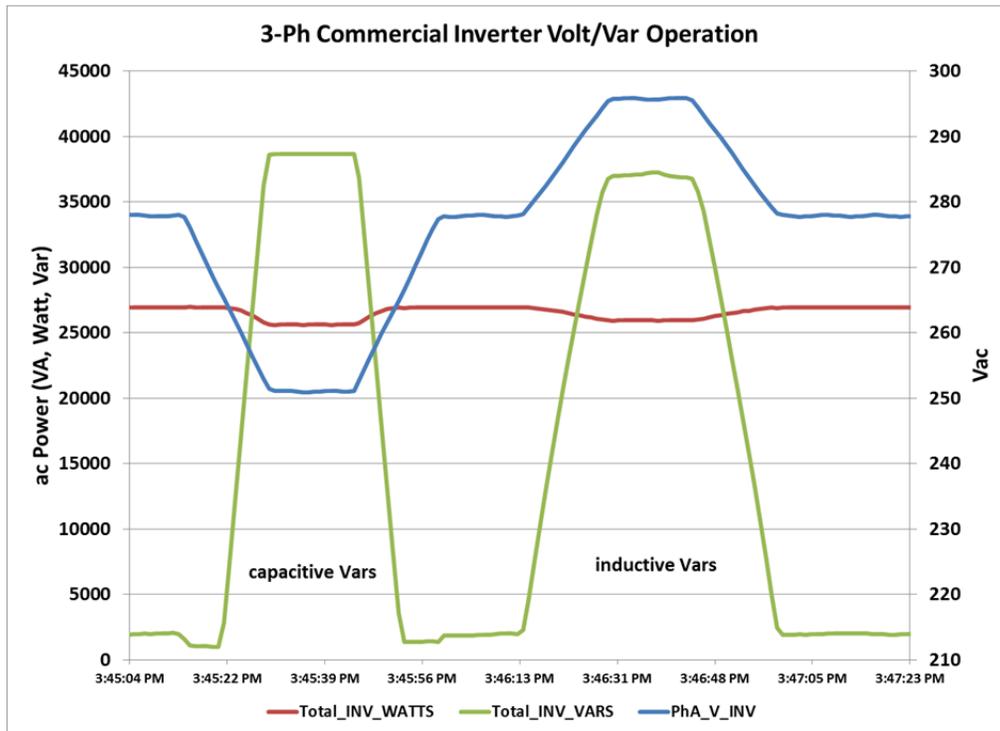


Figure 49. Volt-var test results with a voltage sag and swell

5.4 Summary

SNL has developed a facility that is designed to assess the capabilities of inverters with advanced inverter functions which, when implemented correctly, can address the issues associated with the

high penetration of PV systems. This section describes the test facility and dc and ac sources that provide the means to assess the capabilities and describes the assessment tool developed at SNL. The assessment tool is the SNL inverter interoperability test plan, which has been designed to assess the advanced inverter capabilities that include the different implementation methods of volt-var, L/HVRT and L/HFRT. The test plan is designed to assess the functions as the device under test is externally stimulated to point of utilizing the function. Examples of the test plan are provided as well and the examples of the implementation of the function and results of the function being implemented.

6. CONCLUSIONS

In this report, several advancements have been made in the acceleration of advanced-inverter functions and the evaluation of the interoperability of grid-support functions (GSFs) and anti-islanding in grid-tied distributed PV systems. Specifically, a Sandia-lead team worked with industry in the development of platform-specific transient inverter models in Simulink and validated these models against hardware through the comparison of run-on times. These models were utilized in multi-inverter heterogeneous (different manufacturers and different anti-islanding schemes) system simulations to characterize the islanding performance in high-penetration scenarios. These models were then also merged with GSFs including both volt-var and frequency-watt compensation and tested in simulation. One drawback, however, is the proprietary nature of these models, some of which are “black-box” models; limited information is provided about these in this report. However, new generic models were developed and presented herein to support analytical evaluations of GSFs and anti-islanding interoperability. Through the simulation and analytical work presented, several new insights are provided. In addition, an overview is provided of the Sandia-developed IEEE 1547 draft test protocol. Finally, the Sandia team engaged with industry to acquire pre-commercial hardware capable of GSFs, and support was provided to get the first volt-var operation to function on a pre-commercial unit.

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APPENDIX – GENERIC MODEL SIMULINK LIBRARY

This section describes the models of the detailed generic inverter model components in the Simulink inverter library, co-developed with PC Krause and Associates.

Generic Control Function Models

Several inverter control function models were developed for this effort. They are described below

Current Command Calculation

This block takes the commanded real and reactive power, voltage angle, and rms voltage and calculates the currents needed to achieve the power command.

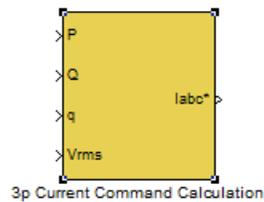


Figure 50. Current Command Calculation control block.

Frequency Ride Through

This block implements the frequency ride through control according to IEEE standard 1547.

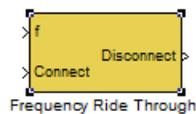


Figure 51. Frequency Ride Through control block.

Maximum Power Point Tracking (MPP)

This block calculates the dc voltage that results in the maximum power point for the solar array. It also calculates the maximum power.

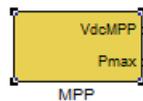


Figure 52. MPP control block.

Phase-Locked Loop (PLL)

The PLL block takes in a balanced three-phase set of voltages and calculates the frequency of the voltages. It also calculates the angle of the first voltage in the three-phase set. When the error of

the PLL is small enough, the Locked output will change from zero to one. The Freeze input (when set to one) prevents the PLL from unlocking even if the PLL error increases.

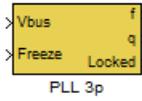


Figure 53. PLL control block and mask.

Voltage Ride Through

This block implements the voltage ride through control according to IEEE standard 1547



Figure 54. Voltage Ride Through control block.

Frequency-Watt

This block calculates the inverter power command. For frequencies above the deadband limit, the power command is reduced proportionally with increasing frequency. It is reduced from the max array power using the slope defined in the mask.

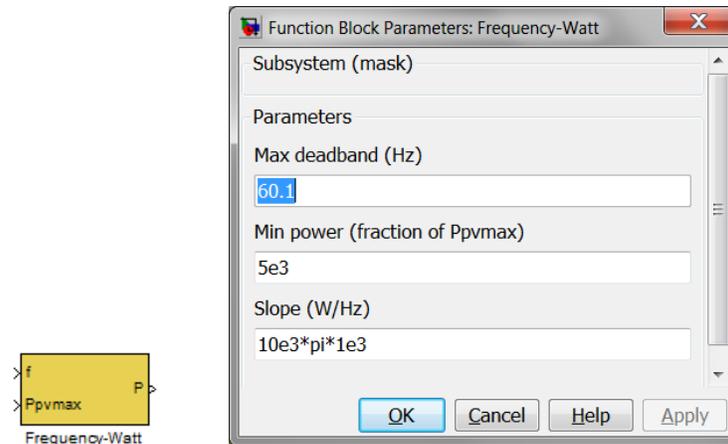


Figure 55. Frequency-Watt control block and mask.

Sandia Frequency Shifting (SFS)

This block implements the SFS control according to Fig. 1(a) in [1]. It takes current commands calculated in the current command block and modifies them according to the SFS control. The c_{f0} parameter in the SFS control switches between 0.01 and -0.01 with a period of 4π in the

[1] X. Wang, W. Freitas, V. Dinavahi, and W. Xu, "Investigation of Positive Feedback Anti-Islanding Control for Multiple Inverter-Based Distributed Generators," *IEEE Trans. Power Systems*, Vol. 24, No. 2, May 2009, pp. 785–795.

electrical angle. The block mask lets the user define the phase offset for the oscillation of this value, which enables multiple inverters to be either in phase or out of phase.

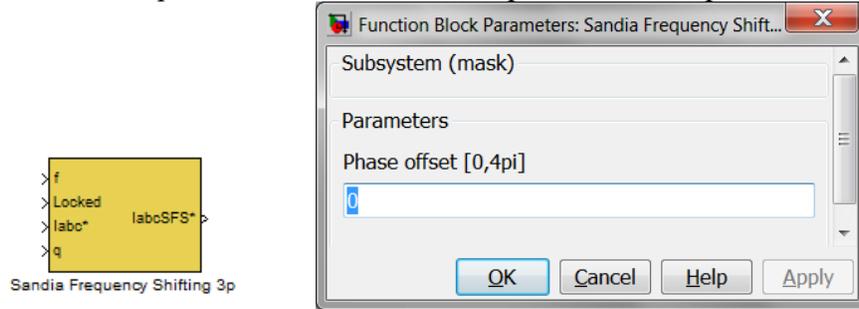


Figure 56. SFS block and mask.

Volt-var

This block defines a reactive power command as a function of the bus voltage rms value. When within the rms voltage deadband, the command is zero. When outside the deadband, the values scale with the incremental voltage outside the band with a slope defined by the last mask parameter. The reactive power command is limited on both the upper and lower ends with user-defined values.

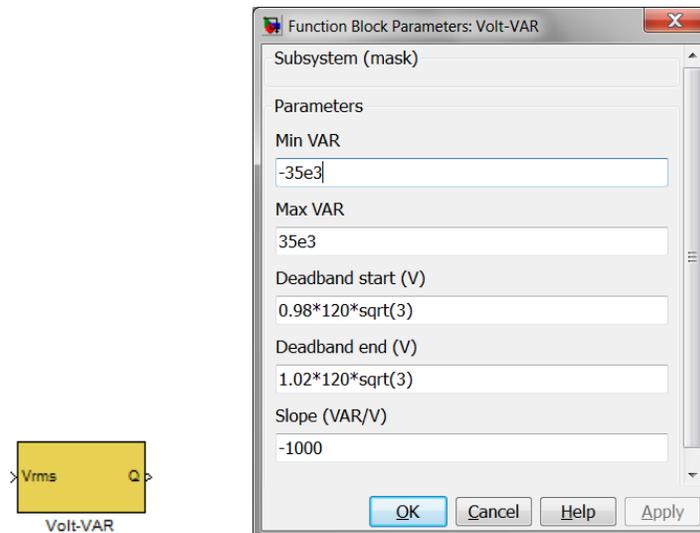


Figure 57. Volt-var control block and mask.

Hardware Models

3-Phase Bus

The three-phase bus model calculates the voltages on a three-phase bus based on the combination of Thevenin and Norton sources that are connected to the bus. Each Thevenin equivalent or Norton connection to the bus should be a vector with six elements. For a Thevenin connection, the six elements should be v_{tab} , r_{tab} , v_{tbc} , r_{tbc} , v_{tca} , r_{tca} , where subscript ab , bc , and ca denotes

line-to-line quantities. For a Norton connection, the elements should be i_{nab} , g_{nab} , i_{nbc} , g_{nbc} , i_{nca} , g_{nca} . The bus block calculates the bus line-to-line voltages, v_{ab} , v_{bc} , v_{ca} , as outputs.

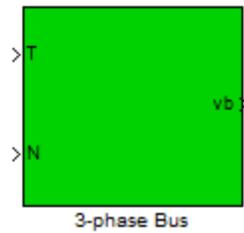


Figure 58 Three-phase bus Simulink block

3-Phase Inverter

The inverter block includes models for the inverter controller and the inverter circuit (Figure 60).

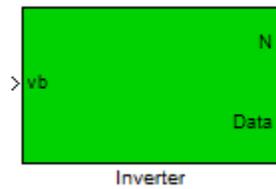


Figure 59 Inverter Simulink block

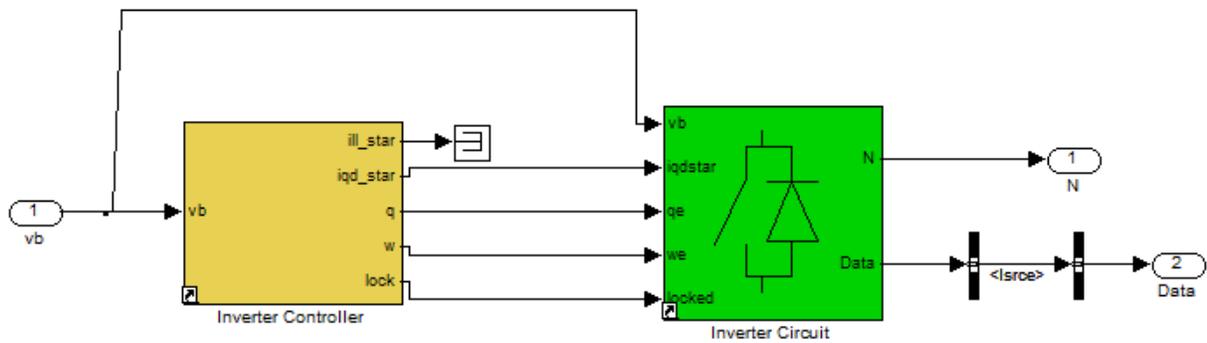


Figure 60 Inverter block structure

The inverter controller monitors the bus, and calculates the magnitude and frequency of the bus voltages. Frequency/Watt, Volt/Var, and Sandia Frequency Shift controls are incorporated into this controller. The output of the inverter controller is the qd current commands to the inverter circuit based on the control functions.

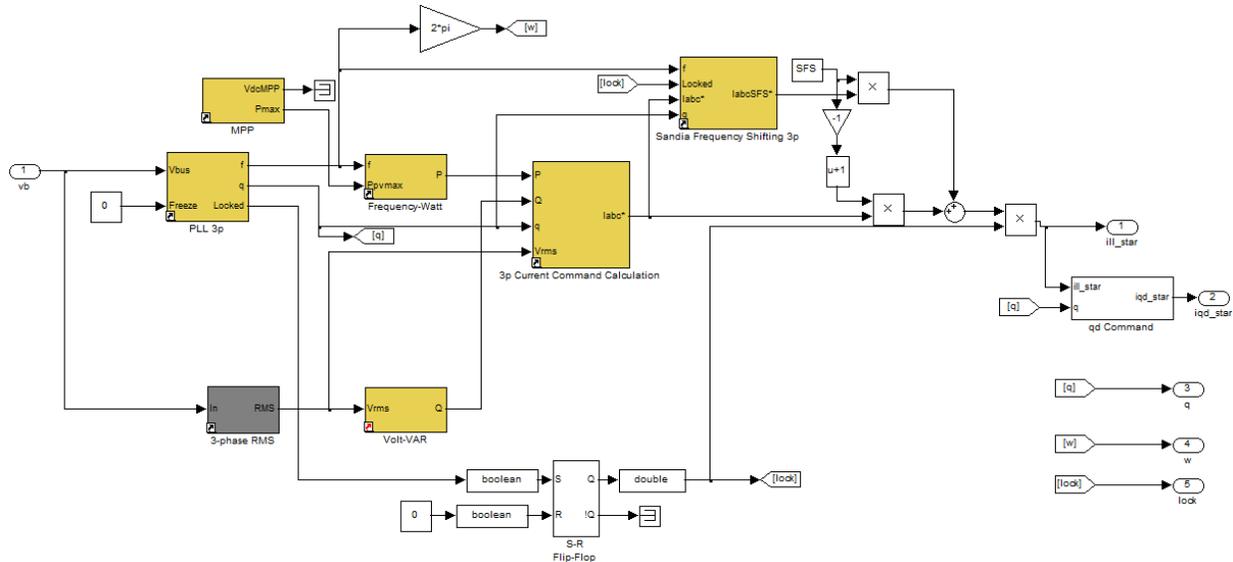


Figure 61 Inverter controller block structure

The inverter circuit block models the dynamics of the inverter circuit. It also contains the lower-level voltage control of the inverter bridge that produces the commanded current at the output.

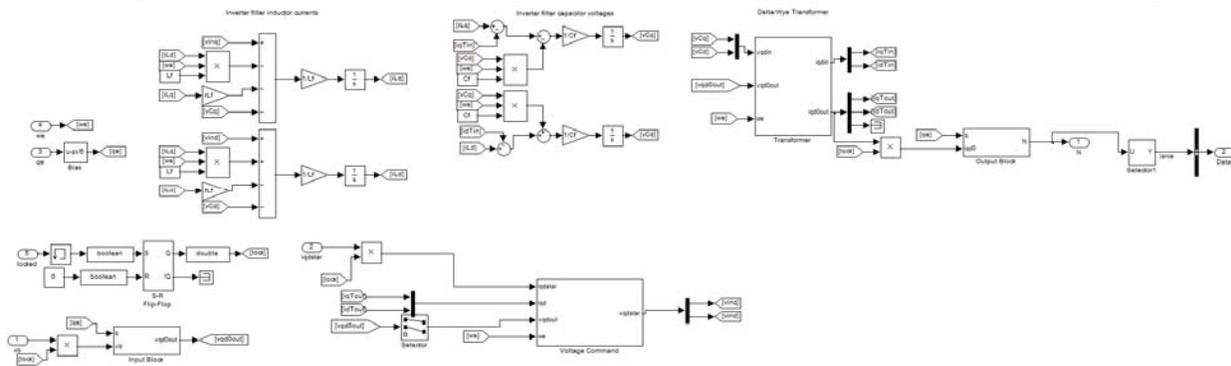


Figure 62 Inverter circuit block structure

3-Phase RLC Load

The 3-phase RLC Load block draws the specified real and reactive power at the nominal voltage and frequency. If the magnitude or frequency of the bus voltage varies, the actual load value varies the way a parallel RLC load does.

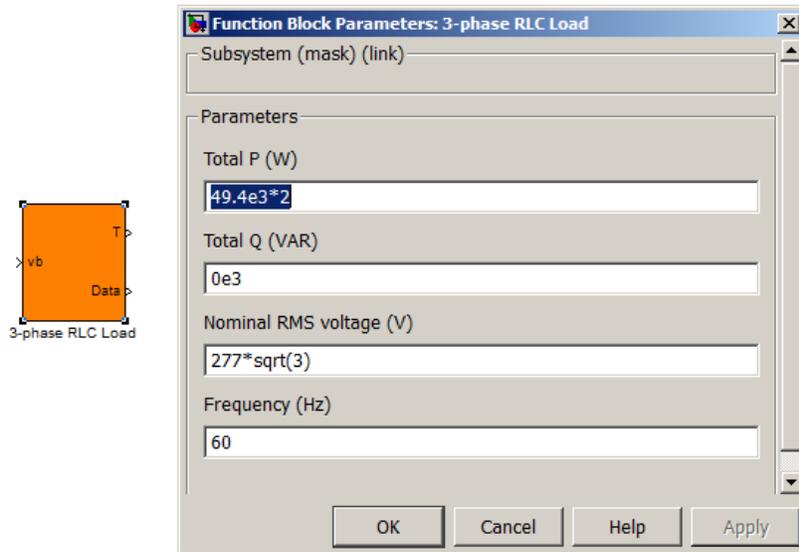


Figure 63 Three-phase RLC load block and mask

3-Phase Grid

The 3-phase Grid block models a stiff grid with constant voltage and frequency. The user can specify the time when the grid is disconnected during simulation. At the preset time, the internal resistance of the grid steps to a large value, effectively disconnecting it from the bus.

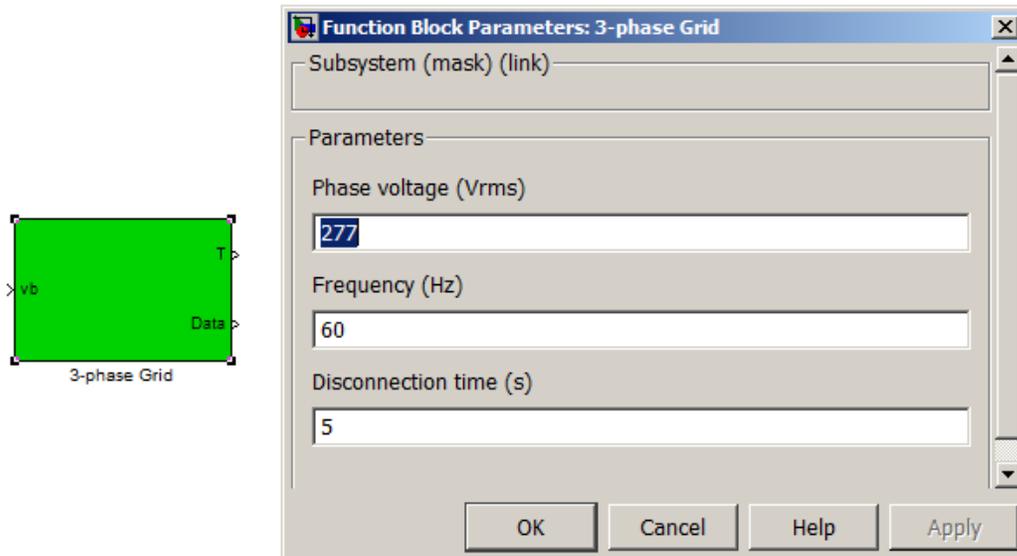


Figure 64 Grid Simulink block and mask

Scripted Simulation Model Development

PCKA implemented MATLAB utility functions to build microgrid/island models with significant complexity. The main functions that are used to build island models are briefly described in Table 8.

Table 8. Main functions for building island models

Name	Functionality
CreateIsland	Create the island structure
AddInv	Add inverter block to the island
AddLoad	Add load block to the island
AddGrid	Add grid block to the island
AddBus	Add bus block to the island
AddBlock	Add generic block to the island
BuildIS	Build the Simulink model of the island

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