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SAND2007-6795

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Printed November 2007

Kinetics and Mechanisms of Nanowire Synthesis

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Synthesis of Silicon and Germanium Nanowires

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Abstract

The vapor-liquid-solid growth process for synthesis of group-IV semiconducting nanowires using silane, germane, disilane and digermane precursor gases has been investigated. The nanowire growth process combines *in situ* gold seed formation by vapor deposition on atomically clean silicon (111) surfaces, *in situ* growth from the gaseous precursor(s), and real-time monitoring of nanowire growth as a function of temperature and pressure by a novel optical reflectometry technique. A significant dependence on precursor pressure and growth temperature for the synthesis of silicon and germanium nanowires is observed, depending on the stability of the specific precursor used. Also, the presence of a nucleation time for the onset of nanowire growth has been found using our new *in situ* optical reflectometry technique.

ACKNOWLEDGMENTS

This study was done in partial fulfillment for my doctoral degree at Arizona State University. Technical discussions with Drs. S. Thomas Picraux and Jeffery S. Drucker Dr. Terry Alford, Dr. Subhash Mahajan, Dr. David Smith, Jason Ng and Dewey Wong, Dr. Molly McCartney, Dr. Jennifer L. Taraci, Jeff Dailey, Sarang Ingole, Jacob Thorp, Pavan Aella, and Dongqing Yang are greatly appreciated.

Thanks are also extended to Dr. Julia W.P. Hsu, research scientist at Sandia National Laboratories in the Surfaces and Interface Sciences division of the Physical, Chemical and Nano Sciences Center for her assistance in obtaining and retaining the Diversity Fellowship which supported this work, as well as the incredibly insightful summer internship concerning micro-contact printing and dip pen nanolithography for patterning gold films.

Lastly, I gratefully acknowledge and appreciate the financial support of the Sandia National Laboratories Fellowship Program and the National Science Foundation, as well as use of facilities within Arizona State University's Center for Solid State Electronics Research and the Center for Solid State Science.

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INTRODUCTION

Semiconducting nanowires represent one of today's most actively researched one-dimensional (1-D) structures, primarily for their potential in nanotechnology applications such as nanoelectronics, nano-optics, and nanosensing.¹⁻⁴ These 1-D structures are the fundamental building blocks for nanoscale architectures, however, the mechanisms and materials science controlling their formation are currently not well understood. Recent studies demonstrate the great potential for nanowires to achieve new and useful properties, but controlling size, morphology and crystallographic orientation are critical in order to advance the science of nanowire growth.

Similarly, recent interest into the effects of highly-strained axial and radial nanowire heterostructures, specifically in altering electron mobility⁵ and modifying valence and conduction band offsets, has prompted new research efforts to identify and control the growth conditions necessary for epitaxial, dislocation-free nanowire heterojunctions with sharp interfaces. Potential applications for nanowires range from low-power sensors to nanoelectronic transistors; the former would use the high surface area of nanowire arrays to achieve sensing on the scale of single-molecule sensitivity, and the later would use the strain effects within nanowire heterostructures to alter the transport within nanoscale electronic devices.

Nanoscale structures and devices such as these are potential opportunities for the ever-shrinking integrated circuit. Gordon Moore, co-founder of the world-leading company in semiconductor chip design and fabrication, predicted by his now renowned "Moore's Law" in 1965 that the number of transistors industry would be able to manufacture on a computer chip would double every year. That predicted rate was later updated to double transistor density every two years. Moore's Law has become the guiding principle for industry to deliver ever-more powerful semiconductor chips with ever-decreasing device dimensions and cost. Challenges to commercialization for near-future nanoscale circuits are analyzed annually and recorded in the International Technology Roadmap for Semiconductors in an effort to predict which technology roadblocks will need further research in order to continue along the path of Moore's law. Specifically listed in **Table 1.1** are the expected gate lengths and challenges to achieving these nano-scale device dimensions, such as the overlay accuracy critical dimension (CD) control, and gate oxide thickness (TOX).

The development of new one-dimensional nanowires has become an area of extreme interest for the semiconductor industry. Nanowire diameters are characteristically grown to have dimensions within the very small dimension requirements of industry, as listed in **Table 1.1**, and there are currently investigations underway to understand the materials issues associated with the production of these new, single-dimension structures. Such multi-disciplined investigations are focused not only by industry, but in part by the efforts of entities such as the U.S. National Nanotechnology Initiative, the Department of Energy, national laboratories, research universities, and several diverse organizations around the world to name but a few.

Table 1-1 Challenges and opportunities for upcoming semiconductor research and design, based upon the 2006 International Technology Roadmap for Semiconductors projections for scaling half-pitch and gate length over 14 years.

Year of Production	2006	2009	2012	2015	2018	2020
DRAM Half-Pitch [nm]	70	50	36	25	18	14
Overlay Accuracy [nm]	13	9	6.4	4.5	3.2	2.5
MPU Gate Length [nm]	28	20	14	10	7	6
CD Control [nm]	7.4	5.3	3.7	2.6	1.9	1.5
TOX (equivalent) [nm]	1.1	0.9	0.5	0.5	0.5	0.5

Most of today’s integrated circuits consist of device arrays constructed from planar semiconductor heterostructures in two dimensions and typically using well-understood “top-down” fabrication techniques, specifically optical photolithography, ultra-violet photolithography, reactive ion etching, and other patterning techniques. In these methods, structures are fabricated on substrates by deposition and removal of thin film layers in order to create electrical devices, components and circuitry as illustrated in **Figure 1.1(a)**. Though this top-down approach is widely used in industry, the massive expense and extensive process control required to maintain the processes of applying photoresist, masking on the nanometer scale, exposing, etching, removing the resist layer, and repeating these steps - sometimes hundreds of times - make it a difficult approach to continue to scale to ever smaller dimensions without massive amounts of labor and very expensive tools.

The counter approach is to use ‘bottom-up’ methods, where complex features are created on substrate materials by self-assembly processes; self-assembly being the processes in which pre-existing parts or disordered components of a preexisting system form structures or patterns without human intervention.⁶ Two types of self-assembly can be defined, static and dynamic. Systems at equilibrium which do not dissipate energy and yet maintain their patterns and order are considered statically self-assembled. Examples of static self-assembled structures include molecular crystals and folded proteins, both of which require some energy to form the ordered structure, but do not require energy to retain that self-assembled structure. Those systems that only occur only within non-equilibrium conditions, such as biological cells and some chemical reactions, are considered dynamically self-assembled. In our studies, the thermal evaporation of extremely thin films to form self-assembled metallic clusters for seeded growth of nanowires, as shown in **Figure 1.1(b)** as shown in, exemplifies a static self-assembled bottom-up process, because the kinetics of the system can define the spatial and geometric characteristics of the metallic clusters.

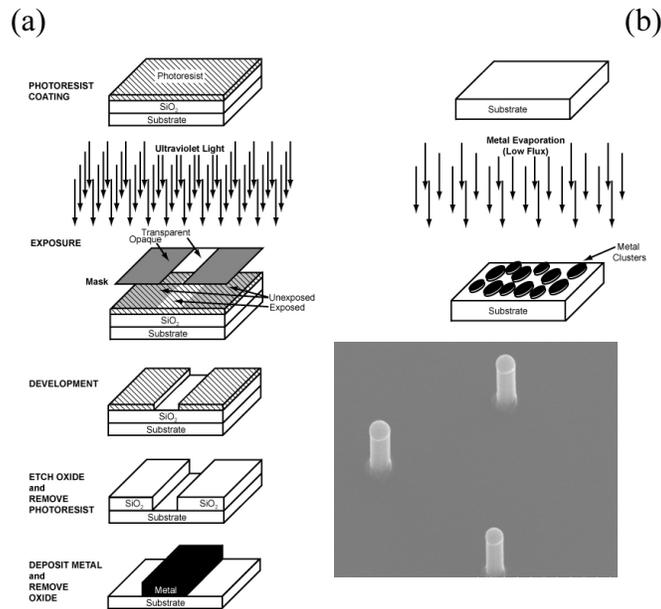


Figure 1.1: top-down (a) versus bottom-up (b) method for spatially defining nanostructures.

These small diameter clusters catalyze semiconducting nanowire growth by the vapor-liquid-solid method, a process which will be described in subsequent sections. When the nanowire structures become exceedingly small, with diameters on the order of less than 10 nm, their characteristic optical and electronic properties are necessarily modified by quantum confinement effects. Similarly, though nanowire heterostructures typically have physical dimensions outside the realm of quantum confinement, by the addition of strain at the heterostructure interfaces, the effective small size of the electronic confinement areas brings quantum confinement effects into play. Representative reduced dimension structures are shown in **Figure 1.2**.

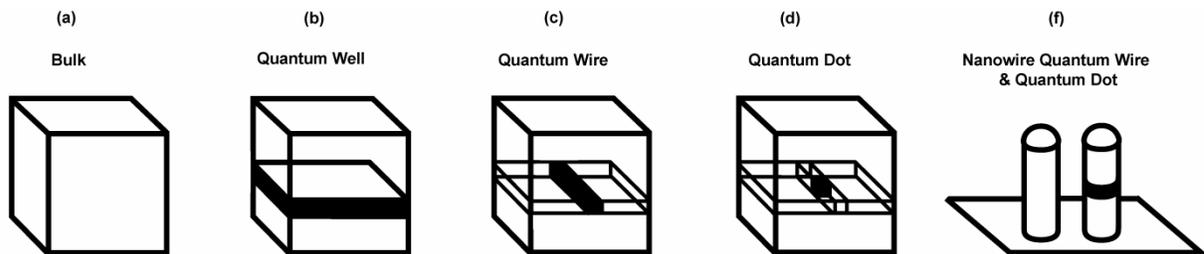


FIGURE 1.2: Electronic properties are affected by the quantum confinement effects within nanoscale structures (nanoscale requires at least one dimension of the structure is less than 10 nm in length). As compared to (a) bulk materials with a 3-dimensional structure (3-D) which are not limited by confinement effects, each of the other nano-size structures (b-f) exhibit quantum confinement in at least one direction: quantum well (2-D), quantum wire (1-D) and quantum dot (0-D).

The seminal works of Wagner and Givargizov over four decades ago introduced one-dimensional crystal growth to the world, namely in the realm of the vapor-liquid-solid (VLS) growth mechanism.⁷⁻¹⁰ The VLS mechanism was identified in 1964 by Wagner and Ellis as an

explanation of their experiments with chemical vapor deposition of Si “whiskers” from SiCl₄ upon Si (111) surface containing deposited Au impurities.⁷ Later, Givargizov proposed an empirical model to describe the VLS growth mechanism during chemical vapor deposition (CVD).⁸ The growth mechanism includes the three phases of materials during nanowire growth: precursor gas in the vapor phase, liquid phase metallic catalyst seeds, and the resulting solid phase semiconducting nanowire. Several sequential processes must occur before nanowires nucleate from the surface – first the catalytic metal seeds deposited on the substrate become molten at elevated substrate temperatures. Then upon introduction of precursor gases, the metal seeds form a liquid eutectic alloy with the growth species. Continued supply of precursor gas leads to a supersaturation of the metal alloy seeds, followed by semiconducting atoms condensing at the substrate interface and nucleating a nanowire. In the VLS reaction, Givargizov inferred that there exists a lower limit on the diameter of wires that can be grown under a given set of conditions due to the cluster surface energy. Using SiCl₄ as the Si source gas, this lower limit was predicted to be in the range 50–100 nm,⁸ however current studies show Si nanowires can be synthesized in the range 10–100 nm. This VLS mechanism, originally described for large whiskers with diameters of approximately 1–100 micrometers, has become the primary method used for the formation of semiconductor nanowires of various types.^{11–14}

Nanowire System Opportunities

After the initial identification of the VLS growth mechanism and subsequent investigations into the materials science of whisker growth, interest in the VLS method declined. For nearly two decades, relatively few articles pertaining to fabrication or control of these interesting semiconducting structures were published. However, with the nanoelectronics boom in the late twentieth century, many researchers, beginning with Westwater in 1997,^{15,16} turned to the idea of self-assembled growth of nanoscale electronic materials, specifically semiconducting silicon nanowires from Au catalyzed VLS growth. Since that time, several groups have delved into semiconductor nanowire growth, in group IV materials^{4, 17–21} and in III-Vs.^{13, 22, 23}

Nanowire Device Realization

Though the number of journal articles for nanowire growth, fabrication, and modification has increased drastically since the mid 1990’s, the limited reporting of actual devices fabricated from nanowires is an indicator of the challenges surrounding the controlled synthesis and integration of nanowires into nanoelectronic devices. Individual nanowire devices such as lasers,²² photodetectors,²⁴ and light emitting diodes²⁵ have been demonstrated recently. The basic building blocks of any electronic circuit, be it microelectronic or nanoelectronic, involve three levels of organization; transistors, interconnects, and architecture.²⁶ Transistors are effectively switches which turn an electric current on or off, and have the capability to amplify signals.^{2,13,27} Interconnects serve to connect the transistors into integrated circuits in order to perform arithmetic or logic operations.^{28,29} Device architectures are the blueprints that define the way in which transistors and interconnects are organized, providing the mechanism by which circuits function. Currently there is little work being done to integrate nanowires into the architecture of integrated circuits, though this will become increasingly important as devices and interconnects are better understood. These three basic elements easily exist at the current microscale circuitry level, with sophisticated device processing already well understood; however, using nanoscale

devices to create similar devices and integrating nanoscale devices into microscopic integrated circuits will require a great deal of additional clever science and engineering. In fact, while several nanowire research groups around the world seek to fabricate nanoscale devices by whatever means necessary, the general understanding of the material science behind nanowire growth and synthesis are not well understood at this point.

NANOWIRE SYNTHESIS

Vapor-Liquid-Solid Growth Technique

The Vapor-Liquid-Solid (VLS) Mechanism

Nanowires of either Si or Ge are grown following *in situ* Au nanocluster deposition by taking advantage of the vapor-liquid-solid (VLS) mechanism. Silicon nanowires (SiNWs) are grown from gaseous disilane (Si_2H_6) or silane (SiH_4) precursors; those of germanium (GeNWs) from gaseous digermane (Ge_2H_4) or germane (GeH_4) precursors. The VLS mechanism, as illustrated in **Figure 2.1**, describes the incorporation of the gaseous species' atoms into the metal nanocluster catalysts as substrate temperatures are elevated, typically above the eutectic melting point.^{7,8,38} Nanowire growth, as demonstrated in **Figure 2.2**, for our experiments occur with precursor pressures between 3×10^{-4} and 9×10^{-2} Torr when the substrate temperature is raised above the Au-Si eutectic point 363°C (see **Figure 2.3**) to temperatures ranging between 380 and 700°C . The small metal seeds form a liquid eutectic alloy with the semiconductor growth material and act as the nucleation point for the formation of nanowires. Directly impinging semiconductor precursor species from the gaseous source serve to supersaturate the liquid metal seed with the growth atoms; these atoms diffuse through the droplet to the low-energy liquid-solid interface and adsorb onto the available lattice sites at the substrate interface. As growth continues, the liquid metal seed rides upon the top of the vertically growing semiconductor nanowire and facilitates further elongation of the nanowire. Thus in traditional adsorption-induced VLS, precursor gases adsorb directly onto the metal catalyst seed, supersaturate the seed, precipitate out at the substrate, and grow the nanowire.

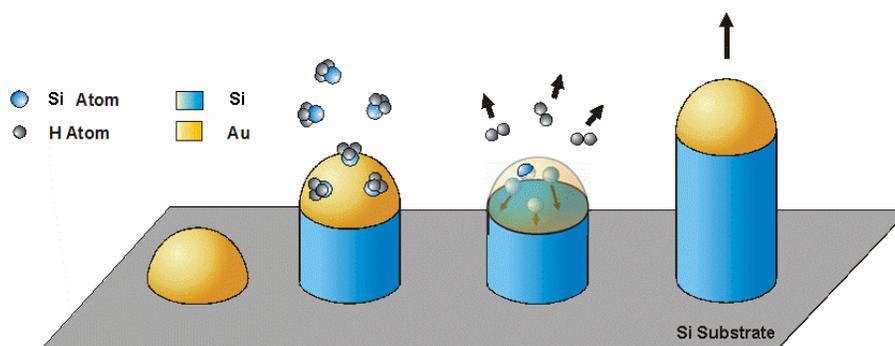


FIGURE 2.2: Vapor-liquid-solid mechanism illustrated for the disilane molecule forming a SiNW.

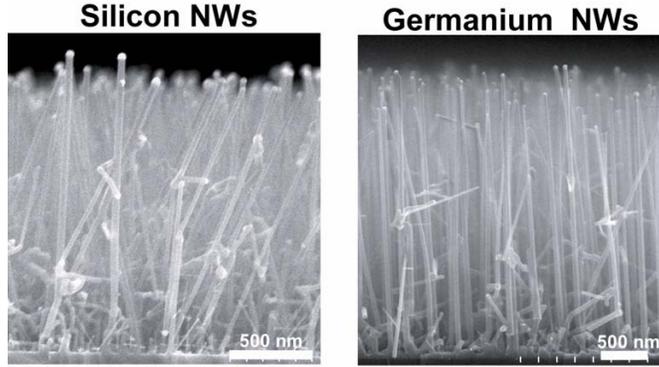


FIGURE 2.3: Demonstrated growth of silicon and germanium nanowires in our system. Growth conditions are (a) 1.0 nm Au deposited at 250°C, disilane source growth at 3 mTorr, 400°C for 15 min and (b) 1.0 nm Au deposited at 250°C, digermene source growth at 15 mTorr, 380°C for 4 min.

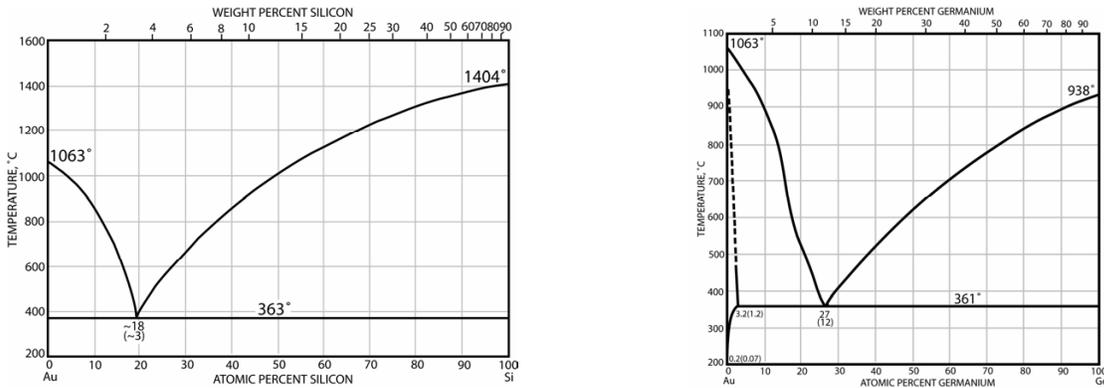


FIGURE 2.4: Au-Si and Au-Ge phase diagram. Nanowire processing typically occurs at temperatures near or above the eutectic temperatures (363 and 361°C, respectively), from the ASM Handbook Online.

Vacuum System for Nanowire Growth

Most experiments on highly pure substances which are intended to form epitaxially perfect nanostructures must be carried out within an extremely clean environment. Ultra-high vacuum (between 7.5×10^{-7} to low 10^{-14} Torr) provides a growth environment which remains free of impurities and contaminants for relatively long periods of time due to the lack of contaminants coming from the system itself. For example, in the ultra-high vacuum regime, the properties of the interior wall of the vacuum chamber become important since the number of molecules on the interior surface of the chamber exceed the number within the chamber itself. However, even under these growth conditions, a monolayer of contaminants will eventually form; the formation time required at 10^{-10} Torr, the base pressure of the system used here, is on the order of four-hundred minutes. **Figure 2.4** illustrates the system used for these CVD nanowire growth experiments, while schematic layout and photos of the system are shown in **Figure 2.5**.

Unique to our nanowire growth system are the capabilities for *in situ* gold evaporation, to form the catalytic seeds for VLS nanowire growth, and a novel *in situ* optical reflectometry setup, to monitor the growth of nanowires during growth. These capabilities enable the growth of nanowires on atomically-clean surfaces as prepared in ultra-high vacuum conditions, and allow for the determination of the nanowire nucleation time; both techniques allow us to precisely

control and monitor the nanowire growth. Specifically, the nanowire growth system is composed of conventional stainless steel ultra-high vacuum compatible hardware (i.e. utilizing Conflat-type, metal-sealed flanges on all feed-throughs and ports). A magnetically-levitated, corrosive-compatible turbo-pump (manufactured by BOC Edwards - formerly Seiko-Seiki - model STP-451C) backed by a fomblinized rotary-vane mechanical pump (BOC Edwards RV-12F) provides the ultra-high vacuum environment, and typical achieves base pressures as low as 1.0×10^{-10} Torr after bake-out. The use of a load lock chamber ensures that the ultra-high vacuum environment remains free of atmospheric contamination upon sample introduction. This load-lock chamber typically achieves pressures in the high vacuum regime, around 7.5×10^{-8} Torr (1.0×10^{-7} mbar), by the use of a small turbo pump (Pfeiffer Balzer TPU 170) and mechanical pump (Alcatel 2004A).

Samples are resistively heated in the UHV environment prior to the start of these experiments. Resistance values across the silicon sample and sample-holder are less than 30 ohms before heating. To bake out any contaminants and impurities, each sample is outgassed at increasing temperatures from 200 to 600 degrees Celsius over the course of an hour. Holding the sample at elevated temperatures of 600°C for 6-12 more hours ensures that all residual gases have been expelled from the silicon sample.



FIGURE 2.5: The nanowire growth chamber – as depicted by Solidworks® renderings.

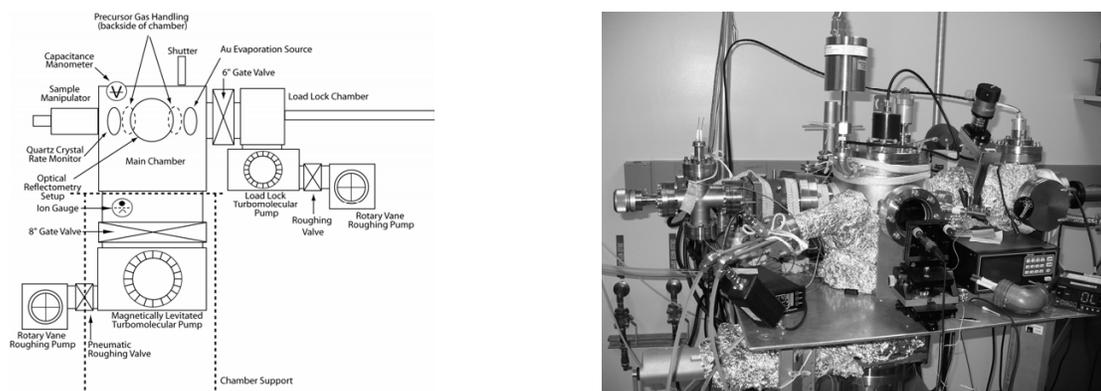


FIGURE 2.6 Schematic representation and photograph of the nanowire growth chamber.

The native oxide is removed from the sample surface after outgassing has occurred and before the experiments occur in our studies, thus providing a crystallographically pristine surface on which the subsequent epitaxial growth takes place. The clean substrate creates a surface where adatoms migrate very efficiently on the substrate. It is known that under UHV conditions that a

clean surface should remain free of surface contaminants for an amount of time proportional to the vacuum system pressure. For example, during our typical *in situ* gold deposition process near 1×10^{-9} Torr, approximately forty minutes elapse before a monolayer of contamination forms (monolayer equivalencies for gold, silicon, and germanium are provided in **Table 2-1**).

Substrates used herein are commercially available Si wafers (Virginia Semiconductor) with one side polished close to the (111) crystallographic plane. It should be noted that this is different than the substrates typically used in industry for fabrication of microelectronic integrated circuits; industry standards nominally use a (100)-oriented substrates that are misoriented (ie miscut) by up to $\theta = 5^\circ$ in an arbitrary direction. In contrast, we use (111) oriented 2-inch Si wafers with a vendor specified $3^\circ \pm 0.5^\circ$ miscut toward the (110) direction. The misorientation of the substrate surface causes intrinsic surface steps on the silicon of one monolayer (ML) height ($h_{1\text{ML,Si}(111)} = \sqrt{6} (a_{\text{Si}})/4 = 0.333 \text{ nm}$)³⁹, and the average lateral separation $d = h/\sin\theta$ of such surface steps is about 6.4 nm. These surface steps and step edges play a significant role in the formation of nanocatalyst seeds and pre-pillars, as will be described in subsequent chapters.

TABLE 2-1: Monolayer thickness equivalencies for group IV nanowire materials and catalyst.

Atomic Species	Areal Density (100) (atoms/cm ²)	Areal Density (111) (atoms/cm ²)	1 ML Equivalent Thickness (nm)
Si	6.78×10^{14}	7.83×10^{14}	0.333
Ge	6.25×10^{14}	7.22×10^{14}	0.346
Au	1.20×10^{15}	1.39×10^{15}	0.500

An extremely fast, fairly convenient method for sample heating uses the resistance of the sample itself to provide the thermal energy necessary to raise the sample temperature by running current through the substrate as mentioned above. This resistive heating technique requires an accurate calibration of sample temperature as a function of heating current (or power, effectively). Assuming the sample's resistivity, width, and length remain constant between samples, the calibration should remain valid for all samples. However, we found that a large variability results from the sample-to-sample variation in contact resistance provided by the mechanical interconnects between the metal contacts on the sample holder and the silicon substrates, prompting a search for a different method of determining sample temperature reliably. Original experiments were conducted using (January 2003 – November 2006) the results of a thermocouple and optical pyrometer calibration scheme; later experiments used individual sample temperature calibrations (November 2006 – present) by addition of a two-color infrared pyrometer to measure the sample temperature directly *in situ*, immediately prior to deposition and growth for each sample.

Chemical Vapor Deposition

Chemical vapor deposition (CVD) is typically defined as the growth of a solid film on a substrate by reactions that occur in the vapor phase. In this growth technique, reactive gases pass over a resistively heated silicon wafer piece. These gases adsorb onto the sample surface and react there, forming a film. By-products of the reaction leave the surface as gases, and are pumped

away. The reactions can be activated either by (a) thermal energy through heating the sample – as used in these studies, (b) radio frequency (RF) energy, or (c) by lamps or laser light. Striking a plasma in the reaction chamber and thus creating energetic electrons that propel the reaction forward is known as Plasma Enhance CVD (PECVD), and is another method also in use by our research group.

In these studies, the precursors used are inorganic gases such as silane, disilane, germane and digermane passing over our resistively heated substrate, thus undergoing a thermally activated CVD growth process. The cold-wall CVD reaction chamber combines an ultra-high vacuum (UHV) and a simple load-lock chamber, to facilitate sample entry to the high cleanliness vacuum environment, as described above.

The processes contributing to CVD growth are illustrated in **Figure 2.6**. Once introduced into the reaction chamber, the precursor gas acts as a reactant that diffuses to the substrate surface; under specific growth parameters, the reactant can nucleate on the surface, undergo surface migration, and complete surface reactions to form thin film structures. Reaction byproducts and unreacted precursors diffuse away from the substrate and are pumped from the chamber. This CVD process typically grows homogenous thin films quickly, as compared to molecular beam epitaxy (MBE) techniques; however, the precursor gases used in these CVD processes have the inconvenience of being highly toxic and extremely pyrophoric.

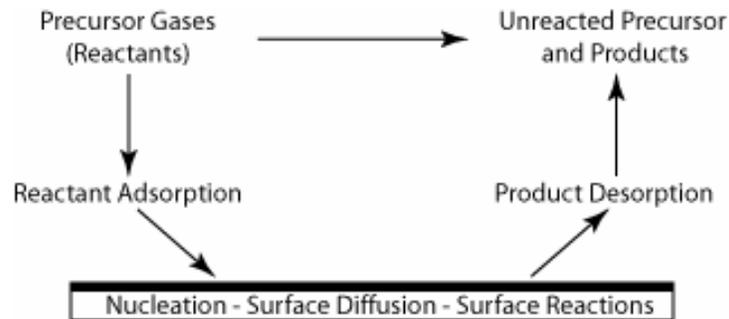


FIGURE 2.7: The Chemical Vapor Deposition (CVD) Process.

In comparison, the VLS process works by providing a catalytic seed where the dissolution of vapor-phase precursor gases can be accelerated. The gold catalytic seeds deposited *in situ* allow gas molecules to incorporate into the seeds at a higher rate than they absorb on the bare substrate surface. The differences between typical planar CVD growth process and the catalytic CVD growth process are shown in **Figure 2.7**.

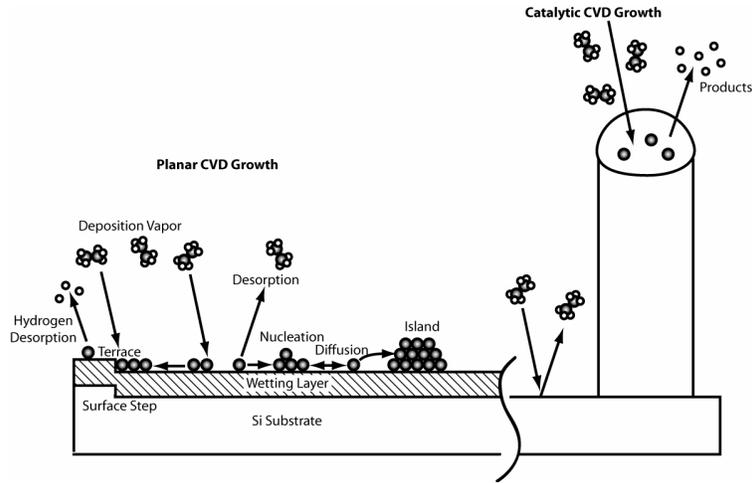


FIGURE 2.7: Typical deposition reactions and surface interactions for planar chemical vapor deposition growth as compared to catalytic CVD growth.

During the CVD process, molecules within the precursor gas continuously collide amongst themselves and with the chamber walls; it is these collisions that define the properties of the gas and which are characterized by the kinetic theory of gases. One can use the velocity distribution of colliding molecules within a gas at a given temperature and pressure to determine the average speed of the gas molecules. From this result, it is possible to calculate the flux of gas molecules impinging on a surface as a function of pressure and temperature,

$$\text{Flux} = \frac{P}{kT} \left(\frac{kT}{2\pi} \right)^{\frac{1}{2}} = \frac{P}{\sqrt{2\pi mkT}}, \quad (0.1)$$

where P is the pressure (in $\text{N}\cdot\text{m}^{-2}$), m is the molecular mass (in kg), and k and T are Boltzmann's constant and temperature (measured in $\text{J}\cdot\text{K}^{-1}$ and Kelvin, respectively).

Table 2-2 lists the molecular flux for the precursors used in these experiments at their typical growth conditions, and **Figure 2.8** shows the trend of molecular flux for each precursor as a function of pressure; note the lighter silanes have a higher flux than the heavier germanes for a given pressure (light and heavy stem from the atomic mass differences between the Si and Ge atoms). Typical nanowire growth conditions include catalytic seeds averaging 10-50 nm in diameter, with subsequent nanowires grown at differing growth rates depending on precursor species, usually approximately 5 nm/sec.

TABLE 2-2: Flux of semiconducting nanowire precursor gas species at room temperature, specifically given for the typical experimental growth pressure of each gas. Also included for reference are the typical growth temperature ranges used for these studies.

	Growth Pressure		Molecular Mass	Molecular Flux	Growth Temp
	(mTorr)	(N/m^2)	($\text{kg}/\text{molecule}$)	($\text{molecules}/\text{cm}^2$)	($^{\circ}\text{C}$)
Disilane	15	2.0	9.33×10^{20}	4.07×10^{18}	350-600
Silane	45	6.0	5.33×10^{20}	1.62×10^{19}	400-600
Digermane	9	1.2	2.51×10^{21}	1.49×10^{18}	300-500
Germane	> 100	> 13.3	1.27×10^{21}	> 2.35×10^{19}	400-500

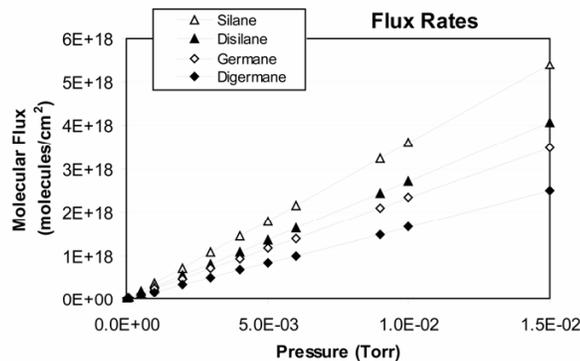


FIGURE 2.8: Precursor flux as a function of pressure given for each precursor.

Upon coming into contact with the catalytic gold seed, the precursor gas devolves to release the excess hydrogen, and incorporate into the catalytic seed to form the eutectic by undergoing the following overall reactions:



Vapor pressures, listed in **Table 2-3** for the various gases determine the maximum allowable pressures we are capable of working with in our gas handling system and are all well above the pressures used here.

Table 2-3 Vapor pressures of group-IV semiconducting nanowire precursor gases.

	Vapor Pressure (Torr)	Measured at Temperature (°C)	Source
Disilane	2588	21.1	Voltaix
Silane	35638	0	Air Liquide
Digermane	558	21.1	Voltaix
Germane	33763	21.1	Voltaix

In Situ Nanodot Seed Formation via Metal Evaporation

Deposition of catalytic seeds requires understanding of the metal evaporation process and the subsequent adatom diffusion and agglomeration on the sample surface. In the typical single-atom deposition methods, such as thermal evaporation described here, the nanoscale metallic seeds are grown directly on the silicon substrate through diffusion and aggregation, two processes which depend on the interactions between surface atoms and deposited metal adatoms.

The evaporation principle is fairly simple. The source material, in this case gold, is heated in ultra-high vacuum above its melting point, ejecting atoms through a cosine distribution trajectory in a straight line toward the substrate, where they condense to form a thin film. The mean free

path of the atoms in ultra-high vacuum is several orders of magnitude higher than the distance from the source to the substrate, so relatively few atomic collisions occur before the atoms deposit on the sample.

Surface energy, σ , is defined as the work required in creating new surfaces. Elastic energy develops when a material of comparably larger (or smaller) lattice spacing is deposited on a substrate of smaller (larger) lattice spacing, and thus the film experiences biaxial compression with

$$a_{\text{film}} = a_{\text{substrate}} (1 + \varepsilon) , \quad (0.2)$$

where a represents the lattice constant of the film (a_{film}) deposited on the substrate ($a_{\text{substrate}}$) and ε is the lattice mismatch between film and substrate materials. Elastic energy increases linearly with film thickness, most notably when the lattice mismatch between film and substrate is great.

Self-assembly occurs when the system spontaneously forms nanoclusters as a result of the surface and elastic energies competing to minimize the system's free energy.

When nanoclusters form, the elastic energy is reduced at the cost of increased surface energy. Thermodynamically, the relative energies of surfaces and interfaces determine which heteroepitaxial growth mode will dominate a specific system; in some instances the deposited film wets the substrate, other times it is more energetically favorable to form clusters or islands. Three equilibrium growth modes for heteroepitaxial films are illustrated in **Figure 2.9** and are known as the (a) Frank-Van der Merwe, (b) Stranski-Krastanov, and (c) Volmer-Weber growth modes. In instances where the substrate surface energy, σ_A , is greater than the surface energy of the deposited layer, σ_B , plus the interfacial energy of the system, γ , the Frank-Van der Merwe growth mode dominates and layer-by-layer growth occurs. In some cases, the deposited layer wets the substrate and grows pseudomorphically in two-dimensions initially, but non-planar islands nucleate with additional growth; this is known as the Stranski-Krastanov growth mode, also known as layer-plus-island growth. In the final case, where the substrate surface energy is less than the sum of the surface and interfacial energies, the Volmer-Weber mode occurs, where islands form exclusively at the beginning of growth with no initial layered growth.

Deposition of Au onto Si(111) substrates is characteristically described by the Stranski-Krastanov growth mode.⁴¹ Diffusion rates for Au, measured experimentally at room temperature on graphite, can be as high as 10^{-8} cm²/s.⁴² The deposition rate and substrate temperature determine the size distribution of small clusters desired for these experiments.

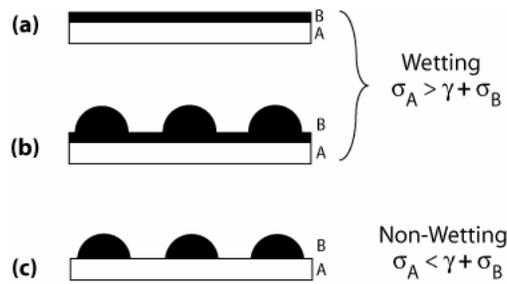


FIGURE 2.9: Heteroepitaxial growth modes in epitaxial systems. When surface energy of the substrate σ_A is greater than the sum of the surface energy of the deposited layer σ_B and the interfacial energy γ , the layer will wet the substrate and grow either in (a) Frank-Van der Merwe (layer-by-layer) mode or (b) Stranski-Krastanov (layer-plus-island) mode. Conversely, the deposited layer will immediately form exclusively islands in the characteristic (c) Volmer-Weber (island) mode.

In Situ Optical Reflectometry

Recent interest in fabricating semiconductor nanowire devices has spurred research related to controlling nanowire growth. Nanowire heterostructures require stringent control of growth parameters and their resulting electrical and optical properties are anticipated to enable valuable electronic, photonic, and sensing applications.⁴³ While many studies have investigated the final dimensions and orientations of semiconductor nanowires,^{18,19} there have been few studies of nanowire synthesis during growth.²¹ Such real time studies can greatly enhance the understanding of growth mechanisms and provide for the controlled fabrication of intricate heterostructured devices that otherwise may be difficult to achieve.

Previous research on laser annealing of amorphous Si and on *in situ* monitoring of layer thicknesses during chemical vapor deposition (CVD) point to the efficacy of *in situ* monitoring using optical reflectivity, both for understanding mechanisms of Si recrystallization⁴⁴ and for real time control of device structures.⁴⁵ In this work we demonstrate that optical reflectivity can provide real time measurement of nanowire growth processes. In combination with *ex situ* scanning electron microscopy, we apply the technique to the *in situ* study of Si nanowire growth and are able to quantitatively determine the incubation time for the onset of nanowire growth, the mean growth rate and the average nanowire length. The technique increases real time controllability of vapor-liquid-solid (VLS) growth, facilitates understanding of nanowire growth mechanisms, and promises utility for fabricating more complex nanowire heterostructures and devices.

The time-dependent reflectance of the incident light, together with knowledge of the wavelength, scattering geometry, and index of refraction for a growing layer, provide a direct measure of the layer growth rate. Starting from the Fresnel equations for reflection from a thin film⁴⁴ and including the absorptive properties of the film through the imaginary part of the complex index of refraction, we can simulate the optical reflectivity as a function of growth time as follows.

In order to simulate both the intensity decay and the oscillatory nature of the nanowire reflectivity spectrum, calculations of (1) the variance in the index of refraction and (2) attenuation constant for the effective nanowire layer were examined. Photon transport within a material is controlled by the complex index of refraction for the individual medium. As an

optical beam propagates through layers of materials having different refractive indices, it undergoes a reflection at each interface. For the case of silicon nanowires, we can assume the nanowires to behave as an effective thin-film layer, much in the same way we consider the optics of any single thin-film deposited on a substrate. Optical reflections will occur at both the vacuum-nanowire and nanowire-substrate interfaces, as shown in **Figure 2.10** below.

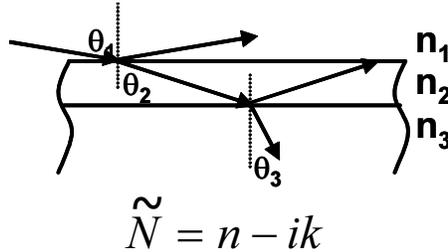


FIGURE 2.10: Laser beam reflection and transmission through the vacuum ($n_1 = 1.0$), the effective nanowire layer (n_2), and the Si substrate ($n_3 = 3.42$). $\theta_1 \sim 83^\circ$ in our experiments; Snell's Law determines the angles θ_2 and θ_3 (i.e. $n_1 \sin \theta_1 = n_2 \sin \theta_2$)

However, because the areal density of the growing nanowires tends to decrease initially with the length of the nanowires, the volume fraction of silicon within the effective layer varies as a function of nanowire length, h . As a result, within the effective nanowire layer the index of refraction also varies with the length of the nanowires, as predicted by a Vegard's Law type rule of proportions.^{46,47} Because the layer is composed of individual nanowires with vacuum (or air) in between, the volume fraction of silicon in the effective layer is not 100% as it would be in a continuous thin-film of silicon, but instead some fraction less than that, which varies as a function of the effective layer thickness. Vegard's Law, though typically used for alloy systems, states that the lattice parameter of an alloy can be calculated by taking a linear interpolation of the elemental constants. Similarly we can determine the index of refraction based on the volume fraction of silicon in the nanowire layer as a function of growth time, and extrapolate to allow the simulation to fit the maxima and minima reflectivity peaks seen in the data. From this fit we see a decrease in the silicon volume fraction of the virtual nanowire layer as the wires become longer, confirming that the nanowires are less dense further away from the surface.

To consider the optics of a single thin-film layer, we first recall that the plane of incidence is defined as the plane that contains both the normal to the surface and the portion of the incoming beam coplanar with the surface normal. The electromagnetic wave oscillating in the plane of incidence is denoted E_p and the electromagnetic wave oscillating normal to the plane of incidence is denoted E_s , as illustrated in **Figure 2.11**.⁴⁸ Both must be considered when examining the reflectance of the nanowire growth front as a function of time. The orientation of the polarized laser in relation to the sample surface establishes the amplitude of E_p and E_s , and specifically for these experiments, the plane of polarization for the 635 nm single-wavelength laser was $\phi = 36^\circ$ away from the plane of incidence.

Fresnel reflection coefficients are well defined for both E_s and E_p . For E_s normal to the plane of incidence the reflectance r_{12} for the air-nanowire interface and r_{23} for the nanowire-substrate interface are given by:⁴⁹

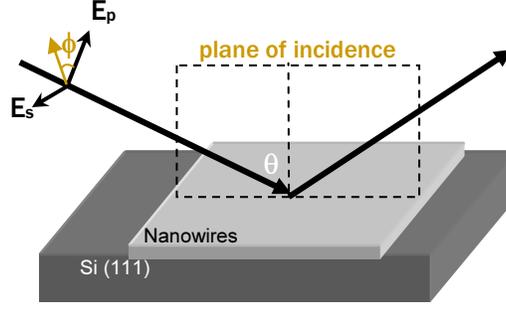


FIGURE 2.11: Sample-beam interaction of the reflected polarized laser beam.

$$r_{12}^s = \frac{n_1 \cos \theta_1 - n_2 \cos \theta_2}{n_1 \cos \theta_1 + n_2 \cos \theta_2} \quad \text{and} \quad (0.3)$$

$$r_{23}^s = \frac{n_2 \cos \theta_2 - n_3 \cos \theta_3}{n_2 \cos \theta_2 + n_3 \cos \theta_3} . \quad (0.4)$$

Similarly, the Fresnel reflection coefficients for E_p within the plane of incidence of the air-nanowire interface and nanowire-substrate interface are defined, respectively:

$$r_{12}^p = \frac{n_2 \cos \theta_1 - n_1 \cos \theta_2}{n_2 \cos \theta_1 + n_1 \cos \theta_2} \quad \text{and} \quad (0.5)$$

$$r_{23}^p = \frac{n_3 \cos \theta_2 - n_2 \cos \theta_3}{n_3 \cos \theta_2 + n_2 \cos \theta_3} , \quad (0.6)$$

where the relation between n_1, n_2, n_3 and $\theta_1, \theta_2, \theta_3$ are determined by Snell's Law ($n_1 \sin \theta_1 = n_2 \sin \theta_2$ and so on). n_1, n_2 and n_3 are the index of refraction of vacuum, the virtual nanowire layer, and the Si substrate, respectively, and θ_1 is the incident glancing angle.

Then, by defining an absorption coefficient, α , and a phase angle, β , for the light as it propagates through the media,

$$\alpha = \frac{2\pi}{\lambda} k \cos \theta_2 \quad \text{and} \quad (0.7)$$

$$\beta = \left(\frac{2\pi}{\lambda} n_2 \cos \theta_2 \right) \cdot h , \quad (0.8)$$

where k and n_2 are constituents of the complex index of refraction for the virtual nanowire layer. We can define equations for the reflectivity, R_s and R_p , as follows

$$R = |r|^2 \quad \text{so} \quad R_s = \left| r_{12}^s + r_{23}^s \right|^2 \quad \text{and} \quad R_p = \left| r_{12}^p + r_{23}^p \right|^2$$

$$R_s = \frac{r_{12}^{s^2} + r_{23}^{s^2} \exp(-2\alpha h) + 2r_{12}^s r_{23}^s \exp(-\alpha h) \cos 2\beta}{1 + r_{12}^{s^2} r_{23}^{s^2} \exp(-2\alpha h) + 2r_{12}^s r_{23}^s \exp(-\alpha h) \cos 2\beta} \quad (0.9)$$

$$R_p = \frac{r_{12}^{p^2} + r_{23}^{p^2} \exp(-2\alpha h) + 2r_{12}^p r_{23}^p \exp(-\alpha h) \cos 2\beta}{1 + r_{12}^{p^2} r_{23}^{p^2} \exp(-2\alpha h) + 2r_{12}^p r_{23}^p \exp(-\alpha h) \cos 2\beta}. \quad (0.10)$$

Using these two reflectivities we can simulate the data acquired by the laser as the light interacts with the growing nanowire layer to create interference patterns in the reflected laser intensity. For a polarization angle ϕ to the plane of incidence, $R = R_p \cos^2 \phi + R_s \sin^2 \phi$ for the simulated reflectivity as a function of layer thickness and growth time $h(t)$. By choosing a polarization angle intermediate between pure s- and p-wave scattering we exploit the phase difference between these signals to obtain increased sensitivity at the early stages of nanowire growth. However to achieve a proper match to the experimental data, variations in index of refraction and the damping coefficient with time are required, indicating that both parameters vary as the nanowires grow. Such simulations, including the reduction of index of refraction as a function of nanowire length, are shown in **Figure 2.12** for Si nanowires grown at 3×10^{-3} Torr and 400°C . The simulation is not able to identically match the experimental data due to diffuse scattering⁵⁰ from the rough nanowire surface, which was found to be difficult to model for this case. Hence, the detailed treatment of the diffuse scattering effects are not considered within this dissertation research.

The index of refraction, n_2 , in the simulations assumes a linear superposition of Si and vacuum values based on the volume fraction of Si present in the virtual nanowire layer. Starting with a linear growth rate obtained from the final nanowire layer thickness we fit the experimentally observed constructive and destructive interference peak positions in **Figure 2.12(a)** to infer the values for n_2 shown in **Figure 2.12(b)**, and the corresponding nanowire volume fraction and k_2 values which are included in the simulation in **Figure 2.12(a)**. The index, n_2 , is seen to decrease during the initial growth stage, suggesting a reduction in the volume fraction of nanowires with distance from the Si substrate, which is consistent with our analysis of the cross section SEM images. This initial reduction in the effective refractive index to a steady state value results from the initial interference between closely spaced nanowires due to the high density of Au seeds used in these experiments. Some of the nanowires do not continue growth due to inclined nanowires colliding into adjacent ones or to surrounding nanowires overgrowing smaller ones to starve them of available disilane flux.

Applications of this *in situ* optical reflectometry approach for monitoring and controlling nanowire growth can be extended beyond homogeneous nanowires. For example, the technique will be valuable for monitoring axial nanowire heterostructure growth due to the change in thickness of the nanowire layer and for core/shell nanowires due to the change in effective dielectric constant of the nanowire layer. Benefits of the reflectance monitoring include more precise control of the position of heterostructure interfaces within the nanowires.

In summary, the oscillations in reflectivity from a growing nanowire layer can be detected and used for real time *in situ* monitoring of nanowire nucleation and growth. Such measurements provide a convenient method to study nanowire growth mechanisms and kinetics, as well as offer the promise of improved ability to control the resulting structures for fabricating heterostructures and devices.

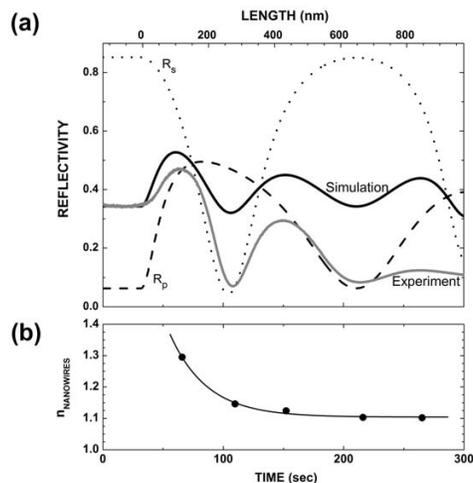


FIGURE 2.12: (a) Simulation and experiment for the optical reflectivity of growing Si nanowires as a function of time. Simulated results are shown for the incident polarization perpendicular (R_s) and parallel (R_p) to the plane of incidence and for the combined reflectivity at an experimental polarization angle of 37° . Diffuse scattering due to surface roughness and inhomogeneities in the virtual nanowire layer are not included in the simulations. (b) Index of refraction as a function of nanowire growth time determined by matching the maxima and minima between simulation and experiment.

Characterization Techniques

Field Emission Scanning Electron Microscopy

The field emission scanning electron microscope is the most efficient analytical technique used to characterize the nanowires created in these experiments. This method scans the surface of the sample with an electron beam in a raster pattern, similar to the raster scanning that occurs in classic cathode ray tube (CRT) television sets. Surface information is obtained by directing the trajectory of an electron beam systematically across the region of interest, and detecting the secondary or backscattered electrons emitted when the incident electrons interact with the sample. A detector collects the electrons as a function of scan position to form a magnified image of the sample surface.

Field emission scanning electron microscopy has the advantage of using an electric field to extract the electrons from a sharp filament tip, as opposed to lower resolution scanning electron microscopes that use thermionic emission as a source of electrons. Electrons are drawn from the filament tip by an intense potential field set up by an anode that lies beneath the tip of the filament. The electrons are then directed from a very small area of the pointed tip and proceed down the column, often this is aided by a second anode that lies beneath the first. The lost electrons are replenished by an electron source attached to the tungsten tip. A primary electron beam generated by a field emission source offers significant advantages over those produced by thermionic emitters used in conventional SEMs. Field-emission SEMs have a smaller initial spot size, typically less than 2 nm as compared to 4-8 nm for conventional SEMs, and a lower accelerating voltage, so a much smaller primary excitation zone is produced. This results in much greater resolution than is capable with a conventional SEM that uses hot tungsten or lanthanum hexaboride (LaB_6) as an electron source.

The surface sensitivity of the SEM depends on the imaging conditions and contrast mechanisms. Here nanowire samples are typically imaged with a working distance of 6.0 mm using a 15 keV beam at a 10 μ A beam current. Under these conditions it is expected that the secondary electrons are created with a beam penetration depth of approximately 10 nm.

Rutherford Backscattering Spectroscopy

Once deposited, thin-films of gold are analyzed for their thickness using Rutherford Backscattering Spectroscopy (RBS). This is a quantitative, non-destructive elemental thin film analysis technique which has the capacity to characterize thin-films compositions and thicknesses (and in fact, the technique can be used for discontinuous clusters on surfaces) by measuring the scattering intensity versus energy when high-energy ions interact with atoms of a solid sample.

The RBS analysis technique irradiates a sample with a collimated, monoenergetic beam of either He^+ or H^+ ions, as illustrated in **Figure 2.13**. As ions collide with surface atoms or penetrate the solid, they lose energy via nuclear collisions and coulombic interactions with the electrons of the sample's lattice atoms. In our measurements a detector with solid angle of 4 milliradians located at a backscattering angle (θ) of 170° collects the deflected particles and sends an electrical pulse corresponding to the energy of the detected particle to the data collection system. The energies create a histogram which is plotted as the counts (how many times the detector collected a particle of a particular energy) versus channel number (representing energy). By observing this spectrum of yield versus energy for the backscattered ions, one can make a quantitative measurement of the mass and areal density of particles present in the sample.

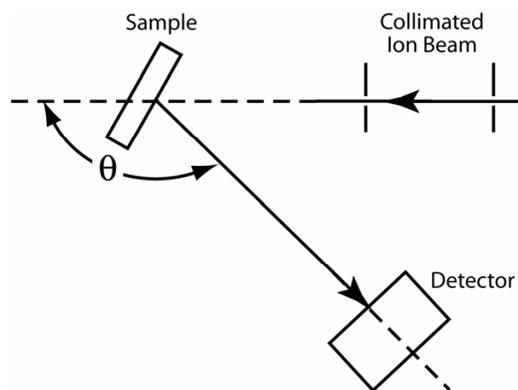


FIGURE 2.13: Beam geometry of the Rutherford Backscattering Spectroscopy (RBS) analysis method.

The ions scatter from the gold clusters on a silicon substrate at the (a) surface, (b) bulk Au, (c) Au-Si interface, and (d) bulk Si as shown in **Figure 2.14**. The total scattering yield within the Au peak of the resulting spectrum is proportional to the total number of atoms in the cluster material on the surface. However, because the analyzing ion beam is larger than the average cluster diameter by many orders of magnitude, the ion scattering profile for these discontinuous thin-films is also known to be dependent upon the cluster diameter distribution, the shape of the clusters (ie height to diameter ratio) – also known as the “cluster shape function,” and the detector resolution.⁵¹ Hence, for our purposes, we use the terminology ‘nominal’ to describe the

average areal density of gold atoms on the substrate in terms of some effective thickness in nanometers or angstroms. The thickness of the film can be determined from the width of the Au peak, ie, the number of channels. In our case the Au cluster thickness is usually small enough that the width of the Au backscattering peak is detector-resolution limited. The area of the peak is used to determine the absolute number of Au atoms per square centimeter and using the Au density, this number is converted to nominal Au thickness.

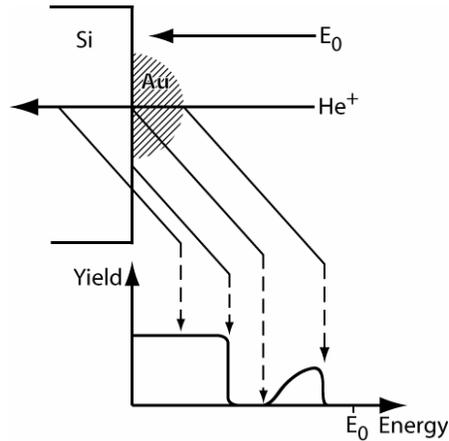


FIGURE 2.14: Energy spectrum produced by Rutherford Backscattering (RBS). Incident He^+ ions of energy E_0 scatter from the surface atoms of the substrate and the surface film (or clusters as illustrated here). The energy lost as the ion scatters from surface atoms is element-specific, depending on the basic energy loss as a result of ballistic collisions. Ions also penetrate deeper within the surface film or the substrate, and hence a depth-scale for each atomic species can be observed from the continuous energy loss recorded in the spectrum.

A quartz crystal rate monitor is used to determine the thickness of the *in situ* deposited gold. The rate monitor determined thickness was calibrated against areal Au density measurements from Rutherford backscattering spectroscopy to determine the tooling factor of the instrument. Tooling factor recalibrates the monitor to account for the geometric setup of the gold evaporation source relative to the sample position and the deposition monitor position. By simply comparing the ratio of measured film thickness, as determined by RBS, to the indicated thickness measured by the rate monitor at a given the tooling factor (TF_1), an updated tooling factor (TF) can be calculated, as denoted by the equations in **Figure 2.15**.

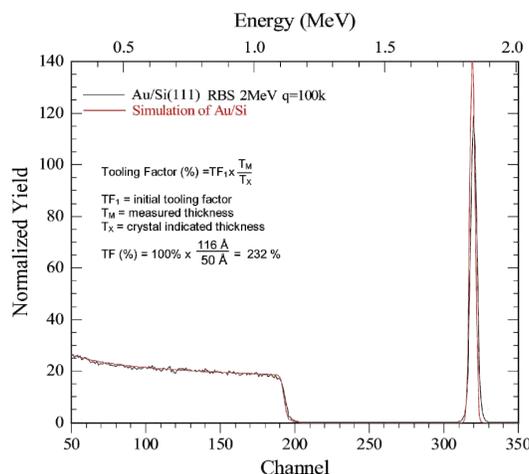


FIGURE 2.15: RBS spectrum to determine the deposited Au thickness; used to calibrate the quartz crystal rate monitor.

The facility for Ion Beam Analysis of Materials (IBeAM) at Arizona State University houses the RBS accelerator and sample measurement chamber. The convenient, fast load-lock and vacuum systems in the RBS system within the IBeAM facility make this an ideal method for rapid analysis of thin films.

Transmission Electron Microscopy (TEM)

The atomic scale analysis of the nanowire structures was achieved using transmission electron microscopy, a high-resolution tool that sends electrons through a thin sample of material, specifically to investigate the nanowire crystal quality and the interfaces for heterostructure samples. In a TEM, the primary electrons from an electron gun are focused onto the sample and are diffracted or scattered as they pass through it. An objective lens focuses the scattered electrons and a magnifying projector lens amplifies them so that they produce, for example, the lattice image of the sample on a phosphorus screen for digital recording, or on photographic film. Images form because different atoms interact with and diffract electrons to a different extent; samples that are too thin do not interact with the beam enough, those that are too thick experience multiple scattering events as the electrons pass through making the resulting image blurred and more difficult to analyze. Hence, care must be taken when creating the nanowire samples for TEM analysis, especially to not break off the nanowires during the preparation.

Cross sectional TEM samples were prepared by mechanically thinning the area of interest, then ion polishing the cross-section surfaces using a cold stage ion mill. The electron-transparent area of the thinned sample is then analyzed with high energy electrons, typically up to 400 kV, to form an image of the sample with atomic resolution, as illustrated in **Figure 2.16**. For strain mapping of nanowires using the TEM micrographs, the nanowires were aligned and imaged along their $\langle 110 \rangle$ direction, ie, so that the primary beam is parallel to the $\langle 110 \rangle$ direction. All the nanowires analyzed in this study via TEM were imaged using high-resolution transmission electron microscopy capabilities in the LeRoy Eyring Center for Solid State Science at Arizona State University.

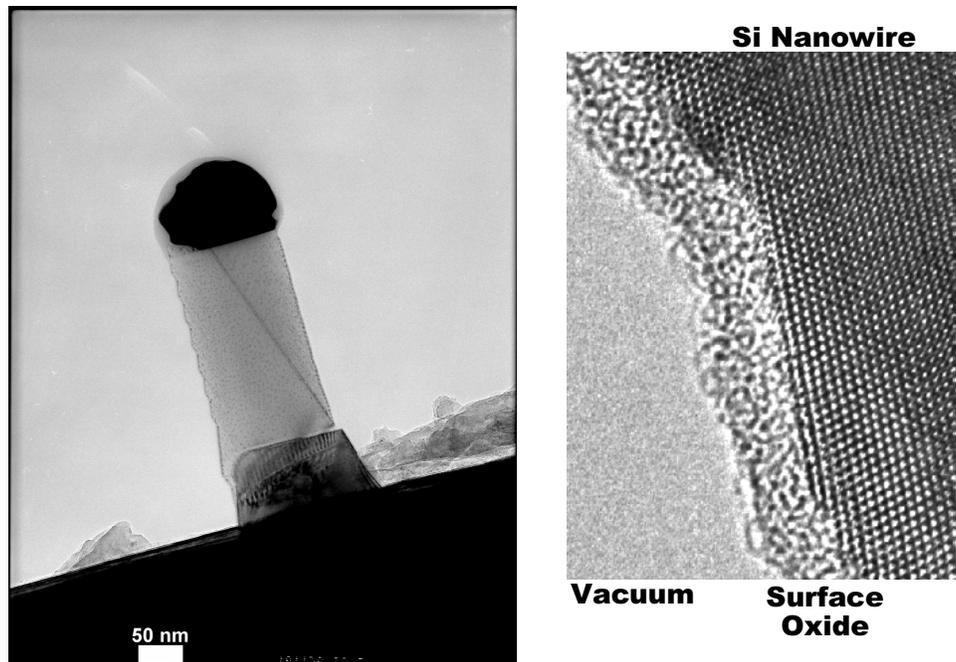


FIGURE Figure 2.16: Transmission electron microscopy image of a silicon nanowire, illustrating the atomic scale resolution for nanowire samples grown using 0.5 nm Au deposited at 250°C and annealed for 5 minutes at 600°C followed by nanowire growth with silane precursors at 45 mTorr and 470°C for 6 minutes.

Strain Measurement using High-Resolution TEM

One-dimensional heteroepitaxial materials, such as nanowires, are advantageous for their ability to incorporate materials not previously possible by their counterparts: laterally-confined, two-dimensional, planar heterostructures. Thus greater lattice mismatch can be accommodated through pseudomorphic growth without defect introduction, since strain sharing between layers can occur and the nanowires can relax laterally at relatively short distances from the heterostructure interfaces. Strain distribution analysis near the heterointerfaces will be necessary at very small length scales to define the limits of strained one-dimensional heterostructure growth.

Controlled introduction of strain via heterointerfaces allows the tailoring of the electronic properties of semiconducting nanowires, and this strain introduction is specifically interesting for its band gap manipulation capability. Using finite element modeling, we are able to quantitatively correlate the strain state of Si and Ge nanowires, Si/Ge core/shell nanowires, or Si/Ge axial nanowires measured using a novel 2-D strain mapping technique. Various heterostructures within the semiconducting nanowires exhibit interesting strain states, and hence an interesting change in the band structure for potential nanoscale devices. Thus, developing experimental techniques for mapping the strain in nanowires is of considerable potential interest.

An illustration of the strain-mapping technique as developed for nanowire characterization is shown in **Figure 2.17** for a Ge nanowire grown epitaxially on Si(111) substrate. The technique begins with a high resolution transmission electron microscope (HR-TEM) image. Geometric phase analysis (GPA), a process which measures deformation of a lattice with respect to a given reference in order to analyze variations in strain in nanostructures, uses the HR-TEM micrograph and fast Fourier transform (FFT) routines⁵² to determine quantitative strain components for ϵ_{xx} ,

ε_{yy} , ε_{xy} , the mean dilatation, and the rotation of the lattice planes within the nanostructure. Performing a FFT of the initial HR-TEM image calculates the local Fourier components, then selecting one of the peaks in the FFT image using a Lorentzian mask (here we choose the (111) peak), a phase image is produced that is highly sensitive to the lattice plane spacing. To obtain accurate strain maps it is important to correct the phase images for electron optical aberration distortion originating from the microscope. This is accomplished by imaging a perfect Si crystal under the exact same conditions, and then effectively subtracting the Si phase image from the original phase images. Combining these corrected phase maps, quantitative determination of the local lattice distortion can be completed. Taraci et al., in our group explored the resulting 2D strain maps in depth^{52,53} and identified the strain information which could be obtained in studies of homogenous semiconducting nanowires, as well as Si/Ge core/shell nanowire heterojunctions. We are currently applying this technique to examine the strain induced in axial nanowire heterojunctions.

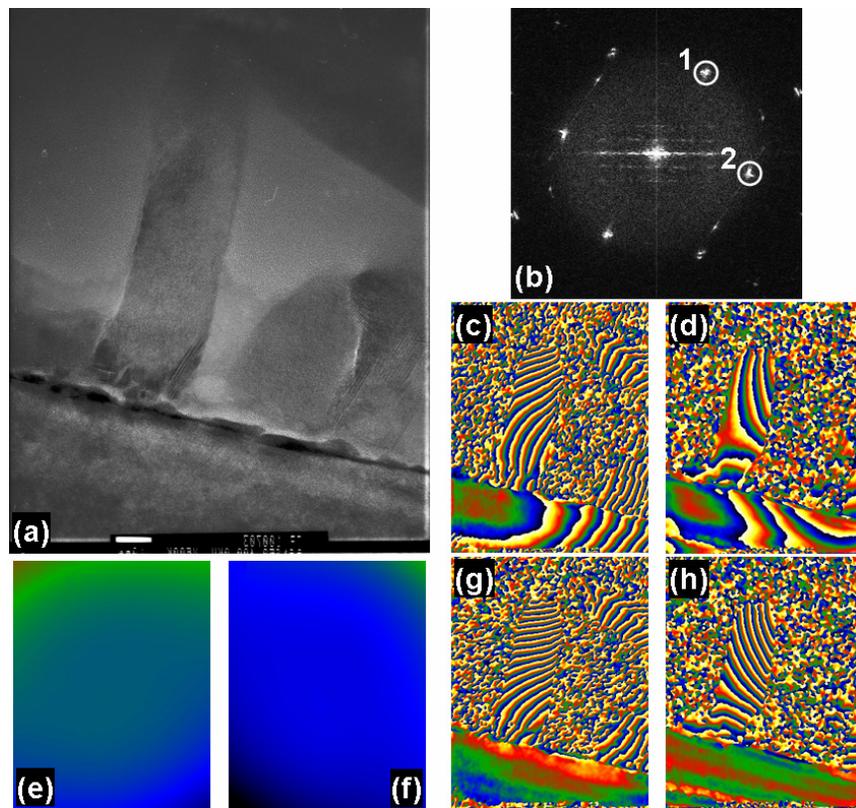


FIGURE 2.17: (a) Digitized HR TEM micrograph used to demonstrate the strain mapping technique. (b) FFT of the entire micrograph shown in (a). Circles 1 and 2 identify the mask areas around the two (111) peaks used to extract the phase images. (c-d) Phase images resulting from the inverse FFT calculation of circle 1 and circle 2 in (b), respectively. (e-f) Two phase images illustrating the phase variation due to the projector lenses aberrations. These images were taken using a perfect Si crystal under imaging conditions identical to those used to obtain (a) and were used to correct the Ge NW phase maps in (c-d). (g) Corrected Ge NW phase map, this is the result of correcting the image shown in (c) for microscope optical distortions. The correction is apparent by observing the smoothness of the Si substrate. (h) Second corrected phase image corresponding to the inverse FFT calculation of circle 2. The colors in the phase images vary from blue (dark if printed in grayscale) to yellow (light) which represents a change between $-\pi$ and $+\pi$.

Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a physical technique used to image and measure sub-nanometer feature dimensions on the sample surface, features such as coalesced thin-film gold clusters for these studies. A small AFM probe tip scans across the sample surface to produce height images of the surface. The tip is mounted on a cantilever from which a highly focused laser beam reflects; as the tip and cantilever bend in response to the sample surface features, the laser beam is deflected into different quadrants of the photodiode detector. Software provided with the microscope records the laser deflection as a function of position on the sample to create a three-dimensional array of points representing the sample height as a function position.

Two working modes of AFM are contact-mode and tapping-mode. Maintaining a constant force between the probe and the sample, contact mode keeps the probe-tip in direct contact with the sample at all times. This is accomplished by a feedback loop in the software that determines from the deflection information of the laser beam whether to move the tip closer to or further from the sample in order to maintain a constant force between the tip and surface. Alternatively, tapping mode oscillates the cantilever at its resonant frequency and maintains constant oscillation amplitude by varying the height of the tip from the sample, again accomplished through the software feedback loop. Tapping mode AFM images constitute the entirety of the AFM work shown in this dissertation.

Measurements of gold cluster heights and morphologies for these studies taken from AFM images such as that shown in **Figure 2.18** allow us to better understand the evolution and coarsening of catalytic metal seeds deposited on clean Si substrates; this subject will be discussed in a later section.

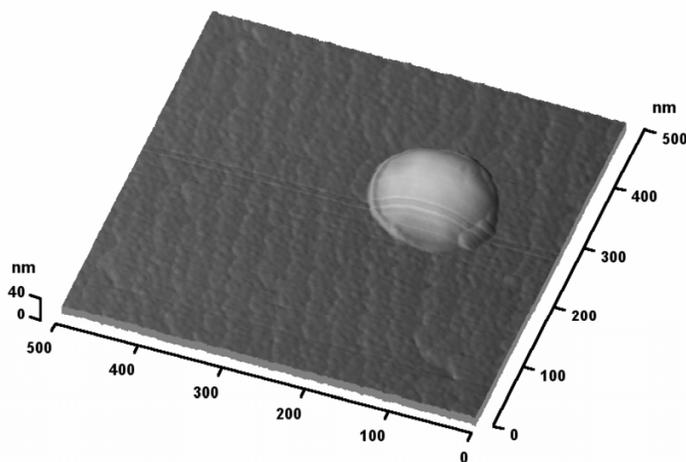


FIGURE 2.18: Height information for a gold catalytic seed prior to nanowire growth imaged using atomic force microscopy in tapping force mode.

SI AND GE NANOWIRE GROWTH

Au Nanocluster Morphologies

Central to the vapor-liquid-solid mechanism for the synthesis of nanowires is the aggregation of small atomic clusters which produce catalytic seeds for nanowire growth. These small clusters exhibit the same properties as their corresponding bulk phases, except that at such atomic size scales the surface-to-volume ratio of these clusters is relatively large, and hence a considerable contribution to the Gibbs free energy comes from the cluster's surface energy. For the very small dimensions ($d_{\text{wire}} < 50 \text{ nm}$) and extremely high supersaturations of our nanoclusters, the atomistic theory of nucleation becomes valid.

Simplistically, a freestanding particle can nucleate within a liquid phase when the liquid cools to below its melting temperature, because the energy associated with the crystal structure of the solid is less than that of the liquid. The difference in Gibbs free energy between the solid and liquid phases is known as the volume free energy, ΔG_v , which increases as the amount of solid increases. Also, the interface created between the solid nucleus and the liquid surroundings maintains a surface free energy σ which increases with particle surface area. Combining the volume free energy and the surface free energy, the total change in free energy of

$$\Delta G = \frac{4}{3} \pi r^3 \Delta G_v + 4\pi r^2 \sigma \quad (0.11)$$

where the first term incorporates the volume and the second term incorporates the surface area of the spherical nucleus.

This simple representation becomes more complicated for cluster nucleation on a solid substrate from the vapor phase, instead of the liquid phase; the Gibbs free energy for vapor deposition of thin films is used here as an approximation to our thermal evaporation of Au to form nanoclusters. Several factors affect nanocluster nucleation time, specifically of concern are surface diffusion, Ostwald ripening of clusters, and the Gibbs-Thompson theory on increased energy contribution at small cluster diameters.

Surface Diffusion

The migration of individual atoms across solid surfaces and their aggregation into clustered nuclei are among the most fundamental interactions in surface science.⁵⁴ A detailed understanding of these basic processes becomes even more important as we attempt to control the growth of semiconducting nanowires, specifically the nanowire diameters which are governed by the catalyst nanocluster diameter. The fabrication of these nanostructures by the VLS mechanism requires an atomic-level understanding of surface diffusion of the catalytic seed atoms and substrate adatoms across the surface.

Fundamental surface processes such as surface diffusion, adsorption, and desorption define the kinetics for clustering on surfaces, and these three dynamic clustering processes are functions of temperature and deposition rate. Adatoms migrating on an atomically clean sample surface have a characteristic surface diffusion coefficient, which is determined by the diffusion activation energy, as described by the equation

$$D = \frac{va_o^2}{4} \exp\left(\frac{-E_d}{k_B T}\right), \quad (0.12)$$

where E_d is the diffusion activation energy and v is the characteristic vibrational energy of the surface atoms. a_o , k_B , and T have their regular meanings: substrate lattice constant, Boltzmann's constant, and substrate temperature respectively. Effectively the surface diffusivity coefficient increases with increasing temperature and decreases when the coordination of the mobile surface adatom increases – for example, when the adatom bonds with other atom(s) on surface steps or within clusters.

The surface diffusion length, $l = \sqrt{Dt}$, where D in our case is the characteristic surface diffusion coefficient of gold adatoms on the silicon substrate, shows that longer diffusion distances occur with longer average diffusion times or with an increase in diffusion coefficient. Consider the case where a monolayer of gold is evaporated on a substrate at elevated temperature; because the diffusion length depends on the allowed time for diffusion, the rate of deposition becomes critical. For high deposition rates, the adatoms deposited have less time to diffuse on the surface before encountering other atoms and with the higher resulting surface concentration nucleation events increase. Hence the short diffusion lengths before collisions causes a high density of clusters on the surface (similar effects occur as a result of low deposition temperatures, as this decreases the diffusion coefficient). Alternatively, at low deposition rates or high substrate temperatures, the Au atoms have more time to diffuse over a larger area, effectively causing a lower density of clusters on the surface. Surface diffusion of Si adatoms and ad-dimers (a dimerized pair of adatoms) originating from the substrate are also shown to affect the nucleation and growth of semiconducting nanowires, and is a topic of discussion in a later section.

Gibbs-Thomson Effect

In the 1920s, Gibbs theorized a limit to the smallest sized liquid cluster which could nucleate solid particles. This later led to what is now known as the Gibbs-Thomson effect, which is a thermodynamic phenomena characteristic of clusters that arises from surface tension, and is an especially important topic of note for surface deposited objects such as clusters, water, and quantum dots.⁵⁵ This effect is traditionally illustrated for a liquid cluster of radius r and surface tension γ , where thermodynamic arguments find that the cluster's curved surface exerts a pressure $2\gamma/r$ on the interior of the cluster. It is worth noting in fact, that the pressure induced by this surface tension in very small clusters can also have an effect on the binary phase diagram of alloys.⁵⁶ A gas which is in equilibrium with the cluster will have a vapor pressure given by

$$P(r) = P_{\text{bulk}} \exp\left(\frac{2\gamma v_m}{rk_B T}\right), \quad (0.13)$$

where P_{Bulk} is the vapor pressure above a supposed flat liquid surface. The cluster's chemical potential is then given by

$$\mu_r = k_B T \ln\left(\frac{P(r)}{P_{\text{bulk}}}\right) = \frac{2\gamma v_m}{r}, \quad (0.14)$$

where v_m is the atomic volume in the liquid cluster. Hence, the smaller clusters have a higher chemical potential and a higher vapor pressure than larger clusters, giving rise to the ripening phenomena in which larger clusters grow at the expense of smaller ones.

Upon heating, the deposited cluster will form a liquid on a surface in the shape of a spherical dome with a contact angle θ that depends on the surface tensions of the various interfaces: vapor-liquid (VL), liquid-substrate (LS), and substrate-vapor (SV), as illustrated in **Figure 3.1**. The angle θ is given by Young's equation: $\gamma_{SV} = \gamma_{LS} + \gamma_{LV} \cos \theta$. When $\theta = 0$, the liquid completely wets the surface; there are no droplets. For $0 < \theta < \pi$, the liquid partially wets the surface. The contact angle θ for the cluster can also be a function temperature and composition of the cluster. Such variations in contact angle lead to variation in nanowire growth, as will be described in subsequent sections.

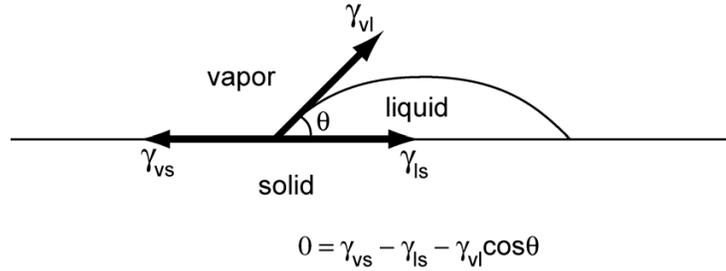


FIGURE 3.1: Three-phase equilibrium schematic for wetting of a surface by the liquid seed droplet, where γ_{vl} represents the liquid-vapor surface tension and γ_{ls} , and γ_{vs} represent the liquid-solid and vapor-solid interfacial energies, respectively.

The application of this theory to nanowire axial growth rate, as explained by Givargizov originally,⁸ hypothesized that nanowires of larger diameter grow faster in length than small wires. This predicted reduction in growth rate at smaller diameters is the result of the increased free energy of the liquid seeds at very small diameters requiring a higher partial pressure for similar supersaturation of the growth species and thus similar growth rates. However, Givargizov's theory dealt with group IV semiconductor whiskers of diameters up to three orders of magnitude larger than contemporary nanowires; today's experiments with smaller diameters tend to show differing behavior and constant, decreasing, and even increasing growth rates with nanowire diameter have been reported, depending on the detailed growth conditions. In fact the growth rate will depend on the rate limiting step in the growth kinetics which may occur at the vapor-liquid or liquid-solid interface and is not well understood at present. However, for sufficiently small nanowire diameters, possibly below those commonly grown at present, the Gibbs-Thomson effect would be expected to become a limiting factor in the growth rate. Also, because the Gibbs-Thomson effect defines the thermodynamic equilibrium vapor pressure of small particles as a function of their size, the melting point of nanoparticles decreases with nanocluster radius, as shown in **Figure 3.2**.⁵⁷

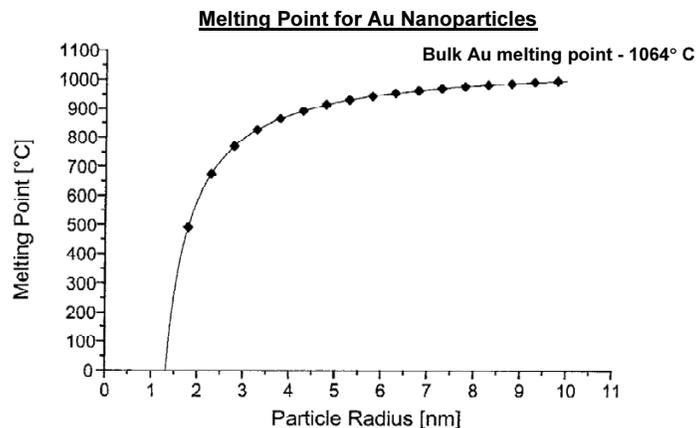


FIGURE 3.2: Calculated melting point for Au nanoclusters of varying radius from Ref 57.

Ostwald Ripening

The continuous attachment and release of Au atom from clusters at elevated temperatures and the net diffusion of adatoms from smaller Au clusters across atomically clean surfaces to larger Au droplets follows a process known as Ostwald ripening. It is driven largely by the Gibbs-Thompson effect described above. The process leads to a distinct size-distribution of nanocluster seeds on the substrate for given deposition parameters, i.e. substrate temperature, impinging atom flux during deposition, surface cleanliness, etc. Ripening can also occur subsequent to deposition during high temperature annealing. Essentially, Ostwald ripening is the coarsening of the cluster size distribution with the associated increase in mean cluster diameter to larger sizes.

Recently it has even been shown that for excessively clean surfaces, Au atoms within small-diameter Au-eutectic seeds atop nanowires can diffuse down their nanowire sidewalls during the nanowire growth process, migrate across the substrate surface to neighboring larger-diameter nanowires, diffuse up the sidewall of said nanowire, and reabsorb into the larger metal-eutectic seeds atop the larger nanowires. This can effectively eliminate small-diameter nanowire growth due to the loss of catalytic eutectic seed, at the benefit of the larger nanowires.⁵⁸ However, it is worth noting that the reported experiments, where this coarsening of the Au seeds during nanowire growth was demonstrated were carried out at extreme growth conditions: high temperatures and extremely low disilane partial pressures, and thus at very slow nanowire growth rates within the highly clean surfaces of an ultra-high vacuum. For our growth temperatures and pressures as well as those typically used by others, this previously observed coarsening during the total nanowire growth time would be negligible. Thus while Au migration certainly plays a vital role during the deposition and coalescence of seeds prior to nanowire growth, such migration is not expected to impact the nanowire growth in our investigations, appropriately high growth rates and median temperatures were used in all our studies to ensure this is the case.

Controlling Catalytic Seed Morphology

Our preliminary investigations of Au vapor deposited for cluster formation showed surface diffusion on silicon (111) and (100) surfaces being hindered greatly by the presence of surface contamination such as residual native oxide layers, and as such, resulted in a wide distribution of nanocluster diameters (see **Figure 3.3(a)**). Au deposition was carried out in an *ex situ* high-vacuum chamber via thermal evaporation, base pressures of 1×10^{-8} Torr, onto an *ex situ* cleaned

silicon substrate to remove native oxide and retain a hydrogen-passivated surface. The substrate cleaning method included rinsing the substrates in acetone for 10 minutes followed by methanol for another 10 minutes. Substrates were then etched with a 1:10 buffered 48% hydrofluoric acid (HF) in deionized water solution for 10 minutes and dried under flowing nitrogen. Samples were deposited with thermally evaporated Au of nominal thicknesses ranging from 0.3 to 2.5 nm and at elevated substrate temperatures of 300–550°C to allow the self-assembly of Au nanoclusters on the surface. The rate of deposition, temperature, and any pre-existing heterogeneous nucleation sites determine the density and size of the metal clusters.⁵⁹ A low flux of Au was maintained (just below 0.2 nm/min) in order to create a lower density of Au nanoclusters, with the resulting density primarily limited by heterogeneous nucleation. Subsequent analysis via Rutherford backscattering spectroscopy (RBS) (**Figure 3.3(b)**) provides an actual thickness for the non-continuous Au film of 1.6 nm and indicates some surface oxide remains for the example as shown in **Figure 3.3**.

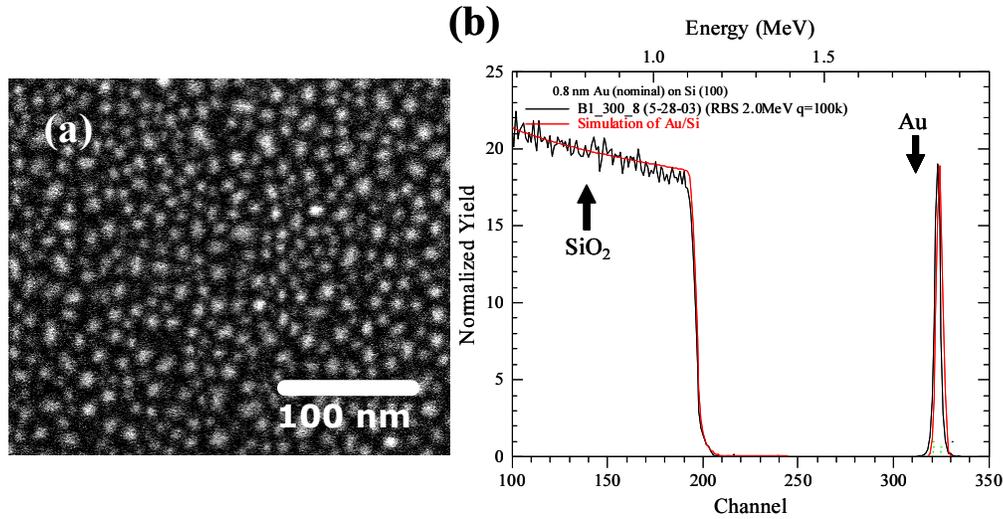


FIGURE 3.3: (a) Heterogeneously nucleated Au nanoclusters, formed by thermal evaporation on a Si(100) substrate at 300°C, effective thickness 1.6 nm, deposition rate 0.2 nm/min, imaged by field emission scanning electron microscope. (b) RBS measurement of effective Au thickness, also indicating some surface oxide.

Nanocluster nucleation and coalescence during evaporation is governed most strongly by the average time an adatom diffuses on the substrate (t_s), but we find that coalescence is only incidentally affected by the substrate temperatures for these *ex situ* deposited films. The surface diffusion length, $l = \sqrt{D_{Au-Si} t_s}$, where D_{Au-Si} is the surface diffusion coefficient of gold adatoms on the silicon substrate, provides for longer diffusion distances with longer average diffusion times. Thicker film deposition, nominally 2.5 nm as opposed to 1.5 or 0.8 nm, allows more time for surface diffusion to occur, hence the agglomeration of larger nanocluster seeds results, as shown in **Figure 3.4(a)**. Similarly, higher substrate temperatures facilitate an increase in surface diffusivity, and hence the nanoclusters seed particles become enlarged and more dispersed at higher temperatures than at lower temperatures for a given nominal thickness, this is illustrated in part (b) of **Figure 3.4**.

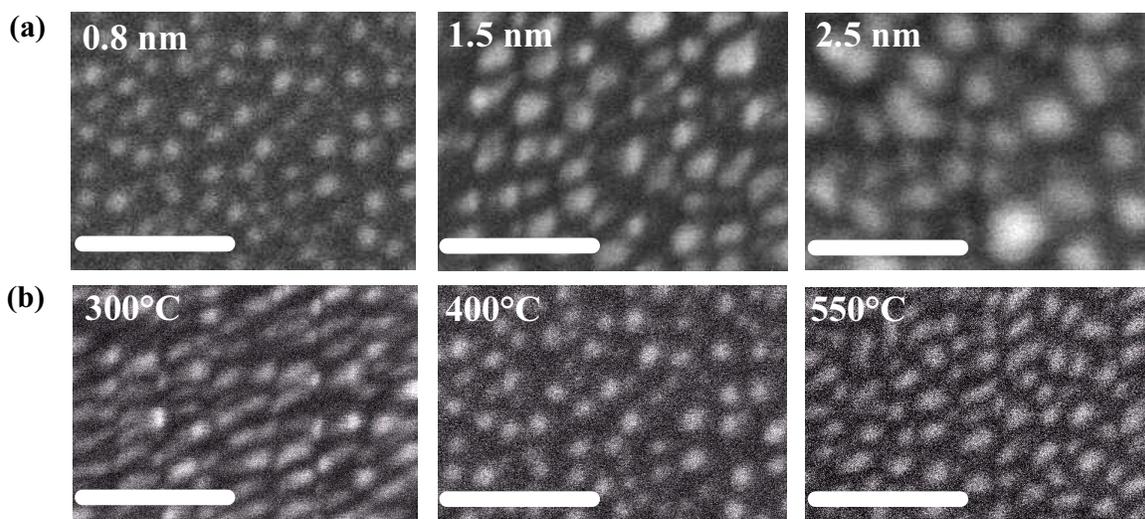


Figure 3.4: (a) Thickness dependence on nanocluster diameter and surface distribution; nominally thicker films create larger nanoclusters with a wide distribution of diameters, all deposited at 550°C. (b) Temperature dependence of Au nanoclusters, all deposited at 0.8 nm nominal thickness. All scale bars = 50 nm.

The relatively disorderly distribution of these deposited Au films, especially as a result of the inability to successfully remove the entire surface oxide during pre-clean and the unpredictable oxidation surrounding the Au nanoclusters during transport from the Au deposition chamber to the UHV nanowire growth chamber, indicated that depositing catalyst seeds *in situ* would improve cluster reproducibility for nanowire growth.

To that end, a thermal evaporation source was fabricated for use within the UHV-CVD nanowire growth chamber to facilitate Au deposition *in situ* on atomically pristine silicon surfaces at elevated temperatures. **Figure 3.5** illustrates the results obtained for Au catalyst seeds formed in ultra high vacuum with no oxygen surface contamination.

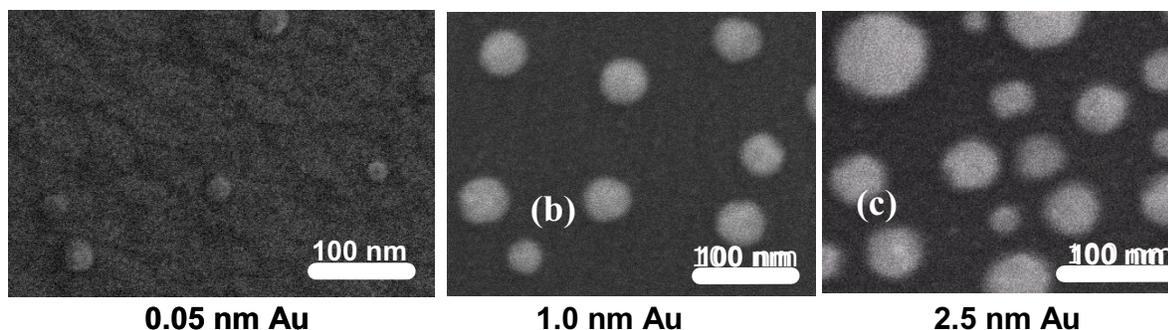


FIGURE 3.5: Au nanoclusters on atomically clean Si(111), in situ deposited at 250°C to nominal thicknesses (a) 0.05 nm, (b) 1.0 nm, and (c) 2.5 nm, as imaged by field emission scanning electron microscope (a & b), and by atomic force microscope (c).

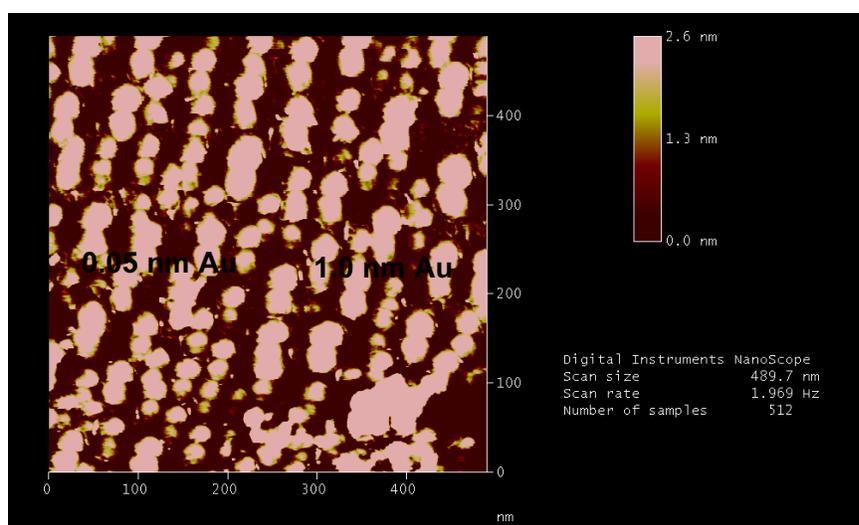


FIGURE 3.6: Atomic force microscopy of 1.0 nm gold seeds deposited *in situ* at 250°C.

Conditions of nanocluster formation by vapor deposition determine the ultimate diameter of the catalytic seed; variables to tune this diameter include deposition temperature, deposition rate, and nominal thin-film thickness.

***In Situ* Studies of Semiconductor Nanowire Growth using Optical Reflectometry**

Nanowires of Si and Ge were grown by the VLS method in a CVD cold-wall ultra high vacuum system (base pressure 1×10^{-10} Torr). Si (111) substrates were first cleaned in the growth chamber by resistive heating to 1250°C to remove the native oxide, followed by *in situ* thermal evaporation of 1.0 nm of Au at 250°C to form self-assembled Au nanoclusters with diameters of 10 to 50 nm in intimate contact with the Si surface. Nanowires were then grown using disilane or digermane precursors at pressures between 3×10^{-4} and 3×10^{-3} Torr at a substrate temperature of 400°C. Optical reflectivity was monitored during growth using a linearly polarized 635 nm diode laser and Si photodiode mounted on the exterior of the CVD reactor on viewports at 180° directly opposite each other with the incident laser beam at a glancing angle of 8° relative to the substrate surface and with a polarization angle $\sim 37^\circ$ relative to the plane of incidence.

In **Figure 3.7(a)**, the observed oscillations in optical reflectance are shown as a function of Si nanowire growth time for three different runs. The growth conditions were identical and the runs were stopped at different times as indicated by arrows A, B, and C and the corresponding field-emission scanning electron microscopy (SEM) cross-section images are shown in **Figure 3.7(b-d)**. The oscillation in reflected intensity with growth time is due to the alternating constructive and destructive interference between light reflected from the bulk Si substrate/nanowire interface and the advancing nanowire/vapor interface, providing a direct measure of the rate of growth and resulting thickness of the nanowire layer. We also observe in **Figure 3.7(a)** an initial time (labeled t_i) during which there is no change in reflectivity, corresponding to an incubation time prior to the onset of nanowire growth. This incubation time varies only slightly from run to run, and when aligned for the same starting time of nanowire growth as was done in **Figure 3.7(a)**, we see that the real-time reflectivity data overlay nearly perfectly. By stopping the growth at three different times along the reflectivity plot, we have monitored the growth rate while independently determining the length of the nanowires by cross-section SEM at multiple points during growth. The SEM observed average length of the nanowires divided by the optically determined growth time (total time minus the incubation time) reveals a somewhat higher growth rate during the early stages of growth with the initial growth rate (at 30 sec) of ~ 6 nm/sec decreasing to ~ 4 nm/sec at long times. This apparent initial decrease in nanowire growth rate varied from sample to sample and was not investigated in detail in these studies.

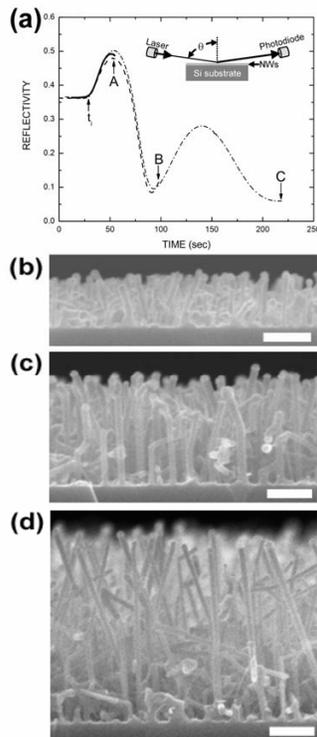


FIGURE 3.7: Optical reflectometry observation of nanowire growth. (a) Time variation of the reflected light intensity during VLS growth of Si nanowires for 3×10^{-3} Torr disilane at 400°C for three separate growth runs extending to times indicated by arrows A, B, and C. (b)-(d) SEM cross sections for runs A, B, and C respectively corresponding to nanowire virtual layer thicknesses of 201 ± 35 nm, 396 ± 75 nm and 651 ± 135 nm. White scale bar in (b)-(d) is 200 nm.

In **Figure 3.8** the reflectivity vs. growth time is shown for disilane pressures ranging from 3×10^{-4} to 3×10^{-3} Torr. The expected increase in growth rate with increasing precursor pressure⁶⁰ is apparent from the more rapid oscillations in the reflectivity at higher pressures. The incubation time, t_i , for the onset of nanowire growth is seen to decrease with increasing pressure as indicated by arrows a-c. The resulting incubation times for the onset on nanowire growth, 30, 47, and 68 sec for 3.0, 1.0 and 0.3×10^{-3} Torr, are shown by the inset in **Figure 3.8**. Comparable incubation times have been previously reported in one study for growth from silane, although the pressures were not reported in that study.⁶¹

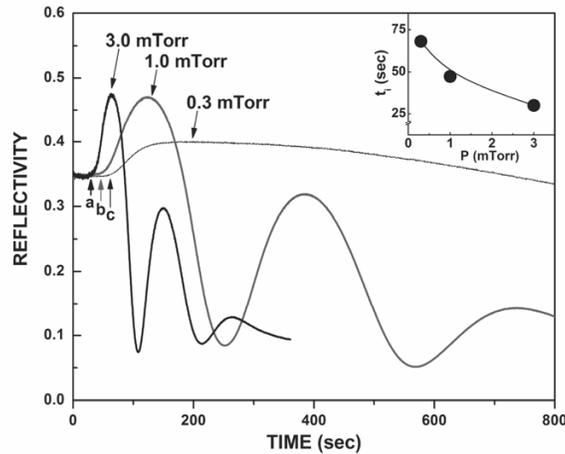


FIGURE 3.8: Optical reflectivity vs. growth time at 400°C for disilane pressures of 3.0, 1.0, and 0.3 mTorr with the incubation times for growth indicated by the arrows a, b and c, respectively.

In the VLS technique two sequential stages are proposed for nanowires to nucleate from the substrate. First, as Si is incorporated into the surface, the metal seed must be converted from solid phase Au to a molten AuSi eutectic phase by propagation of a liquid AuSi/solid-Au interface through the seed; we associate this process with a eutectic formation time, t_e . Second, sufficient supersaturation of Si in the liquid eutectic droplet due to the gaseous disilane overpressure must occur to initiate formation of a nanowire from the substrate surface; we associate this with a nucleation time, t_n . Our measured incubation time $t_i = t_e + t_n$. To estimate t_n we turned the resistively heated Si substrate temperature off at an intermediate stage of nanowire growth in the presence of disilane and then after a period of time back on again for continuation of nanowire growth, but now without the need to nucleate the nanowires. The observed time to resume growth, 15 sec, provides a measure of the eutectic formation time (assuming that the seed particle is depleted of Si during cooling) and also corrects for the thermal time constant of the system. Subtracting this value from the incubation times of Figure provides nucleation times ranging from 15 to 50 sec with decreasing pressure, and suggests the presence of a nucleation barrier. The existence of a barrier is consistent with an excess energy required to initially form a small pillar with the liquid eutectic droplet wetting the pillar top rather than a flat surface. Arguments based on the energy to form a critical height to nucleate nanowires have also been advanced for ZnSe to explain the observed change in growth direction with nanowire diameter.⁶²

Nanowire Growth Morphologies and Kinetics

Ge and Si nanowires grown on Si (111) substrates are routinely fabricated in our UHV CVD chamber using silane, disilane, and digermane sources, as previously reported.^{17, 18} Although our initial investigations dealt exclusively with disilane and digermane precursor gases, the majority of other researchers utilize silane and germane for nanowire growth. Disilane is generally known to be more reactive than silane;⁶³ This greater reactivity of the dimolecular species versus the molecular species is consistent with our observation that disilane and digermane result in nanowire growth at lower pressures and temperatures than silane and germane, respectively. This section describes our observations of the variation in nanowire growth kinetics using these four most commonly used Si and Ge precursor gases: disilane, silane, digermane and germane.

Disilane Nanowire Morphologies

Disilane has been found to be highly reactive and to readily produce high quality nanowires as compared to the other gases used in these studies. Nanowire growth has been observed within the temperatures between 400-600°C and pressures between 3-15 mTorr in these studies. **Figure 3.9** illustrates the effect of nanowire growth temperature on the morphology of SiNWs. High aspect ratio, uniform, non-tapered nanowires are observed to grow without kinks along the $\langle 111 \rangle$ orientations at lower growth temperatures of 400°C. Note that the orientation of the nanowires are consistent with the growth being seeded epitaxially from the Si(111) substrate. At higher temperatures, one observes growth instabilities at the liquid-solid interface, resulting in the abrupt change of the growth direction along individual nanowires (kinking) between the available $\langle 111 \rangle$ orientations. At the highest growth temperatures (600°C), in addition to kinking, strong faceting is observed on the nanowire surfaces. Smooth side-wall nanowires such as those grown at 400°C would be highly desirable for electronic device applications. Strong faceting with high temperature growth would be expected to strongly scatter long-wavelength phonons, with possible thermoelectric applications.

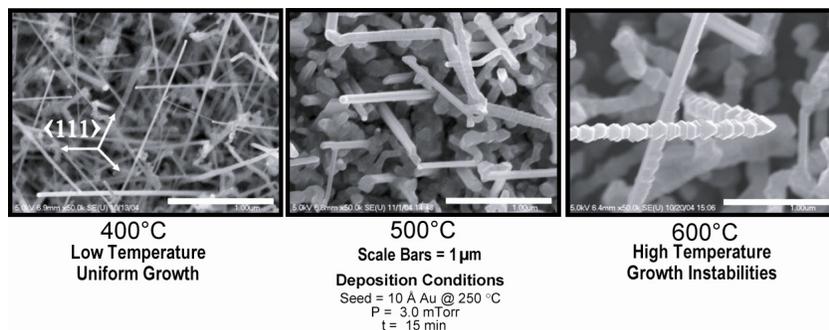


FIGURE 3.9: Disilane nanowire growth morphologies as a function of temperature after fifteen minutes at pressures of 3.0 mTorr. Lower temperatures result in uniform growth, whereas higher temperatures induce defects, kinking, and surface faceting in the nanowires.

Analysis by high resolution transmission electron microscopy indicates at high temperatures stacking faults are induced along the nanowire length, with the number of stacking faults increasing with temperature. Such stacking faults are often located at the kinks and may account for the change in growth direction. The highly-faceted structure and (111) stacking faults are shown in **Figure 3.10**. Note from the HRTEM micrographs the dark spots on the (111) faceted sidewalls of the SiNW. These spots are inferred to be Au clusters released from the

catalytic Au-Si liquid seed situated atop the growing nanowire. However, the tiny cluster sizes did not allow definitive identification by electron diffraction. The small Au clusters, stacking faults, and faceting are all indicative of instability at the liquid-solid growth interface during high temperature growth. The increased surface roughness, stacking faults and other defects observed at higher growth temperatures would result in reduced mobility within the structure, making high temperature disilane growth unfavorable for electronic nanowire device applications.

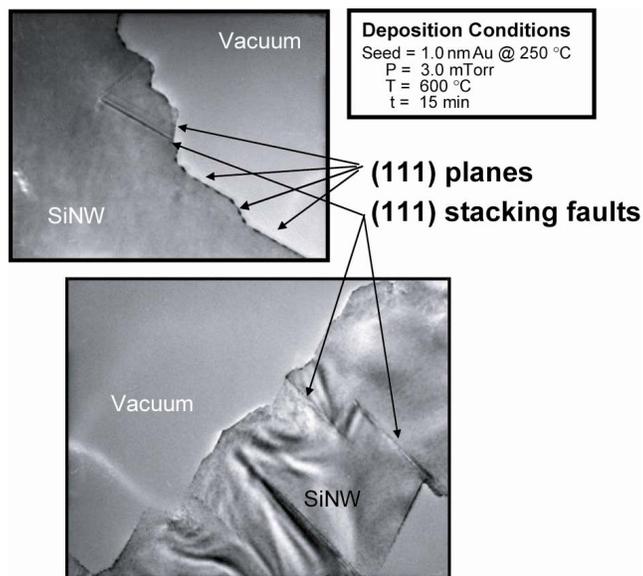


FIGURE 3.10: Transmission electron micrographs of silicon nanowires grown at high temperatures (600°C) illustrating the presence of stacking faults and surface facets along the nanowire length.

The nanostructures grown with disilane also are shown to depend on precursor pressure. They evolve from mixed nanowire- and nanopillar-type growth at low pressures to primarily nanowire growth as precursor pressures are increased. Planar growth of silicon prior to nanowire nucleation results in nanopillar growth, and it is believed that these structures grown at low disilane pressures could inhibit nanowire nucleation. As a result, relatively low densities of nanowires are nucleated at low pressures. Essentially, the very low concentration of disilane molecules will eventually prefer to form a thin-film layer on the substrate surface and block nanowire nucleation. So while some nanowires do nucleate, their growth rate is excessively slow; even to the point that the nanowire growth rate is comparable to the thin-film planar growth on the bare silicon substrate. Increasing pressure provides a higher source of precursor species incident on the metal-silicon eutectic seed and allows for higher growth rates and shorter nucleation times. **Figure 3.11** shows the evolution of nanowire morphology in cross-sectional SEM images. Lower pressures exhibit a slower growth rate and more planar type undergrowth, whereas higher pressures show faster growth rates desirable for straight, smooth sidewall nanostructures. These results are qualitatively consistent with our previous kinetic studies¹⁸ for digermane nanowire growth which found the growth rate to increase linearly with digermane pressure.

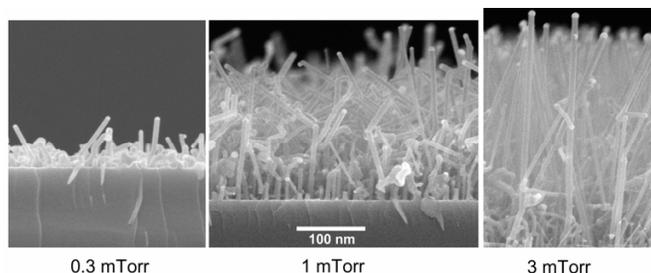


FIGURE 3.11: Silicon nanowires grown at specified disilane pressures result in nanostructures that evolve from mixed nanowire- and nanopillar-type growth to nanowire growth as pressure increases. The 1.0 nm nominal thickness Au catalytic seeds are deposited *in situ* at 250°C followed by disilane precursor growth at 400°C for 15 minutes.

Nanowire growth kinetics also depend on temperature, with increasing growth rates resulting from higher temperature. The growth rates are determined by stopping nanowire growth after specified growth times and measuring the mean nanowire length in a scanning electron microscope. Using the *in situ* optical reflectivity monitoring, the nucleation time was independently determined. Subtracting the nucleation time from the total time at growth conditions yields the actual nanowire growth time. For example, a sample that takes 45 seconds to nucleate, and remains at elevated temperature with the precursor gas present for five minutes will only actually grow for four minutes, fifteen seconds. Results of growth rate as a function of temperature are plotted in **Figure 3.12** with 3.0 mTorr disilane pressure on 1.0 nm nominal Au seed thickness. By knowing the nanowire growth rates as a function of temperature, the activation energy for silicon nanowires growth can be determined by the slope of the semi-log plot to be approximately 0.30 eV.

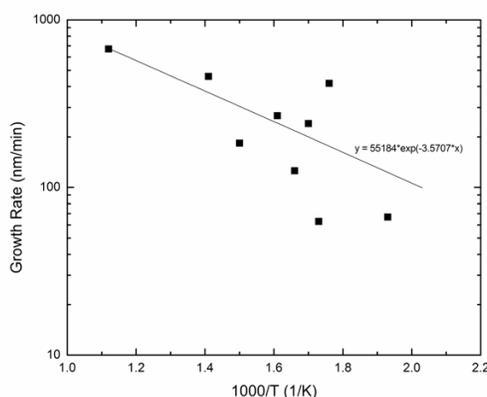


FIGURE 3.12: Disilane nanowire growth rates, as a function of growth temperature. From the slope we can infer an activation energy of approximately 0.30 eV is required to grow SiNWs using this precursor species by catalytic CVD growth in UHV conditions.

Digermene Nanowire Morphologies

A strong morphology dependence on pressure has been documented for the digermene nanowire growth system.¹⁸ Even at growth temperatures above the Au-Ge eutectic temperature of 361°C, at low precursor pressures (5×10^{-4} Torr) growth tends towards nanopillar-type morphology. However, the VLS nanowire growth dominates at higher pressures (near 3.0×10^{-3} Torr), and at intermediate pressures, both growth modes are active, thus allowing nanowires and nanopillars to nucleate and grow simultaneously.

Two germanium nanowire characteristic morphologies are observed from the digermane precursor at the higher pressure regime: those with uniform diameter throughout the length of the nanowire and those with highly-tapered, decreasing diameter sidewalls along the length of the wire. Tapered nanowire growth results from planar-type growth on the nanowire sidewall. The constant sidewall growth combined with axial wire growth results in a linear tapering effect. Here we report tapered nanowires, shown in **Figure 3.13**, with average tip diameter from 22 to 29 nm and average base diameters 64 to 78 nm; average lengths are 1300 nm for sample grown by *in situ* depositing 0.2 nm Au at 250°C with immediate anneal at 500°C for 20 minutes. Subsequent nanowire growth proceeds with digermane at 9.0×10^{-3} Torr and 300°C for 5 minutes. Comparisons of our measured lateral growth rate at 300 and 400°C are given in **Figure 3.14**. A similar lateral growth rate for the tapered nanowires at 300°C was reported in previous experiments by Dailey et al. Higher temperatures clearly show more tapering, consistent with the increased planar growth rates with increasing temperature. Thus, the strong tapering with increasing temperature indicates that the highly reactive digermane grows non-catalytically on the nanowire sidewall in addition to the Au-catalyzed vertical growth.

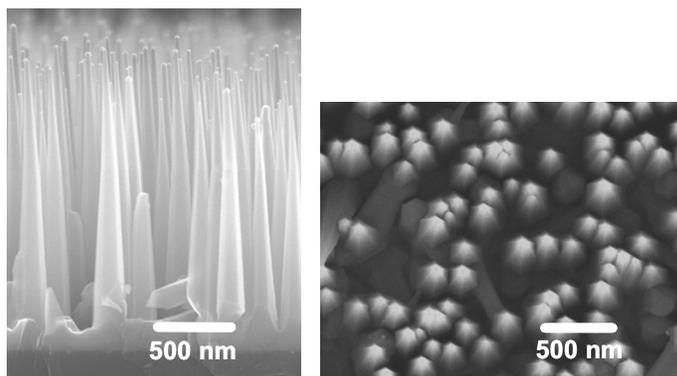


FIGURE 3.13: Highly-tapered germanium nanowires grown at 3.0 mTorr digermane pressure, 350°C for 15 minutes (nucleation time 2 minutes as observed by optical reflectometry) with Au seeds 1.0 nm nominal thickness at 250°C.

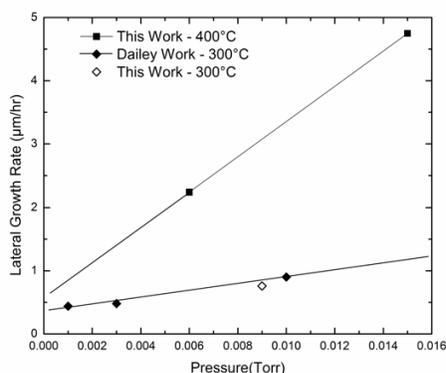


FIGURE 3.14: Lateral growth rates deduced from tapered Ge nanowires as a function of precursor gas pressure at a growth temperature of 400°C. Previous work by J.W. Dailey et al.¹⁸ correlate to current growth processing conditions at 300°C (note these results, previously quoted at 400°C, have been corrected for improved temperature calibration of the system).

The strong morphology dependence for digermene nanowire growth with pressure and temperature is summarized in **Figure 3.14**. At low pressures catalyzed lateral growth dominates, whereas at higher pressures catalyzed nanowire growth dominates. At higher temperatures nanowire growth is observed. We also note from the trends shown that the nanowire taper increases with increasing temperature and pressure. Our results indicate that the optimal conditions for non-tapered germanium nanowire growth with digermene precursors occurs at 9.0 mTorr and temperatures between 260-300°C.

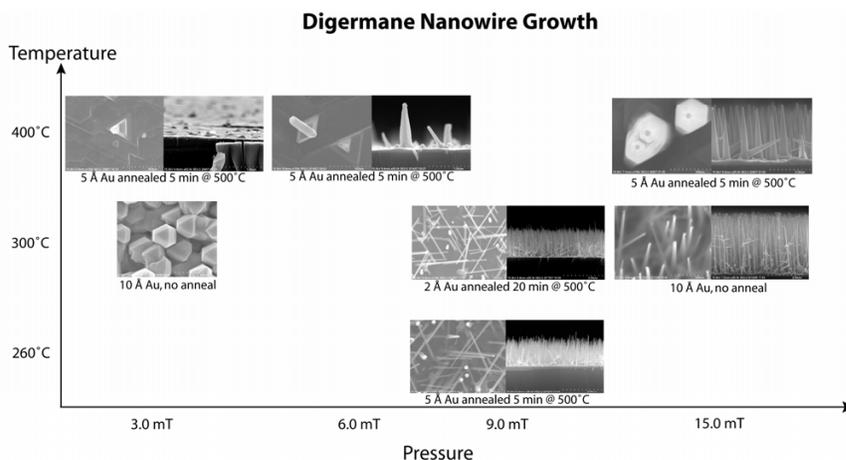


FIGURE 3.15: Digermene growth morphologies as a function of pressure and temperature on Si(111) substrates.

As discussed above, under appropriately selected processing conditions, non-tapered germanium nanowires can be grown quite readily as illustrated in **Figure 3.16**. These GeNWs show far less kinking than the disilane grown nanowires discussed previously, indicating that the liquid Au-Ge eutectic-nanowire interface remains stable as growth proceeds. Also there is no tapering along the nanowire which is often present when growing nanowires from germane precursors except at 350°C or above. GeNWs typically form epitaxially on the Si(111) substrate, as evidenced by the growth along the vertical $\langle 111 \rangle$ direction (bright white dots) and 3 inclined $\langle 111 \rangle$ directions (at 120° angles) as viewed in plan view. Other nanowire researchers and our own colleagues using a PECVD growth system observe the VLS-grown Si nanowires can take on $\langle 110 \rangle$ and $\langle 112 \rangle$ orientations at smaller nanowire diameters with this transition occurring at approximately 25 nm diameter. Ge $\langle 110 \rangle$ and $\langle 112 \rangle$ nanowires are also expected here for the smaller diameter nanowires, however a detailed analysis (which would require cross section SEM to distinguish $\langle 110 \rangle$ and $\langle 111 \rangle$ orientations) was not carried out in the present case. **Figure 3.16** shows the relative orientations of the $\langle 111 \rangle$ and $\langle 110 \rangle$ nanowires as viewed in plan view by FESEM,.. With the sample oriented such that the normal to the (110) cleave plane is parallel to the horizontal image axis, the $\langle 111 \rangle$ -oriented and $\langle 110 \rangle$ -oriented nanowires overlay each other in plan view projection, and grow at 120° from the horizontal image axis, as indicated by the arrows in **Figure 3.16**.

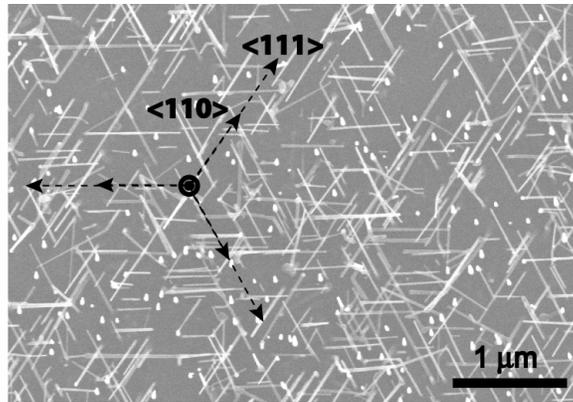


FIGURE 3.16: Nanowire growth orientation projections onto (111) plane for non-tapered germanium nanowires on Si(111); Nanowires are grown by *in situ* depositing 0.2 nm Au at 250°C with immediate anneal at 500°C for 20 minutes, and subsequent nanowire growth with digermene at 9.0×10^{-3} Torr and 300°C for 5 minutes.

At growth temperatures below the eutectic temperature (361°C), nanowire growth transitions from an exclusively vapor-phase growth mode to a bimodal solid- and vapor-phase growth mode, depending on the diameter of the catalytic seed, as shown in **Figure 3.17**. Recall that small diameter metal seeds have a lower melting point than their larger metal counterparts; it is this difference in melting point that allows small diameter nanowires to grow in the liquid-phase VLS method with consistent diameters along the length of the wire, while large diameter nanowires show much less oriented growth and a non-uniform, worm-like morphology and are inferred to be formed by gold-catalyzed solid-phase growth. While liquid-phase growth, seen for small-diameter nanowires, incorporates atoms from the precursor gas directly into the catalytic seed to eventually supersaturate the Au-Ge eutectic seed and nucleate an epitaxially perfect nanowire structure, the solid-phase growth mode incorporates the germanium atoms into the growing structure primarily by surface and interface diffusion mechanisms. These larger nanowires have difficulty maintaining a strongly oriented growth direction, due to the lack of thermal energy to melt the larger catalytic seed and thus an inability to incorporate germanium atoms from the vapor phase directly into a liquid-solid growth interface. Worm-like nanowire structures evolve as a result.

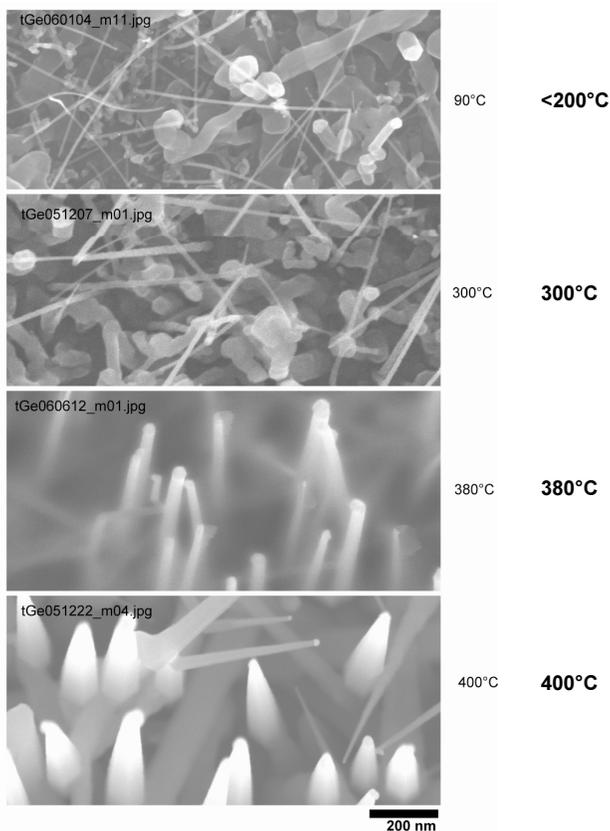


FIGURE 3.17: Germanium nanowire morphology as a function of growth temperature. Low temperatures, ie below the eutectic temperature as in (a) and (b), solid-phase growth of non-epitaxial structures from large diameter clusters occurs, while at the same time, the small-diameter catalytic seeds grow nanowires by vapor-phase growth. Just above the eutectic temperature (c), straight, non-tapered epitaxial nanowires nucleate and grow. Increasing temperature beyond the eutectic temperature leads to tapered germanium nanowire growth (d). Also shown in panel (a) are small diameter nanowires, approximately 7 nm, achieved using low-growth temperatures. All growths at 3.0 mTorr digermane; growth times for (a)-(d) are 4 min, 10 min, 4 min, and 3 min, respectively.

Silane Nanowire Morphologies

Pressure and temperature effects on silane-grown nanowires follow similar trends to those for disilane. The lower reactivity of silane compared to disilane requires higher partial pressures to nucleate nanowires on similar time-scales and with comparable growth rates. Factors affecting the nanowire growth rate include precursor pressure and growth temperature.

Silane pressures between 15-45 mTorr were investigated and were found to exhibit morphologies similar to the disilane growth at pressures between 0.3-15 mTorr. **Figure 3.18** shows the morphology change for silane grown nanowires as a function of precursor pressure; at higher pressures, the quality of nanowires is the greatest – a majority of the nanowires are uniform in diameter with relatively few kinks. At the lower pressures, nanowire growth is overcome by the lateral growth of silicon on the substrate. As a result, the density of nanowires for low-pressure growth decreases. Also, it is difficult to nucleate nanowire growth, particularly for smaller diameter seeds, for silane at pressures below 15 mTorr, as seen in **Figure 3.18**. From the measured nanowire growth rates, **Figure 3.19** plotting the log of growth rate upon inverse temperature allows us to calculate an activation energy for the nanowire growth with the silane precursor.

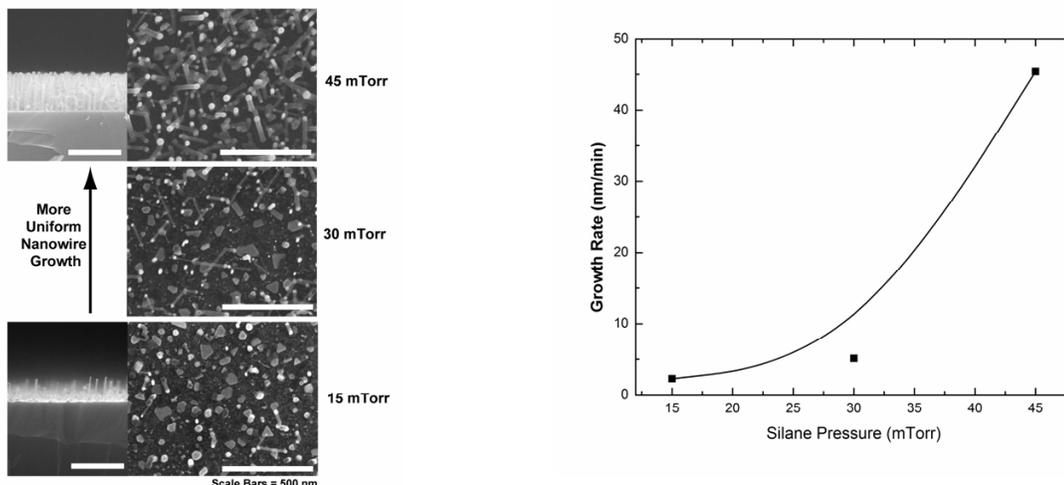


FIGURE 3.18: Silane growth variations as a function of pressure with a growth temperature of 600°C; more nanowire-like growth occurs at higher precursor pressures. The inset plot shows nanowire growth rate increasing with silane pressure.

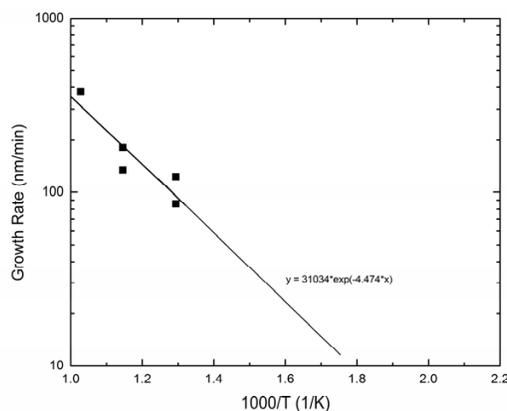


FIGURE 3.19: Silane nanowire growth rate as a function of growth temperature at silane pressure of 45 mTorr. Activation energy = 0.39 eV.

Plotting the Arrhenius relationship of nanowire growth rate upon temperature for the silane and disilane precursor gases that exhibit wire-type growth, we calculate the activation energy for nanowires grown at the optimal pressures for each precursor species. For comparison, the activation energies are found to be $E_{A, \text{disilane}} = 0.30 \text{ eV}$ and $E_{A, \text{silane}} = 0.39 \text{ eV}$ for the growth of nanowires specific to our system, as plotted in **Figure 3.20**. Comparatively, literature values for activation energy of silane grown nanowires tends around 0.7 eV; the cause for this discrepancy could be the ultra-high vacuum conditions under which these experiments are performed, as opposed to the typical low pressure chemical vapor deposition tube furnaces used by our contemporaries. Such growth systems routinely open to atmospheric conditions, and the potential for contaminants to hinder the growth of those systems' nanowires.

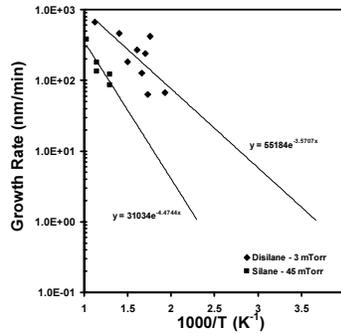


FIGURE 3.20: Growth rate comparison for nanowires grown via disilane and silane precursors at their optimal growth conditions.

Germane Nanowire Morphologies

Being the least reactive of all the precursors studied herein, germane molecular decomposition provides the largest barrier to nanowire growth. It is reported that this precursor requires higher partial pressures in order to nucleate and grow nanowires, typically on the order of 150 mTorr or greater. Though several other nanowire research groups have successfully grown using the germane source, our nanowire growth chamber is restricted to pressures below 100 mTorr at present. Growth conditions for straight-walled, high density films are reportedly grown by colloidal gold particles nucleating germanium nanowires on Ge (111) surfaces using a cold-wall, lamp heated, chemical vapor deposition system with GeH_4 flowing at a partial pressure of 285 mTorr.¹⁴ A two stage temperature scheme allows for nucleation of the nanowire by growth at 350°C for five minutes, then decreasing temperature to 280°C for the remainder of the thirty-minute growth sequence; thus vertical nanowires are grown while avoiding the well-known tapering problem seen at higher growth temperatures.

Though the deposition chamber used in our studies cannot achieve high enough pressures for efficient nanowire growth, the low pressure, mostly planar growth can be evaluated for its usefulness in future work.

Growth on Patterned Substrates

The aligned growth of semiconducting nanowires in periodic arrays is a major barrier to the implementation of nanowire structures and heterostructures in integrated circuits and large-scale devices. In order to define a growth location for the nanowires, the catalytic seeds must be directed to the appropriate nucleating point on the sample surface; this is a non-trivial task, typically achieved by *ex situ* patterning substrate.

Typical Patterning Approaches

Many potential patterning techniques for lithographically defining nanowire growth locations exist: traditional photolithography, microcontact printing, focused-ion beam deposition, and electron beam lithography to name just a few. Early in these studies, experiments on photolithographically patterned gold thin films showed that the surface cleanliness of the (a) the gold-cluster – silicon-substrate interface, (b) the substrate diffusion area directly adjacent to the catalytic seed, and (c) the vacuum-gold interaction surface dramatically affect the growth of semiconducting nanowires. The cluster-substrate interface must be free of contaminants that

would hinder the nucleation of semiconducting atoms at the interface to begin growing a nanowire. Similarly, the high mobility of species on the surface is critical to the initial, orientation-determining stage of nanowire growth, a process that will be described in detail in subsequent sections. Thirdly, the interface between gold and vacuum must be maintained in clean conditions in order for precursor gases to readily react on the catalytic surface. Silicon is reported to diffuse through the Au cluster slowly even at room temperature (possibly migrating within a thin surface liquid surrounding the Au cluster itself) to form a thin capping layer of silicon dioxide over the catalytic seed that blocks nanowire nucleation and growth. Hence any nanowire growth experiment attempted must maintain a clean silicon surface prior to catalytic seed deposition, something difficult to achieve at times with the more common lithographic techniques.

The major complication of many lithographic techniques resides in the photoresist required to create masked structures; chemical resists such as polymethyl-methacrylate (PMMA) must be removed from the substrate after pattern definition, but prior to nanowire growth process to be compatible with the ultra-high vacuum environment. However should any resist be left behind on the substrate, surface diffusion will be severely hindered and initial stages of nanowire formation may be blocked. Patterning techniques attempted throughout the course of our investigations include such techniques as focused-ion beam deposition, soft lithography techniques (microcontact printing and dip-pen nanolithography), and electron beam lithography, the most efficient technique being the later, which we discuss briefly here.

Electron Beam Lithography (EBL) Patterned Oxides

Selective growth of nanowires in desired spatial locations has been the primary motivation for use of the electron beam lithography technique in these studies. Using the EBL, a lithographically defined patterning of ultra-small holes can be fabricated in a thin oxide layer; for oxide thicknesses of approximately 12 nm, and oxide hole-sizes down to 35 nm have been achieved. Experiments to selectively deposit Au into the oxide windows and grow nanowires solely from these source droplets have yielded promising results. The Au depositions were done at high temperatures (up to 700°C) to induce preferential evaporation of the Au from the oxide surface and prevent Au cluster formation there while allowing Au clustering in the patterned windows.

The nanowires in the larger, 500 nm square oxide windows grew vertically as expected, however, growth in the 200 nm and 35 nm windows was limited to deformed growth, with no obvious Au seed and suggestive of solid-phase growth. One possible explanation for the lack of Au in the smaller-sized windows is that the Au atoms landing on the silicon and oxide surfaces diffuse across the oxide and then re-evaporate to vacuum. The probability of all the adatoms re-evaporating is fairly small, and the remaining atoms migrate on the surface to the windows.

Seed density measurements for 1.0 nm Au deposited on a bare Si(111) substrate at 700°C show on the order of 1 seed per square micron; hence the Au surface diffusion lengths are quite long. The Au has ample opportunity to migrate across the oxide surface into or out of the EBL patterned windows of 200 nm and below, especially at the elevated deposition and anneal temperatures used to coalesce the catalytic seeds within the opened oxide windows. Au deposition temperature and rate (or both) affect the diffusion of Au atoms on the oxide, but at

some point the selective nature of the high temperature deposition is lost for smaller windows. While the process for growing vertical Si nanowires in spatially controlled areas has been demonstrated, additional work is required to optimize the process for very small windows.

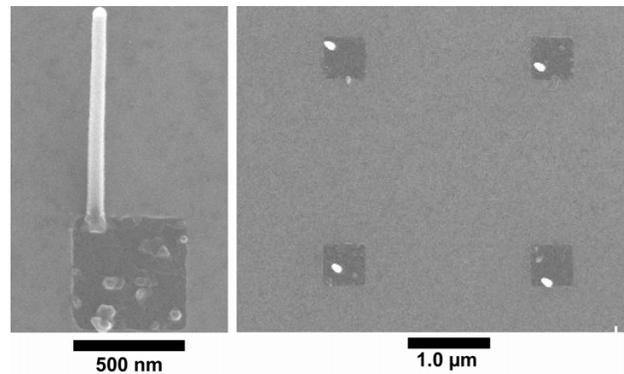


FIGURE 3.21: Square windows in 12 nm oxide, patterned for spatially controlled nanowire growth. Window edge = 500 nm, pitch = 2.0 μm . Note from these inclined (left) and top (right) views that most of these wires grow vertically, having nucleated from gold deposited preferentially on the bare Si(111) substrate within the windows.

CONCLUSIONS

Silicon and germanium nanowires synthesized by the vapor-liquid-solid mechanism with silane (SiH_4), disilane (Si_2H_6), germane (GeH_4) and digermane (Ge_2H_6) precursor gases at various pressures and temperatures have been demonstrated. The unique aspects of this project begin with the nanowire growth chamber: an ultra-high vacuum chemical vapor deposition system with base pressures near 1×10^{-10} Torr; such cleanliness enables the samples to be flash cleaned *in situ* to obtain ultra-clean surfaces on which these experiments are conducted without hindrance of contaminants. Additionally, control of the nanowire growth characteristics are enhanced by the addition of an *in situ* gold source for depositing discontinuous thin-films on atomically clean Si(111) surfaces to form the necessary catalytic seeds. Inclusion of the four precursor gases primarily used in nanowire synthesis allows interesting heterostructures to be created within one chamber. A novel optical reflectometry technique to monitor the nanowire growth process has been added to the system, such that nucleation time, growth rate, and average length of the effective nanowire layer, can be monitored throughout the course of the experiments from the oscillatory reflectometry.

Nanowire morphologies vary drastically across the range of precursor gases within the pressure-temperature space, 1×10^{-4} Torr to 9.0×10^{-2} Torr and 280-700°C study. The optimal nanowire growth conditions are summarized in **Table 4-1** below.

TABLE 4-1: Growth conditions for precursor gases used in these studies; pressure and temperature ranges of interest for each gas.

	Growth Pressure		Molecular Mass	Molecular Flux	Growth Temp
	(mTorr)	(N/m^2)	(kg/molecule)	(molecules/ cm^2)	(°C)
Disilane	15	2.0	9.33×10^{20}	4.07×10^{18}	350-400
Silane	45	6.0	5.33×10^{20}	1.62×10^{19}	400-500
Digermane	9	1.2	2.51×10^{21}	1.49×10^{18}	300-400
Germane	> 100	> 13.3	1.27×10^{21}	> 2.35×10^{19}	400-500

Though there are still a number of questions to be answered, an increased understanding the fundamental materials science behind nanowire synthesis has been obtained. Nanowire structures produced by silane, disilane, germane, and digermane have been demonstrated, and proof-of-concept samples for nanowire heterostructures have been grown. New synthesis control and novel analysis techniques have been introduced to provide nucleation time and growth rate determination not previously available during nanowire growth, both of which are critical aspects to the controlled formation of nanowire devices and heterostructures. From the studies provided herein, the *in situ* nanowire growth-monitoring via optical reflectometry is expected to provide unprecedented insight into the kinetics of VLS nanowire growth, in addition to becoming a widely applied growth monitoring tool. The high-resolution transmission electron microscopy strain mapping technique promises to provide quantitative analysis of strain states at nanowire heterojunctions and throughout the nanoscale structure.

Specifically of interest for future work emerging from the insights gained in these studies are the precisely grown axial and core-shell nanowire heterostructures, and their band-modification possibilities as a function of induced strain. One could imagine that advances in the understanding of nanowire synthesis might enable a wider range of nanowire materials combinations, from ordered arrays to novel three-dimensional nanoscale heterostructures with useful applications in areas of interest such as resonant tunneling diodes, surround gate transistors, thermoelectric materials and highly efficient photovoltaic and photo-detector devices, and single molecule electronic sensing.

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