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MEMS-based Arrays of Micro Ion Traps for Quantum Simulation Scaling

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MEMS-BASED ARRAYS OF MICRO ION TRAPS FOR QUANTUM SIMULATION SCALING

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Abstract

In this late-start Tier I Seniors Council sponsored LDRD, we have designed, simulated, microfabricated, packaged, and tested ion traps to extend the current quantum simulation capabilities of macro-ion traps to tens of ions in one and two dimensions in monolithically microfabricated micrometer-scaled MEMS-based ion traps. Such traps are being microfabricated and packaged at Sandia's MESA facility in a unique tungsten MEMS process that has already made arrays of millions of micron-sized cylindrical ion traps for mass spectroscopy applications. We define and discuss the motivation for quantum simulation using the trapping of ions, show the results of efforts in designing, simulating, and microfabricating W based MEMS ion traps at Sandia's MESA facility, and describe is some detail our development of a custom based ion trap chip packaging technology that enables the implementation of these devices in quantum physics experiments.

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Background and Motivation

The mathematical basis for quantum information processing (QIP) is relatively well established, but the engineering of the physical technologies necessary for implementing QIP is only just beginning. QIP algorithms for factoring and searching have been shown to provide great gains in computational efficiency over classical algorithms. Separate from these information processing applications, significant advances are expected in the ability to simulate quantum processes by using quantum devices to perform quantum simulation (QS). The simulation of quantum dynamical systems is difficult because as the number of elements of a quantum system increases linearly, the complexity of the equations modeling it grow exponentially. For example, to completely describe the dynamics of just 40 spin-1/2 particles requires $2^{40} \times 2^{40} = 10^{24}$ matrix elements, orders of magnitude greater than what can be stored on any classical supercomputer.

This complexity is why we cannot even determine the correct theoretical behavior of some important systems. Our understanding of quantum phenomena such as superconductivity, antiferromagnetism, behavior of f-electrons in solids, and so on, is seriously limited. Only recently, quantum information theorists have begun to map these problems onto experimentally accessible atomic systems, urged on by correspondingly recent advances in coherent manipulations of those systems, and it has been proposed that several paradigms of condensed matter physics can be modeled in trapped-ion systems. There are several other technologies that have been identified as potential contenders for evolving to provide practical quantum simulation operations, but all of these technologies suffer from scalability and control engineering problems. Ion trap techniques are among the most promising of approaches and constitute a fertile area of research, but few research organizations are able to fabricate them, much less fabricate entire arrays of ion traps that would be required to perform meaningful quantum simulations.

In collaboration with ion trap physicists at LANL working on the experimental realization of quantum simulation (D. Berkeland, co-author here), we are designing and building microfabricated ion traps to extend the current simulation capabilities of macro-ion traps to tens of ions in one and two dimensions. Such traps are being microfabricated and packaged at Sandia's MESA facility in a unique tungsten MEMS process that has already made arrays of millions of micron-sized cylindrical ion traps for mass spectroscopy applications. The purpose of the effort documented here was to 1) demonstrate viable ion-trap array fabrication and packaging techniques and 2) collaborate with external partners (LANL in particular) to validate the applicability of these devices in trapped ion experiments.

Technical Approach and Accomplishments

This project was funded initially as a one year Seniors Council Tier 1 LDRD project and work began several months into FY2005. For FY2005 we designed, simulated and microfabricated ion trap electrode structures that are micrometer in scale and multiplexed for discrete control of individual ion trap segments, as segmentation of ions is necessary for both QIP and QS. Using the design and processing knowledge established in our prior efforts to microfabricate massively parallel arrays of 3-D cylindrical ion traps (CITs) as micro mass analyzers, we built the first MEMS-based two-dimensional linear ion traps, to confine single and parallel, interacting ion chains (a spin ladder), and to confine ions in configurations such as a hexagonal closepacked arrays. In addition, we simulated proposed ion trap electrode arrangements to finalize trap electrode designs before the microfabrication of the ion trap chips (ITCs). Prior work showed outstanding success in fabricating air gap metallic structures that can accommodate the high conductivity and low capacitance RF requirements necessary to trap ions at these dimensions. In addition, the traps built and packaged in the work here were designed to provide the laser optical access to the ions that is necessary to manipulate their electronic and translational eigenstates. Our initial microfabricated traps were found to be unable to support the levels of RF necessary for trapping to occur and was the result of excessive capacitance between the RF electrodes and RF ground. Much important knowledge, however, was gained regarding design aspects of the ion traps. In particular, it was determined that the capacitance of the air bridge leads that bring the RF to the trap region must be minimized, the tungsten trap electrodes could not be cantilevered by arbitrarily large distances over the edge of the Si hole, and the top of the ion trap chip surface, initially a dielectric material consisting of SiO_2 and SiN, must be metallized, preferably with Au. Additionally, the necessity of developing a common ion trap chip packaging platform that could accommodate the demands of laser access to the trapping region, a minimum 300 degree C vacuum bake out, and operation of the ion traps at 10^{-11} Torr vaccum levels, was recognized and became an over-riding issue in the implementation of microfabricated ion traps.

For FY2006, while we continued work on the long term goal of microfabricating a revised trap design, the newly recognized importance of trap packaging was recognized: hence it became necessary to develop a custom, high-vacuum/high-temperature trap package that is compatible with the experimental implementation of an ion trap chip for quantum simulations. Therefore our research focused on developing a common packaging platform for implementing ion trap chips for experiments in QS. As noted above, the goal was to have an ion trap chip package able to accommodate 3-dimensional laser access to the trapping region, a minimum 300 degree C vacuum bake out, and operation of the ion traps at 10^{-11} Torr. To achieve this we developed a custom ion trap chip packaging process utilizing a standard 100 pin PGA package modified for housing the ion trap chips. The custom packaging process included:

- the realization of a countebore and a through hole in the package base by modification of the COTS package to accommodate 3D optical access to the ions

- the Au metallization of the package backside and the sides of the counterbore and through hole to provide electrical continuity from the back to the Au package base, thereby allowing for the pinning of surface potentials near the trapping region

- the simulation and selection of a die attach adhesive that would be compatible with the vacuum and temperature requirements of the quantum simulation experimental apparatus

This custom modification was successfully demonstrated. Additionally, a metallization process was designed for post-die attach evaporation of Au onto the chip and package backs and fronts prior to wire bonding.

The development of this custom ion trap chip packaging technology is a significant advance in the application of microfabricated ion trap chips to quantum simulation and quantum information processing approaches based on trapped ions. This is an enabling technology that increases the number of applications of Sandia's ion trap chip technology, for example in the development of ultra-small scale mass analyzers for explosives and chemical detection.

The following figures, taken from our 2006 LDRD Day poster, briefly describe some of the aspects and details of quantum simulation, the use of trapped ions for quantum simulation, simulation of ion trap potentials of and the fabrication results for Sandia microfabricated MEMS-based ion traps, the modeling results and development details for the custom packaging of microfabricated ion traps, and the results of a proof of concept demonstration of ion trapping performed by NIST on Sandia fabricated and packaged ion traps.

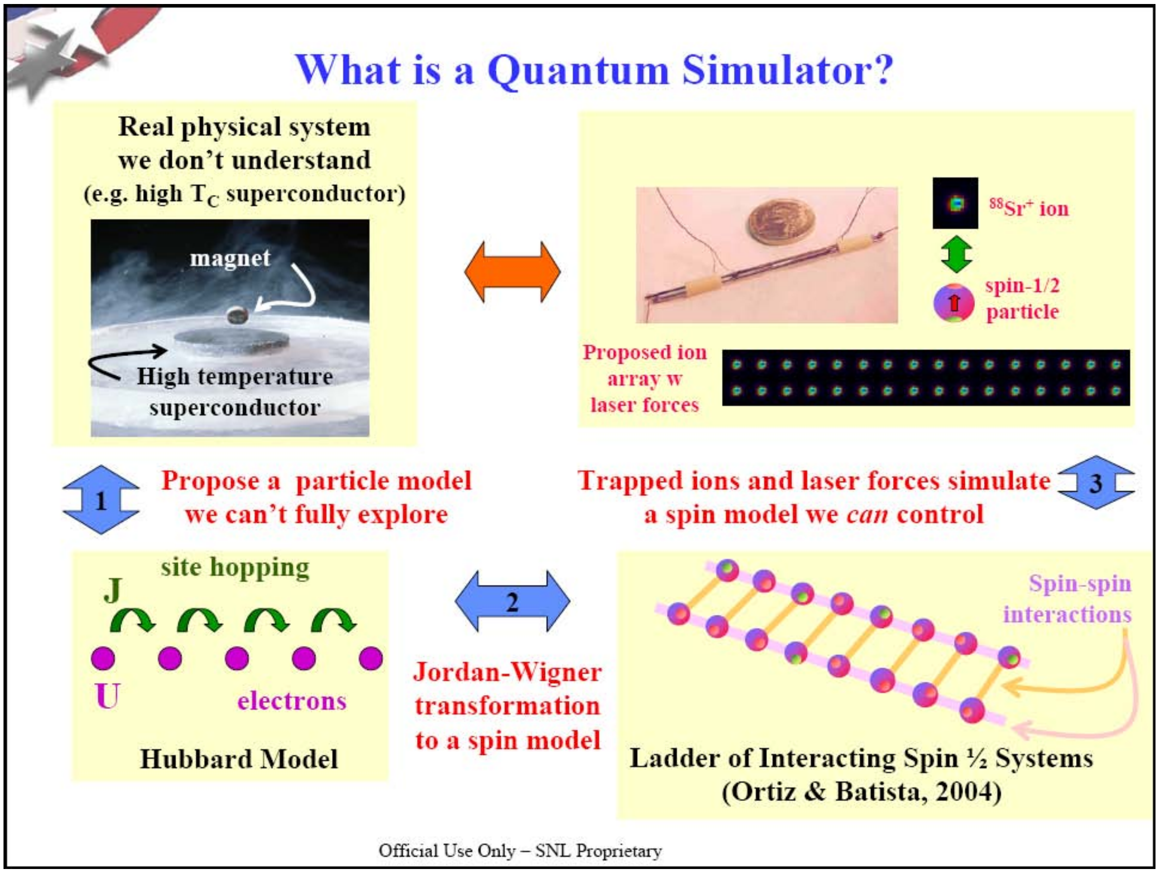


Figure1: Notional description of Quantum Simulation (QS).

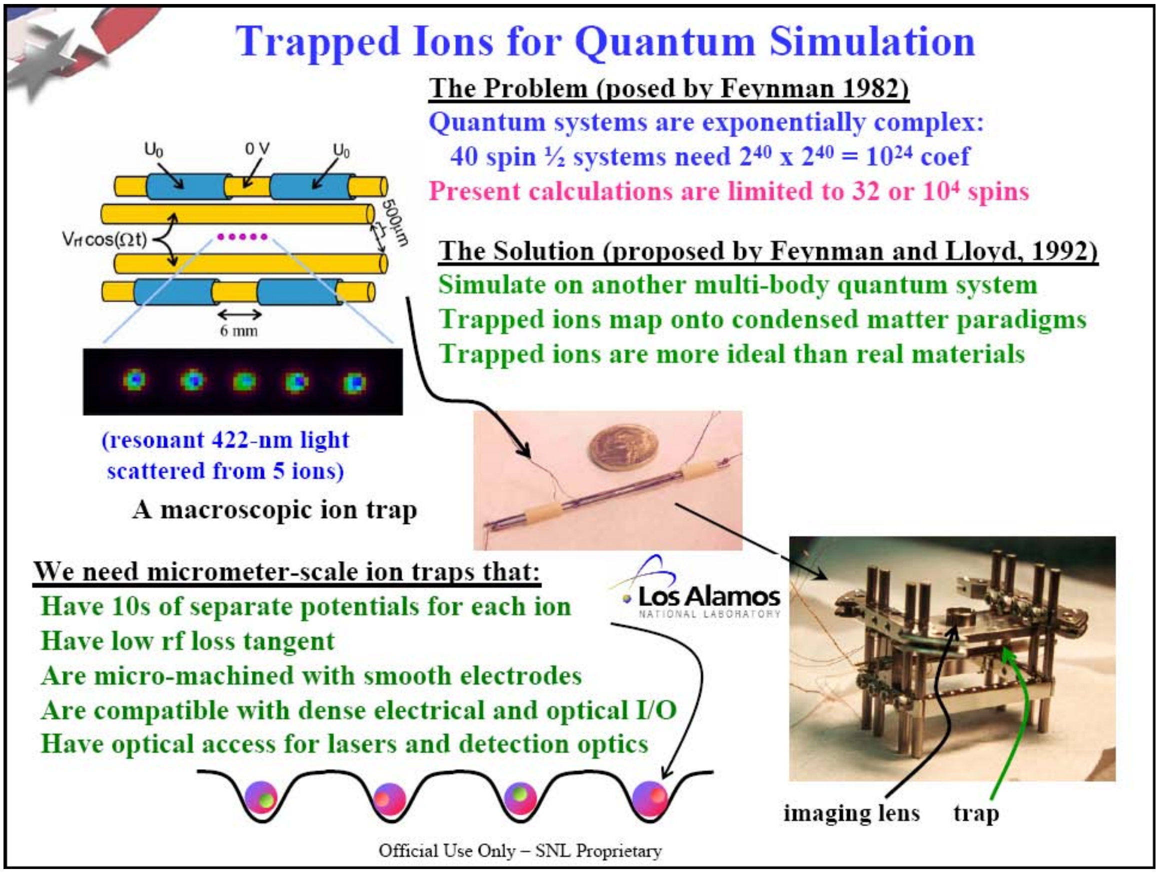


Figure 2: How trapped ions are implemented for quantum simulation.

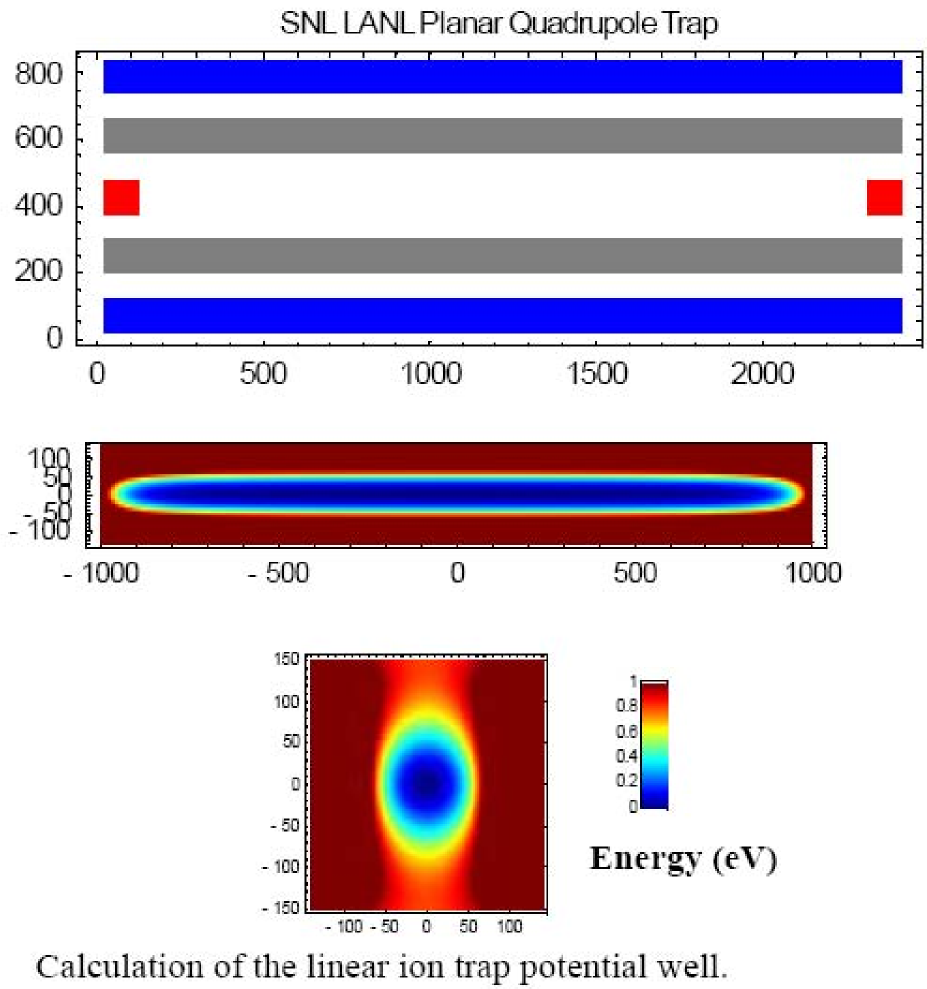


Figure 3: Example of a simulation of the trapping potentials in a Sandia microfabricated linear Paul trap.

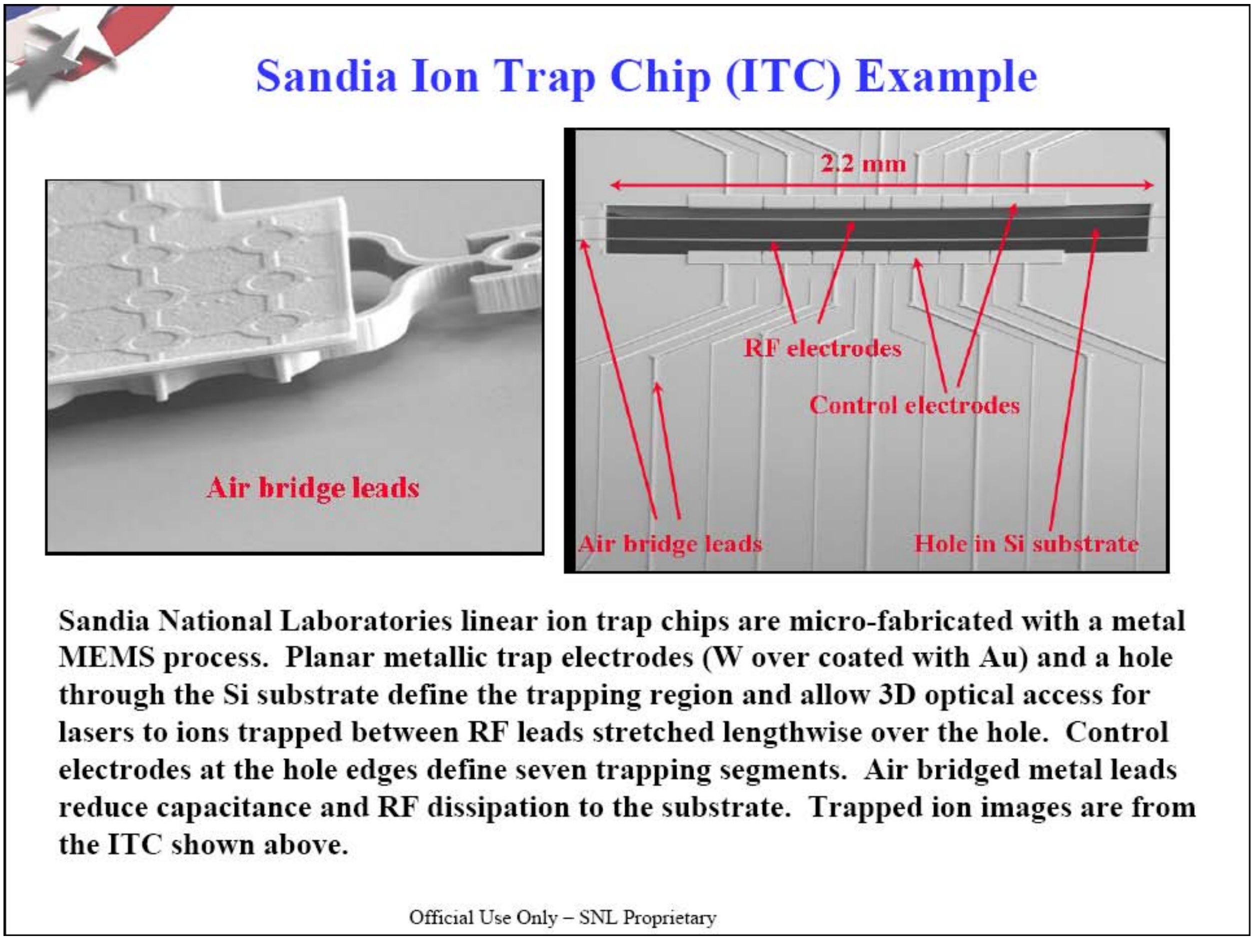


Figure 4: Example of a Sandia ion trap chip.

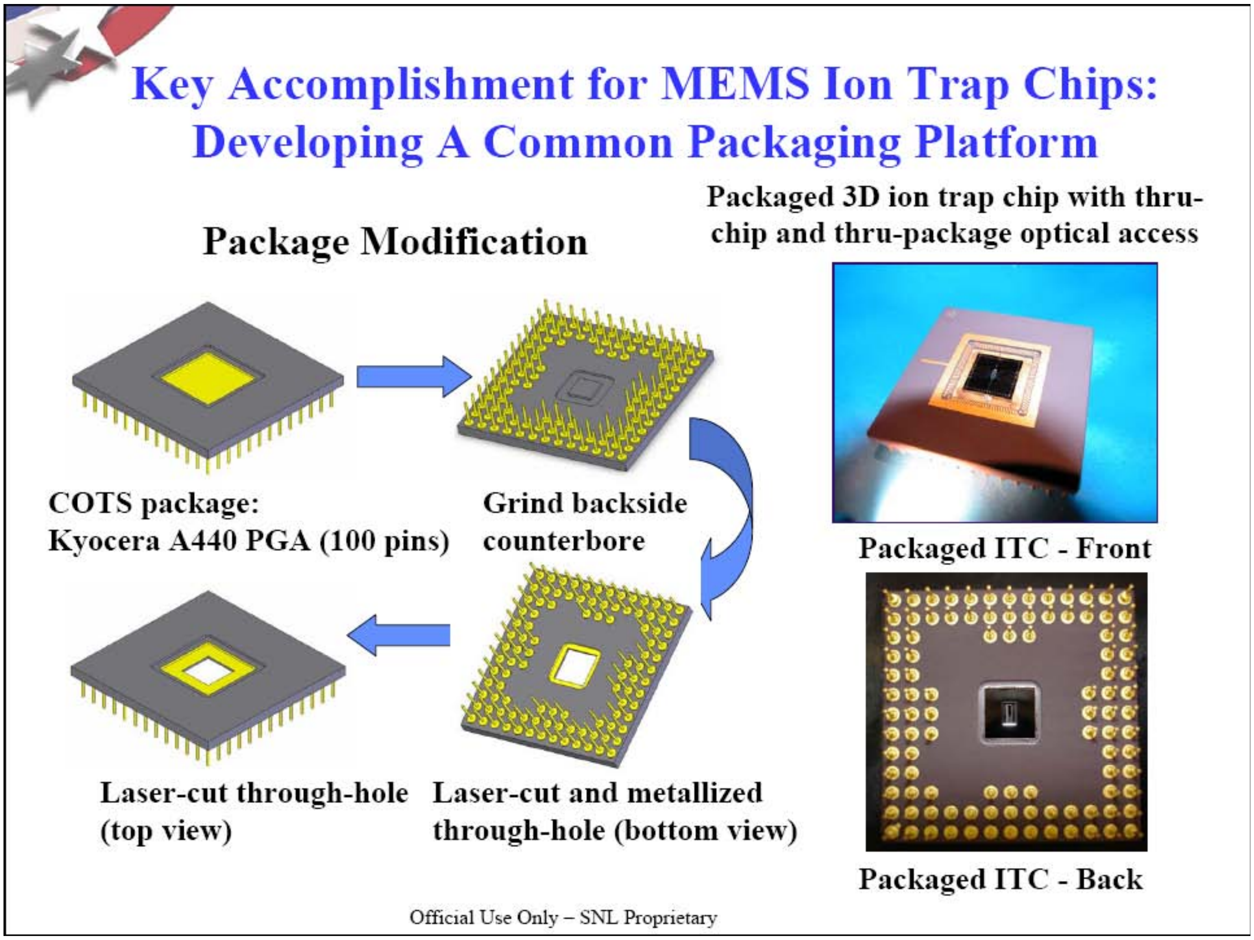
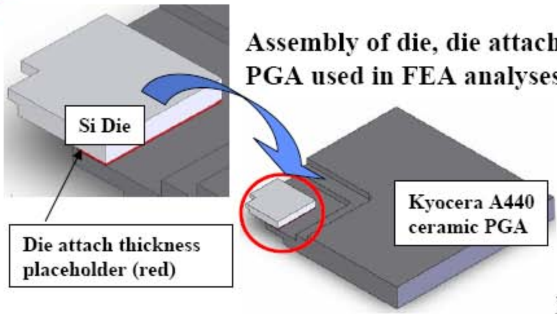


Figure 5: Development of a custom package for ion trap chips.



Assembly of die, die attach and PGA used in FEA analyses.

Analysis of Packaging Materials Properties

		CTE (ppm/C)	Young's Modulus (GPa)	Yield Strength (MPa)	Thermal Conductivity (W/mK)
Kyocera A440 (Al_2O_3) ceramic	PGA package bulk	7.1	310	300	14
Elemental silicon (Si)	Die	2.49	112.4	120	124
Gallium Arsenide (GaAs)	Die	5.4	82.7	unk	50
Gold-Germanium (88Au12Ge) solder	Die attach	13	72.7	185	43.9
Sauriesen cement	Die attach	4.68	300	1.7	1.6
JM7000 cyanate ester	Die attach	33	0.01	17.2	1.1
6061-T6 Aluminum	comparison	23.6	69	276	167
Mild steel	comparison	11.7	200	250	60.5

- **Hard solders (Au-Si, 80Au20Sn and 88Au12Ge) are not flexible enough to accommodate large die.**
- **Epoxies were developed and readily used to mitigate the stress between die and package due to CTE mismatch.**
- **JM7000 was tested and successfully performs at 10^{-11} Torr after 300°C bake-out**

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Figure 6: The properties of candidate materials for a custom ion trap chip package are used as input for finite element analyses of the behavior of packaged ion trap chip under the conditions of a trapped ion quantum simulation experiment.

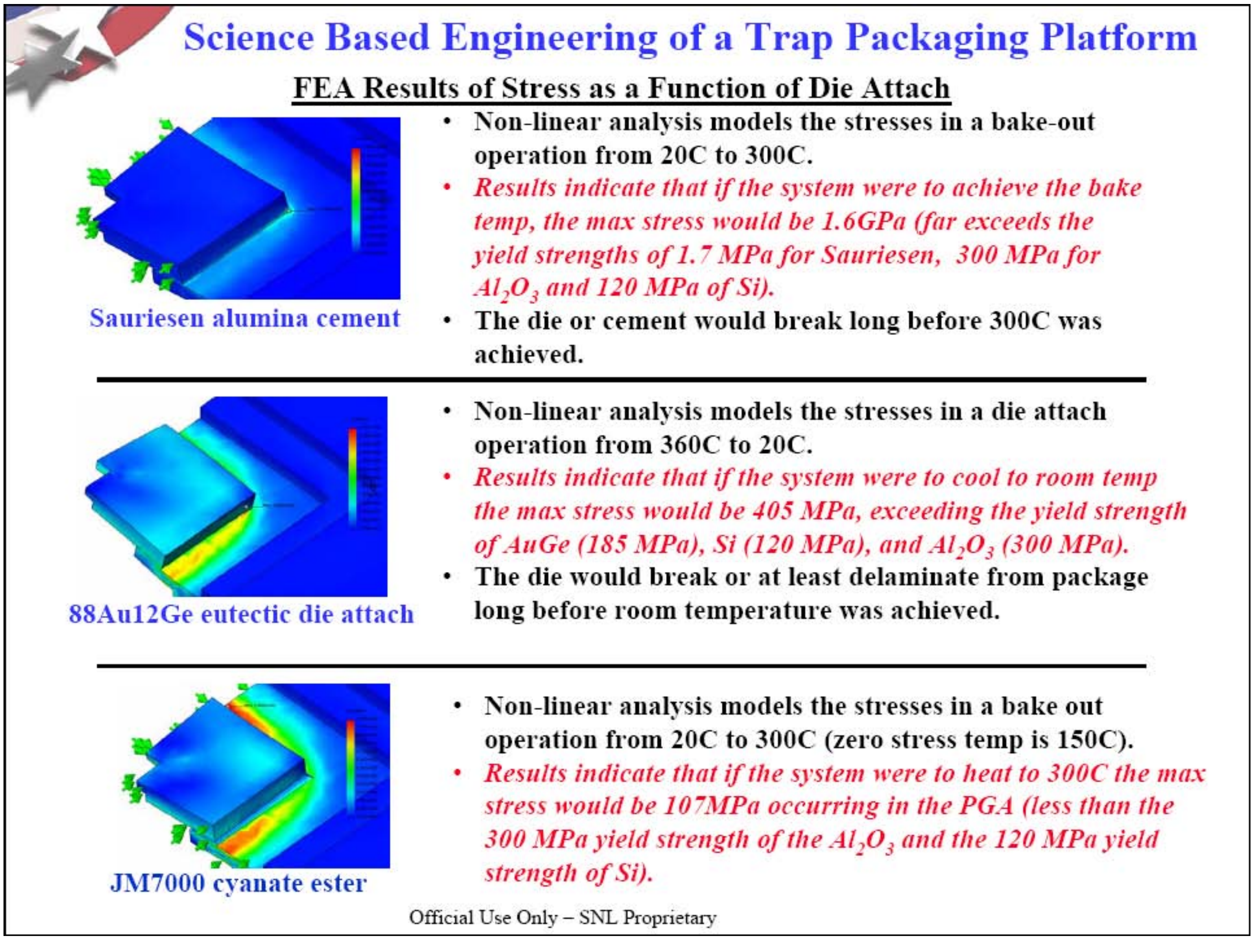

Figure 7: Results of finite element analyses of package/chip stress as a function of candidate die attach materials.

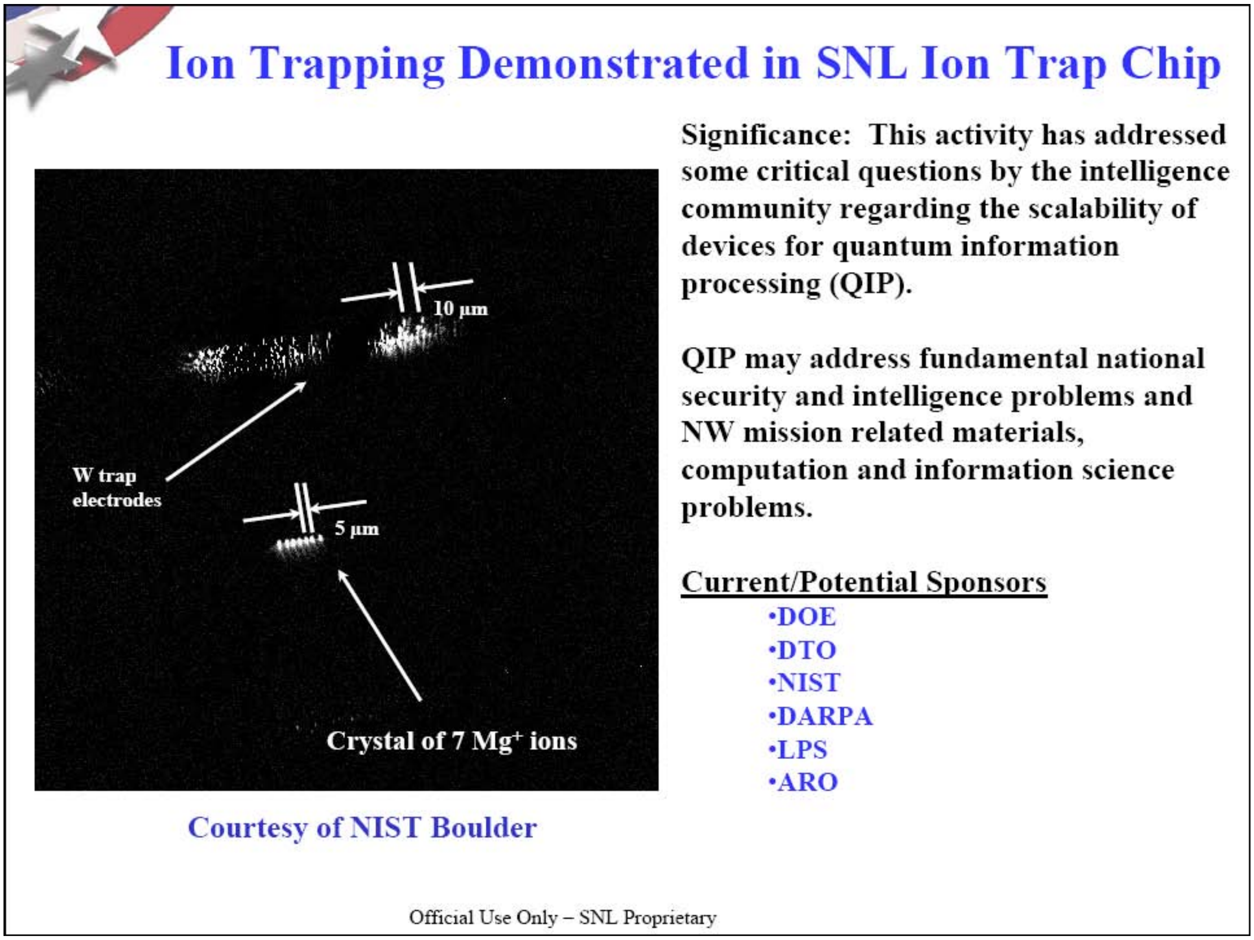

Figure 8: Demonstration of ion trapping in SNL ion trap chip.

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