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## **Status and Needs of Power Electronics for Photovoltaic Inverters**

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**Abstract Follows**

## ABSTRACT

Photovoltaics is **the** utility connected distributed energy resource (DER) that is in widespread use today. It has one element, the inverter, which is common with all DER sources except rotating generators. The inverter is required to transfer dc energy to ac energy. With all the DER technologies, (solar, wind, fuel cells, and microturbines) the inverter is still an immature product that will result in reliability problems in fielded systems.

Today, the PV inverter is a costly and complex component of PV systems that produce ac power. Inverter MTFF (mean time to first failure) is currently unacceptable. Low inverter reliability contributes to unreliable fielded systems and a loss of confidence in renewable technology. The low volume of PV inverters produced restricts the manufacturing to small suppliers without sophisticated research and reliability programs or manufacturing methods. Thus, the present approach to PV inverter supply has low probability of meeting DOE reliability goals.

DOE investments in power electronics are intended to address the reliability and cost of power electronics. This report details the progress of power electronics, identifies technologies that are in current use, and explores new approaches that can provide significant improvements in inverter reliability while leading to lower cost. A key element to improved inverter design is the systems approach to design. This approach includes a list of requirements for the product being designed and a preliminary requirements document is a part of this report. Finally, the design will be for a universal inverter that can be applied to several technologies. The objective of a universal inverter is to increase the quantity being manufactured so that mass-manufacturing techniques can be applied.

The report includes the requirements and recommended design approaches for a new inverter with a ten-year mean time to first failure (MTFF) and with lower cost. This development will constitute a 'leap forward' in capability that leverages emerging technologies and best manufacturing processes to produce a new, high reliability, inverter. The targeted inverter size is from two to ten kilowatts.

The report is organized into four sections. A brief introduction by Sandia is followed by Section Two from Millennium Technologies (a company with UPS experience). Section Three is provided by Xantrex (a PV manufacturing company) and the University of Minnesota provided Section Four. This report is very detailed and provides inverter design information that is irrelevant to the layman. It is intended to be a comprehensive documentation of proven technology and the manufacturing skills required to produce a high reliability inverter. An accompanying report will provide a summary of the recommended approach for inverter development.

<a href="#"><u>Section 1. An Inverter for the 21<sup>st</sup> Century</u></a> .....	1
<a href="#"><u>1.1. The Problem</u></a> .....	1
<a href="#"><u>1.1.1. Proposed Program</u></a> .....	1
<a href="#"><u>1.1.2. The Desired Product</u></a> .....	4
<a href="#"><u>1.1.3. References for Section 1.1.</u></a> .....	4
<a href="#"><u>1.2. Approach</u></a> .....	4
<a href="#"><u>1.2.1. A Business Plan</u></a> .....	4
<a href="#"><u>1.2.2. The Next Generation Inverter Will Result From Engineering Innovation</u></a> .....	6
<a href="#"><u>1.2.3. The Need for Systems Engineering</u></a> .....	6
<a href="#"><u>1.2.4. Preliminary Requirements</u></a> .....	9
<a href="#"><u>Section 2. Millennium Technologies Inputs</u></a> .....	12
<a href="#"><u>2.1. Status of Power Electronics</u></a> .....	12
<a href="#"><u>2.1.1. Importance of Power Electronics</u></a> .....	12
<a href="#"><u>2.1.2. Present Manufacturing Issues that Affect PV Inverter Lifetime and Cost</u></a> .....	12
<a href="#"><u>2.2. Tools of a Mature Manufacturer</u></a> .....	14
<a href="#"><u>2.2.1. Some Manufacturing Issues</u></a> .....	14
<a href="#"><u>2.2.2. Utilizing an Experienced Manufacturer</u></a> .....	15
<a href="#"><u>2.2.3. ISO-9000 and Quality Management Systems</u></a> .....	17
<a href="#"><u>2.3. Design and Manufacturing Approaches that Can Lower Cost and Increase Lifetime</u></a> .....	20
<a href="#"><u>2.3.1. Overview and Definitions</u></a> .....	20
<a href="#"><u>2.3.2. HALT Verses DVT - the Difference is the Purpose</u></a> .....	21
<a href="#"><u>2.3.3. Choosing HALT Stresses and Equipment</u></a> .....	22
<a href="#"><u>2.3.4. Preparing for HALT and Planning the Test</u></a> .....	22
<a href="#"><u>2.3.5. Margin Discovery – the Core of HALT</u></a> .....	24
<a href="#"><u>2.3.6. HASS – Maintaining Optimization</u></a> .....	27
<a href="#"><u>2.3.7. Accelerated Testing Summary</u></a> .....	30
<a href="#"><u>2.4. Current State-of-the-Art Technologies</u></a> .....	31
<a href="#"><u>2.4.1. Power Semiconductor Devices</u></a> .....	31
<a href="#"><u>2.4.2. Status of Converters (Inverters)</u></a> .....	31
<a href="#"><u>2.5. Problems With Existing PV Inverters</u></a> .....	33
<a href="#"><u>2.5.1. Lack of Universality</u></a> .....	33
<a href="#"><u>2.5.2. Old Technology Resulting in Short Lifetime, Low Quality and High Cost</u></a> .....	34
<a href="#"><u>2.6. Candidate Technologies that Could Result in Ten-year Lifetime of an Inverter</u></a> .....	34
<a href="#"><u>2.6.1. Soft-switching Technology (a developing technology)</u></a> .....	34
<a href="#"><u>2.6.2. Hard-switching Technology (presently dominates the industry)</u></a> .....	36
<a href="#"><u>2.6.3. Hard Versus Soft Switching</u></a> .....	37
<a href="#"><u>2.6.4. DSP Control Methods</u></a> .....	38
<a href="#"><u>2.6.5. Made-to-Order Power Electronics</u></a> .....	40
<a href="#"><u>2.6.6. Engineering Approach</u></a> .....	44
<a href="#"><u>2.7. Soft Switch May be a Suitable Approach to Reliability</u></a> .....	46
<a href="#"><u>2.7.1. Soft Switching Technique</u></a> .....	46
<a href="#"><u>2.7.2. Resonant Inverters</u></a> .....	48
<a href="#"><u>2.7.3. Specifications for a Large Power Inverter</u></a> .....	54

2.7.4. <a href="#">Brief Description of 400 kW Parallel Dual Inverter System</a> .....	60
<a href="#">Section 3. Xantrex Technology</a> .....	72
3.1. <a href="#">Present Status of Power Electronics Technology</a> .....	72
3.1.1. <a href="#">Safe Operating Area (SOA)</a> .....	72
3.1.3. <a href="#">Power Switch Thermal Management</a> .....	73
3.1.4. <a href="#">Semiconductor Reliability</a> .....	73
3.1.5. <a href="#">Power Switch Transient Effects</a> .....	78
3.1.6. <a href="#">Paralleled Switching Devices</a> .....	79
3.1.7. <a href="#">Magnetics Core Losses</a> .....	81
3.1.8. <a href="#">Transformer Saturation</a> .....	82
3.1.9. <a href="#">Fans</a> .....	82
3.1.10. <a href="#">Filters</a> .....	85
3.1.11. <a href="#">Electrolytic Capacitors</a> .....	86
3.1.12. <a href="#">Electromechanical Components</a> .....	88
3.1.13. <a href="#">Environmental</a> .....	90
3.2. <a href="#">Present Manufacturing Barriers to a 10 Year MTTF</a> .....	90
3.2.1. <a href="#">Quantity</a> .....	91
3.2.2. <a href="#">Quality Control</a> .....	91
3.2.3. <a href="#">Resource Limitation</a> .....	93
3.2.4. <a href="#">Production Testing</a> .....	94
3.2.5. <a href="#">Beta Testing</a> .....	96
3.2.6. <a href="#">Design for Manufacturability</a> .....	96
3.3. <a href="#">Candidate Technologies</a> .....	97
3.3.1. <a href="#">DSP</a> .....	97
3.3.2. <a href="#">Made-to-Order Power Electronics</a> .....	101
3.3.3. <a href="#">Soft Switching</a> .....	108
3.3.4. <a href="#">Technology Approach Summary and Conclusions</a> .....	112
3.4. <a href="#">Universal Software Modules</a> .....	113
3.4.1. <a href="#">Reusing Software Designs</a> .....	113
3.4.2. <a href="#">Modular Software</a> .....	114
3.4.3. <a href="#">DSP Modules</a> .....	116
3.4.4. <a href="#">A Vision for Future Software</a> .....	117
3.5. <a href="#">Universal Functional Block Architecture</a> .....	119
3.5.1. <a href="#">Control Assembly</a> .....	120
3.5.2. <a href="#">Low Voltage Power Supply</a> .....	120
3.5.3. <a href="#">Half-Bridge</a> .....	120
3.5.4. <a href="#">3-Phase Power Bridge</a> .....	120
3.5.5. <a href="#">Universal DC-DC Isolated Boost Converter</a> .....	121
3.5.6. <a href="#">DC-DC Isolated Buck Converter</a> .....	122
3.5.7. <a href="#">EMI Filter</a> .....	122
3.5.8. <a href="#">Remote Display</a> .....	122
3.5.9. <a href="#">DAS with Modem and Graphical User Interface</a> .....	123
3.6. <a href="#">High Reliability Manufacturing Considerations</a> .....	123
3.6.1. <a href="#">Comparable Industries</a> .....	124

3.6.2. ISO Compliance .....	132
3.6.3. Quality Assurance .....	133
3.6.4. Accelerated Product Life Testing .....	133
3.6.5. Automated Assembly .....	134
<b>Section 4. University of Minnesota Inputs .....</b>	<b>136</b>
4.1. Required Ratings of DC Energy Sources .....	136
4.1.1. Background .....	136
4.1.2. Energy Sources .....	137
4.1.3. Anticipated Inverter Output Configurations .....	137
4.1.4. Proposed Inverter Configuration .....	138
4.2. DC Converter Topology .....	140
4.2.1. Converter Features .....	140
4.3. A Detailed Description of the Power Stage .....	145
4.3.1. Design of the Power Stage .....	145
4.3.2. PWM Inverter Design .....	146
4.3.3. Output Filter Design .....	147
4.3.4. Switch Ratings .....	148
4.3.5. High Frequency Isolator Design .....	148
4.3.6. Voltage Regulator Design .....	151
4.3.7. ZVS of the MOSFET .....	153
4.3.8. Power Stage Design Conclusions .....	153
4.4. Simulation Results .....	154
4.4.1. Voltage Regulator .....	155
4.4.2. ZVS Operation .....	156
4.4.3. High Frequency Isolator .....	157
4.4.4. PWM Inverter .....	160
4.4.5. Simulation Conclusions .....	161
4.5. PWM Controllers .....	161
4.5.1. Structure of the Utility Interactive System .....	162
4.5.2. Current Loop Design for the PWM Inverter .....	163
4.5.3. Maximum Power Point Tracker .....	165
4.5.4. PWM Controller Conclusions .....	169
4.6. Inverter Protection Features .....	170
4.6.1. Protection Schemes at the Input .....	170
4.6.2. Protection Schemes at the Output .....	172
4.6.3. Over-Temperature Protection .....	174
4.6.4. Summary of Protection Approaches .....	175



## Table of Figures

<a href="#">Figure 2.1. Basic DC-link Soft Switching Inverter</a> .....	35
<a href="#">Figure 2.2. Representative DC-link Inverter Waveforms Under Discrete Pulse Modulation</a> .....	36
<a href="#">Figure 2.3. Basic Voltage-source Inverter with Resistive Load</a> .....	38
<a href="#">Figure 2.4. Basic Zero Current Switch Circuit</a> .....	47
<a href="#">Figure 2.5. A ZCS DC-DC Converter</a> .....	47
<a href="#">Figure 2.6. Basic Zero Voltage Switch Circuit</a> .....	47
<a href="#">Figure 2.7. A ZVS DC-DC Converter</a> .....	48
<a href="#">Figure 2.8. A Conceptual Circuit of Resonant DC-Link Inverter and its Waveforms</a> .....	49
<a href="#">Figure 2.10. Passively Clamped Resonant DC-Link Inverter</a> .....	50
<a href="#">Figure 2.11. Actively Clamped Resonant DC-Link Inverter</a> .....	50
<a href="#">Figure 2.12. A Quasi-resonant Commutated Pole</a> .....	51
<a href="#">Figure 2.13. An Auxiliary Resonant Commutated Pole</a> .....	52
<a href="#">Figure 2.14. A Delta-Configured Auxiliary Resonant Snubber Inverter</a> .....	53
<a href="#">Figure 2.15. A Zero-Current Switched Voltage-Source Resonant Inverter</a> .....	54
<a href="#">Figure 2.16. System Configuration of the Line Interactive Power System</a> .....	63
<a href="#">Figure 2.17. System Configuration of the Line Interactive Power System</a> .....	65
<a href="#">Figure 2.17. Control Block Diagram of Line Interactive Power System</a> .....	67
<a href="#">Figure 2.18. Single Phase Equivalent Circuit of a Stand-Alone System</a> .....	68
<a href="#">Figure 2.19. Control Block Diagram of the Voltage Feedback Scheme for Stand-Alone Applications</a> .....	69
<a href="#">Figure 2.20. Load Current Feed-Forward Control</a> .....	70
<a href="#">Figure 2.21. Load Current Feed-Forward Control + Resonance Damping</a> .....	70
<a href="#">Figure 2.22. The “Beat” Effect of dc Voltage Variation</a> .....	71
<a href="#">Figure 3.1. Simplified Resonant Pole Inverter Circuit</a> .....	108
<a href="#">Figure 3.2. Resonant Pole Inverter Waveforms</a> .....	109
<a href="#">Figure 3.3. Resonant Link Inverter Circuit With Active Clamping</a> .....	110
<a href="#">Figure 3.4. Resonant Link Voltage Synthesis</a> .....	111
<a href="#">Figure 3.5. Hard Switching Inverter Circuit</a> .....	112
<a href="#">Figure 4.1. Proposed Inverter Configuration</a> .....	138
<a href="#">Figure 4.2. Proposed First Stage</a> .....	141
<a href="#">Figure 4.3. Topology of the Isolated DC-DC Converter</a> .....	142
<a href="#">Figure 4.4. Topology of the PWM Inverter</a> .....	143
<a href="#">Figure 4.5. Circuit Topology of the PWM Inverter</a> .....	147
<a href="#">Figure 4.6. Circuit Topology of the High Frequency Inverter</a> .....	149
<a href="#">Figure 4.7. Low Frequency Equivalent Circuit of the Isolator</a> .....	150
<a href="#">Figure 4.8. Circuit Topology of the Zero Voltage-Switched Boost</a> .....	152
<a href="#">Figure 4.9. SABER Implementation of the Boost Converter</a> .....	155
<a href="#">Figure 4.10. Input Current and Output Voltage Waveforms for the Boost Converter</a> .....	156
<a href="#">Figure 4.11. ZVS Operation at Different Load Currents</a> .....	157
<a href="#">Figure 4.12. Resonant Circuit (left)</a> .....	157
<a href="#">Figure 4.13. Resonant Circuit Current Measurements (right)</a> .....	157
<a href="#">Figure 4.14. SABER Implementation of the High Frequency</a> .....	158
<a href="#">Figure 4.15. Transformer Model Used in Simulation</a> .....	158
<a href="#">Figure 4.16. Zero-voltage Turn-on of the MOSFETs</a> .....	159
<a href="#">Figure 4.17. Primary Current of the Transformer</a> .....	159
<a href="#">Figure 4.18. SABER Implementation of the PWM Inverter</a> .....	160
<a href="#">Figure 4.19. Output Voltage and Inductor Currents of the PWM Inverter</a> .....	161
<a href="#">Figure 4.20. Output Voltage Ripple (left)</a> .....	161
<a href="#">Figure 4.21. Inductor Current Ripple (right)</a> .....	161
<a href="#">Figure 4.22. Basic Structure of the Utility Interactive System</a> .....	162
<a href="#">Figure 4.23. Block Diagram of the Current Loop Controller</a> .....	163
<a href="#">Figure 4.24. Average Model of the System Used for Testing the Current Loop</a> .....	165

<a href="#">Figure 4.25. Simulation Results - Current Loop Response</a> .....	166
<a href="#">Figure 4.26. V-I Characteristic of the 2 kW Solar Array</a> .....	166
<a href="#">Figure 4.27. Power vs Current Plot for the Solar Array</a> .....	166
<a href="#">Figure 4.28. Maximum Power Point Tracker Algorithm</a> .....	167
<a href="#">Figure 4.29. SABER Schematic of the Proposed System</a> .....	168
<a href="#">Figure 4.30. Output Power and Output Current of the Solar Array</a> .....	168
<a href="#">Figure 4.31. Grid Voltage and Current Injected into the Grid</a> .....	169
<a href="#">Figure 4.32. Input Side Protection Against Failure</a> .....	171
<a href="#">Figure 4.33. Protection Against Reverse Connection</a> .....	172
<a href="#">Figure 4.34. Protection for the Paralleled Inverter</a> .....	174

## **Section 1. An Inverter for the 21<sup>st</sup> Century**

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### **1.1. The Problem**

PV inverter mean time to first failure (MTFF) is currently<sup>1</sup> about five years. This results in unreliable fielded systems and a loss of confidence in PV technology. Large volume customers of power electronics have driven power electronics development. These markets include motor drives, UPS, electric cars, inverters/converters for solar, micro-turbines, fuel cells, and switching mode regulated ac and dc power supplies. The results of product evolution are benefiting all users; however, there are problems unique to distributed generation that has limited the manufacturers of PV inverters to a few smaller companies. These companies have not had the required sophisticated research and reliability programs or manufacturing methods necessary to develop a mature product. Thus, the present approach to PV inverter supply has low probability of meeting DOE reliability goals. Several factors lead one to believe that inverter reliability can be dramatically improved. These include improvements in technology, increasing numbers of product, and constantly improving manufacturing techniques. These will eventually spill over into distributed energy inverters; however, a significant R&D effort could accelerate that process so that the "Inverter for the 21<sup>st</sup> Century" could be developed in about 18 months as opposed to ten or more years.

#### **1.1.1. Proposed Program**

The generation of this document was the first step in development of a high reliability inverter. It is a detailed accounting of the existing methodologies required to manufacture a highly reliable product. It includes the preliminary design of a high reliability inverter and discusses in detail the attributes of a mature manufacturer that are required to produce such an inverter. Much discussion is devoted to a universal design; however, the first goal is high reliability and, at this point, the design of the future inverter is not fixed. A grid-tied inverter with backup appears to be the best candidate. The requirement for a mature manufacturer does not exclude existing small PV manufacturers; however, such a smaller company could best demonstrate the required structured manufacturing environment by teaming with larger, more established companies.

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<sup>1</sup> R. Pitt, "Improving Inverter Quality," Proceedings, NCPV Program Review Meeting, April 16-19, 2000, Denver, CO, pp. 19-20.

The objective is to develop a high reliability inverter that has a mean time to first failure (MTFF) greater than ten years with a cost of less than 65 cents/watt. A universal design is desired to maximize the quantity of product produced. The program will first use a systems engineering approach to define inverter requirements. A complete set of specifications will be developed and appropriate technologies identified. The next phase of the program will produce prototype inverters. Two major program elements will be addressed during this development phase, the first will concentrate on automated assembly and the second will concentrate on the inclusion of new emerging technologies. The program will address many areas including the following.

**New Technologies** will be required to achieve the goal of a high performance, high reliability inverter. These are so important that they are introduced in the next numbered paragraph. Much more detail is included in sections from the technical contributors.

**Automated Assembly** results in lowest cost, product uniformity, and improved product quality, but requires assembly of approximately 300 units/day for economic viability. A universal design may be best suited to achieve this product volume. With this approach, the inverter would be designed for use in multiple applications and for multiple technologies. The inverters required for multiple applications can use identical dc-to-ac circuitry ( $\approx 95\%$  of the inverter). Designing a dc-to-dc converter module for each application will support multiple applications (example: a maximum power tracker for PV). Automated assembly will require the involvement of a sophisticated manufacturer with experience in large quantity manufacturing, ISO certification, quality programs, and systems engineering design practices.

**Lowered Conduction Losses** increase efficiency and decrease heating. Every time the semiconductor is switched, transition losses occur during the turn-on/off times. To maintain acceptable losses, the turn on/off losses must be lower in devices switched at higher frequencies. Devices, such as the MOSFET and IGBT, are gated with voltage instead of current and thus require less power in the drive circuits.

**Faster response** can greatly reduce stresses. The integration of "smart" features on board the power device allows much faster response to over-stress conditions. This allows the power device to protect itself and therefore improves reliability of the power module. The development of on-board "smart" features in the application specific intelligent power module (ASIPM) allows for the protection of other system components. For example, overheating of a transformer or battery can be avoided.

Power Electronics Building Block (PEBB) a program, largely financed by the US Navy, is designed to advance the **integration** of power electronics.

**Compliance with Regulations**, such as FCC Part 15 is required for grid-tied inverters. RFI filters that ensure compliance with FCC regulations are commercially available. Other passive components that are used to control the flow of energy may be manufactured in modules that are readily assembled to the laminated bus.

Magnetics are a significant portion of the initial cost, and their weight and bulk have a major impact on inverter size. Bulky inverters further add to the cost of handling and installation. Currently, higher frequency inverters still lower cost due to the reduced size of transformers and inductors.

**Heating** is a major problem with power electronics. The quickest means of reducing heat generation problems is to generate less heat by using devices with lower losses or switching schemes such as soft switching. Advanced concepts that redirect energy from dissipation in components to the output also reduce the heat dissipation needs. Sophisticated computer modeling of heat flow can improve thermal management by identifying hot spots and quantifying heat flow for various physical schemes. Additionally, improved heat dissipation is possible through better bonding, higher heat conductivity materials, and more massive paths for heat conduction.

**Packaging** should remove thermal energy, possess minimal electrical parasitics, maintain high mechanical reliability, reduce assembly time, and reduce cost.

**Laminated DC bus bars** or stripline circuit boards provide low inductance and distributed capacitance with reduced resistance while eliminating some wire connections. A major source of stress to the power-switching device is voltage overshoot that results from the interruption of current through an inductance. Configuring the power switches as components on a stripline or a laminated bus dramatically reduces the series inductance, balances it with built-in capacitance, and thus reduces the voltage overshoot.

**Wire bonds** are potential failure points and contain parasitic inductances. Improved connection methods that remove the wire lead include bonding of copper posts directly to the power device. This requires significant planning in the layout so that all dimensions are compatible. The Virginia Polytechnic Institute is doing considerable work in this area of bonding techniques.

Most power electronics equipment is custom-designed and requires labor-intensive manufacturing processes. These are prone to lower reliability, higher

manufacturing costs, and greater performance variability. A **systems-level design** of inverters, supported by design software, can go far toward improving this situation. More designs can be standardized and configured for automated assembly. The design process should also include power utilities, applications, packaging, maintenance, and supply specialists, as well as power electronics design engineers.

### **1.1.2. The Desired Product**

The desired product is a new inverter with ten-year mean time to first failure (MTFF) and with lower cost. This development will constitute a 'leap forward' in capability that leverages emerging technologies and best manufacturing processes to produce a new inverter for multiple technologies (PV, fuel-cell, storage, etc.) and in multiple applications (grid-tied, off-grid, and UPS). The targeted inverter size is from two to ten kilowatts.

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## **1.2. Approach**

### **1.2.1. A Business Plan**

The first step in the development of a new product is the development of a business plan. Just as a business plan would be required to receive funding from a lending institution, it will greatly enhance the probability of the successful development of an inverter if a business plan is required by all government procurements. This ensures the rigorous review of all the issues related to the

product development. The business plan must show that the company has the resources to develop and fabricate the product, that a market exists, and that sufficient profit will be obtained by sales to justify the product line. Although it is assumed that most businesses clearly understand these issues, the concept is so important that a few points concerning the subject will be made in this section.

**Roadmap to Success.** "A business plan is essentially a map to your targeted destination"<sup>2</sup>. The successful elements include:

*Company Description.* In addition to financial status, the company products, services, and agreements with distributors should be defined. A clear picture must be given of how the company will distribute and service the fielded inverter.

*Industry Analysis and Trends.* Inverter developers must clearly understand potential markets prior to product development. PV has had significant growth, but the opportunities vary according to the world situation. For example, recent concerns over Y2K and grid reliability have opened new opportunities in grid-tied inverters with backup. The manufacturer must target either an opportunity to sell in a large market or have a market niche with little competition. A properly designed inverter can also be used in other applications such as fuel cells. Finally, a clear view of the competition is essential. Target the products expected in the future, not what is working poorly today.

*Risk Analysis.* An honest assessment of what makes your product unique and sellable, what the future market opportunities are, and how flexible the product is to adapt to future trend changes is another essential element of a business plan. For example if the manufacturer develops a grid-tied inverter, how difficult is it to reapply that development to an off-grid inverter. Flexibility reduces risk. The manufacturer must also keep a wary eye on competition. As the PV industry grows it will attract larger and stronger players; failure to anticipate and account for this could result in an unanticipated drop in sales.

*Marketing, Distribution, and Maintenance.* A well-developed marketing plan is essential in today's business environment. Relationships with distributors and a viable means for maintenance are an essential part of that plan.

*Technology Plan.* This will be heart of an inverter proposal and will describe the approach to the development of a high reliability, low-cost inverter. For an inverter the proposed software, its portability, and the required development time are just as important as a description of the hardware.

*Milestones and Long-term Plans.* The milestones in the project and the means for evaluating success must be clearly defined. In this manner one can clearly visualize the success of the product development, the need to seek additional resources, or to change direction. Long-term plans should include product replacement and future products.

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<sup>2</sup> "The Successful Business Plan:", Rhonda Abrams, 2000, "R" Media

*Financial Plan.* A three-year financial plan will include the total cost for product development and distribution and the expected cash flow once the product sales begin. Goals must be clearly established in advance so that the painful decisions associated with a negative cash flow can be made without undue emotional influence.

### **1.2.2. The Next Generation Inverter Will Result From Engineering Innovation**

**Emerging technologies.** There are three emerging technologies that can be used to greatly enhance the performance of inverters; digital signal processing (DSP), made-to-order power electronics, and new control methods such as dead-beat or repetitive control. DSP performs extremely fast signal analysis that provides inputs to low-level decisions (example: control of power bridges) and to higher-level decisions (example: control of battery charging).

The use of **DSP** will provide a reliable, low-cost method for removing dc levels from the ac output, eliminating the need for costly and bulky output transformers. Other DSP benefits include rapid response to utility transients, low harmonic distortion, and a means for switching from current source to voltage source (necessary to change from grid-tied to stand-alone operation). This approach to inverter control will result in fewer parts and longer life.

**Made-to-order power electronics** is a capability that results from the fact that power electronic switches, designed with software, can now cost-effectively tailor a new power module for smaller markets. With the help of DSP, the inverter can now be designed for end-of-life and can be derated as it ages. The inverter layout can also be tailored to the application, thus minimizing parasitic losses, optimizing heat transfer, and resulting in faster switching and lower heat losses.

**New control methods** may result in a lower switching frequency, counting on improved DSP control to ensure power quality while limiting the size and cost of the inverter magnetic components. Conversely, the trend in semiconductor switches toward lower on resistance and lower switching losses has led to higher switching frequencies and larger operating voltages and currents. This new control method could utilize the best of both worlds; lower switch losses and less frequent, lower-stress switching.

### **1.2.3. The Need for Systems Engineering**

Photovoltaics is an emerging technology. The effort planned herein, to develop the next generation photovoltaic inverter, requires careful planning and understanding of the issues. It is thus imperative that a systems engineering

approach be used for the inverter design. Systems engineering is primarily concerned with problem stating, not problem solving. Problem definition should be accomplished in simple language, avoiding ambiguity and the premature selection of a solution. In this process one must determine:

- what the system is supposed to do. For example, if the answer is simply to provide refrigeration for vaccine, then no failures are permitted, and it is known immediately that the system must be over-designed to provide the proper safety for the vaccine.
- how performance will be judged. For example, the refrigeration system can brook no failures. Loss of a single batch of vaccine can be judged a failure.
- what is available to build the system. For example, from the onset one must understand the limitations of batteries in third world countries, and the development status of components such as hybrid inverter,s i.e. are you getting a beta unit.
- methods of resolving conflicting performance specifications. For most systems there is a tradeoff between acceptable cost and high reliability. An example of an additional tradeoff for an inverter would be weight versus peak power.
- testing requirements. All testing requirements must be identified early in the process. For example, if an inverter is required to have rfi (radio frequency interference) levels compatible with FCC requirements, then rfi filters must be incorporated into the design. In addition to requiring the design of the inverter to optimally accommodate filters, the need to achieve FCC compliance could demand other design considerations such as shielding, lower switching frequency, and component placement.

From the problem definition phase one emerges with a specification, a decision on the technology approach, identification of technology challenges, and a test plan.

Design. A key element of successful systems engineering is the involvement of all stakeholders (e.g. manufacturer, suppliers, distributors, sales staff, users, funding authorities) in the development of requirements and the preliminary design. At least one design option should be thoroughly examined by all stakeholders before a prototype is built. Thus potential additions or changes to the design will not challenge “all the work we have done.” Some key elements of the design process are:

- preliminary design and drafting
- modeling
- prototyping

- subassembly testing
- failure analysis
- design review
- build integrated prototype
- testing
- failure analysis
- design review
- final design

**These processes or variations thereof are already in place in many successful companies.**

**New Work:** To accelerate the use of Systems Engineering in the design of PV products and systems Sandia proposes:

1. A guide for preparing RFQ's (requests for quotes) that ensures important elements of systems engineering are included in each acceptable proposal.
2. A guide for industry that outlines the systems engineering process and relates it to PV systems.
3. An outreach program that provides a systems engineering class for interested parties.
4. Software tools to assist in product design will be identified.

Other stages of product development include the following:

**Implementation.** In this phase of development the system/product is taken from the design board to a finished product. Past Sandia efforts in this area have included quality and reliability programs at the manufacturers' facilities. These have resulted in a formal method of configuration control, formal documentation, incoming parts screening, employee training, and other essential components of a quality program. Continued work in these areas will provide big dividends in reliability improvement. Modeling of the system performance will provide a base for comparing actual performance to predicted. If shortfalls in performance are discovered, the modeling will provide a method for identifying and correcting problems.

**Acceptance Testing.** Acceptance testing has long been a part of Sandia's core program. New work in the areas of certification will remove barriers to the implementation of PV Systems. These proposed efforts are discussed elsewhere in this plan.

**Operation.** Operation and Maintenance have long been neglected in many PV systems. This subject is discussed further in subsequent paragraphs.

**Retirement.** Retirement implies that the need for the product is concluded or that a replacement is needed. For example, in a 25-year lifetime PV system the cost of replacement power electronics must be planned for.

#### 1.2.4. Preliminary Requirements

With the understanding that the Inverter for the 21<sup>st</sup> Century will require systems engineering, it is understood that one the task of gathering requirements must be initiated. What follows is a first attempt. The best of all worlds is an inverter that would work with all sources and in all applications with very minimal adjustment. That may or may not be feasible. Thus the requirements are separated into grid-tied and off-grid. An inverter that addressed both applications would combine these two. Further it is important to include "nice to have" characteristics. These are separated from requirements and labeled as features.

### 1. Requirements – All PV Inverters

- a) invert dc to ac (direct current input/ac output)
- b) ten year MTF (mean time to first failure)
- c) efficiency > 94%
- d) UL 1741 certification
- e) meets FCC Part 15, Class B
- f) adequate dc and ac disconnects that meet NEC
- g) heavy duty power connections
- h) dc and ac over current protection (over load of 50% for 30 sec)
- i) nonvolatile memory
- j) HALT (highly accelerated lifetime testing) during development
- k) surge protected per IEEE C62.41

### 2. Requirements – Grid-Tied PV Inverters

- a) cost of < \$.75/watt
- b) TDD (total demand distortion) < 5% (IEEE 519, Table 10.3)
- c) compliance with IEEE 929
- d) power factor can equal one (as allowed in IEEE 929)

### 3. Requirements – Off-Grid PV Inverters (required loads will be defined and will vary with application)

- a) cost of < \$1/watt

- b) supply all loads
- c) resistive, reactive
- d) surge capability adequate to start motors
- e) supply nonlinear current
- f) power quality adequate for load
- g) interface with batteries
- h) manual or automatic control of engine generator battery charging
- i) initiate engine generator battery charging manually or automatically on low voltage or time interval
- j) selection of regulation voltages and time at regulation voltage
- k) automatic or manual equalize interval with programmable regulation voltage and time at regulation voltage
- l) temperature compensation

#### **4. Desired Features – All PV Inverters**

- a) combined grid-tie/off-grid capability
- b) sound pressure level < 80 dB (note: 0 db = 20  $\mu$ Pa, where Pa is the symbol for Pascals)
- c) outdoor operation
- d) light weight
- e) efficiency > 98%
- f) maximum power tracking for PV
- g) dc level compatible with both PV and fuel cell (perhaps 48  $V_{dc}$ )
- h) 120  $V_{ac}$ /240  $V_{ac}$  operation
- i) cooling without fan
- j) observable readings
- k) dc and ac voltage
- l) dc and ac current
- m) inverter on/off
- n) kilowatt-hours provided
- o) communication port for data acquisition & control (SCADA)
- p) installation
- q) twenty minute installation
- r) easy mounting
- s) easy wire connection
- t) parallelable modular assembly (perhaps increments of 1 or 2 kW)

#### **5. Desired Features Grid-Tied PV Inverters**

- a) test jack for utility to validate protection

## 6. Desired Features – Off-Grid PV Inverters

- a) control of battery charging
- b) selection of battery type
- c) three stage charge algorithm
- d) programmable equalize interval
- e) temperature compensation
- f) generator start command
- g) interface with other energy sources
- h) smooth transition from battery to generator & generator to battery (inside ITI curve)
- i) ability to charge batteries from generator
- j) good power quality
- k) sine-wave inverter
- l) meets ANSI C84.1 nominal voltage range during steady state operation
- m) surge power to twice rated power for 10 seconds
- n) high efficiency with low loads (adjustable low load sensing)
- o) automatic shut-down for loads  $< P_{\text{quiet}}$ , ( $P_{\text{quiet}} < \text{few watts}$ )

## **Section 2. Millennium Technologies Inputs**

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### **2.1. Status of Power Electronics**

#### **2.1.1. Importance of Power Electronics**

The importance of power electronics in industrial automation, energy conservation and environmental pollution control has already been reported in several literatures. As the cost of power electronics is falling and the system performance is improving, its applications are proliferating in industrial, commercial, residential, utility, aerospace and military systems. It is expected that this trend will continue with high momentum in this century. Modern computers, communications, and electronic systems get their life-blood from power electronics. Modern industrial processes and transportation and energy systems benefit tremendously in productivity and quality enhancement with the help of power electronics. The environmentally clean sources of power, such as wind, photovoltaics and fuel cells that will be highly emphasized in the future, heavily depend on power electronics.

#### **2.1.2. Present Manufacturing Issues that Affect PV Inverter Lifetime and Cost**

##### **2.1.2.1. Low Volume, Small Manufacturers**

Current power converter systems for renewable energy sources are uniquely designed for each energy source and only suited for one kind of energy source. This translates to low volume and low quality. Because of low volume, mass production techniques are not used. The low volume of power electronic converter systems produced for renewable energy sources restricts the manufacturing base to small suppliers without sophisticated research and reliability programs or sophisticated manufacturing methods.

Inverter manufacturers typically use an analog or analog/micro-processor hybrid control system to control the power converter. There are many problems associated with analog or analog/microprocessor hybrid control systems. They include aging effect and temperature drift of analog devices, higher component count, difficulty in adjustment, high cost, electrical environment inflexibility, low noise immunity and high EMI. An advanced control algorithm is not easily implemented. Also for system monitoring and user interface, a separate microprocessor system must be used. These problems lead to a shorter life and lower quality. All these problems contribute to the fact that existing power electronic converters for various renewable energy sources have a Mean Time to

First Failure (MTFF) of less than five years. This results in unreliable fielded systems and a loss of confidence in renewable energy technology.

#### 2.1.2.2. Inadequate Quality Processes

There are numerous aspects to consider when attempting to effectively solve the difficult technical quality problems of PV inverters. They include: 1) having access to the necessary technical information and skills to accurately analyze the details of the problem, 2) having a disciplined process for analyzing the data, 3) being able to identify solutions and evaluate which is best, 4) having the authority to implement the solution and 5) knowing how to effectively plan the implementation of the solution. However, because of the inadequate quality processes that most PV inverter manufacturers have, it is hard to effectively solve difficult technical quality problems.

A major consideration in high quality manufacturing is discipline. Another issue is documentation control. Typically, design control is one of the most serious problems. In general small manufacturers do not have a system that documents and controls all functions performed on a repetitive basis, (i.e., all processes). Documentation of processes is an absolutely critical requirement for successful PV inverter development and manufacturing. Failure to do so will adversely affect quality.

#### 2.1.2.3. Minimal Staff With Inadequate Time

In poorly staffed companies, manufacturing engineers will spend more than 90 percent of their working time in troubleshooting. They have the mentality of “quick fix,” because they have minimal staffs with inadequate time. Also the development engineers are frequently under intense pressure to bring products to market as quickly as possible, often because of the unrealistic schedules imposed by management. Shortsighted attitudes are frequently imposed on engineers. This must be controlled because time to market is not just design time, but also the time it takes to get a product into the customer’s hands at a competitive price. If it takes multiple redesigns to meet specifications or to lower manufacturing and test costs, and/or to fix glitches because of inadequate design verifications, the advantage of rushing a design is negated.

#### 2.1.2.4. Minimal Pre-field Testing

Because all PV inverter manufacturers face the pressure of time-to-market, they tend to bring the product to market with minimal pre-field testing; this is a mistake. Accelerated testing methods are not widely implemented in this industry. Sometimes, testing and test methods are not clarified during the development of the product modules. Electrical, mechanical, material, physical, and environmental test are not specified in the early design stages. The design team does not implement the appropriate application of concurrent engineering

and methods when the design criteria are reviewed and analyzed during the development process.

#### **2.1.2.5. Company Features that Enhance Product Reliability**

The above observations lead to a minimal set of issues that must be addressed in order to produce a highly reliable product. These include:

- adequate technical and management staff
- access to adequate facilities for manufacturing
- in-place quality program that includes
  - documentation of manufacturing procedures and processes
  - configuration control
  - training
  - inspections
  - formal system for feedback and correction of problems.

Also essential is experience in system engineering including:

- development of customers
- development and validation of system requirements
- definition of performance and cost measures
- design review process
- reliability engineering to include a formal system for documentation and problem correction.

## **2.2. Tools of a Mature Manufacturer**

### **2.2.1. Some Manufacturing Issues**

To optimally design an assembly line one needs to understand the nature of the product. The expected volume and product characteristics determine what type of production line is suitable for an application. There are nine different types of production line that could be chosen from. These manufacturing techniques are listed below:

- 1) Craftsmanship cells: Craftsmanship cells are single person work stations where the assembler typically performs multiple operations that require a high skill level and extensive training.
- 2) Manual assembly cells: Manual assembly cells are areas of mechanical assembly that are usually sub-assemblies for printed circuit boards or chassis / top assemblies. These cells are usually located adjacent to the next level of assembly.

- 3) Component prep islands: Component prep islands are isolated work areas where various circuit board components are usually routed through the work center before proceeding to the point of assembly. They consist mainly of semi-automated component lead bending and cutting machines. They may also contain various fixtures and custom tooling for lead cut-off and component height spacing. These islands occasionally perform circuit board component sub-assembly such as heat sinks and power transistor attachment to heat sinks.
- 4) Manual assembly islands: Manual assembly islands are isolated areas of manual product assembly always divided into cHASSis/top assembly or printed circuit boards. No conveyors are used and the batch (kit) sizes vary widely.
- 5) Manual assembly lines – with conveyors: Manual assembly lines with conveyors (powered and un-powered) are lines of various numbers of assemblers performing printed circuit board assembly or cHASSis / top assembly.
- 6) Automation islands – through hole: Automation islands – through hole, are comprised of through hole component insertion machines that are sometimes inline connected by conveyors.
- 7) Automation islands – surface mount: Automation islands – surface mount, are always a complete process including a solder paste printer, component placement, and solder reflow, all usually connected in line by conveyors.
- 8) Automated conveyor lines with integrated manual assembly stations: Automated conveyor lines with integrated manual assembly stations are comprised of through hole component insertion machines and various numbers of manual assemblers usually performing printed circuit board assembly.
- 9) Fully automated assembly lines: Fully automated assembly lines are comprised of through hole component insertion machines and/or surface mount process equipment and are always a complete process including solder reflow and/or wave solder machines. Always connected in line by conveyor systems.

### **2.2.2. Utilizing an Experienced Manufacturer**

A high volume experienced manufacturer who has the ability to manage the production line design and manufacturing process will significantly enhance reliability. To optimally design an assembly line specific for PV inverter application, the use of proven and sophisticated “Program Management Tools” is essential. These tools consist of the following elements:

- 1) Implementation planning/Advanced quality planning
- 2) Microsoft Project timing/Master dot methodology

- 3) Action item tracking/Reporting/Act-Fast format
- 4) Budgetary controls/Project cost matrix
- 5) Process evidence books/Summarizes simultaneously
- 6) Engineering (process development) results
- 7) Weekly project status & issues meeting/Identify needs
- 8) Change management/Summary roll-ups every 2 weeks
- 9) Project business meetings/Review status & issues
- 10) Internal timing meetings/Review status & issues
- 11) Executive review every 2 months/status & issues

With the help of the above-mentioned program management techniques the design of an optimal assembly line for PV inverter systems, will gain the following benefits:

- a) Consistent proven approach for all phases of the project
- b) Direct communication flow with the PV inverter designer
- c) Strong budget focus and emphasis on cost reduction
- d) Constant emphasis on timing and meeting milestones/delivery dates
- e) Quality assurance and system performance
- f) Single point of contact dedicated to the project
- g) Overall control and responsibility at top management

We can use the “Five Phase Approach” that has been used by most high volume automotive applications:

- Phase 1: Implementation planning/Scope definition
- Phase 2: Process integration/Mouse-to-Machine (M2M)
- Phase 3: Design & Build/Cost Validation
- Phase 4: Integration/System run-off
- Phase 5: Installation/Lunch? support

This “Five Phase Approach” is further divided into the following 7 steps:

- Step 1. Conceptual Development
  - Understanding of customer expectation
  - Establish preliminary project direction
  - Generate 2 conceptual ideas
- Step 2. Discrete Event Simulation
  - System throughput analysis
  - Labor & robot utilization

- Models from IGRIP
- Models & experiments maintained for the life of project
- Customer's confidence in solution
- Value added analysis
- Step 3. Process Development
  - Detailed process development
  - Cycle time analysis
- Step 4. Work-Cell Simulation
  - Cell configuration finalization
  - Facility layout
  - Safety requirements
  - Tooling and equipment content established
- Step 5. Systems Design
  - CATIA tool design established
  - Tooling and equipment verification
  - Final design
- Step 6. Process Verification
  - Final tooling check
  - Final robot paths
  - Final safety buyoffs
- Step 7. System Start-Up
  - Download program
  - All models and paths updated as build condition

The result from using these techniques are listed as following:

- (1) Speed
- (2) Quality
- (3) Value

### **2.2.3. ISO-9000 and Quality Management Systems**

ISO-9000 is an **internationally recognized and accepted standard** that specifies the quality system to be established by manufacturing and service firms. It also is a system for establishing, documenting and maintaining a management system for ensuring consistent quality, minimizing waste and increasing corporate efficiency.

ISO-9000 is **important** because:

- It utilizes standards that are necessary to do business in a global economy.
- It supports new quality philosophies that emphasize the control of processes via total cooperation.
- It recognizes that world markets demand higher quality and lower costs.
- It helps to reduce unplanned variations in the processes we use, which increases the efficiency of cooperation and the quality of the products.
- It also helps the company to define processes, which reduces both the cause and occurrence of variations.

ISO-9000 **is or will be a necessary requirement** to do business with many domestic and international companies. Many companies that have implemented ISO-9000 have a distinct advantage in the market because their quality system is certified and is not a point of concern when a customer is considering suppliers.

The primary **goals or purposes** for implementing the ISO-9000 quality management program are:

- Corporate Efficiency
- Customer Satisfaction
- The secondary results from achieving these goals are:
  - Departmental Cooperation
  - Increased Product Quality
  - Increased Productivity
  - Increased Customer Base
  - Improved Finances

The Quality Management System **requires** a “culture” of quality throughout the organization, in other words, the responsibility for quality goes beyond the manufacturing floor to every area in the organization from sales to shipping and every function in between. The Quality Management System is to improve how we make things, and how we do things. Two important aspects of achieving cultural change in an organization are education and cooperation. Employees need to know what their responsibilities are, to understand how they perform their responsibilities affects other departments, and to understand what is expected in order to contribute to the corporate goal.

The key to a successful Quality Management System is **documentation**. In order to perform a function consistently in the most efficient manner, that function must be documented. This is the most demanding and time consuming of tasks, yet is the single most important aspect of a Quality Management System.

The basic philosophy behind the ISO-9000 Standard is “say what you do and do what you say”, within the elements of the standard, and be able to prove it if required. Documenting the necessary functions in the company and reviewing these procedures, results in improvements and a better understanding of inter-departmental cross functions.

### **Experience in Management of Cost, Production, Marketing and Accelerated Testing, and Adapt Just-in-Time System**

Having a PV inverter production line set up is only half of the task. Implementation of various manufacturing techniques that are specific to the PV inverter systems is also needed. Further a reduction in assembly time for components that are specific to PV inverter systems must be examined. For example, reductions in assembly time are achievable due to the fact that it can take less time to assemble one module into the next level assembly than it does to pre-assemble various components, encapsulate them, and test them prior to the insertion of the in-house built unit into the next level assembly.

Reductions in component level testing are achievable when the module is pre-tested, or tested in the system, rather than testing all of the individual components prior to, or during, the various assembly operations that may be required.

Simplification of rework, field repairs, service, and maintenance is achievable because one module is simply easier to work with than several different parts or components.

Keeping components and subsystems small and modular also enables local control of faults and minimizes development time. These are steps that are needed to efficiently produce high quality PV inverter systems.

Another interesting finding is that in today’s competitive market designing a product or developing a technological breakthrough is only half of the challenge. The other half is getting products introduced onto the market quickly, in sufficient volume, and at a reasonable price. To meet this challenge, we need to restructure the engineering department. Instead of keeping the R&D engineering and manufacturing/sustaining engineering group separate, we need to integrate them into one.

Final test is an important part of most power supply manufacturing operations. Testing is a type of inspection and should be eliminated whenever possible; however, the final unit test is usually a necessity. Workers wanting to cut processing time can avoid putting units through final test, shipping these units with possible defects. The temptation to do this rises as test yields go up.

A test stamp, placed on a completed power supply, is a traditional indicator that tests have been completed. This method is flawed for several reasons. Testers “save time” by stamping a group of units at one time instead of waiting until each one has passed test. When breaks or lunches occur, it may be difficult to remember which units have been tested, especially if someone has moved the units around. In other cases, units may be packed without the final test stamp and inspectors have not noted this.

To eliminate final inspection for a test stamp and to ensure that only tested units get shipped, this process can be programmed into the test set to signal the shipping label printer when the test has passed. The label will be printed only when the test has passed. To use an even more detailed methodology, the serial number of the unit can be scanned into the test set to ensure that the label is printed only for that particular unit.

The concurrent engineering approach also can help to reap larger profit over the life of the product. The overall product cycle in the business moves in the direction of design, manufacture, test, and finally service. The design activity is a non-recurring cost, or at least it is supposed to be, while the others are recurring activities. The objective of concurrent engineering is to make the right decisions during the nonrecurring activity. By making good decisions early, we can maximize productivity during the recurring activities that may last for years.

In order to achieve a 10-year life for the PV inverter, new methods have to be explored to test the units. We have researched the HALT and HASS methods. It is believed that, by employing these reliability measurement methods in the PV inverter’s development and manufacturing process, the life-time and reliability of the product will be greatly increased.

## **2.3. Design and Manufacturing Approaches that Can Lower Cost and Increase Lifetime**

### **2.3.1. Overview and Definitions**

In recent years, the test techniques known as HALT<sup>3</sup> (Highly Accelerated Life Testing) and HASS (Highly Accelerated Stress Screening) have been gaining advocates and practitioners. These test methods, quite different from standard life testing, design verification testing and end-of-production testing, are becoming recognized as powerful tools for improving product reliability, reducing warranty costs and increasing customer satisfaction. This report provides a basic description of these techniques, highlights the differences between these techniques and more conventional testing and provides a guideline for their implementation. HALT is a test that is performed on a product as part of the design process. Typically, it is performed on a product when pre-pilot or pilot run units are available, before the design verification testing begins. During HALT, a

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<sup>3</sup> G. K. Hobbs, *Accelerated Reliability Engineering, HALT and HASS*, John Wiley & Sons, 2000.

product is stressed far beyond its specifications as well as far beyond what the product will encounter in a typical use environment. The actual functional and destruct limits of the product are found and pushed out as far as possible. These limits are used as the basis for the performed on products built as part of the production process. Since HALT is required for the implementation of HASS, HALT will be discussed first.

### **2.3.2. HALT Verses DVT - the Difference is the Purpose**

When first exposed to the concept of HALT, many design engineers are skeptical of the method. Much of this skepticism stems from the fact that these engineers are used to doing standard life testing and design verification testing, and the HALT methods differ so dramatically from these conventional methods that they seem to be almost at odds with them. The key to understanding the value of HALT lies in understanding the basic difference in the purpose of the testing being done. The basic purpose of Design Verification Testing (DVT) is well understood - it is to demonstrate that the product meets its specifications, and to demonstrate that the product will function in its intended environment. DVT is considered successful when all the tests are passed, with no failures detected. The purpose of HALT is dramatically different. In HALT, the goal is to over-stress the product and to very quickly induce failures in the product. By applying these stresses in a controlled, stepped fashion, while continuously monitoring the product for failures, the testing results in the exposure of the weakest points in the design. At the completion of HALT, the functional and destruct limits of the product are known, and a "laundry list" of design and process limitations are defined, with corrective actions often defined as well.

In short, the goal of HALT is to quickly break the product and learn from the failure modes the product exhibits. The key value of the testing lies in the failure modes that are uncovered and the speed with which they are uncovered. HALT is considered a success when failures are induced, the failure modes are understood, corrective action has been taken, and the limits of the product are clearly defined and extended as far as possible.

Unlike DVT, HALT is not a pass/fail test. It is a process of discovery and design optimization. Although these failure modes are induced by stresses in excess of specification, they are typically valid failure modes that would show up in the product in the field. A full failure analysis of all modes found will help confirm this. The important thing to remember is that HALT is finding the weakest parts of the design. These weak links will be the source of warranty problems in the field. The controlled over-stresses applied during the HALT process simply accelerated the precipitation of these failures to allow early detection and correction. The advantage of HALT is that it quickly finds failure modes that would not be brought out in DVT. A typical HALT will take only three to five days. Because the purpose of the tests is so clearly different, HALT is not intended to replace DVT. It is true that HALT will find most, if not all, of the failure modes that would show up in DVT (along with many more). However, HALT will not provide you with the documented evidence that you often need to prove that your

product meets specification. By doing HALT before DVT is started, you help insure that your DVT will be completed in one pass, with no defects found. This will greatly speed your time to market, avoiding the slow process of repeating DVT until no more failures are precipitated and detected.

### **2.3.3. Choosing HALT Stresses and Equipment**

The basic concept of HALT can be implemented using many different stresses. However, the stresses most often used are thermal extremes, extreme thermal rates of change, vibration and the combination of thermal and vibration. Other stresses, such as voltage margining, frequency margining, power supply loading and power cycling can also be applied, resulting in additional valid failure modes being exposed. It is worth remembering that HALT is not intended to demonstrate that a product will function in its intended environment. Consequently, the stresses do not attempt in any way to duplicate those expected in “real life”. Rather, the stresses are specifically designed to quickly bring out failure modes. This logic affects the choice of chamber used to apply the stresses as well as the type of vibration fixturing used and the routing of the air flow through the product. Given that extreme stresses are to be applied, the chamber must be capable of reaching both hot and cold thermal extremes, executing very fast thermal ramps and providing high vibrational energy that will quickly bring out failure modes. This, of course, precludes the use of mechanical refrigeration systems. The vibration system that has been proven to be the most effective for HALT is a Repetitive Shock (RS) system with a wide frequency and acceleration range and six degrees-of-freedom vibration. In order to rapidly and effectively bring out failure modes it is important to excite the product at the resonant frequency of all assemblies, sub-assemblies, components and leads and legs of components in the product. This is regardless of what that resonant frequency, or the orientation of the assembly or component, may be. An RS shaker, designed to provide energy from 2 Hz to 10,000 Hz, will do this most effectively.

### **2.3.4. Preparing for HALT and Planning the Test**

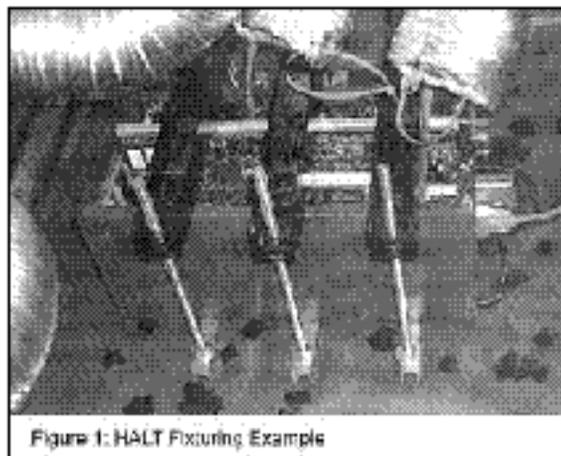
Once the purpose of HALT is understood and accepted, the process and stresses used during the testing begin to make more sense. Because the stresses applied are increased until failure occurs, it is not necessary to test a large population of product to insure that a failure mode will be found. A relatively small sample - typically 4 to 6 units - is adequate. This number will allow verification of a failure mode in more than one unit as well as providing for a spare or two in the event of a catastrophic failure of a unit under test. In order to preserve these samples and get as much information as possible from them, the stresses are applied starting with the least destructive and going to the most destructive.

For the thermal and vibration stresses, this means starting with cold step stressing, then hot, then rapid thermal extremes, then vibration, followed by a final combined thermal/vibration environment. If the product being tested is more

complex than simply a single board or small system, then one of the first questions to consider is what level of the product to test. In general, the goal of HALT is most effectively met by testing at the lowest possible subassembly. Card cages or other assemblies can dampen vibration and block air flow, reducing the stresses applied to subassemblies inside them.

Of course, the trade-offs of functionality and testability must be considered. Also, there will be interconnect circuitry and connections that may not be tested at the subassembly level. An ideal HALT on a complex product would include HALT on all subassemblies, with a final HALT on the upper level assembly as well. The functional test equipment used during HALT is extremely important. Since the value of HALT is the detection of failure modes induced, it is critical to be able to detect the failures when they happen. This means that the units under test must undergo complete diagnostics while they are being stressed. Much valuable information will be lost if the product is stressed without being monitored, then removed from the stress and tested at ambient. By testing under stress, you will be able to detect “soft” failures that only show up under a particular stress or combination of stresses. These soft failures define the operating limit of your product, and can be the source of troublesome “no defect found” failures when the product reaches the field.

The vibration fixturing used in HALT is very different from that used when testing with typical Electro-Dynamic (ED) or hydraulic shakers. In HALT, the fixture is not designed to mimic the real-life mounting of the product. Instead, it is designed to maximize the transmission of energy into the product to speed the precipitation of failures. This results in simple, inexpensive fixturing with the goal of simply clamping the product to the vibration table as tightly as possible. Figure 1 shows a typical product fixtured in a HALT chamber. To maximize air flow through the product as well as to improve the transmission of the low frequency energy, the product is set up on an aluminum u-channel rather than being placed directly on the table top. The u-channel across the top of the product and the all-thread rod and nuts clamp the product to the table.



Airflow through the product is also planned with the HALT goal in mind. Using flexible air ducts, the airflow is routed to maximize the temperature rate of change on the thermally sensitive parts of the product and to insure that all parts of the product experience maximum temperature extremes. The normal airflow through the product during use is not considered when the ducting is designed. If necessary, holes should be cut in the product's case to allow sufficient air flow across its components. To aid in failure analysis and to insure that the stresses are being coupled into the product effectively, it is important to instrument the product under test. Thermocouples should be placed at key points on the product, and accelerometers can be placed on boards and subassemblies to evaluate the transmission of energy into the product. However, the actual accelerometer placement should be delayed until after the thermal portion of the stressing is complete, since the accelerometers would be exposed to stress levels that may shorten their life.

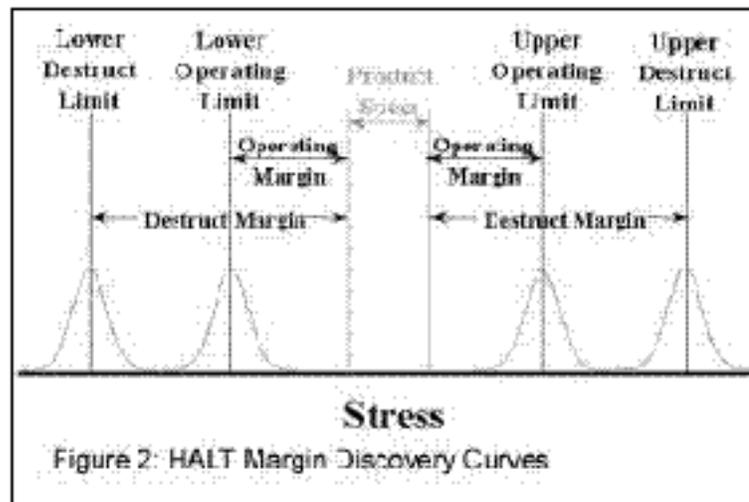
A final, important part of the HALT setup is to clearly define what parameters in the product will be monitored, and what constitutes a failure. This fairly obvious step in the test process can be easily missed, making the interpretation of HALT findings more difficult.

### **2.3.5. Margin Discovery – the Core of HALT**

With the test set up, the process of Margin Discovery can begin. As mentioned above, HALT will uncover the operational and destruct limits of your product. During testing, the stress is steadily increased in a stepwise fashion, with a complete functional test done at each step. The operational limit is defined as the stress necessary to cause a product to malfunction, but the product returns to normal operation when the stress is removed. Essentially, it is the point of “soft” failure. The destruct limit, as you may guess, is the level of stress necessary to cause a permanent, or “hard” failure to occur. The difference between these limits and your operating specifications is your margin for that particular stress. As the failure modes are found and eliminated that are responsible for these limits, you push the limits further and further out, maximizing your margins and increasing your product's life and reliability.

Figure 2 graphically represents these limits. The stress applied is shown in the X axis, with number of failures shown in the Y axis. The curve drawn around each of the limits represents the distribution of the failure that is responsible for that particular limit. The operating specifications and margins are also shown. This figure can be helpful in gaining an intuitive understanding of the value of HALT. Consider a failure mode – say, a high ripple on the output of a power supply – that causes a unit under test to fail. If you were able to test hundreds of units, you could see and understand the distribution on that failure mode, as sketched on the graph.

However, you do not typically have that luxury. By increasing the stress until the failure is seen, then it doesn't matter where in that distribution the unit under test falls – the failure mode will be detected. If the tail of that distribution happens to fall in the operating specifications, then the failure mode would have been an out-of-box failure mode on some fraction of your products. By doing HALT and stressing to failure, you will find the failure mode without having to hope that your sample size is big enough to exhibit the failure within operating specifications. But, what if the tails of the distribution are well outside of the product specification, as shown on the graph? Is the high ripple a failure mode that can be ignored? Consider for a moment what happens to this distribution and the limits as your product ages in the field.



Components fatigue and begin to drift out of specification, power cycles and lightning strikes stress the product, and these limits begin to creep in. If you have chosen to ignore the failure, then you will find that it is one of the first failures to begin showing up in-warranty issues. By pushing the stress until the failure occurs, you have effectively accelerated time, precipitating a failure mode in just a few days that could have taken months to come up in the field. As illustrated in the above example, a failure mode found beyond the operating limits of the product can, indeed, be a “valid” failure mode that could cause warranty problems in the future. However, it is also clear that you may find a failure mode that is completely due to the extreme stress applied, and would never occur in the field.

Consider a failure mode precipitated by the softening of a plastic boss at high temperature. A brief failure analysis will reveal that the distribution on this failure mode is clearly understood, will never have a tail that is in the product specification, and will not shift with time and fatigue. Consequently, this failure mode can be safely ignored. Of course, the distribution on most failure modes is not that easily understood. This is one reason why a complete failure analysis is always necessary on HALT failures. In general, it is unusual when a HALT

failure can be safely ignored. It is important to resist the urge to ignore a failure mode simply because it happened outside of the specification for the product. As you test to higher and higher extremes of stress, pushing limits further and further, an obvious question comes up – When do I stop testing?

The stopping point will be either the limit of the test equipment, or the fundamental limit of the technology. This fundamental limit is the point where multiple failures begin to occur with small increases in stress. Failure analysis reveals fundamental and catastrophic failures across several devices, with corrective action being prohibitive or impossible. In vibration testing, multiple components are coming off the board. With this understanding of the margin discovery process, the process of margin discovery can begin. As described earlier, stresses are applied starting with the least destructive and progressing to the most destructive. This helps conserve samples.

Cold step is done first. Cold step testing begins at ambient temperature. The temperature is dropped in 5° C steps. At each step the temperature is allowed to stabilize for 10 minutes. This dwell time helps ensure that the entire product is stabilized at this temperature, and makes the testing more repeatable. At the end of 10 minutes, a full functional test of the product is done. If the product passes, the temperature is dropped again, and the process repeated. When a failure occurs, the testing is stopped and an investigation into the failure is done. Often, once the failure mode is defined, it is possible to “work around” the failure with a quick patch and continue testing, saving the intensive failure evaluation for later. As described above, this step process is continued until you reach the limits of your test equipment or until you reach the fundamental limit of the technology.

After the cold step is completed, hot step testing is done in a similar manner. Again, testing is started at ambient, then increased in 5° C steps. The dwell and functional testing are identical to those done in cold step testing.

The third stress applied in HALT is rapid thermal extremes. Now, the product is functionally tested continuously while the product temperature is changed as rapidly as allowed by the chamber. The upper and lower limits of these ramps are determined by the results of the step stressing, and stay within the operating limits found there (there is no point in repeating failures that were found earlier). If the product cannot tolerate these maximum thermal ramps, then the ramp rate is decreased, and then increased in a stepwise fashion, similar to the thermal step stressing. When failures are encountered, they are addressed in a similar fashion as before.

With the thermal only portion of the testing completed, the product is now exposed to vibration. With accelerometers applied to the product to verify adequate energy transmission to the product, vibration testing is begun at a stress level of three to five GRMS. Just like in the thermal phase, there is a 10-minute dwell, and then a complete functional test of the product is executed.

Again, the stress is stepped up, in three to five GRMS increments, until the chamber limit is reached or you begin to see the catastrophic failures indicative of the fundamental limit of the technology.

The final environment is combined stresses, thermal and vibration. Now, the temperature is ramped as it was during the “rapid thermal extremes” portion of the testing, while the vibration is stepped up as it was during the vibration only portion. It is important to remember that the HALT will be made more effective if additional stresses can be incorporated. By combining more and more stresses, you will bring out failure modes that may occur in the field only under a unique stress situation. This can eliminate a failure mode that could cause a lot of headaches if you were forced to look for it using traditional methods, after the product was released. At the completion of the step stress testing, you will have found many valuable failure modes for your product. You will have a clear understanding of the margins in your product. You will know not only what your limits are, but WHY they are where they are, giving you a unique understanding of the weaknesses in your product. After doing a root cause failure analysis on all failures found and implementing corrective action, you can do a verification HALT to test your fixes and make sure you have not introduced any new “weak links” in the design with your changes. In the end, you will have optimized the design of your product so that it will last as long as possible in the field.

### **2.3.6. HASS – Maintaining Optimization**

After your design is ruggedized through HALT and you have completed DVT, you will begin production. As anyone who has seen a product into production knows, the production process can introduce many failure modes that are not related to a faulty design, and the sustaining process can certainly introduce new design problems. HASS is intended to catch these new failure modes more quickly and more effectively than burn-in or other ESS testing done in production. Once again, an understanding of the purpose of the test is helpful. Burn-in is designed to weed out infant mortality in a product, aging it to induce early life failures before the product ships. HASS has a broader purpose. The goal in HASS is to verify that no new “weak link” has crept into the product since HALT that has shifted either the operational or destruct limits found in HALT. An important first step to setting up HASS is the completion of HALT on the product. The HASS limits will be set based on the operational and destruct limits found in HALT. Prior to setting up HASS, it is important that corrective action has been implemented on all HALT failures and a verification HALT has been done.

#### **2.3.6.1. The HASS Process and Equipment**

The equipment used to do HASS is similar to that used in HALT, although often a larger chamber is used to accommodate production quantities. The fixturing can be quite different in HASS, simply to accommodate the production flow. The speed with which product can be fixtured in the chamber becomes important, as well as maximizing the number of products in the chamber. Quick release

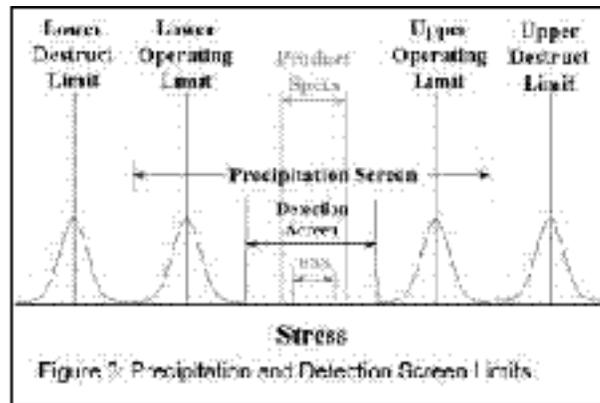
clamps are often used in lieu of nuts and bolts for securing the product. An important part of designing a fixture for HASS is the mapping of the fixture. The goal is to insure that the vibration and thermal stresses at each point in the fixture are roughly equal (although precise uniformity is not important). Mapping the fixture involves taking accelerometer and thermocouple readings on a product in each of the fixture locations. It is important the fixture is completely loaded with product for the test, since the load will affect the vibration characteristics. Thermal inconsistencies can be corrected by changing air flow through baffling or other air distribution changes. Vibrational inconsistencies can be corrected through fixturing changes, with the introduction of dampening materials or changes in clamping mechanisms. During HASS, the stresses are applied simultaneously. Typically, the product is subjected to continuous vibration while the temperature is ramped between its limits, with short dwells at the extremes.

#### 2.3.6.2. Defining the Screen

The levels of the stresses to be applied during the screen are based on the limits found during HALT. There are two parts to the screen. The first part is the Precipitation screen. This screen stresses the product beyond the operational limits and near the destruct limits found in HALT. It is intended to precipitate failures in the product due to latent defects. Because the product is being stressed beyond its operational limit, you do not expect it to function properly, so no testing is done on the product at this point. The product should be powered, however, since applied power can be a significant stress for the product in itself when combined with the other stresses of HASS.

The second part of the screen is the Detection screen. During the Detection screen the product is stressed to near the operational limit found in HALT. Now, the product is being functionally tested. Any hard failures induced during the Precipitation screen will be detected, as well as any soft failures that may be induced by the stresses. Figure 3 can provide an overview of the purpose and limits of these screens. It shows the margin discovery curves, overlaid with the Precipitation and Detection screens. The limits on the screens are set so that they are outside of the tails of the distribution of the failure mode(s) that define the operational and destruct limits for the product. Consequently, product that has no new latent failure modes should pass the screen undamaged. Any new failure mode, however, will be exposed. Figure 4 illustrates a typical thermal profile for a HASS screen. There is one key problem with setting up the limits on the screens from this data – the small sample size used in HALT means that you really have no idea what the distribution looks like on these limits or where the tails may be. Consequently, a more empirical method is used. A baseline for the stresses is derived by guard banding the limits found in HALT.

Typically, vibration is reduced by 50% and thermal excursions are reduced by 20%. These limits can be used as a starting point for the Proof of Screen process. Proof of Screen (PoS) is a critical part of HASS implementation. The goal of PoS is to demonstrate that the screen will reliably find defects without



inducing failures or significantly reducing the life of the product. The process of PoS is fairly straightforward. A sample of product – typically a full chamber load – is run through the proposed HASS multiple times. The sample includes some seeded failures – perhaps some “no defect found” failures from field trials. The final configuration of the screen will depend on two factors – the number of cycles through the screen necessary to precipitate the seeded failures, and the number of cycles of good product is able to tolerate before exhibiting end-of-life failures.

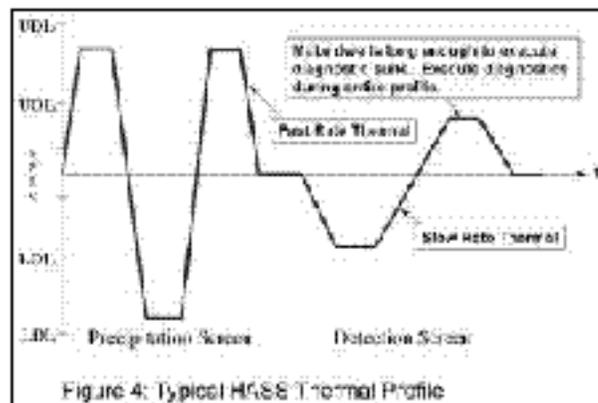
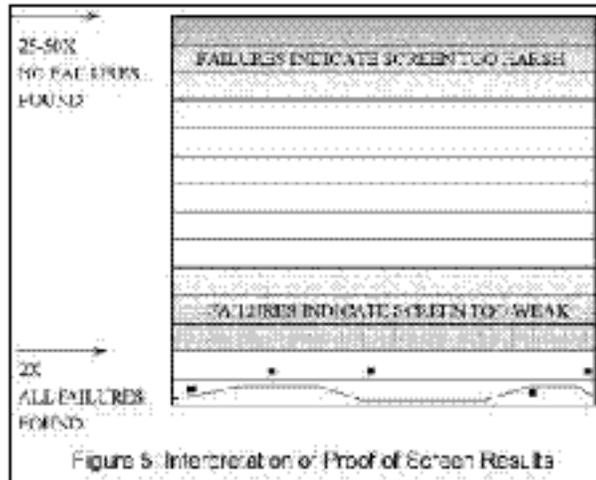


Figure 5 demonstrates the logic behind PoS. Ideally, one or two cycles through the screen will precipitate all the seeded failures. This will yield a short, efficient screen, typically lasting less than two hours. As Figure 5 shows, if seeded failures are not precipitated until several passes through the screen, then the severity of the screen should be increased. This part of the PoS verifies that the screen will reliably find defects. Multiple repetitions of the screen will demonstrate that the screen is not taking an unacceptable amount of life out of the product. Ideally, good product will tolerate 20 to 50 passes through the screen without exhibiting failures. If end-of-life failures are seen before 20 or more cycles are complete, the screen may need to be reduced in severity.



A rough estimation can be made of the amount of life being removed from the product by the screen by simply comparing the number of cycles in the proposed production screen to the number of cycles necessary to cause end-of-life failures to occur. For example, if your production screen consists of two passes through the precipitation and detection screens, and your proof of screen showed that 20 cycles through the screen induced no end-of-life failures, then your screen is removing less than 2/20, or 10 %, of the useful life of your product. The stress levels can be adjusted, or the vibration duty cycle can be changed, to achieve the proper balance between the number of cycles necessary to bring out defects versus the amount of life being taken out of the product. If stresses are increased as a result of the PoS, the PoS must be repeated on new, unstressed samples. In reality, it can often be difficult to seed failures sufficiently to accurately verify that the screen will find defective units. Consequently, it is typically necessary to make a conservative estimate of the number of passes through the screen that are necessary, then tune the screen after a reasonable population of product has been through it.

If you find that all of your failures are being precipitated in the first one or two passes through the screen, then no more than two passes should be necessary. Conversely, if you are running three passes through the screen and are seeing equal failures in each pass, you should either make the screen more aggressive or increase the number of passes through the screen. Once your HASS process is defined and proven, it is not necessarily “set in stone”. Product changes can bring acceptable changes in the limits, if they are understood. However, it is always important to base your decisions on a complete failure analysis and a thorough understanding of the impact of the change. Remember that a verification HALT is a useful tool when considering these changes.

### 2.3.7. Accelerated Testing Summary

A clear understanding of the unique goals of HALT and HASS provides the basis necessary for introducing the techniques into an R&D and production process. This understanding will also enable you to intelligently make changes in the process. If carefully executed, the end result will be increased product life and reliability, reduced warranty expenses, faster time to market and delighted customers.

## **2.4. Current State-of-the-Art Technologies**

The current state of power semiconductors and inverters is summarized below.

### **2.4.1. Power Semiconductor Devices**

Today's progress in power electronics has been possible primarily due to advances in power semiconductor devices. Historically the power electronics age began with the invention of glass-bulb mercury-arc rectifier at the beginning of last century (1901). The modern era of solid-state power electronics started with the invention of the thyristor in the late 1950's. Gradually, other devices, such as the triac, gate turn-off thyristor (GTO), bipolar power transistor (BJT), power MOSFET, insulated gate bipolar transistor (IGBT), static induction transistor (SIT), static induction thyristor (SITH), MOS-controlled thyristor, and integrated gate commutated thyristor (IGCT) were introduced. As the evolution of new and advanced devices continued, the voltage and current ratings and electrical characteristics of the existing devices began improving dramatically. Power electronics evolution generally followed the device evolution. Also, the advances in microelectronics have heavily influenced device evolution.

### **2.4.2. Status of Converters (Inverters)**

In addition to device evolution, innovations in converter topologies including Pulse Width Modulation (PWM) techniques, analytical and simulation methods, control and estimation techniques, computers, digital signal processors, Application Specific Integrated Circuit (ASIC) chips, control hardware and software, etc. have also contributed to progress in power electronics. A converter uses a matrix of power semiconductor switches to convert electrical power at high efficiency.

The most common type of converter operating on a utility system is the Graetz bridge. Diode or phase-controlled converters using thyristor type devices distort line current and thus degrade power quality. The latter, particularly, deteriorates line power factor. Rigorous IEEE-519(US) and IEC-1000(European) standards have been formulated to restrict harmonic loading on the utility system. The IEEE-519 standard limits harmonic loading at the point of common coupling by the consumer (but not the individual equipment), whereas IEC-1000 restricts harmonic generation by individual pieces of equipment. Since diode and thyristor

type converters are very common and have increasing quantities connected to utility systems, various types of passive, active and hybrid filters have been proposed to combat distortion problems.

In the 1960's, when inverter-grade thyristors appeared, various types of voltage-fed force-commutated thyristor inverters, such as the McMurry inverter, McMurry-Bedford inverter, Vehoef inverter, ac-switched inverter and dc-side commutated inverter were introduced. Many other commutation techniques were highlighted in the literature. However, this class of inverters gradually faced obsolescence because of the advent of self-commutated GTO's and bipolar transistors. BJT's became obsolete with the advent of IGBT's; MOSFETs and IGBTs have now replaced the BJT almost completely. The recent introduction of S-FET technology in 1996 enabled very low on-state resistance in the low voltage range ( $V_{br} < 100 \text{ V}$ ; e.g.,  $R_{dson} < 6 \text{ m}\Omega @ V_{ds}=30 \text{ V}$ ). The development of the Cool-MOS<sup>4</sup> in 1998 enabled a further reduction of the on-state resistance  $R_{dson}$  by the factor of 5 to 10 compared to a conventional vertical MOSFET for the same chip area in a voltage of  $V_{br}=600\text{-}1000 \text{ V}$ . The introduction of vertical p-strips in the drift region and the resulting extension of the space charge region also in the horizontal direction, allow a distinct reduction of the device thickness and therefore reduced on-state and switching losses and a lower gate drive power of the Cool-MOS. Today, MOSFETs are available up to a maximum switch power of 100 Kva. IGBTs have gained significant importance since their introduction on the market in 1988. Today there are 600 V, 1200 V, 1700 V, 2500 V, and 3300 V IGBTs up to currents of 2400 A on the market. Samples of 4500 V IGBTs have been tested in the laboratories of several device and converter manufacturers. Recently Eupec introduced 6500 V IGBTs for currents of 200 A, 400 A and 600 A. Samples of 6500 V IGBT modules are available. The device structure allows punch through (PT) and non-punch through (NPT) structures to be distinguished. Both types of IGBTs are offered on the market, up to a voltage of 3300 V. However, there is a trend toward NPT IGBTs that are inherently more rugged in the short circuit failure mode, simpler to parallel due to a positive temperature coefficient of the collector-emitter saturation voltage, and less expensive to manufacture.

Among the PWM techniques, sinusoidal voltage controlled PWM and hysteresis-band instantaneous current control PWM have become very popular. Digital computation intensive space vector PWM (SVM) with isolated neutral loads was introduced in the 1980s. SVM performance is superior to sinusoidal PWM but computation time restricts the upper switching frequency limit. Because of superior performance, the recent trend is to replace current control PWM by voltage control PWM. Three-level topology, used in high voltage high power applications, provides better harmonics performance without increasing PWM switching frequency. Recently, attempts have been made to replace the multi-megawatt thyristor phase-controlled cycloconverters for utility use with the IGBT-based three-level converter system. The system is more economical than a

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<sup>4</sup> L. Zverev and J. Hancock, Infineon Technologies Application Note "CoolMOS Selection Guide."

cycloconverter system. Since IGBT's have higher switching frequency and their voltage and current ratings are increasing, there is a growing trend to replace two-level GTO converters in the lower end by three-level IGBT converters. As IGBT voltage ratings increase there is also a trend to replace three-level IGBT converters by the corresponding two-level converters giving large size and cost benefits. Typically, the two level PWM converters are used in the converters that have low power (200 Kva and less) and three level PWM technique are used for larger power size (250 Kva and above).

Interest in soft switching technology is evident in recent literature. Traditional converters with self-controlled devices use hard switching. Soft switching of devices at zero voltage or zero current (or both) tends to minimize or eliminate device switching loss, thus providing higher efficiency. Other advantages include: elimination of snubber loss, improvement of device reliability, less dv/dt stress on machine insulation, and reduced EMI. Soft-switched converters<sup>5</sup> can be generally classified as resonant link dc, resonant pole dc, and high frequency ac link systems. The resonant link dc can be either voltage-fed or current-fed type. The former again can be classified as free-resonance or quasi-resonance types, or active or passive clamp types. Soft-switched high frequency ac link systems can be resonant (parallel or series) or non-resonant type. This class has the advantages of transformer coupling, although the number of components increases. Unfortunately, in spite of the technology evolution for more than a decade, soft-switched converters have barely entered the market place. The need for extra components to clamp the higher switching spikes and control complexity are likely reasons for their limited success.

## **2.5. Problems With Existing PV Inverters**

The existing grid-tied power converter systems problems are discussed below.

### **2.5.1. Lack of Universality**

PV inverters are specially designed for each energy source. This translates to low volume and, consequently, low quality for the system. A universal design is one means for dramatically increasing the quantity of components manufactured. The component could consist of an entire inverter unit but is more likely to consist of inverter subcomponents such as a power module or a control module.

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<sup>5</sup> Converter is a general term related to four different conversions (AC-to-AC, AC-to-DC, DC-to-AC, and DC-to-DC). Inverter and rectification are two commonly used terms in PV applications that refer to DC-to-AC and AC-to-DC conversion, respectively.

## **2.5.2. Old Technology Resulting in Short Lifetime, Low Quality and High Cost**

PV inverters typically use analog or analog/micro-processor hybrid control system to control the power converter system. There are many problems that are associated with analog or analog/microprocessor hybrid control systems. For example: aging effect and temperature drift of analog devices, higher component count (this leads to low life and quality), difficult field modifications, high cost, inflexible adoption to different electrical environments, low noise immunity, high EMI, and an advanced control algorithm that is not easily implemented. Also, a separate micro-processor system has to be used for system monitoring and user interface. All these problem contribute to the fact that existing power electronic converter systems for various renewable energy sources have Mean Time Between First Failure (MTFF) of less than five years.

## **2.6. Candidate Technologies that Could Result in Ten-year Lifetime of an Inverter**

### **2.6.1. Soft-switching Technology (a developing technology)**

Soft-switching techniques were developed to overcome the fundamental limitations on switching frequency that derive from loss considerations in hard-switched converters. The basic idea is to use additional circuit components, usually resonant circuits, in a way that ensures that voltage or current is held at zero during switching intervals, thus eliminating the switching loss.

Snubbers that are used in hard-switched power converters tend to reduce the rate-of-rise of voltage/current and thus reduce loss in the switch; however, losses then occur in the snubber itself. Resonant snubbers were developed to minimize losses, and were further developed to hold switch voltage at zero during turn-off. Resonant converters, typically the so-called “load-resonant converters,” have been developed for DC-to-DC conversion wherein an LC circuit is used to force zero-crossing where switches are turned ON or OFF.

The resonant DC link concept was developed by Divan<sup>6</sup> and has gained wide acceptance. This circuit will be briefly, if somewhat simplistically, described here to summarize the basic ideas of soft switching. The original version of the circuit is shown in Figure 2.1.

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<sup>6</sup> Deepak Divan, IEEE Transactions On Industry Applications, March/April 1989.

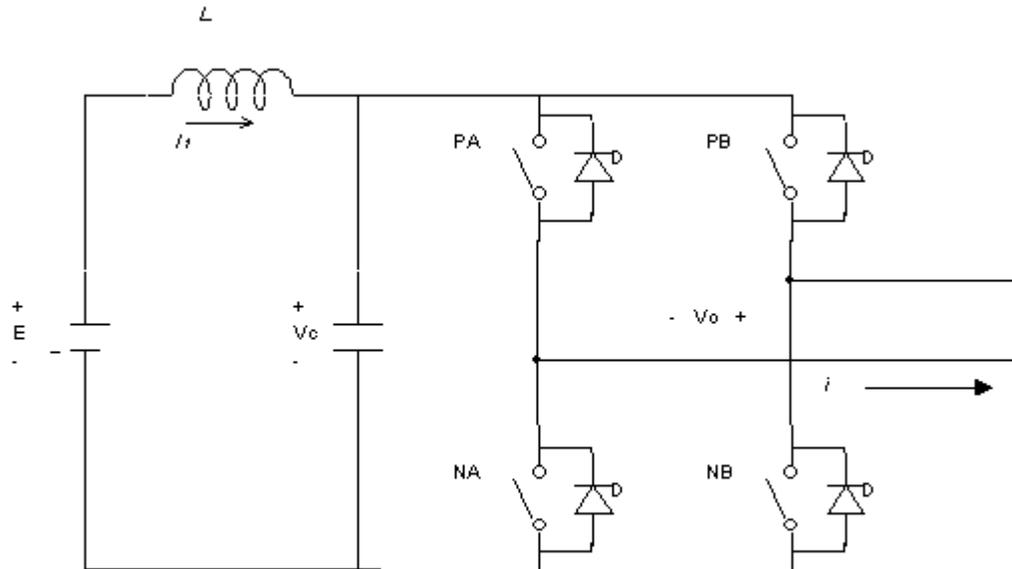


Figure 2.1. Basic DC-link Soft Switching Inverter

Suppose at a given instant appropriate switches are ON so as to short-circuit the capacitor. The inductor current  $I_1$  will then rise. If the switches are now turned OFF, the capacitor maintains essentially zero voltage during the short turn-off period. Thus the switches turn OFF with zero loss. Suppose now, at this point, switches PA and NB are ON, to supply current to the load in a manner similar to the basic single-phase inverter. If the inductor current is sufficiently larger than the current delivered to the load, excess current is forced into the capacitor, essentially establishing a resonant oscillation. The capacitor now charges and then discharges to zero volts, provided that the original inductor current is sufficiently large. The switching of devices can now be organized to again short the capacitor and maintain the voltage  $V_c$  at zero volts for a short period of time. Loss-less switching can again be performed and the cycle repeated.

Although the switching scheme is now more complicated, it is seen that switching can be organized so as to obtain the waveform of DC bus voltage  $V_c$  as shown in Figure 2.2. Given this waveform, strategies such as pulse density modulation (PDM) can be used to synthesize an AC voltage  $V(0)$ . As illustrated in Figure 2.2, switches PA and NB are switched ON and OFF under zero-voltage conditions to generate discrete positive-voltage pulses in the first half-cycle of output voltage, then the second half-cycle is synthesized using switches NA and PB. This strategy is called discrete pulse modulation.

The basic circuit discussed here eliminates switching losses, which permits higher frequency switching. The circuit has the disadvantage of requiring much higher voltage and current ratings for the switches because the switches must carry resonant components of voltage and current. Equally important limitations are the complexity of control and the lack of true PWM capability. Substantial research in this area has led to modifications that have essentially removed the high rating requirement limitation and control schemes have been developed that approach true PWM.

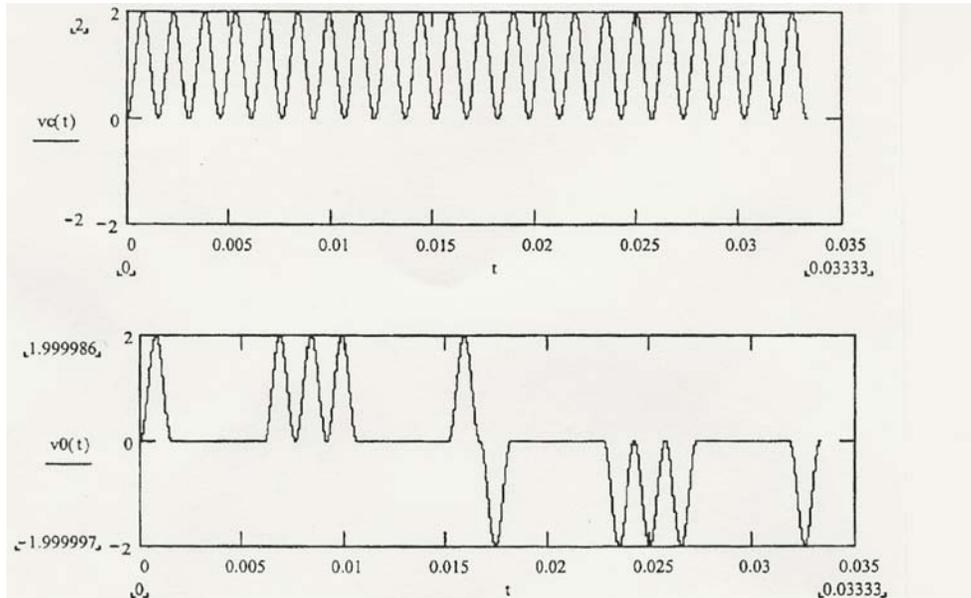


Figure 2.2. Representative DC-link Inverter Waveforms Under Discrete Pulse Modulation

### 2.6.2. Hard-switching Technology (presently dominates the industry)

Figure 2.3 shows the simplest inverter that delivers energy from a battery to a resistive load. The ideal battery produces a voltage,  $E$ , that is DC, it does not change with time as illustrated in the time waveform at the bottom left of the figure. The battery is connected to a bridge of switches. Each switch can be turned ON or OFF. When ON, the switch conducts current in the direction of the arrow.

The Voltage-source Inverter operates by alternately turning the P and N switches ON and OFF. When the P switches are ON a positive voltage, equal to battery voltage  $E$ , is applied to the load; when the N switches are ON the load voltage becomes the negative of the battery voltage (i.e.,  $-E$ ). Thus, a periodic AC voltage is synthesized at the load, which appears as the square wave shown at the bottom right of the figure. In a resistive load, the waveforms of voltage ( $V$ )

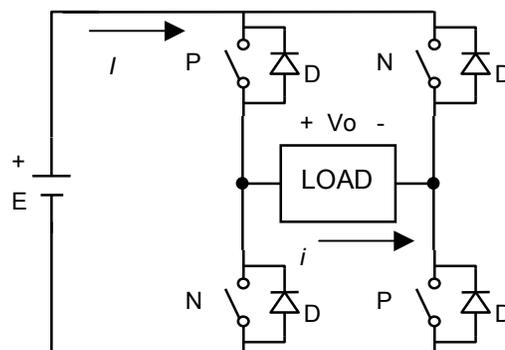
and current ( $I$ ), are identical. Thus an alternating current results. The current ( $I$ ) from the battery is DC.

### 2.6.3. Hard Versus Soft Switching

A key consideration in custom power electronics is whether to use hard or soft switching. Soft switching is accomplished at zero current or zero voltage to reduce switching stresses and power losses and employs resonance between an inductor and a capacitor to establish appropriate voltage and current conditions for the switching. The basic idea is to separate the voltage and current switching transients and minimize their overlap so that the net switching power loss can be reduced.

A study by Divan, while at the University of Wisconsin in Madison, concluded that soft switching costs more than hard switching. Suppose a switching system is needed for a voltage source inverter meant for motor control. Of the two options, a soft one would require the higher current rating. Likewise, a zero-voltage switching system would require the higher voltage rating. However, a higher current rating demands a larger die size and a higher voltage rating requires a thicker drift region in the semiconductor device. So the cost rises for both of the soft-switching schemes, sometimes more than doubling for the same application.

The real advantage of soft switching is much lower switching power loss plus significantly reduced current and voltage rates of change stress. Although hard switching is more sensitive to circuit parasitic effects (inductance, for example), soft switching tightly couples its lesser parasitic effects to local circuit loops. Hence, even soft switching is sensitive to circuit parasitic effects, and these, if care is not taken, will cause high frequency ringing in switch current waveforms, especially in a zero-current switching converter. The effect on performance is serious, as it gives rise to electromagnetic noise. These parasitic effects will also decrease the turn-off current rate of change, increase the switching power loss, and reduce the switching speed, especially in a zero-voltage switching converter.



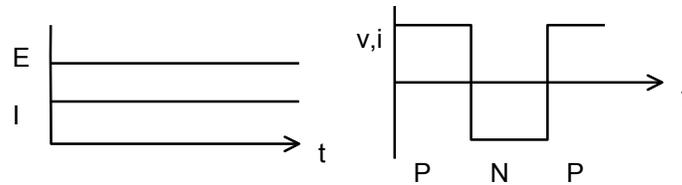


Figure 2.3. Basic Voltage-source Inverter with Resistive Load

In summary, hard switching is simple and less expensive than soft switching but it also faces technological challenges such as heat dissipation. This is particularly so with regard to the miniaturization of power-processing equipment. Hard switching cannot employ numerous circuit configurations like soft switching does.

Hybrid solutions are in wide use in a number of key applications, such as power supplies for computer and communications systems, and are being pursued in automotive electronics and motor control. Called zero-voltage transition switching, it is a compromise between true zero-voltage switching and hard switching; the device is switched at zero voltage using auxiliary circuits rather than a fully resonant circuit.

#### 2.6.4. DSP Control Methods

With the aid of advanced micro-electronic technology, digital control of power converter systems has become feasible. The newly introduced low-cost, high performance DSPs, with features such as single-cycle multiplication and accumulation with on-chip PWM mechanism and A/D converters, provide the CPU bandwidth and peripheral mix needed to implement sophisticated control techniques required for interfacing with various renewable energy sources. A digital controller has many advantages over its analog counterpart. There are no hardware adjustments, fewer components, less aging effects and smaller temperature drifts in a digitally controlled system. With a digital controller, adjustment of control parameters for adapting to different electrical environments is easy and flexible. Software damping functions for output filters that are used in a power converter are easily implemented. Thus no hardware damping components are required for the output filter's resonance. They provide other advantages such as: fully digital control, fewer components, high noise/EMI immunity, high reliability, reduced heating of power switches, lower harmonics, less filtering, faster fault response, no dc components, higher efficiency. Additionally it is easy to include other system level functions such as battery charging, power factor correction, reactive power compensation, fuzzy logic control, parallel operation, and on the fly frequency change to adapt to different environments and applications. User interface and communication are also easily included.

The advanced and fast DSP can use the same sampling loop to carry all the control loops. DSP control can reduce heating of power switches and also can change the switching frequency on the fly; this means that they can use a higher switching frequency to ensure continuous current and smaller magnetic effects for the renewable source interface. This is done while using a lower switching frequency for battery charging, thus minimizing the switching losses and maximizing the system efficiency. The user parameters set-up feature can help to maximize the user control flexibility. Integrated digital control gives the maximized security and faster fault response leads to higher reliability. In addition, a user's interface and communications capability are also easily incorporated.

Another advantage of using a DSP control system is that the PWM converters used for power conversion compose a discrete system and should be treated as such when the control system is designed. Traditionally, a PWM converter (without DSP) is treated as a continuous system when the control system is designed. That means that higher bandwidth and higher switching frequency are required with an analog controller; this leads to high switching losses. With DSP control, PWM converters can be treated as a discrete system when the control system is designed. This means that to achieve the same performance as an analog control inverter, lower switching frequency is allowed with the same filter parameters. This will reduce the switching losses.

Because of the advantages of digital control over analog or analog/micro-processor hybrid control, it is obvious that a DSP controller is the choice to control a universal power converter system for renewable energy sources. DSP controlled, universal power converter systems can be configured for multiple renewable energy sources (Solar, Fuel Cell, Micro-turbine, Flywheel, Wind-mill, etc). They also can be configured for multiple applications (grid-tied, off-grid, uninterruptible power supply (UPS), voltage sag compensator, active power filter, harmonic power compensator, etc). They could have the same hardware with specific dc interface software (kernel) for each renewable energy source. The interface software (kernel) could be configured by user/integrator to work with a specific renewable energy source or in a specific application. Because of the universal configuration, the production volume of such power converter systems could be high. That will result in higher quality and lower cost for the power converter system. Also the power converter system could be paralleled for N+1 redundancy and maximum reliability. The universal power inverter system could also provide single phase or three-phase, four wire connection. They can be designed to not have dc offset problems in the output voltage and have no unbalanced output voltage problems under unbalanced load conditions; a bulky output transformer is not required to combat dc offset and neutral forming problems. Thus they can be cheaper and lighter. They could deliver up to rated power with any output power factor (leading, lagging, or unity). They could also be configured as an Active Power Filter to help customers compensate power factor and thus avoid utility excessive power factor charge.

With advanced DSP control, low frequency passive filter and high frequency filter damping circuits are not required for the proposed universal power. This results in simple system configuration, high reliability, low cost, smaller footprint, and lighter weight. Other benefits from a DSP controlled universal power converter approach include: maximum output Total Harmonic Distortion (THD) is less than 3% under linear load and less than 5% under nonlinear load, also maximum single harmonic is less than 3%, they meet or exceed the IEEE-519 standard and they do not put stress the utility's and user's equipments, they have  $\pm 1\%$  output voltage regulation, and system efficiency is larger than 96%. With leading edge control technology and optimized system configuration, the DSP controlled universal power converters completely eliminate sub-synchronize resonance and instability on soft grid problems and provide premium power quality for sensitive electronic equipments.

### **2.6.5. Made-to-Order Power Electronics**

With advances in computer aided design it is now possible to custom-make power electronics semiconductors and modules. These can have:

- inclusion of application information in the switch design process
- design for end of life
- de-rating the SOA as inverter ages
- minimal on-resistance.

The reliability issue for power converter systems has become one of the major concerns for a successful renewable energy program. Therefore "the pressure is on manufacturers<sup>7</sup> of power semiconductors and designers of power electronic systems to achieve lifelong system reliability, and to do so while containing cost." This dilemma has awakened semiconductor manufacturers to the virtues of a joint custom approach that includes collaboration on the design so that they can fit the product to the application. Rather than work in isolation, makers and users can together optimize each switch for its intended use throughout its life. Large volume of product will be necessary to justify the cost of this approach.

This strategy has evolved over the past 10 years. Its focus is on two system fundamentals: performance and reliability. In pursuit of the first, the goal is to minimize the power loss in power devices for a given application by minimizing such parameters as on-state resistance. The reliability goal is to extend the device's operational life by, for example, reducing the thermal stress of switching at high frequencies. "High" typically means over 500 kHz in power supplies for

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<sup>7</sup> Made-to-Order Power Electronics, Krishna Shenai, University at Chicago, IEEE Spectrum July 2000.

computer and communications systems and over 1 kHz in power inverters for traction systems. These goals apply to any type of power semiconductor, including the commonly used MOSFETs and insulated-gate bipolar transistors (IGBTs).

An important future goal for this strategy is to have manufactures make it possible to de-rate power electronic devices over time so as to avert premature failure. The de-rating would involve adjusting the safe operating area (the current-voltage boundary within which the device can be operated safely) as the device ages- an approach called “design for end of life.”

An early beneficiary of the custom approach is an integrated IGBT inverter for traction from Asea Brown Boveri (ABB), Baden-Dattwil, Switzerland. The customer was ADTranz, a rail car manufacturer in Zurich, Switzerland. Circuit designers and device manufacturers from different departments within ABB tailored the design to ADTranz’s needs. What they did was to individually optimize each switch, plus the associated parallel diode that provides a current path when the switch is off, plus the entire package. What they produced was a switch that operated at frequencies over 1 kHz, higher than the typical few hundred hertz in earlier systems, so that the system was reduced to about one-third of its original size.

Traditionally in either use, hard or soft switching, it has been the circuit designers who model the load, determine the applied voltage, and define the application requirements (Note. in hard switching, the device is switched on when it blocks full voltage, and off when it conducts rated current, whereas soft switching is done at zero current or zero voltage).

Next the circuit designers have selected a control technique – pulse-width modulation, for example – and designed the circuit on the assumption that the components are less. Finally they have determined the ideal voltage and current ratings and picked a power semiconductor switch from data sheets.

However, with custom power electronics, it is the device designers who determine the specifications of the device. Then they optimize it based on a detailed circuit simulation, taking into account such applications constraints as load variation, switching scheme, anticipated thermal stress as a result of overheating, and ambient temperature. The simulation analyzes the device’s physical model with either a Spice-type analysis, in which the circuit is represented by lumped components, or by its simplified behavioral model, which replaces the complex Spice circuit with simpler analytical expressions. Such treatment applies realistic stresses to the device simulation without incurring the complexities of simulating full circuit operation.”

## **Dealing With Non-linearity**

Custom power electronics provides a mechanism for dealing with non-linearity in power semiconductors, as well as non-uniform temperature stresses within and among chips in power electronics modules.

Consider a generic power electronic system; for example, a full-bridge dc-ac inverter represented by four MOSFET switches and a filter. Here, individual switch temperature does not bear a linear relationship to such key parameters as voltage and current rates of change –  $di/dt$  and  $dV/dt$ , respectively. Note, too, the so-called intrinsic body diode presented across each switch. It provides a current path when the switch is off, except that too fast a turnoff (under 50 ns) may cause the diode to avalanche, increasing current and power loss and raising temperature even further. Custom design addresses the issue by simultaneously optimizing the main switch and its intrinsic body diode while considering all the circuit-level nonlinear interactions.

For power modules, custom design concentrates on heat removal by accounting for non-uniform thermal gradients and thermal properties of the semiconductor and package materials. In such modules, power semiconductor chips are supported by electrical isolation and a thermal management system, including a copper base-plate with aluminum nitride substrates on which the chips are placed, and a silicone gel that conducts heat from the chip.

For moderate current rating (a few hundred amperes), wire bonds are generally used to connect to the module's top conducting electrode. The electrical interconnects give rise to parasitic inductances, while the poor thermal conductance and capacity of the module layers do a less than perfect job of removing heat. Further, the temperature is not uniform within each chip but is a function of local current density and electric field intensity. The local hot spots thus created may lead to current filamentation, the term for severe constriction of current within the semiconductor chip. In a module, if too little heat is removed, current flow may be confined to certain interconnects, like the wire linking the left chip to the emitter.

The resulting uneven temperature rise forces wire bonds to break, solder to delaminate, and possibly cracks to arise within materials (such as the aluminum nitride substrate) between the dice and base-plate. Aggravating the situation are residual material defects within a chip, such as crystal imperfections and contaminants like sodium ions, which tend to congregate in high stress regions of the device, eventually leading to failure.

To work around the heating problem, a device designer would characterize the entire device as uniform in temperature and assume that this temperature is identical to its hottest junction. However, this grossly oversimplifies the complex electro-thermal physics of a device beset by too much heat. For example, a steep temperature gradient and current crowding (filamentation) tend to breed hot spots within an IGBT where temperature may range from 650 K to as high as 830 K, when the load is short-circuited.

## Improving Performance

Today's power conversion technology relies for the most part on the conventional hard-switching technique. To reduce power loss, semiconductor manufacturers have, over the years, steadily reduced on state resistance with innovative design and wafer-manufacturing technologies. In the MOSFET, not only the main channel, but also the bulk semiconductor and the bulk-to-channel transition region contribute to resistance. The MOSFET's resistance can be minimized by adjustments to the doping profile and the use of VLSI fabrication techniques to increase the packing density of individual current conducting cells within the device.

Removing obstructions to a uniform current flow also helps enhance performance. The obstruction in the transition region is caused by the presence of an equivalent junction FET in the current path. To eliminate the JFET action, a trench gate structure (applicable to any MOS power device) injects channel current directly into the drift region, thereby unifying the current flow. (In a conventional planar MOSFET, current flow starts out horizontal and then shifts to vertical, the transition introducing the JFET action. In a non planar, trench-gate structure, the current flow is only vertical.)

In a bipolar device such as the IGBT, designers have increased the on-state conduction. The effect is to lower the on-state resistance by enhancing the increase in conductivity that occurs with a rise in current density. In turn, this conductivity modulation increases the charge within the device's drift region. The higher on-state current density entails higher on-state power density, such that less area is needed to deliver a given amount of power and the device can be smaller and cost less. But there is a tradeoff. A limit is set to switching speed because greater on-state current density also results in greater turn-off current density.

Still higher device conductivity can be obtained by the use of thyristor-like MOS-controlled devices. This structure allows a silicon device to approach its highest attainable conductivity and affords the least on-state voltage drop of all controllable power devices. However, physical and structural constraints further impede the effort to reach the basic power-handling capability of a semiconductor material.

The maximum electric field strength of 200 kV/cm, energy bandgap of 1.1 eV, and thermal conductivity of 1.3 W/C between them restrict silicon devices to a highest achievable voltage rating of 10 kV (for a single wafer) and a highest achievable operating temperature of 200C. The tradeoff from these material limitations also determines the highest switching frequency. Power switching using materials with much higher power handling capability than silicon, such as silicon carbide (SiC), is promising, however this technology is in its infancy.

Finally, during turn-off, a semiconductor's current density is fundamentally limited by the power (and heat) being dissipated in localized regions. For instance, silicon devices packaged in a TO-220 assembly have a typical turn-off current density under 200 A/cm square. Therein lies a challenge to custom power semiconductor design – make the devices perform best within their physical limit while maintaining acceptable reliability throughout their life.

### **Shrinking Power Loss**

Turn-off energy (and power loss) can be lowered by more than an order of magnitude if charge-carrier recombination in local regions of an IGBT can be accelerated under careful control. Semiconductor manufacturers have been bombarding regions of excess charge with high-energy ions, like protons, to reduce carrier lifetime in regions of excess charge. The technique is powerful. Improvements in performance are lower on-state voltage and faster switching speed. The increased time to failure during a load short circuit improves reliability. Being selective, proton bombardment allows a much broader tradeoff in performance and reliability parameters than does the well-established electron irradiation. This latter process hastens carrier recombination indiscriminately, throughout the volume of the semiconductor switch; it tends to add to the forward voltage drop by subtracting from the charge density throughout the bulk. Electron irradiation is also a more expensive process.

For robust power electronics to guarantee zero failures in the field, its development requires a new design philosophy based on end-of-life design. The semiconductor power switch in a power electronic converter absorbs most of the electrical and thermal stresses. Often, it is the target for reactive energy dissipated in the circuit. The switch must therefore be protected from such persistent stress, making its reliability of paramount importance.

This reliability is therefore being specified in terms of an adjustable safe operating area, to become available, in time, from all power semiconductor device manufacturers. Rather than remaining constant throughout the life of the switch (as shown in traditional power electronics device datasheets), the area should be adjusted down in time. Its time-dependent rate of shrinking is a strong function of the device's prolonged electrical and thermal cycling. It would seem that the more aggressively power semiconductor manufacturers pursue the development of application-specific power switching technologies, the brighter the future of custom power electronics looks.

### **2.6.6. Engineering Approach**

The key to the successful implementation of made-to-order power electronics is to include the device designer (or company) as a member of the system design team during the entire product development. This ensures the optimal use of power devices for product longevity. The concurrent engineering approach has to

be implemented. The common approach today is for the system engineer to model the system, the design engineer to design the circuits, then for the component engineer to pick the power device to match the circuit design and specification. The component engineer should work with the power device manufacture from early on in the project and provide the system models and possible circuits to the device manufacture so that they understand the system model and power electronic application. One example of this approach is Tyco electronics' program to custom-make power electronics to fit specific applications. To implement this strategy, the sales volume of the power devices has to be high enough to justify the process. Most power device manufacturers are reluctant to pursue this route because they view this approach as custom made and they cannot justify the expense. However, adequate volume may be achieved if the power electronics community works together to derive a common requirement for various power electronic converter applications. This, in turn, will lower the cost for development; it can be shared among several different products.

Another issue for the system designer is the inclusion of an adjustable SOA for power devices. One possible implementation for this approach is for the device manufacturer to provide derating SOA information based on time and thermal recycling of the device. The system designer would then embed this information into the system design to automatically de-rate the power devices. Derating information can be programmed into DSP software. After several years of service or a fixed number of thermal cycles, DSP can automatically limit or reduce the power output of the system. One possible approach is to design a fuzzy logic system to incorporate this function into DSP software.

Some device manufactures embed a micro-processor into a power device. With this approach all intelligent protect and derating functions can be performed by the imbedded micro-processor. When the micro-processor detects a fault or a number of thermal cycles of usage, it will alert a control circuit or limit output power by limiting the output current. This is an expensive way to incorporate the protection and derating SOA function into the power converter design. The devices that are embedded with the micro-processor cost more than double compared to non-embedded power converters. We believe that all protection and derating SOA functions can be implemented by DSP software at the system level. Because DSP exists for other system functions, there is no added cost for the system if protection and derating SOA functions are implemented.

One issue with a SOA derating function is how to derate the voltage. Typically, when a system is designed, the DC link voltage is first determined so that the voltage rating of the power device can be determined. Once the DC voltage is fixed, it is hard to adjust the voltage rating of the power device after a number of thermal cycles. There are two ways to derate the voltage of a power device after a number of thermal cycles. One method is to lower the DC voltage, which will, in turn, produce a lower inverter ac voltage. If the tap of the output transformer can be switched, the rated output voltage is still attainable. Another method (for three phase systems only) would lower the DC voltage and then add certain zero

sequence content to boost the output voltage. To derate the current rating of power devices, simply limit the maximum output current. One issue that may arise is how to alert the customer to the derating of the power converter. The intelligent power converter should be able to incorporate automatic load shedding so that part of the output is guaranteed for the life of power converter while some part of output is only guaranteed for a limited life time and will be shutdown after a defined number of years of service.

## **2.7. Soft Switch May be a Suitable Approach to Reliability**

### **2.7.1. Soft Switching Technique**

A goal of power conversion techniques is to construct power conversion equipment with high efficiency, small size, light-weight, low switch stress and low electromagnetic interference (EMI). Based on conventional power conversion techniques, hereafter referred to as hard-switching, increasing switching frequencies can reduce the size and weight of magnetic components and filter capacitors and consequently reduce the cost, size, and weight of power conversion equipment. However, at high switching frequencies switch stress, switching power losses, and EMI, produced due to large  $di/dt$  and  $dv/dt$ , become significant. These increase linearly with the switching frequency. As a result it not only decreases the system conversion efficiency, but also degrades the switching device. Additionally, the strong EMI may easily make an impact on the neighboring equipment, especially communication equipment. In order to overcome the disadvantages of power conversion equipment operating in the hard-switching mode at high switching frequency, soft-switching techniques are thought of as promising alternatives. In recent years, significant progress in soft-switching techniques has been made and some of these techniques have been applied in industrial applications.

Until now, there have been a variety of soft-switching topologies available and each of them has its features for certain applications and operational situations. In this study, for the sake of simplicity, we would like to just introduce the basic soft-switching technique and a few typical soft-switching topologies. The more specific soft-switching techniques used in particular applications will not be discussed here.

#### **2.7.1.1. Basic Type of Zero Voltage Switching And/or Zero Current Switching**

The basic concept intended to minimize the shortcomings of hard-switching is to utilize a combination of proper topologies and switching strategies to make each switching instant take place only when the voltage across it and/or the current through it is zero. This minimizes switching power loss and reduces  $dv/dt$  and

$di/dt$ . This approach has yielded a large number of soft-switching topologies. Some additional components and control strategies are essential so as to shape the switch voltage and current. The most basic type of soft switching is discussed below.

### ZCS (Zero Current Switching)

The basic type of Zero Current Switching (ZCS) topology is shown in Figure 2.4. With ZCS the switch can turn on and off at zero current, thus eliminating switching losses and also minimizing switch  $di/dt$ . The peak switch voltage remains the same as in hard-switching, but there is a peak resonant current flowing through the switch.



Figure 2.4. Basic Zero Current Switch Circuit

It is necessary to assure that the discharge of inductor  $L_s$  is complete before turning the switch on. A typical practical topology of the ZCS is shown as Figure 2.5.

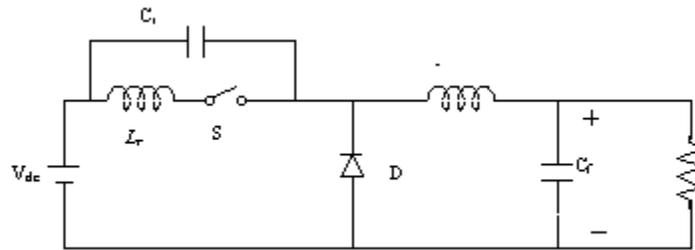


Figure 2.5. A ZCS DC-DC Converter

### ZVS (Zero Voltage Switching)

The basic type of Zero Voltage Switching (ZVS) topology is shown in Figure 2.6. The switch is turned on and off at zero voltage, thus eliminating switching loss, and also suppressing switch  $dV/dt$ .

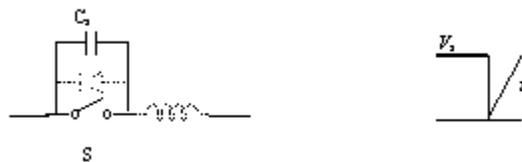


Figure 2.6. Basic Zero Voltage Switch Circuit

The peak switch current remains the same as in its hard-switching counterpart, but there is a peak resonant voltage across the switch. A typical practical topology of the ZVS is shown as Figure 2.7.

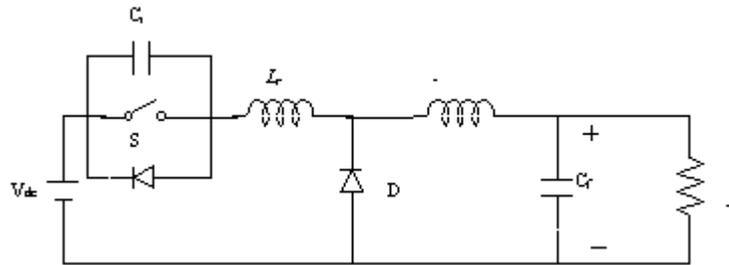


Figure 2.7. A ZVS DC-DC Converter

Since most of the soft-switching techniques utilize the resonance due to the additional inductor and capacitor and/or auxiliary switches, the resulting converters are also referred to as resonant converters. For some applications, a resonant converter includes the combination of the above basic types and some auxiliary components that are required to improve performance. The resonant converters are categorized according to the differences of type and position of the resonant circuits that produce the various types of resonant converters.

Soft-switching techniques have been broadly applied to industry. Most of their applications are for resonant DC-DC converters. That is because the soft-switching technique of DC-DC converters is relatively simple to realize. Realization of soft-switching DC-AC converters (inverters) is more complex. This is due to the fact that, in general, inverters are controlled based on two distinct operating frequencies. One is the carrier wave frequency to be used for modulation and the other is the control wave frequency to be used as the fundamental output frequency. Frequently, there is bi-directional power flow between the DC bus and the AC output, and soft-switching operation is required over a wide load range. For resonant inverters, there are a few typical topologies, which are shown below.

## 2.7.2. Resonant Inverters

### 2.7.2.1. Resonant-DC-Link Inverters

Unlike conventional DC-AC inverters, where the DC input voltage  $V_d$  is constant, in the resonant-DC-link inverters the input voltage varies around  $V_d$  due to resonance of the LC circuit that provides a zero voltage period during which the DC-AC inverter can be switched. This results in zero-voltage switching.

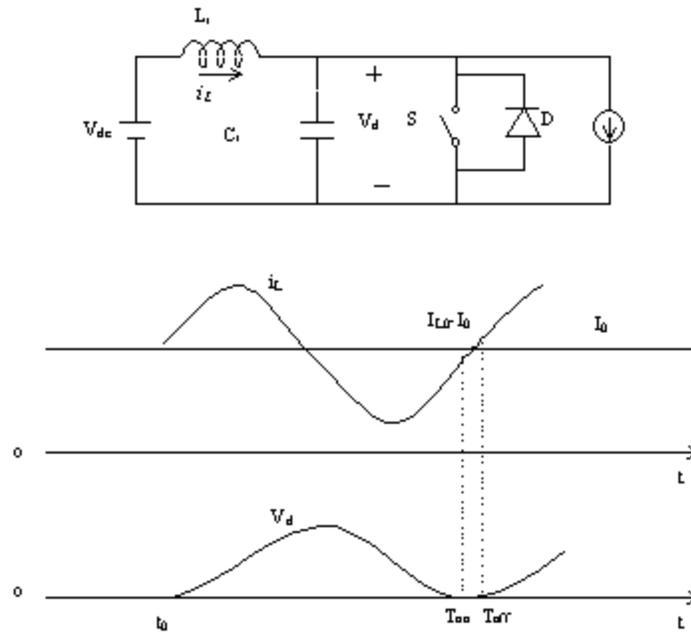


Figure 2.8. A Conceptual Circuit of Resonant DC-Link Inverter and its Waveforms

A basic conceptual circuit of a resonant DC-link inverter is shown in Figure 2.8. The  $L_r$  and  $C_r$  make up a resonant tank, and interact with the switch  $S$  and an anti-parallel diode. The current  $I_o$  is the load current. For most applications, since the resonant frequency is much higher than the fundamental frequency, it is reasonable to assume  $I_o$  to be constant in magnitude during a resonant cycle. As shown in Figure 2.8, when the switch is turned on the current  $I_L$  builds up linearly. When it reaches  $I_o$  the switch is turned off at zero voltage. In turn, a resonant process occurs. After one resonant cycle from the turn off of the switch,  $V_d$  returns to zero, providing a zero voltage switching condition. Obviously, in order to fulfill the function of turning on and turning off at zero voltage, the resonant  $V_d$  has to have zero voltage intervals during which the switch is turned on and turned off. For that, sufficient energy has to be stored in  $L_r$ , that is to say  $I_L$  must be greater than  $I_o$ , before the switch is turned off, to ensure that the capacitor voltage will return to zero. Therefore, the inverter actively controls the current difference of  $I_L$  and  $I_o$  to ensure that the inverter has the same resonant cycle initial conditions and provides a zero-cross link voltage. An application of this concept to a three-phase resonant DC link inverter is shown in Figure 2.9. The switches in any of the three inverter legs can be turned on and turned off at zero voltage.

The L-C resonant circuit can result in high peak voltage stresses, typically a voltage stress of  $2 V_{dc}$ . Consequently, the resonant DC link circuit is always used with a function to clamp the peak voltage across the switches to less than twice the input DC voltage. Two possible types of passively clamped or actively clamped resonant DC link inverters are shown in Figures 2.10 and 2.11,

respectively, where the use of a seventh device restricts voltage stress to less than twice the DC supply voltage.

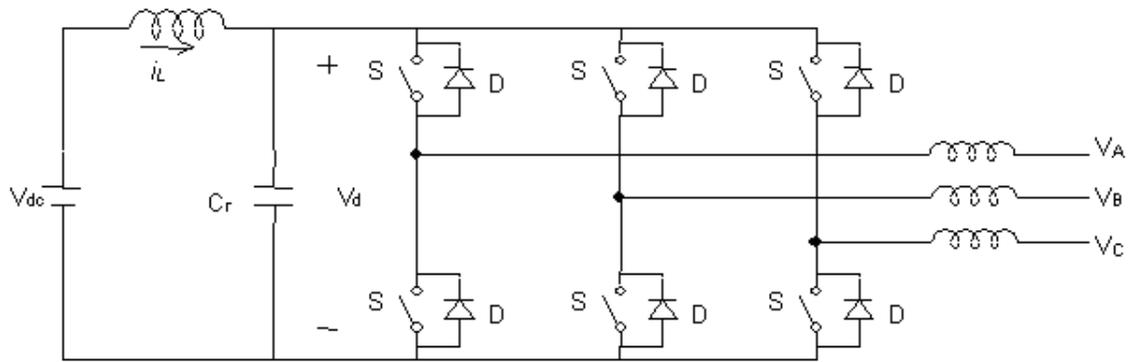


Figure 2.9. Three-phase Resonant DC-Link Inverter

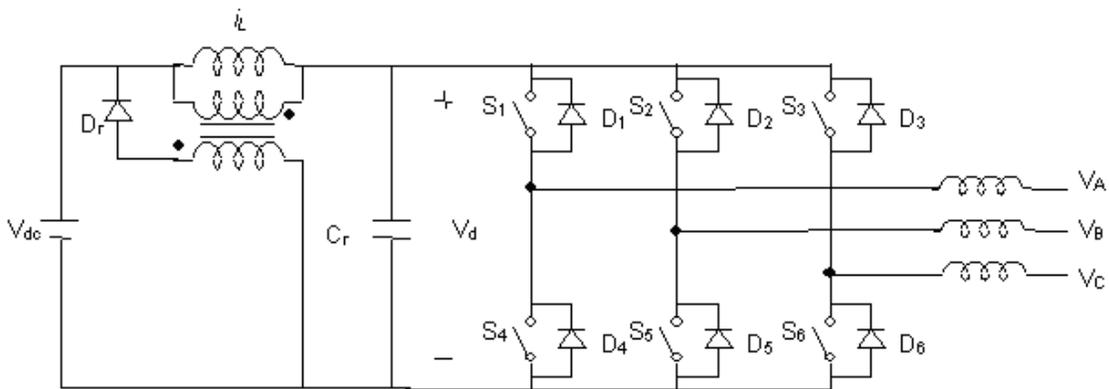


Figure 2.10. Passively Clamped Resonant DC-Link Inverter

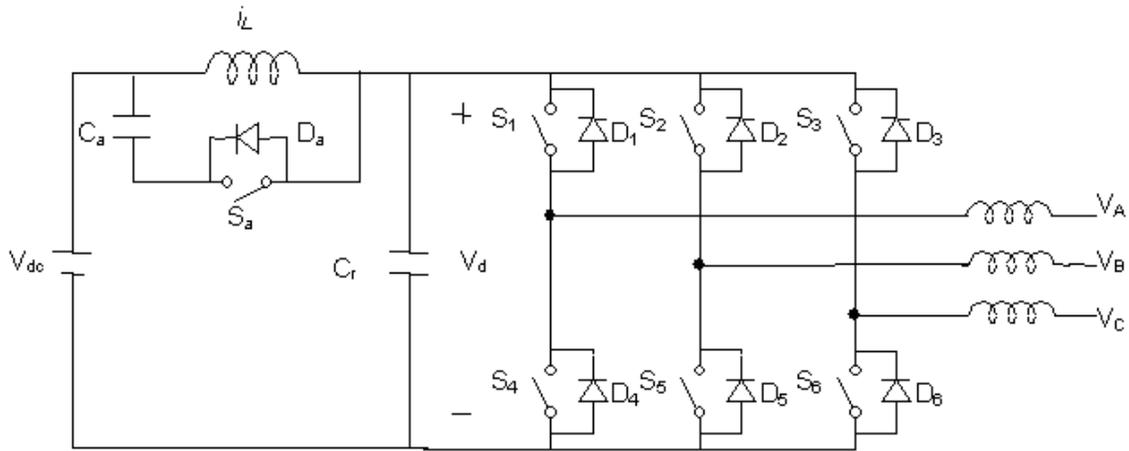


Figure 2.11. Actively Clamped Resonant DC-Link Inverter

The quasi-resonant DC link inverter, which maintains PWM control and achieves soft switching is another type of resonant DC link inverter. Unlike the resonant DC link inverter with a continuously oscillating bus, the resonant bus is clamped to a near constant value during the power delivery mode and goes into a state of resonance when the pulse is terminated or during the rise of the bus voltage to the clamp level. The resultant near-square wave pulses are similar to those of conventional hard switching. Figure 2.12 shows a quasi-resonant DC link inverter.

One advantage of quasi-resonant link inverters is that they can be controlled by conventional PWM techniques. The benefits of this include both the high efficiency of zero-voltage switching and the familiar spectral performance of PWM schemes. However, since suitable modifications of the standard PWM techniques are generally needed to comply with the resonant operation of the inverters, there exist certain modulation constraints.

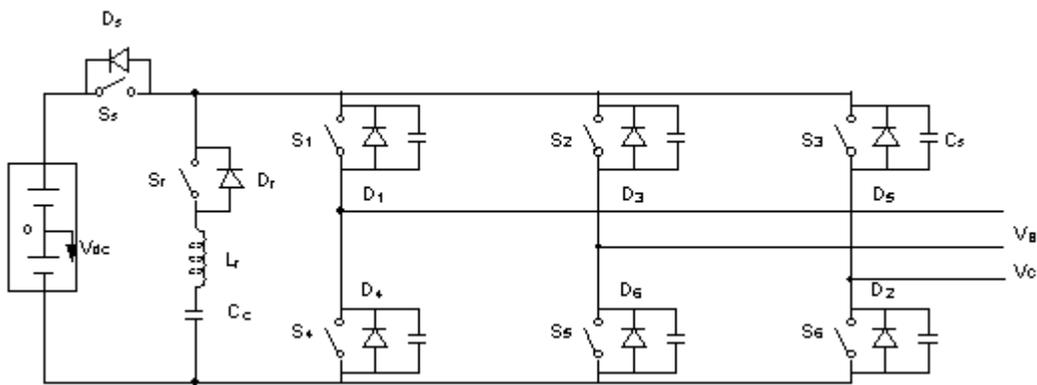


Figure 2.12. A Quasi-resonant Commutated Pole

### 2.7.2.2. Resonant Pole Inverters

Resonant pole inverters tend to use one set of reactive L-C components per inverter phase to achieve ZVS and/or ZCS of the switches in the phase. Additional and resonant elements are distributed into every phase of the inverter. Since every phase of the inverter has its own resonant circuit, the operation of the three phases is completely independent from each other. This provides a control advantage for this inverter configuration.

A phase leg of an auxiliary resonant commutated pole inverter is shown in Figure 2.13. In this figure, an inverter pole consists of switches S1 and S2. In order to achieve ZVS, a resonant inductor and auxiliary switches  $T_{A1}$  and  $T_{A2}$  are configured as shown. The auxiliary switches  $T_{A1}$  and  $T_{A2}$  supply an LC snubber circuit, so as to achieve ZVS for the main devices. A resonant current is initiated in the L-C circuit by turning on an auxiliary device to ensure that the main devices

are carrying some current, which can then be turned off under a zero voltage switching condition. The auxiliary switches turn-off when the current in the L-C circuit naturally reaches zero. Their advantage is independent control, the disadvantage is a large number of elements.

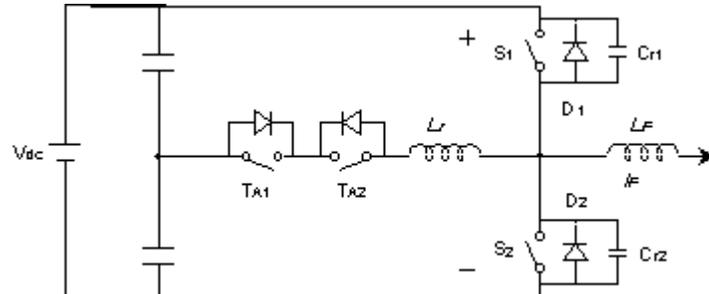


Figure 2.13. An Auxiliary Resonant Commutated Pole

### 2.7.2.3. Auxiliary Resonant Snubber Inverters

The basic principle of auxiliary resonant snubber inverters is to use an auxiliary active switching device along with lossless passive snubber components to achieve soft switching. The parasitic inductance and stray capacitance are utilized as a part of the resonant components. There is no over-voltage and over-current penalty in the main inverter switches. Figure 2.14 shows a delta-configured auxiliary resonant snubber inverter. This configuration avoids using additional bulky capacitors and generating over-voltage in the conventional resonant snubber inverters. Each auxiliary branch consists of an auxiliary switch and an inductor. The blocking diode is in series with the auxiliary switch to protect the switch from reverse voltage breakdown. For a three-phase configuration, in order to simplify the logic design and reduce the conduction duty of the auxiliary switches, the bi-directional auxiliary switches are used as shown. State space vector modulations can be used to control the operation of the circuit.

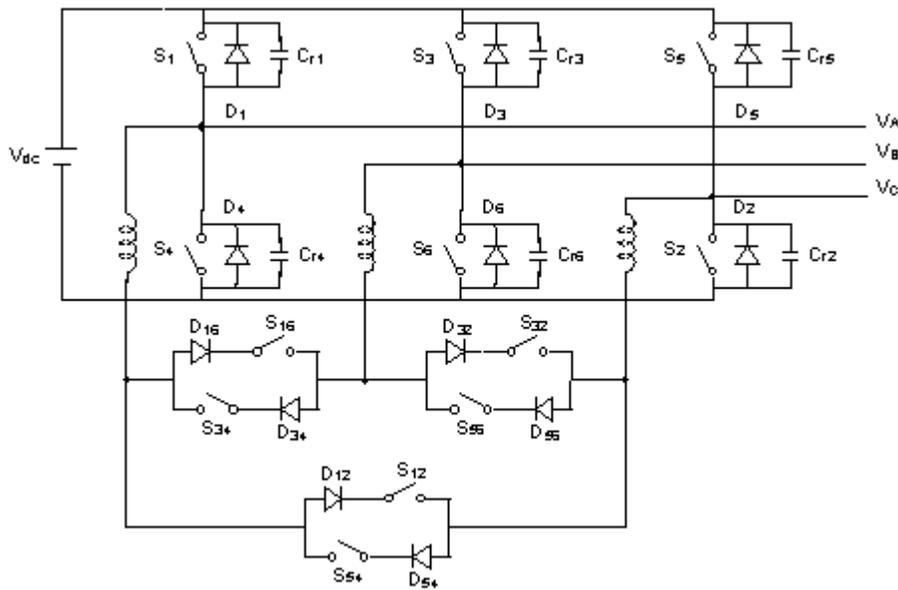


Figure 2.14. A Delta-Configured Auxiliary Resonant Snubber Inverter

#### 2.7.2.4. Load Resonant Inverters

In these inverters, a series LC or a parallel LC circuit named LC resonant tank is required, and is connected with a load in series or parallel. So, according to source type, they can be sub classified voltage-source series resonant inverters and current-source series resonant inverters. According to the connection between the resonant LC circuit and the load, they can be sub classified series-load resonant inverters, parallel-load resonant converters, and hybrid-resonant inverters.

The LC resonance results in oscillating load voltage and current that provides the switch turn on and turn off at zero-voltage and/or zero-current constant voltage. Figure 2.15 shows a zero-current-switched voltage-source resonant inverter equipped with resonant circuits on the AC load side. The current flowing through a switching device, i.e., an IGBT is the sum of the load current and the resonant current. If the amplitude of the resonant current is larger than that of the load current, the current in a switching device becomes zero at one instant in each resonant cycle. This allows the switching device to be turned on or off at the zero current. The zero-current-switching makes a significant contribution to reduction of switching losses and electromagnetic noises.

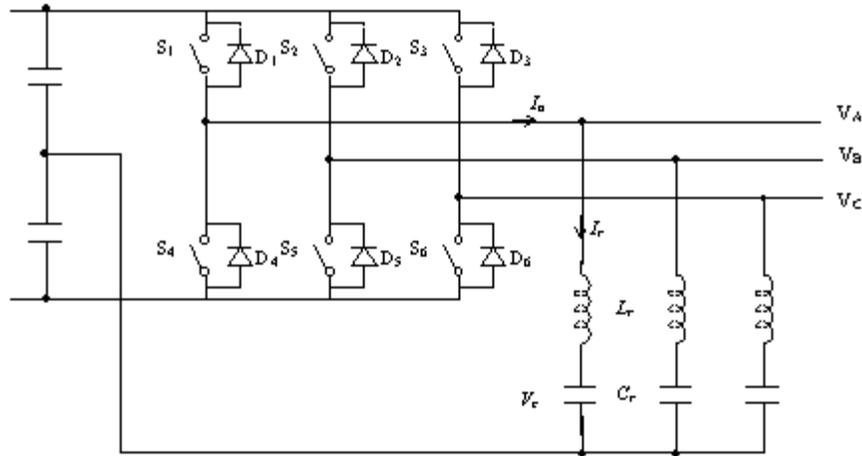


Figure 2.15. A Zero-Current Switched Voltage-Source Resonant Inverter

The high-frequency-link inverter is another type of soft switching inverter. This type of inverter needs to use bi-directional switches and the input is a high frequency sinusoidal AC. These inverters can be synthesized to supply a low-frequency AC of adjustable magnitude and frequency. Controlling the turn on or turn off of switches at the zero crossings of the input voltage can complement soft switching operation.

Due to significant advantages of soft switching over hard switching converters, new and extensive resonant inverter topologies are being developed. Practical industrial field use is limited by design and control complexity, with many constraints to resonant condition and load status (especially at light load), and requiring an auxiliary commutation circuit. Some systematic synthesis methods to analyze, compare, and are required. A significant obstacle for the application of soft switching techniques is a mature design for resonant inverters. Such a design would result in improvements in cost effectiveness, size and weight, marketing time and reliability.

### 2.7.3. Specifications for a Large Power Inverter

The following are samples of specifications for four large inverters. They are based on the authors understanding of what should be possible given the current state-of-the-art. There are four inverter descriptions; these include:

- 100 kVA grid-tied with stand-alone capability
- 300 to 500 kVA grid-tied inverter
- Parallel dual inverter structure for a 400 kVA inverter
- DSP controlled 40 kVa inverter.



## 1.2 Output Voltage

- Delta, 3 phase
- Grid Mode 208 V Line to Line, +/- 10 %
- Stand Alone 208 V Line to Line, +/- 3 % From No Load to Full Load.

## 1.3 Output Frequency

- 50 Hz or 60 Hz Based:
- Grid Mode +/- 3 Hz
- Stand Alone Base Frequency +/- 0.5 Hz

## 1.4 Harmonic Distortion

- 5 % THD, Maximum 3 % Any Single Harmonic.
  - Grid Mode: Measured Parameter: Current
  - Stand Alone: Measured Parameter: Voltage

## 1.5 Output Current DC Bias

The DC current component of the inverter output shall have a maximum of 0.5 % of the full load rated current under all load and transient conditions. The inverter shall incorporate a means that regulates this parameter to zero and maintains this value for all operation conditions.

## 1.6 Grid Synchronization

The inverter shall incorporate a phase lock loop type of grid synchronization, that will synchronize to the base frequency +/- 3 Hz. This should also allow a synchronized transfer from stand alone to grid within +/- 5 degrees.

## 1.7 Lighting Protection

The inverter shall protect, without damage, all components within the inverter when subjected to transients listed in IEE C62.41.

## 1.8 Performance

### 1.8.1 Efficiency

Total efficiency of inverter operating at full power shall be 96 % minimum.

### 1.8.2 DC Link Range

The DC link voltage will be regulated at 400 VDC.

### 1.8.3 Fault Protections, Alarms and Warnings

#### 1.8.3.1 DC Link Under Voltage

Protect inverter from any abnormal faults such as, but not limited to, reverse power from utility, other modules when operating in parallel, or abnormal utility transients.

#### 1.8.3.2 DC Link Over Voltage

Protect inverter from any abnormal faults such as, but not limited to, reverse power from utility, other modules when operating in parallel, or abnormal utility transients.

#### 1.8.3.3 Inverter Over Current

Inverter shall protect semiconductors within safe current operating parameters. The inverter shall detect over current and automatically

*regulate to overload current limit value for a specified time duration. The overload and current limit values are stated in the table.*

#### *1.8.3.4 Input AC Protection*

- Utility Voltage Trip Point: Adjustable in 1 Volt Steps*
- Input Frequency Steps: 0.1 Hz*
- Disconnect Time: Inhibit inverter within 50 ms and open main contactor within 100 ms. These can be extended for customer requirements.*
- Reconnect Time: Adjustable in 6 sec increments to 30 minutes.*

#### *1.9 Functions - Synchronized Transfer From Stand Alone to Grid*

*A means of synchronizing inverter frequency and phase to grid frequency and phase shall be provided. The accuracy shall be within 5 degrees. This variance shall be small to prevent saturation of the load during synchronization interval.*

#### *1.10 Paralleling*

##### *1.10.1 Synchronize Signal*

*A means shall be provided to synchronize all parallel units, up to eight units so that they share power within 3 %, under all steady state, transient, short circuit and no load conditions.*

##### *1.10.2 Voltage Intertie*

*A control means shall be provided so that all modules in a parallel system act as one module under all steady state, transient, short circuit and no load conditions and share power within 3 % of each module's rating.*

*When individual modules are operated as single units, no hardware modifications are expected.*

#### *1.11 CAN Messages*

*The CAN message shall include at least the following measurement with 2 % accuracy:*

- Inverter Line to Neutral Voltages*
- Inverter Currents*
- Power Factor*
- Total Output Kilowatts*
- DC Link Voltages*

#### *1.12 Calibration*

*The unit when operating in grid-tied mode shall have appropriate sensing to monitor the grid voltage and frequency within the specified increments listed in specifications. The sensing shall maintain accuracy over the total temperature range for the design life of the equipment. The sense circuit trip points will be settable via the CAN bus from external hardware. The parameters will reside as permanent values until they are changed with appropriate password protected protocol. The voltage and frequency trip points will have the capability to verify trip point values and time from external inputs.*

#### *1.13 Anti Islanding*

*The unit shall use a phase lock loop to synchronize to the utility and incorporate a means to detect and prevent islanding as specified in IEEE P1547.*

### 2.7.3.2. 300 to 500 kVA PV Inverter Specifications

- System power: 400 kW, 500 kVA
- Power factor: +/- 0.822 (compensation over that range)
- 3 phase, 4 wire inverter
- Voltages: 480/277 V, 3 phase, 4 wires
- No transformer
- 2 per unit fault current for 10 seconds ("pullback" or fold back curve)
- 50 % unbalance, any line to neutral
- 0.5 % DC current injection
- < 2 % THD (V) over claimed operating range (i.e, 50 % - 100 % linear load), < 5 % with non-linear load
- Noise: 65dbA@3 meters
- MTBF = 50,000 hours
- Loss of any element results in power reduction <= 50 %
- Weight Target <= 1 pound per kW
- Package: Width: 3 feet, Height: 4 feet, Depth: 1.5 feet
- Environment: Temp: -40 C to 60 C, Altitude: up to 10,000 feet
- Humidity: 95 % relative humidity, non-condensing
- Operating Modes: Import, Export, Stand Alone, Parallel
- Voltage source/current source: master/slave

#### **Interface Characteristics**

<b>Characteristic</b>	<b>Requirement</b>
Voltage	
a) Nominal	900 Vdc
b) Voltage Range	781 Vdc to 1034 Vdc
c) Voltage Ripple	1 % of nominal

### Output Requirements

<b>Characteristic</b>	<b>Requirement</b>
Voltage nominal	450 rms.
a) Tolerances	
1) Average of three line to line voltages	0.5 %
2) Any one line to line voltage including a)1 and a) 3	1.167 %
3) Line Voltage unbalance	1 %
4) Voltage cyclic variations	1 %
b) Voltage transient	
1) Voltage transient limit	+/- 5 %
2) Voltage transient recovery time	250 ms
c) Voltage wave form	
1) Total harmonic distortion (THD)	2 %
2) Maximum single harmonic	1 %
Frequency	
1) Nominal	60 or 400 Hz
2) Frequency tolerance	+/- 0.5 %
3) Frequency transient	+/- 0.5 %
4) Frequency transient recovery time	250 ms
Full load Rating	300 kWatts, 240 <a href="#">kVA@.8</a> pf @ Vin = 860 Vdc
Over load rating	2 p.u. for 5 seconds
Step Loading	+/- 5 % deviation
1) No load to 1 p.u.	250 ms recovery time
2) 0.5 p.u. to +/- 0.5 p.u.	
3) From 1 p.u. to 0 p.u.	

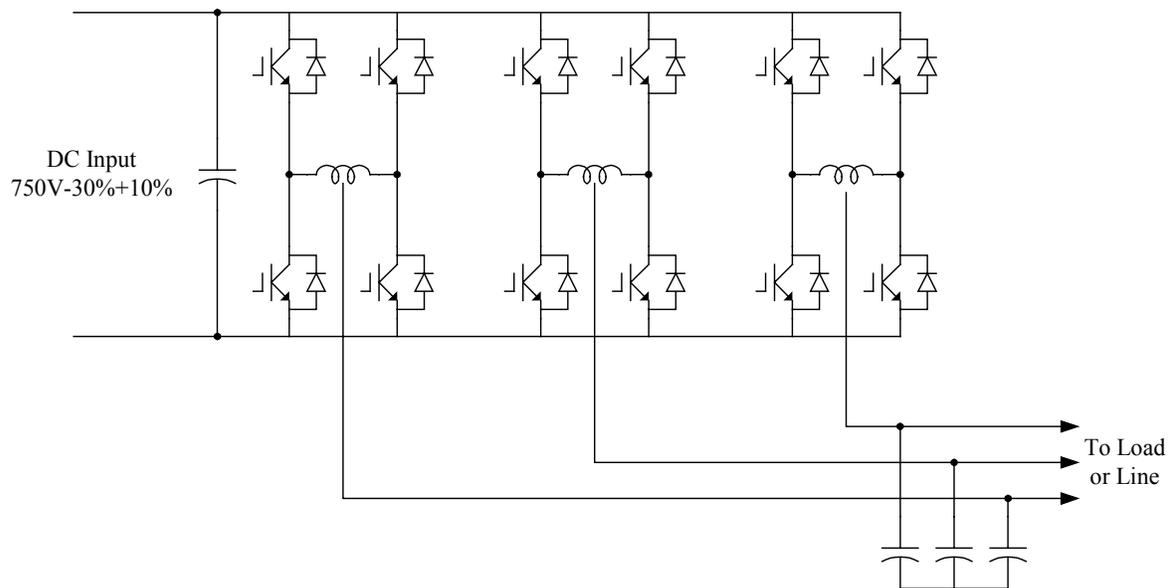
#### 2.7.3.3. Possible Inverter System Structure for Large Power Application

##### **Parallel Dual-Inverter Structure:**

Parallel Dual-Inverter Features that **cannot be obtained** from mere parallel operation of multiple inverter systems:

- Wide DC input range 750 V – 30 % + 10 % for 480 Vac output
- No circulating current
- Higher efficiency

- Lower switching frequency
- More compact and lighter weight
- Less component count
- High reliability
- Less THD
- Only one output filter
- Less cost
- Only one unified control circuit
- Less EMI
- No interference between inverters nor load sharing problems
- No DC voltage/DC current problems



#### 2.7.4. Brief Description of 400 kW Parallel Dual Inverter System

The 400 kW parallel-dual-inverter system employs two inverters connected in balanced-parallel fashion by using common and economical IGBTs to reach the power rating, high efficiency, compactness, and less THD that is desired. The two inverters operate interactively together as one inverter system apparent to the load or utility line. As a result, the equivalent inverter switching frequency is doubled, thus minimizing power losses and output filter size. At the same time, the reliability is greatly improved and device derating is not necessary compared with the single inverter system using parallel IGBTs because of the redundancy

and no device-sharing problems. In addition to the basic requirements, some other main features and operating conditions are summarized as follows:

- Flexible for multiple system parallel operation
- DC bus voltage:  $750\text{ V} \pm 50\text{ V}$
- IGBT switching frequency: 5 kHz, equivalent inverter switching frequency: 10 kHz
- Inverter efficiency:  $> 98.5\%$  @ 400 kW
- Minimized switching ripples and EMI

DSP Controlled Universal Power Converter Specifications:

- Texas Instruments (TI) TMS320F240 Digital Signal Processor for control applications with 20 MIPs
- Three-phase power converter/inverter system with AC-DC, DC-DC and DC-AC stages
- Sine voltage and sine current output
- Any shape of voltage or current output
- Suited for motor drives, utility interface, active power filters, UPS, etc
- DSP controlled, flexible reconfiguration, customized control possible
- DC-DC boost chopper for various DC voltage sources (e.g., fuel cell, battery, photovoltaic, micro-turbine generator, wind power, etc.)
- Inverter is suited for three-phase 3 wire or three-phase 4 wire systems
- Over temperature, over current, over voltage, under voltage, short-circuit protections are embedded for reliable operation
- Universal current and voltage sensors included for various applications

#### 2.7.4. A DSP Controlled Universal Power Converter Design

A line interactive power system could be developed for interfacing a renewable energy source, such as a solar, to a utility line. The proposed power system is rated at 40 kW, 208/120 V and 60 Hz three-phase base, capable of delivering up to 40 kW power with unity power factor to the line and loads. The current waveform will meet IEEE 519 requirements with a total distortion factor (THD) of less than 5 %.

The power system can be configured as a stand-alone distributed power system providing power to loads with a precise voltage ( $208\text{ V} \pm 2\%$ ) and frequency (60 Hz or  $50\text{ Hz} \pm 0.01\%$ ) regulation. The three-phase voltage is well balanced and sine wave with THD less than 5 % under nonlinear loads with a current crest factor of three.

The power system is based on an insulated-gate-bipolar-transistor (IGBT) inverter switching at up to 10 kHz, controlled fully by a TMS320C240 DSP board, and equipped with all necessary protections, such as over-voltage, over-current, and over-temperature shut-down, shoot-thru protection, unsynchronized operation protection, and under-voltage lock-out.

The power system is featured with power control loop, current control loop, voltage control loop, and DC interface. Compensation for DC voltage variation is incorporated into the voltage control. A digital phase-lock loop (PLL) is used to synchronize the control with the line. A damping control of the output filter's resonance is provided to enhance the dynamic performance, thus fastening the response time and widening the control bandwidth.

Detailed technical information of this type of line interactive power system follows.

### **System Configuration**

Figure 2-16 shows the system configuration of the line interactive power system. The terminals R, S, T, and 0 are connected to the primary power source. A seven pack IGBT integrated power module (IPM) is employed for converting DC power to 60 Hz or 50 Hz AC power. The IPM is rated at 600 V and 300 A with a pre-drive and protection circuit. A passive LC filter is used to eliminate the inverter's PWM switching ripples and reduce EMI. Center-tapped DC capacitors are used to provide a constant DC voltage and a neutral for three-phase 4-wire applications so that the output transformer can be eliminated. As a result, the power system is much more compact and lighter weight.

The inverter control circuit consists of three printed circuit boards: mother board, DSP board, and gate drive board. In the mother board, voltage sensors, signal conditioning circuit, and digital logic circuit are disposed. The voltage sensors detect the three-phase voltages ( $V_{sa}$ ,  $V_{sb}$ , and  $V_{sc}$ ) and DC voltages ( $V_p$  and  $V_n$ ). The signal conditioning circuit provides level shifting and scaling functions and feeds all analog signals needed to the DSP A/D converters. The current signals are obtained from DCCTs. The digital logic section provides: (1) Power-on reset to gate drive circuit, (2) Stop/Run signal to the DSP board, (3) Power device alarm/protection signal interface to the DSP, (4) Gate block signal interface, and (5) Gate signal interface. The DSP board piggybacks on the mother board. The gate drive board includes four isolated DC/DC converters providing power to the gate drive circuit and an opto-coupler circuit isolating the gate drive circuit from the digital logic circuit. A power supply board is used to provide + 5 V and +/- 15 V power to the control boards. The power supply board can be fed from either the DC link or the utility line (120 V or 208 V).

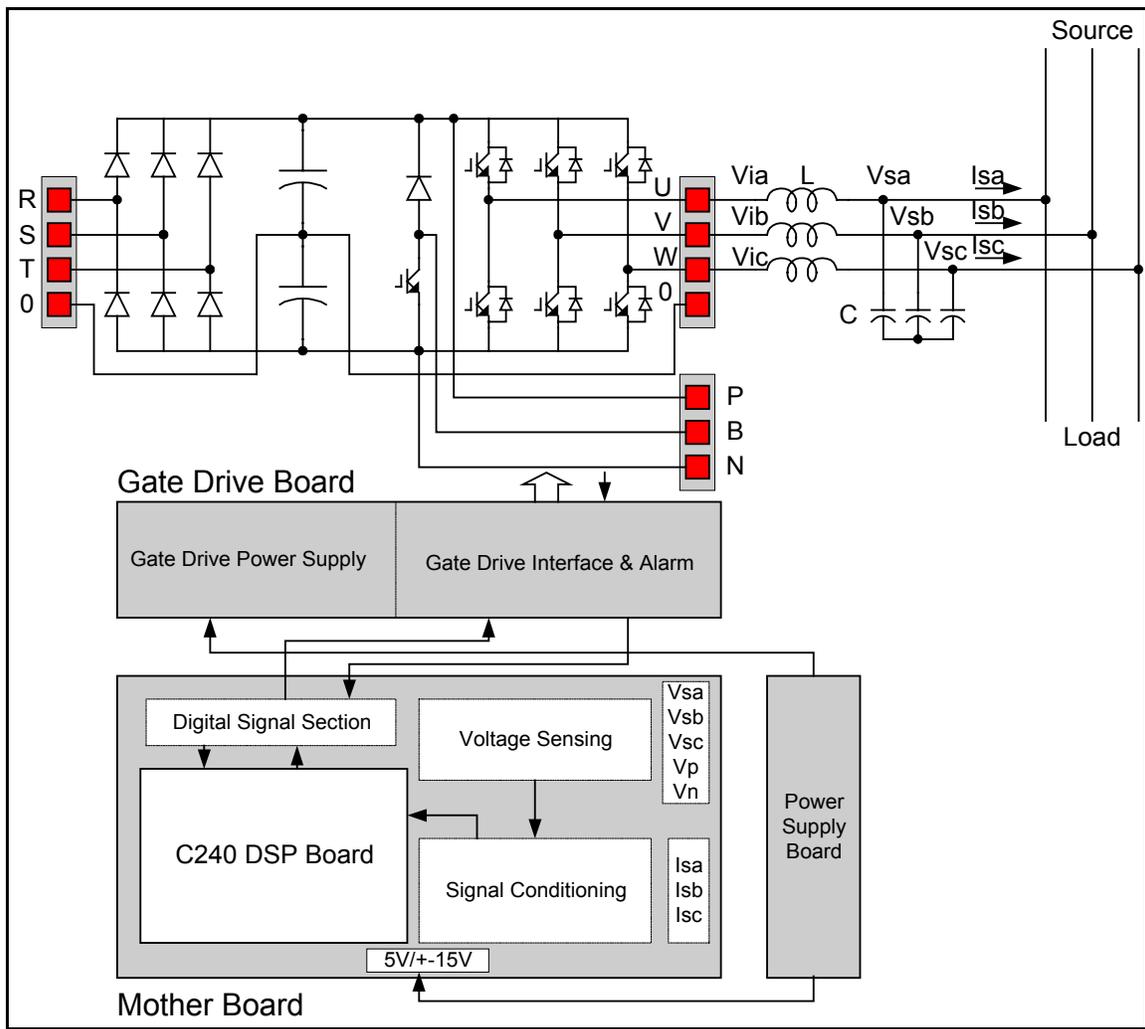


Figure 2.16. System Configuration of the Line Interactive Power System

### Design of a 40 kW Inverter

The design of a line interactive power system is presented. The unit can be used for interfacing a power source, such as a renewable energy source, to a utility line. The power system is rated at 40 kW, 208V/120V, 50/60Hz with a three-phase base. It is capable of delivering up to 40 kW power with unity power factor to the line and loads. The current waveform meets IEEE 519 requirements with a total distortion factor (THD) of less than 5%.

The power system can be configured as a stand-alone distributed power system providing power to loads with a precise voltage ( $208V \pm 2\%$ ) and frequency (60Hz or  $50Hz \pm 0.01\%$ ) regulation. The three-phase voltage is a well balanced sine wave with THD less than 5% under nonlinear loads with a current crest factor of three .

The power system is based on an insulated-gate-bipolar-transistor (IGBT) inverter switching at up to 10 kHz, controlled fully by a TMS320C240 DSP board, and equipped with all necessary protections, such as over-voltage, over-current, and over-temperature shut-down, shoot-thru protection, unsynchronized operation protection, and under-voltage lock-out.

The power system is featured with power control loop, current control loop, voltage control loop, and dynamic braking. Compensation for dc voltage variation is incorporated into the voltage control. A digital phase-lock loop (PLL) is used to synchronize the control with the line. A damping control of the output filter's resonance is provided to enhance the dynamic performance, thus reducing the response time and widening the control bandwidth.

This report describes the detailed technical information of this line interactive power system, including the system configuration, design details, control schemes (theory).

## **System Configuration**

The system configuration of the line interactive power system is shown in Figure 2.17. The terminals R, S, T, and 0 are connected to the primary power source. A seven pack IGBT integrated power module (IPM) is employed for converting dc power to 60Hz or 50Hz ac power. The IPM is rated at 600V and 300A with pre-drive and protection circuit. A passive LC filter is used to eliminate the inverter's PWM switching ripples and reduce EMI. Center-tapped dc capacitors are used to provide a constant dc voltage and a neutral for 3-phase 4-wire applications so that the output transformer can be eliminated. As a result, the power system is much more compact and lighter weight than traditional systems.

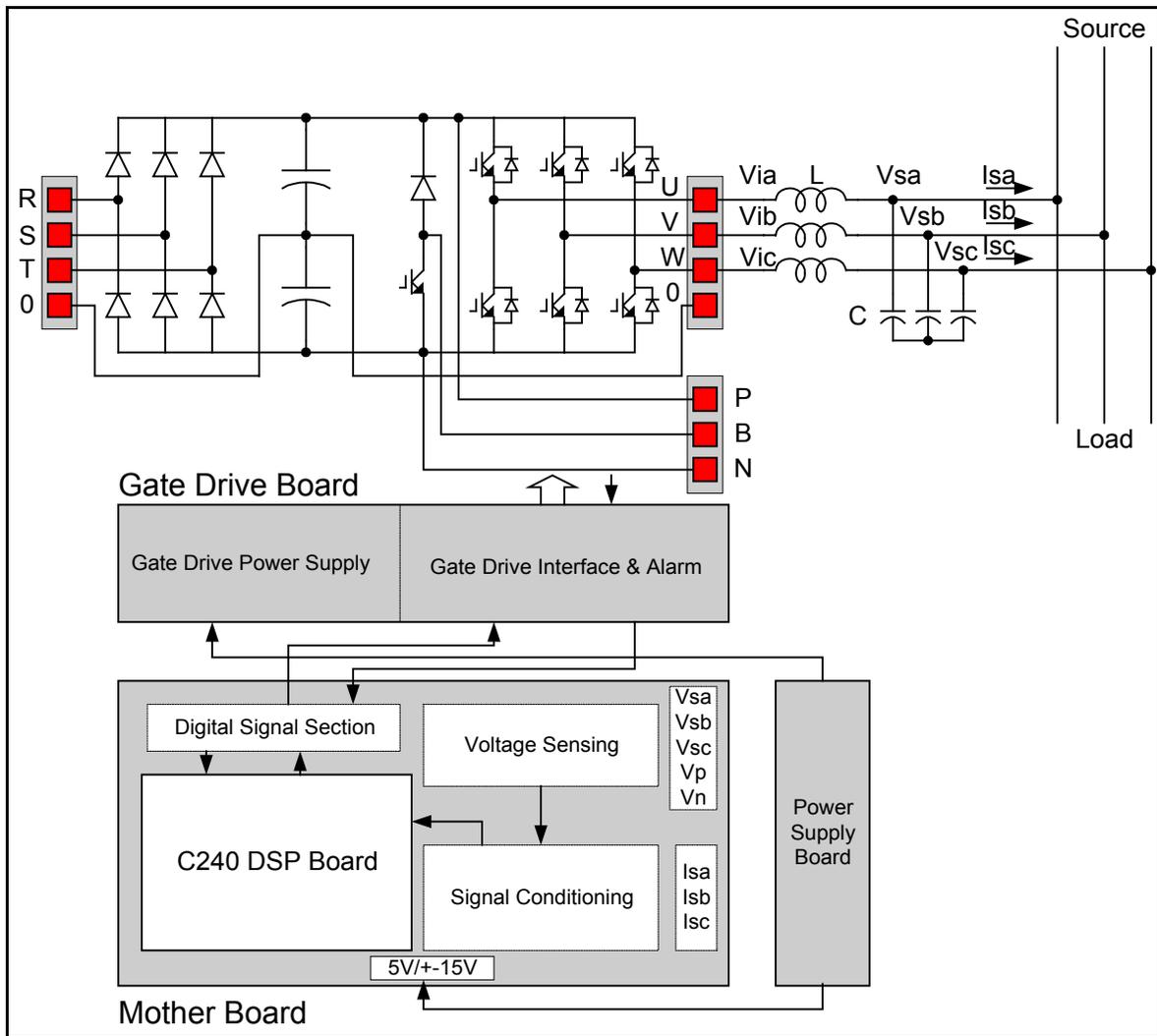


Figure 2.17. System Configuration of the Line Interactive Power System

The inverter control circuit consists of three printed circuit boards: motherboard, DSP board, and gate drive board. In the motherboard, voltage sensors, signal conditioning circuit, and digital logic circuit are disposed. The voltage sensors detect the three phase voltages ( $V_{sa}$ ,  $V_{sb}$ , and  $V_{sc}$ ) and dc voltages ( $V_p$  and  $V_n$ ). The signal conditioning circuit provides level shifting and scaling functions and feeds all analog signals needed to the DSP A/D converters. The current signals are obtained from DCCTs. The digital logic section provides: (1) power-on reset to the gate drive circuit, (2) Stop/Run signals to the DSP board, (3) power device alarm/protection signal interface to the DSP, (4) a gate block signal interface, and (5) gate signal interface. The DSP board piggy backs on the motherboard. The gate drive board includes four isolated DC/DC converters providing power to the gate drive circuit and opto-coupler circuit isolating the gate drive circuit from the digital logic circuit. A power supply board is used to provide +5V and  $\pm 15V$  power to the control boards. The power supply board can be fed from either the dc link or the utility line (120V or 208V).

## System Design

### Main Switching Devices:

The power rating is 40 kW at 60Hz 3-phase 208V and 139A. The dc voltage is 360V. The peak ac current, neglecting PWM ripple current, is 200A. A 7-pack 600V/300A IGBT IPM is used since dynamic braking is required.

### DC Capacitor:

The IGBT inverter can switch at up to 10 kHz. Therefore, we have

$$C_{dc} = \frac{I_{ripple} \Delta T}{\Delta V} = \frac{200A \cdot (4.0_{crest\_factor} / 2) \cdot (3.3ms / 6)}{6\% \cdot 360V} \cong 10mF. \quad (1)$$

### Output LC Filter:

Consider that the IGBT inverter's switching frequency is 10 kHz. A cutoff frequency should be set to 1k Hz to obtain 1:100 attenuation at the switching frequency. Therefore one has the following relations:

$$\frac{\omega_c}{\omega_1} = \frac{1}{\sqrt{LC}} = \frac{1kHz}{60}, \quad (2)$$

$$\frac{\omega_c}{\omega_1} L = \frac{1}{2I_{PWM-ripple}}, \quad (3)$$

where  $\omega_c$  is the cutoff frequency,  $\omega_1$  is the line frequency,  $L$  and  $C$  are the filter inductor and capacitor in per unit ( $pu$ ).  $I_{PWM-ripple}$  is the maximum allowed ripple current in  $pu$ . In equations (2) and (3), we have  $L=7.5\%$  and  $C=4.5\%$  when

$$I_{PWM-ripple} = 38\%.$$

### Diode Bridge:

Based on the power rating, a 600V/160A 3-phase diode bridge is employed. The generator's neutral is connected to the center tap of the dc capacitors so that a balanced dc voltage is applied to each capacitor.

## System Control Theory and Schemes

The power system is fully controlled by the DSP. For line interactive applications, power control is generally needed. For stand-alone applications, a precise voltage control (or regulation) is required in order to provide high quality power to loads, linear or nonlinear. This section describes all necessary control schemes to satisfy the requirements.

### Control Scheme for Line Interactive Applications:

Figure 2.17 shows the control block diagram for line interactive applications, where  $P^*$  is the power command, the power that the inverter should convert and feed into the line.  $V_s_{abc}$  are the three line phase voltages, and  $I_s_{abc}$  is the actual current into the line that the power system generates. There are six main blocks in Figure 2.17. The following sections will explain each block's function.

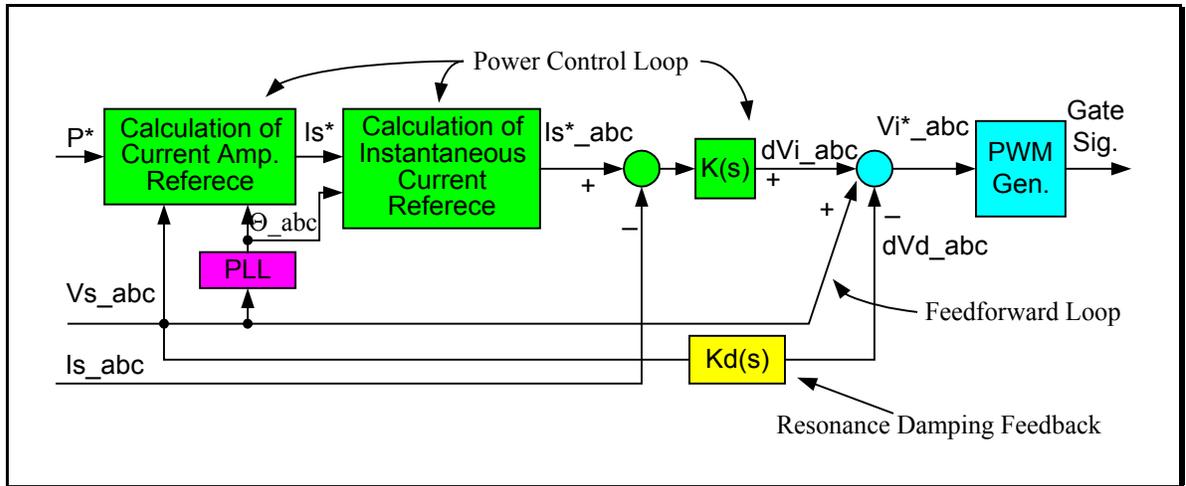


Figure 2.17. Control Block Diagram of Line Interactive Power System

### Power Control Loop

The power control loop consists of four blocks: the “calculation of current amplitude reference” block, the “calculation of instantaneous current reference” block, the summation block, and the “K(s)” block. The relations of these blocks can be expressed as follows:

$$I_S^* = \frac{2P^*}{\sqrt{3}V_S}, \quad (4)$$

$$I_{S\_abc}^* = I_S^* \cdot \sin \Theta_{\_abc}, \quad \text{and} \quad (5)$$

$$dV_{i\_abc} = K(s) \cdot (I_{S\_abc}^* - I_{S\_abc}), \quad (6)$$

where  $V_S$  is the peak value of the line voltage,  $\Theta_{\_abc}$  is the phase angle provided by the phase lock loop (PLL). In this power control loop,  $K(s)$  is the only design parameter. It can be determined as follows:

$$\|K(s)\| \geq \frac{L}{\Delta P}, \quad (7)$$

where  $\Delta P$  is the tolerance error in  $pu$ . In the system, considering  $\Delta P=5\%$  one has  $\|K(s)\| \geq 1.5pu$ , as  $L=7.5\%$ .

### Digital Phase Lock Loop (PLL)

A digital PLL is implemented in DSP to provide synchronization with the line and phase angles ( $\Theta_{\_abc}$ ) to the current calculation block. The PLL needs to provide absolutely stable phase lock to the line frequency even when the line has a relatively large frequency variation.

## Resonance Damping Feedback Loop

A derivative feedback loop is added to damp the output filter's resonance. A resonance may occur between the output filter inductor  $L$  and capacitor  $C$  or between the capacitor  $C$  and the line impedance, especially when the line is relatively weak. This loop provides a damping function to the resonance, thus increasing dynamic response. The feedback loop is expressed as:

$$dV_{d\_abc} = K_d s \cdot V_{S\_abc} \cdot (8)$$

This feedback loop changes the system equation from  $[LCs^2 + RCs + 1]$  to  $[LCs^2 + (RC + K_d)s + 1]$ , thus enhancing a damping factor.  $R$  is the equivalent resistance of the inductor.  $K_d$  can be designed using the following guideline:

$$K_d \geq \frac{1}{\omega_c} = \sqrt{LC} \cdot (9)$$

## Feed-forward Loop

A feed-forward loop is included to enhance dynamic response and stability because it can reduce the required loop gain,  $\|K(s)\|$ , in the power control loop.

Without this feed forward loop, equation (7) should be modified as:

$$\|K(s)\| \geq \frac{1}{\Delta P} \cdot (10)$$

The inverter output voltage reference  $V_{i\_abc}^*$  is represented as:

$$V_{i\_abc}^* = V_{S\_abc} + dV_{i\_abc} + dV_{d\_abc} \cdot (11)$$

From the voltage reference, PWM gate signals are generated by C240 DSP itself using triangular comparison.

## Control Scheme for Stand-alone Applications:

For stand-alone applications, voltage regulation and THD control are required. Figure 2.18 shows the single phase equivalent circuit. Three voltage control schemes can be used to achieve the voltage regulation and THD requirements, which are described as follows.

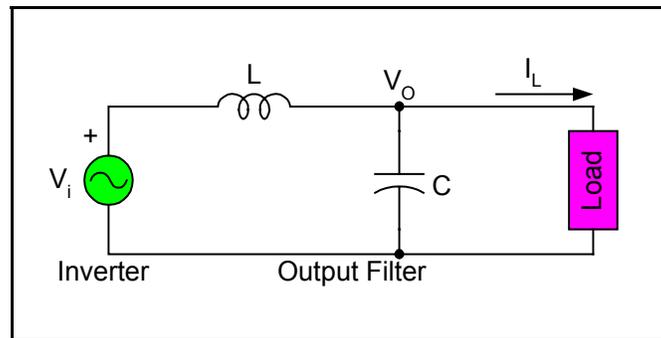


Figure 2.18. Single Phase Equivalent Circuit of a Stand-Alone System

## 1. Voltage Feedback Method

Figure 4 shows the control block diagram of the voltage feedback scheme for stand alone applications, where  $V_o^*$  is the voltage reference,  $I_L$  is the load current,  $V_i$  is the inverter output voltage,  $V_o$  is the output voltage of the power system,  $K(s)$  is the feedback transfer function given as

$$K(s) = K_p + K_d s, \quad (12)$$

$K_p$  is a proportional gain and  $K_d$  is a derivative gain.

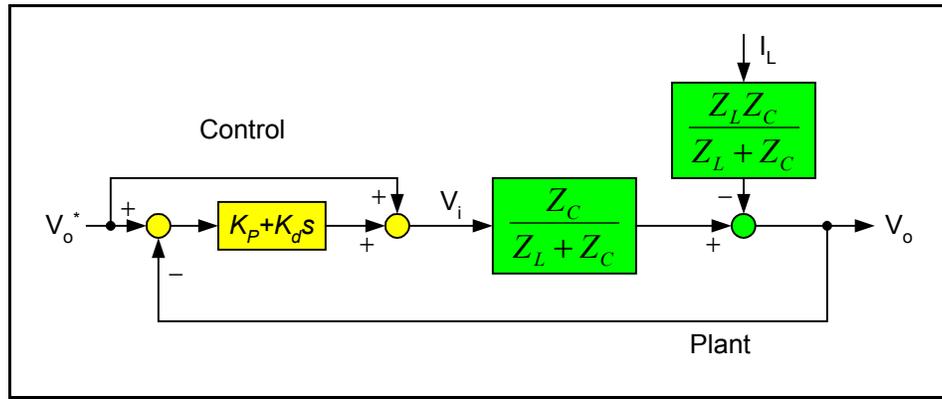


Figure 2.19. Control Block Diagram of the Voltage Feedback Scheme for Stand-Alone Applications

From Figure 2.19, we have

$$V_o = \frac{K_d s + (1 + K_p)}{LCs^2 + K_d s + (1 + K_p)} V_o^* - \frac{Ls}{LCs^2 + K_d s + (1 + K_p)} I_L. \quad (13)$$

It is clear from (13), that the larger the  $K_p$ , the closer the output voltage  $V_o$  approaches to the reference  $V_o^*$ .

## 2. Load Current Feed-forward Method

Figure 2.20 shows the control block diagram of the load current feed-forward control scheme for stand alone applications, where the inverter voltage is given as

$$V_o = V_o^* + Ls \cdot I_L. \quad (14)$$

One has the following output voltage characteristics under this control method:

$$V_o = \frac{Z_c}{Z_L + Z_c} V_o^*. \quad (15)$$

Equation (15) shows that the output voltage is independent of the load current, which is desirable.

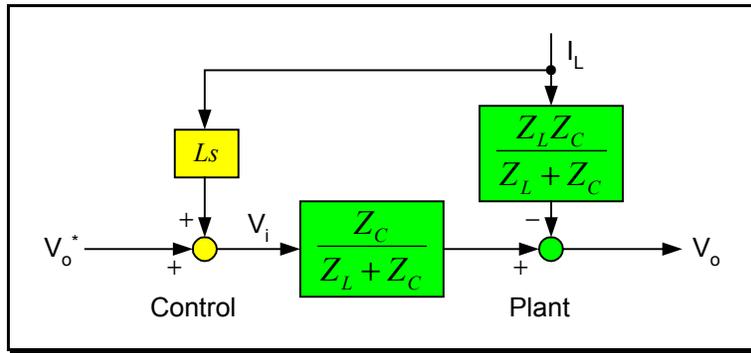


Figure 2.20. Load Current Feed-Forward Control

### 3. Load Current Feed-forward Control with Resonance Damping

Figure 2.21 shows the control block diagram of the load current feed-forward control scheme with resonance damping for stand alone applications, where the inverter voltage is given as

$$V_o = V_o^* + Ls \cdot I_L - K_d s. \quad (16)$$

On has the following output voltage relation under this control method:

$$V_o = \frac{1}{LCs^2 + K_d s + 1} V_o^*. \quad (17)$$

Equation (17) shows that the output voltage is independent of the load current and free of resonance, which is desirable.

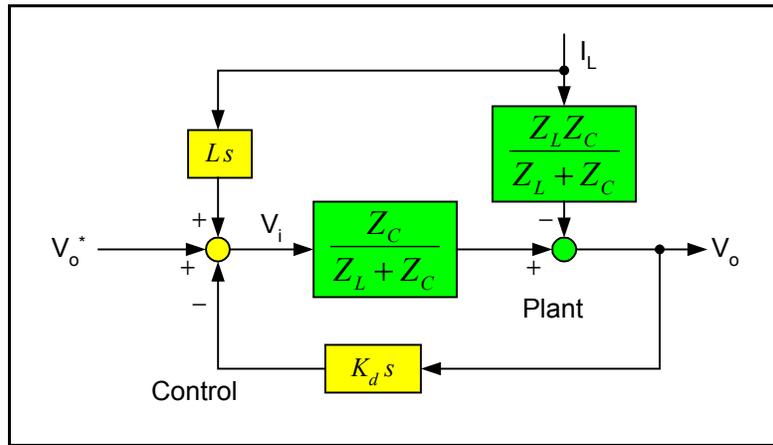


Figure 2.21. Load Current Feed-Forward Control + Resonance Damping

### PWM Compensation of dc Voltage Variation

The traditional triangular comparison PWM assumes that the dc voltage is constant. Therefore, the carrier's peak value is set constant, which makes the output voltage "beat" accordingly with the dc voltage variation. Figure 2.22

illustrates the “beat” effect. Figure 8 shows a compensation method that eliminates the “beat.”

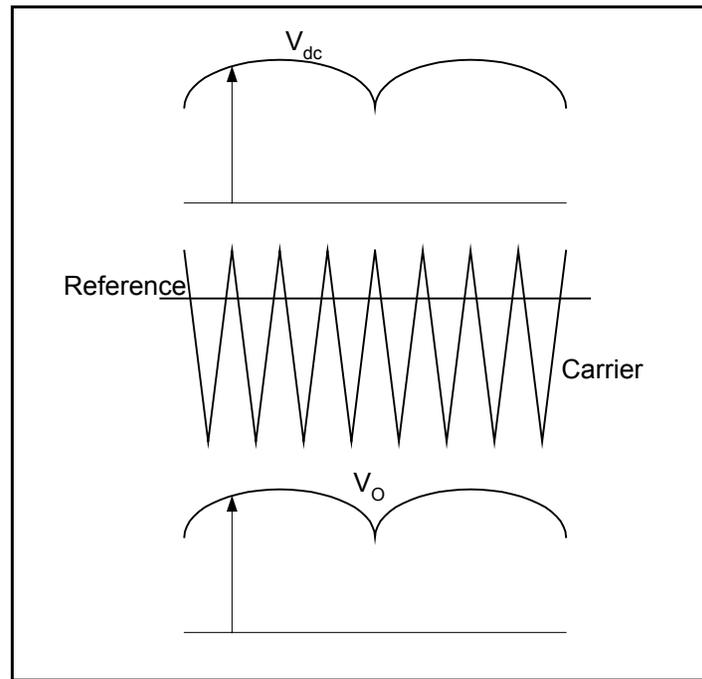


Figure 2.22. The “Beat” Effect of dc Voltage Variation

## **Section 3. Xantrex Technology**

### **3.1 Present Status of Power Electronics Technology**

#### **3.1.1. Safe Operating Area (SOA)**

Power semiconductor IGBTs and FETs operate in power inverters to control the flow of energy from the PV array to the AC Line. They are typically placed in the circuit between a bank of capacitors storing a large amount of energy, and an inductor connected to the AC output. The flow of energy is controlled by commanding the power devices to switch on and off repeatedly. When the semiconductor switch is in the off state, the inductor current must continue to flow, and a diode is placed in the circuit for this purpose.

The Safe Operating Area (SOA) for a power semiconductor IGBT or FET is a maximum operating condition which must be met during the switching transients. This condition is a function of the simultaneous voltage imposed across the device and current flow through it. These transients may be described as turn-on and turn-off, and each of these transients may have a characteristic stress on the power semiconductor device.

The SOA of a device is absolute and the failure mode for exceeding this rating is catastrophic failure of the device. Therefore, the effect of derating is to allow room for unexpected or unseen elements of the applied voltage and current stress without exceeding the SOA.

For the highest reliability, devices should be chosen which have an SOA which allows the highest worst-case transient current simultaneously with the highest input voltage switching spike that may arise, even though these are not expected to occur at the same time.

### **3.1.2. Turn-On Switching**

Turn-on imposes the highest transient current stress through the device. During turn-on, a large initial voltage is present and the device turn-on current will rise to a current equal to the sum of the output inductor current and the diode recovery current, before the device voltage begins to drop to the saturation voltage of the device. Diode recovery currents can be quite high, so during turn-on a current much higher than the steady-state current is drawn through the device while the full input bus voltage is present. Particular attention must be paid to the diode temperature characteristic because the diode recovery time is typically very temperature dependent. Turn-on SOA stress may be reduced with the use of faster diodes and by reducing the turn-on speed of the device.

#### **3.1.2.1. Turn-Off Switching**

Turn-off imposes the highest voltage stress across the device. During turn-off the output inductor current continues to flow as the device turns off, as the voltage across the switch device rises to the point where the diode is forward biased and the inductor current flows through the diode. Due to the inductance of the component interconnections and the impedance of the bus capacitors, the voltage rise due to the inductor current will exceed the bus voltage, sometimes by hundreds of volts. There may be many frequency components of the voltage overshoot, and identifying and controlling this factor is critical to maintaining compliance with the SOA requirements of the semiconductor switching device. Device turn-off stresses may be reduced with the use of dampening circuits called snubbers. These circuits can reduce the overshoot by dampening the ringing, and can conduct some of the inductor current away from the device.

### **3.1.3. Power Switch Thermal Management**

Semiconductor reliability is quantified according to the period of time for which the device will perform its specified function in a given environment. The longer the time period, the greater the reliability of the device. Failure of the device to perform its specified function may occur as a parametric failure or a catastrophic failure. Parametric failures of power devices in inverters are not likely to cause reduced performance of the inverter. Rather, these devices most often continue to degrade until catastrophic failure occurs.

#### **3.1.4. Semiconductor Reliability**

The most frequently used reliability measure for semiconductor devices is the failure rate ( $\lambda$ ). The failure rate is obtained by dividing the number of failures observed, by the product of the number of devices observed and the number of

hours operated, usually expressed as the percent of failures per thousand hours, or failures per billion device hours (FITS).

The failure rate of semiconductor devices is inherently low. As a result, the industry uses a technique called accelerated testing to assess the reliability of semiconductors. During accelerated tests, elevated stresses are used to produce, in a short period, the same failure mechanisms as would be observed during normal use conditions. Temperature, relative humidity, and voltage are the most commonly used stresses used during accelerated testing. The devices are tested near their maximum junction temperatures and failures are analyzed to verify that they are of a type that is accelerated by temperature. Known acceleration factors are then applied to estimate the failure rates for lower junction temperatures.

Following are some sample reliability data for IGBTs and FETs manufactured by Intersil, International Rectifier, and ON Semiconductor:

INTERSIL POWER DEVICE RELIABILITY SUMMARY				
DEVICE: IGBT		PACKAGE: TO-247		
PROCESS N IGBT => 600 V NON PUNCH THRU				
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
THERMAL FATIGUE Pd=40 w, Delta=100 deg c	0	76	760,000	CYS
OPERATING 15 volts, T=200 deg c.	0	79	79,000	HRS
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	0	80	80,000	HRS
HIGH TEMP GATE BIAS 100% Rated voltage, 150 deg c.	0	80	80,000	HRS
TEMPERATURE CYCLE -65 to 150 deg c. Air/Air	0	80	120,000	CYS
AUTOCLAVE T=121 deg c, 15 psig	0	80	7,680	HRS
HUMIDITY BIAS 80% Rated(40v max) 85c/85rh	0	79	79,000	HRS
<b>FAILURE RATE @ 55 Deg. C, 60% Confidence, 1.0 EV Activation: 4.102629 FIT</b>				

INTERSIL POWER DEVICE RELIABILITY SUMMARY				
DEVICE POWER MOS		PACKAGE TO-262		
PROCESS MEGAFET PCH PWR MOS STD GATE				
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
THERMAL FATIGUE Pd=4.75 w, Delta=100 deg c.	0	160	1,600,000	CYS
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	0	160	160,000	HRS
HIGH TEMP GATE BIAS 100% Rated voltage, 150 deg c.	0	160	160,000	HRS
TEMPERATURE CYCLE -65 to 150 deg c. Air/Air	0	160	160,000	CYS
AUTOCLAVE T=121 deg c, 15 psig	0	120	20,160	HRS
HUMIDITY BIAS 80% Rated(40v max) 85c/85rh	0	160	80,000	HRS
<b>FAILURE RATE @ 55 Deg. C, 60% Confidence, 1.0 EV Activation: 2.051315 FIT</b>				

INTERNATIONAL RECTIFIER POWER DEVICE RELIABILITY SUMMARY				
DEVICE: FET		PACKAGE: TO-247		
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
THERMAL FATIGUE Pd= $\Delta T_J / \theta_{JA}$ , $\Delta T_J = 100$ deg c	0	255	1,275,000	CYS
TEMPERATURE CYCLE -55 to 150 deg c. Air/Air	1	2,472	2,472,000	CYS
AUTOCLAVE T=121 deg c, 15 psig	0	590	56,640	CYS
HUMIDITY BIAS 100v 85c/85rh	4	1018	1,018,000	HRS
HIGH TEMP GATE BIAS 100% Rated voltage, 150 deg c.	5	510	510,000	HRS
<b>Equivalent Failure rate @ 55 Deg. C: 1.21 FIT</b>				
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	29	1,363	1,363,000	HRS
<b>Equivalent Failure rate @ 55 Deg: 147 FIT</b>				
INTERNATIONAL RECTIFIER POWER DEVICE RELIABILITY SUMMARY				
DEVICE: IGBT		PACKAGE: TO-247		
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
THERMAL FATIGUE Pd= $\Delta T_J / \theta_{JA}$ , $\Delta T_J = 100$ deg c	0	20	10,000	CYS
TEMPERATURE CYCLE -55 to 150 deg c. Air/Air	0	307	15,965	CYS
HUMIDITY BIAS 100v 85c/85rh	7	70	6067	HRS
HIGH TEMP GATE BIAS 100% Rated voltage, 150 deg c.	0	80	8,268	HRS
<b>Equivalent Failure rate @ 55 Deg: 904 FIT</b>				
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	0	110	9,142	HRS
<b>Equivalent Failure rate @ 55 Deg: 57 FIT</b>				

ON SEMICONDUCTOR POWER DEVICE RELIABILITY SUMMARY				
DEVICE: FET TMOS VII		PACKAGE: TO-220		
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	0	2520	1,309,760	HRS
<b>Equivalent Failure rate @ 55 Deg: 2.324 FIT</b>				

ON SEMICONDUCTOR POWER DEVICE RELIABILITY SUMMARY				
DEVICE: IGBT		PACKAGE: TO-220		
APPLIED STRESS	FAILURES	SAMPL E	CUMUL. TIME	UNIT S
HIGH TEMP REV BIAS 80% Rated voltage, 150 deg c.	0	2,032	1,160,256	HRS
<b>Equivalent Failure rate @ 55 Deg: 2.62 FIT</b>				

In order to utilize these data, it becomes necessary to determine the failure rate required for a 10 year MTTF.

For this analysis we will use the scenario that the inverter has a total of 12 semiconductor power switch devices die; either 4 IGBTs in each phase of a 3-phase inverter, or a parallel configuration of FETs in a single phase inverter. Ten years contain a total of 87,600 hours. If we assume an average of 12 hours per day of inverter operation, then a 10 year MTTF will require a failure rate of:

**12 (devices)\* (87,600 / 2) = 525,600** hours of operation per device failure,  
or  
 **$\lambda = 1,903$  FITS.**

We might further assign that 40% of the total allowable inverter failures may be due to semiconductor power switch device failures related to operating temperature, reducing our allowable failure rate to:

**$\lambda = 0.4 * 1903 = 761$  FITS.**

The data presented above applies to operation at 55 Deg. C. Failure rate increases at the rate of a factor of 2 for each 10 Deg. C. increase in junction temperature, so for a junction temperature of 95 Deg. C. the allowable failure rate is reduced to:

$$\lambda = 761 / (2^{((95-55))/10}) = 48 \text{ FITS}$$

This type of data is called a point estimate because it is based on a portion, or sample, of the total devices manufactured. Therefore the data often vary as the sample size varies, and also because some production runs perform better than others. Looking at the data above we see 1 lot that does not satisfy our goal. In fact the failure rate of that lot is 904 FITS, which in this example would result in almost 2 failures per year at a junction temperature of 95 Deg. C. In order to achieve a 10 year MTTF these parts would have to operate at a junction temperature of only 50 Deg. C., which is not practical.

All of the other device lots will exceed our requirements for a 10 year MTTF. However, additional measures such as burn-in and protection from humidity are needed to prevent some production runs from falling short of the goal.

### **3.1.5. Power Switch Transient Effects**

Transients can be caused by unexpected internal operation commands and by external events. Transient effects can cause failure of the semiconductor power switch devices by exceeding the device SOA, and by exceeding the device maximum operating junction temperature. The power devices are protected from transients by circuitry and software that inhibit or modify operation during transients.

As discussed in an earlier section of this paper, the SOA of a power device might be exceeded during transients, even though it has margin during normal operation. To mitigate this failure mode, the designer must take into account the protection setpoints and the reaction time of protection circuitry. The peak voltage and current values that may be reached during these times must allow for the turn-off of devices under those conditions without exceeding the SOA, or inverter failure will result.

Short-term dissipation in semiconductor power switch devices may exceed the average dissipation by a factor of 100 and more. When this peak dissipation lasts for only several hundred nanoseconds, the effect on junction temperature may be only a few degrees. However, after several microseconds the device junction begins to heat up substantially. When protecting switch devices from transients, the set points and reaction times must be considered to maintain acceptable junction temperature during the sustained portion of the transient as well as the device turn-off.

### 3.1.6. Paralleled Switching Devices

When several semiconductor switching devices are connected in parallel to reduce the dissipation in each device, and thus the junction temperature of each, steps must be taken to ensure that the power dissipated is spread somewhat evenly between the devices.

#### 3.1.6.1. Conduction Losses

Power MOSFETs and IGBTs have a positive temperature coefficient. Therefore, if one device rises to a higher temperature than the others, it will then conduct a smaller percentage of the total current, thus reducing its share of the total dissipation. This eliminates the likelihood of a thermal runaway condition where the hottest device draws an increasing share of the power, which raises its temperature, thus causing even more dissipation. However, for the best current sharing, devices may be tested for initial saturation voltage, and matched up in sets with similar characteristics.

This positive temperature coefficient results in very good sharing of load current during the conduction part of the switching cycle of these components, and the major remaining concern for current sharing is during transients.

#### 3.1.6.2. Transient Losses

In addition to the types of transients addressed in section 1.4, *Power Switch Transient Effects*, there are repetitive transients as the devices switch on and off as described in section 1.1, *Safe Operating Area*.

Current sharing during the repetitive switching transients requires close attention during the design of an inverter. This current sharing is affected by the gate threshold and the switching speed of the devices to be paralleled. These parameters are not specified in sufficient detail by the manufacturers to ensure suitable power sharing during switching. Instead, they can be measured during the design phase of an inverter, so that the final circuit design is such that the semiconductor power switch devices share the power of the switching transients. When current sharing during switching transients is inadequate, there are two probable failure modes; exceeding the SOA, and exceeding the maximum junction temperature. Each of these failure modes may be mitigated by taking measures to ensure current sharing during switching and by allowing suitable design stress margin.

#### 3.1.6.3. Gate Threshold

The gate threshold of MOS devices is specified at very low current and voltage, and usually has a range of 2 volts. In order to promote concurrent switching of

the power devices, it is necessary to approximate a current source into each MOS device gate, so that they each establish a gate voltage at its individual threshold. This is accomplished by having individual gate resistors for each device, and ensuring that the driver(s) have sufficient current handling ability that they are able to fully saturate while delivering gate current to all of the devices. If the gate resistors are too small for the driver's capability, the driver will come out of saturation due to the large current demand, and the devices with the highest gate threshold will receive a different gate charge rate than those with the lowest threshold.

#### 3.1.6.4. Switching Speed

Switching speed is affected by a parameter called Total Gate Charge. Fortunately, the same resistor and driver configuration used to address gate threshold will provide a means to regulate the gate charge rate. The circuit designer can control only the gate charge rate – the total gate charge of devices to be paralleled must be similar to ensure that they switch together. The gate charge parameter is often specified by manufacturers only as a typical value, and wide range may be allowed. For example, the IRFP250 specification states a typical value of 79nC and a maximum gate charge of 120nC, with no minimum specified. Therefore, switching speed cannot be controlled completely by the designer, and sufficient margin must be allowed for one device to carry more of the switching power than another. Favorably, the fastest switching device will carry more of the turn-on transient power dissipation, while the slowest one will carry more of the turn-off transient power dissipation.

#### 3.1.6.5. Thermal Management of Paralleled Devices

Conduction losses naturally match quite well due to the favorable temperature coefficient, and can be made to match very closely with parametric screening and matching. Switching losses, however, will vary somewhat from one device to the next. The thermal management of an inverter design must allow for the added temperature rise of the hottest device. This variation in temperature rise will exist from the device junction to the heatsink, and must be allowed for in calculating the maximum operating junction temperature.

The use of a heatsink methodology which minimizes the junction-to-heatsink thermal impedance will control the thermal impact of the variation in paralleled devices. It is necessary for the thermal resistance of the heatsink to be sufficiently low that there is little temperature gradient within the heatsink, which is accomplished by choosing a heatsink with suitable thickness on the device mounting surface. The remaining thermal gradient of heatsink-to-ambient is not affected by device power sharing.

### 3.1.6.6. SOA of Paralleled Devices

Of great concern is the SOA of paralleled devices. It is not always possible to match the switching of paralleled devices without comprehensive matching of components, which is beyond the capability of many manufacturers. It has been shown that careful design and thermal management can mitigate the thermal effects due to variations in these components. The SOA of each device must be observed, also.

The safest way to ensure that the SOA is not violated is to consider the total switched current and peak switching voltage, and to choose devices which have an SOA which includes that condition. In this case the devices are operated in parallel to reduce the total dissipation in each device, and thus reduce the typical operating junction temperature of each device, in order to achieve the desired MTTF. SOA failures are eliminated by ensuring that even in the worst-case scenario where an entire transient could be imposed on one of the devices, it would not exceed the device SOA.

### 3.1.7. Magnetics Core Losses

Magnetic devices called inductors are utilized in an inverter to convert the transient switching nature of the semiconductor power switching devices into a continuous 60Hz sine wave. These inductors are often very large and heavy, and contribute greatly to the weight and power losses of an inverter. The inverter manufacturer is therefore compelled to take steps in the design of an inverter to minimize the size of the inductors.

After passing the output current through the inductor, the resulting sine wave will still have an imposed component, called ripple, at the switching frequency of the power devices. In order to avoid the very large size of inductor that would be required to reduce this ripple to the necessary level, a second inductor is generally utilized to reduce this ripple, creating a 2-stage filter. The total weight and dissipation of these two inductors is much less than that which would be required for acceptable operation with a single inductor. A higher switching frequency of the inverter also has the available benefit of allowing the use of smaller inductors, however, steps must be taken to avoid excessive dissipation at higher frequencies.

Inductors dissipate power from losses in the wire and in the core. Of primary concern when attempting to reduce the size of an inverter by increasing the operating frequency is that the core losses of magnetic materials escalate rapidly with increased operating frequency. Specialized materials are available to operate at higher frequencies. These materials come at a much higher dollar cost than standard materials. Fortunately, the higher cost of these materials is

offset somewhat by the fact that the cores required for higher frequency operation are smaller.

### **3.1.8. Transformer Saturation**

An inverter connected to the utility line will drive AC power into the line. This line power is supplied through a series of step-up and step-down transformers in the utility supply. These transformers can pass only the AC power. If the inverter has a DC element in its output, this DC element will travel only as far as the secondary winding of the nearest transformer. In this transformer, this DC element will contribute to the dissipation in the secondary winding of the transformer, and also to the core excitation in that transformer. The power due to this DC element is negligible, as it is seldom more than a few percent of the delivered AC output current.

Core saturation of the utility transformer has become an issue of concern lately. It is a fact that DC current in a transformer secondary will shift the excitation of the core and cause the peak flux density to increase somewhat. The concern is that this shift could cause a non-linear excitation of the power transformer resulting in power line distortion and, in the worst case, cause a utility fuse to open.

Sensing and measurement of high DC current is usually achieved with the use of Hall effect devices. These devices boast the high voltage isolation of a transformer while achieving the capability to sense direct current. Magnetic devices such as these are subject to residual magnetic effects, which limit their offset accuracy. Closed-loop op-amp circuitry may be employed to correct the non-linearity of these devices for high currents; however, the low-level DC accuracy may still be limited to about 1% of the full scale capability of the device.

DC offset does not affect the reliability or operation of the inverter. Rather, the concern is for the capability of the utility transformer to withstand this condition. To reduce DC offset below 1% without increased dissipation, more sophisticated control mechanisms may be feasible, which can detect and correct for the DC offset of the sensing device.

### **3.1.9. Fans**

Natural convection cooling requires a large amount of surface area. Often the most efficient finned heatsink cannot effectively cool the semiconductor devices in an inverter without adding considerable volume and weight to the unit.

Fans are used in conjunction with finned heatsinks to create forced air convection cooling which achieves highly efficient cooling in a space volume

commensurate with the size of the inverter. In addition, the cooling efficiency of forced air can reduce the heatsink temperature to temperatures not achievable with natural convection, and the lower temperatures correspond to reduced failure rates of components within the inverter.

The reliability of fans is best quantified in a different manner than that of electronic components. Reliability, within the reasonable life expectation, is a measure of the occurrence of random failures. Many electronic components have virtually no mechanism of failure except such random events for a very long service time. They are therefore often characterized by mean-time-between-failures, the accumulated service for the population between successive failures of two members.

Mechanical systems do not have constant rates of random failures in the same manner as electronic components. Random failures, if they exist, are so uncommon as to be indistinguishable among characteristic wear-out failures. Wear-outs are also broadly distributed over time, but follow a pattern of increasing frequency with age. For rotating equipment of many types, including fans, the bearing system controls average life expectancy. Usually, its life characteristic is represented as a Weibull function, where the fraction of a population failing in elapsed time,  $t$ , is:

$$F = 1 - e^{-(t / \alpha)^\beta}$$

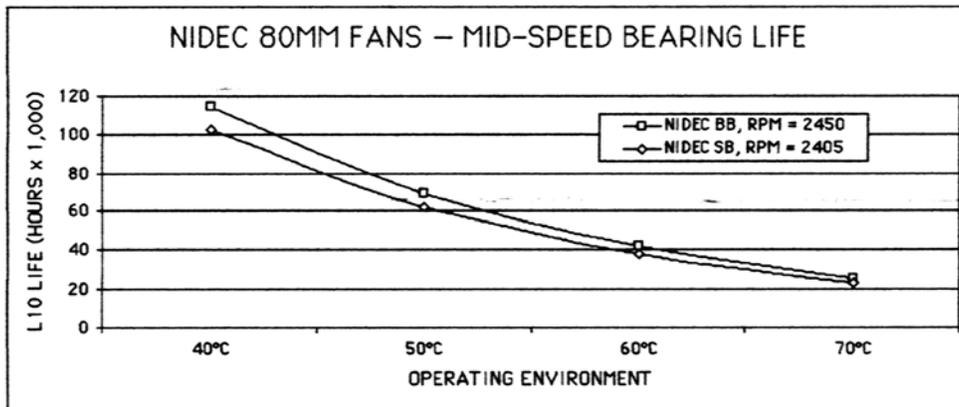
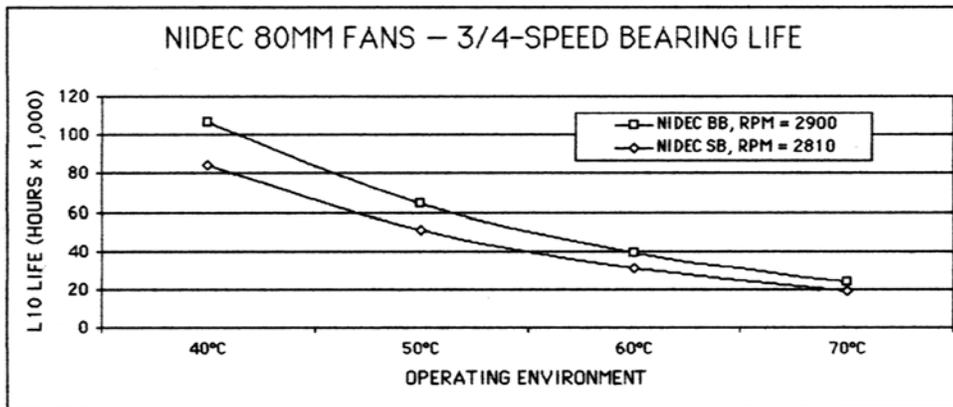
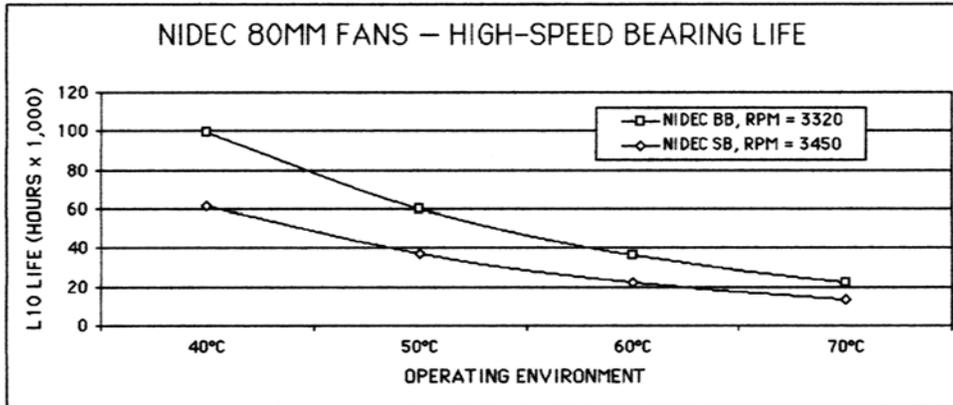
where alpha and beta are constants for each product and set of operating conditions.

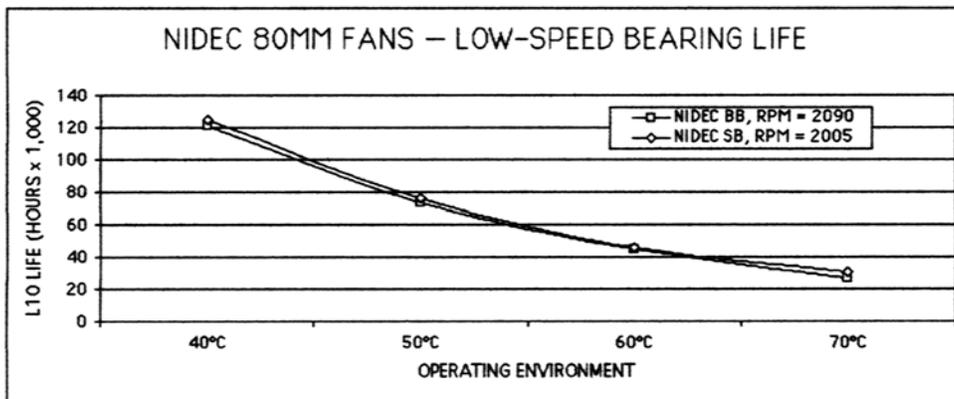
Because fan failures are primarily end-of-life failures, the fan failure rate may be considered separately from the MTTF due to semiconductor failures. Commonly, fan life is identified as a value for L10, the time at which 10 percent of the fans have failed. The use of a fan under conditions which yield an L10 parameter of 10 years will result in 1 out of every 10 units failing within the first ten years of operation. An overall MTTF for a manufacturing lot of inverters is therefore achievable with a fan L10 value of 10 years.

For the purpose of this discussion, a simplistic approximation will be used. The fan will be assumed to operate for an average period of 12 hours every day. The L10 fan life must therefore be:

$$L10 = 12 * 365 * 10 = 43,800 \text{ hours.}$$

Following are examples of reliability graphs from a fan manufacturer:





These graphs show that the desired L10 reliability of 43,800 hours can be accomplished with low-speed fans of ball bearing or sleeve bearing construction at operating temperatures of up to 60 Deg. C., or with high-speed fans of ball-bearing construction at temperatures up to 55 Deg. C.

### 3.1.10. Filters

Air particulate filters may be utilized to protect the heat sink, fan, and internal components of the inverter from detrimental effects of airborne dirt, dust, insects and the like. Unfortunately, as filters accumulate airborne material they load up and begin to restrict airflow. Some increase in temperature rise is inevitable as the airflow is restricted. The design must contain sufficient cooling capacity margin to allow for adequate cooling during this restricted airflow condition. Additionally, maintenance procedures must be developed to clean the filters before the airflow is restricted to the point that the heat sink temperature exceeds the design goal

A coarse filter may be utilized to catch only insects and large dust. This filter will not require as much maintenance as a fine filter, however if used with a large airflow, it will allow fine dust to accumulate within the inverter. Additional protection may be required, such as conformal coating of circuit boards.

Maintenance may be reduced, along with the probability of the inverter experiencing an over-temperature condition due to clogged filters, by separating the internal air from the heat sink air. In this manner, the heat sink may be subjected to a large volume of airflow that will require little or no filtering. The electronics inside the inverter may be vented for natural convection only, or by a low airflow fan, with a screen to prevent invasion by insects. If a filter is used also, the low airflow will extend the maintenance period of this filter.

### 3.1.11. Electrolytic Capacitors

Almost all inverters utilize electrolytic capacitors. Their ability to quickly store and discharge large amounts of electrical energy in a small space is unequalled by any other type of component. For single phase inverters, these are a necessity to allow the PV array to continuously deliver energy into the inverter while the output energy is in the form of a sine wave.

Electrolytic capacitors, like fans, have a limited lifetime. The manufacturers of these components have performed extensive life testing and have data available as a function of the operating parameters of each component. Following are the results of a reliability analysis of a CDE brand capacitor rated at 470  $\mu$ F and 450 VDC:

CDE Thermal Applet for Snapmount Capacitors, Rev. 09-15-00

#### INPUTS:

Type: 381L  
Size (D×L): 35×50  
Rated DC Voltage: 450  
Capacitance ( $\mu$ F): 470  
ESR (milliohms at 25 °C, 120 Hz): 112.8  
Applied DC Voltage: 420  
RMS Ripple (A) 1: 8  
Frequency (Hz) 1: 15000  
RMS Ripple (A) 2:  
Frequency (Hz) 2:  
Air Speed (lfm, still air =50): 50  
Air Temperature (°C): 50

#### OUTPUTS:

Part Number: 381LX471M450A052  
Calculated ESR at Frequency 1: 32.7 milliohms at core temperature  
Calculated ESR at Frequency 2: milliohms at core temperature  
Dissipated Power (W): 2.09  
Core-to-Case Thermal Resistance (°C/W): 2.6  
Case-to-Ambient Thermal Resistance (°C/W): 7.3  
Initial Core Temperature (°C): 76  
Average Core Temperature over Life (°C): 81  
Expected Life (Hrs): 46200

#### INPUTS:

Type: 381L  
Size (D×L): 35×50  
Rated DC Voltage: 450  
Capacitance ( $\mu$ F): 470  
ESR (milliohms at 25 °C, 120 Hz): 112.8  
Applied DC Voltage: 360  
RMS Ripple (A) 1: 8

Frequency (Hz) 1: 15000  
RMS Ripple (A) 2:  
Frequency (Hz) 2:  
Air Speed (lfm, still air =50): 50  
Air Temperature (°C): 50

OUTPUTS:

Part Number: 381LX471M450A052  
Calculated ESR at Frequency 1: 32.7 milliohms at core temperature  
Calculated ESR at Frequency 2: milliohms at core temperature  
Dissipated Power (W): 2.09  
Core-to-Case Thermal Resistance (°C/W): 2.6  
Case-to-Ambient Thermal Resistance (°C/W): 7.3  
Initial Core Temperature (°C): 76  
Average Core Temperature over Life (°C): 81  
Expected Life (Hrs): 62900

INPUTS:

Type: 381L  
Size (D×L): 35×50  
Rated DC Voltage: 450  
Capacitance (µF): 470  
ESR (milliohms at 25 °C, 120 Hz): 112.8  
Applied DC Voltage: 420  
RMS Ripple (A) 1: 8  
Frequency (Hz) 1: 15000  
RMS Ripple (A) 2:  
Frequency (Hz) 2:  
Air Speed (lfm, still air =50): 50  
Air Temperature (°C): 40

OUTPUTS:

Part Number: 381LX471M450A052  
Calculated ESR at Frequency 1: 35.0 milliohms at core temperature  
Calculated ESR at Frequency 2: milliohms at core temperature  
Dissipated Power (W): 2.24  
Core-to-Case Thermal Resistance (°C/W): 2.6  
Case-to-Ambient Thermal Resistance (°C/W): 7.3  
Initial Core Temperature (°C): 67  
Average Core Temperature over Life (°C): 73  
Expected Life (Hrs): 79400

INPUTS:

Type: 381L  
Size (D×L): 35×50  
Rated DC Voltage: 450  
Capacitance (µF): 470  
ESR (milliohms at 25 °C, 120 Hz): 112.8  
Applied DC Voltage: 375  
RMS Ripple (A) 1: 8  
Frequency (Hz) 1: 15000  
RMS Ripple (A) 2:  
Frequency (Hz) 2:

Air Speed (lfm, still air =50): 50  
 Air Temperature (°C): 40  
 OUTPUTS:  
 Part Number: 381LX471M450A052  
 Calculated ESR at Frequency 1: 35.0 milliohms at core temperature  
 Calculated ESR at Frequency 2: milliohms at core temperature  
 Dissipated Power (W): 2.24  
 Core-to-Case Thermal Resistance (°C/W): 2.6  
 Case-to-Ambient Thermal Resistance (°C/W): 7.3  
 Initial Core Temperature (°C): 67  
 Average Core Temperature over Life (°C): 73  
 Expected Life (Hrs): 100900

To summarize the results:

TEMPERATURE DEGREES C.	VOLTAGE VDC	LIFE HOURS
50	420	46,200
50	360	62,900
40	420	79,400
40	375	100,900

For the purpose of this discussion, a simplistic approximation will be used. The capacitors will be assumed to operate for an average period of 12 hours every day. The lifetime-required lifetime of the capacitors is:

$$12 * 365 * 10 = 43,800 \text{ hours.}$$

End-of-life for electrolytic capacitors is typically a parametric failure of reduced capacitance and increased ESR. The inverter design must be such that it will operate in a satisfactory manner upon this reduction of performance of the capacitors. In our example, any of the above applications will yield the desired reliability.

It is also apparent that the electrolytic capacitors must be located within the inverter such that their surrounding temperature is close to the ambient temperature, and that the applied voltage must be considered, to achieve acceptable failure rates of these components. The lifetime of electrolytic capacitors can be extended to 20 years with careful application.

### 3.1.12. Electromechanical Components

Contactors, relays and switches may utilize various materials depending on the voltage and current levels that they are to act upon. Following is a summary of relay and switch materials:

	Material	Characteristics
Contact material	Ag (silver)	Electrical and thermal conductivity are the highest of all metals, exhibits low contact resistance, is inexpensive and widely used. One disadvantage is that it easily develops a sulfide film in a sulfide atmosphere. Care is required at low voltage and current levels.
	AgCd (silver cadmium)	Exhibits the conductivity and low contact resistance of silver as well as excellent resistance to welding. Like silver, it easily develops a sulfide film in a sulfide atmosphere.
	AgW (silver tungsten)	Hardness and melting point are high, arc resistance is excellent, and it is highly resistant to material transfer. High contact pressure is required. Contact resistance is relatively high, and resistance to corrosion is poor. Also, there are constraints on processing and mounting to contact springs.
	AgNi (silver nickel)	Equals the electrical conductivity of silver, excellent arc resistance.
	AgPd (silver palladium)	At standard temperature, good corrosion resistance and sulfidation resistance. However, in dry circuits, organic gases adhere, and it easily develops a polymer. Gold clad is used to prevent polymer buildup; expensive.
	PGS alloy (platinum, gold, silver)	Excellent corrosion resistance, used mainly for low-current circuits. (Au:Ag:Pt=69:25:6.)
Surface finish	Rh plating (rhodium)	Combines perfect corrosion resistance and hardness. As plated contacts, used for relatively light loads. In an organic-gas atmosphere, care is required as polymers may develop. Therefore, it is used in hermetically sealed relays, such as reed relays; expensive.
	Au clad (gold clad)	With its excellent corrosion resistance, Au is pressure welded onto a base metal. Special characteristics are uniform thickness and the nonexistence of pinholes; especially effective for low-level loads under relatively adverse atmospheres; often difficult to implement clad contacts in existing relays.
	Au plating (gold plating)	Similar effect to Au cladding; depending on the plating process used, supervision is important because of the possibility of pinholes and cracks. Relatively easy to implement gold plating in existing relays.
	Au flash plating (gold thin-film plating)	Purpose is to protect the contact base metal during storage of the switch or device with built-in switch. However, a certain degree of contact stability can be obtained even when switching loads.

According to the Siemens Electromechanical Components division, the electrical life expectancy of general purpose and power relays and switches is generally rated at 100,000 operations minimum, while the mechanical life expectancy is one million operation or more. For a device that operates twice per day for 10 years, only 7,300 operations are required. Clearly, the key to reliable operation of relays and switches is in selecting the proper contact type for the application.

### 3.1.13. Environmental

Environmental intrusion upon the components within an inverter can have detrimental effects on the inverter operation. Primarily, these effects are due to either over-heating or short-circuits.

Inverters use finned heat sinks to cool the electronic power devices. Natural or forced air convection is used to cool the heat sinks, the magnetic components, and the electronic circuitry within the inverter. If the cooling air is filtered, there is the possibility of restricted airflow as the filters load, causing an over-temperature condition. Scheduled maintenance is needed to maintain clean filters. Unfiltered air may be used to cool a heat sink and large magnetic devices, however it is not suitable for cooling electronic devices because the dust and insects may become conductive and result in an unwanted conduction path, which could cause a malfunction or arc within the inverter.

The electronic components within the inverter may be kept in a separate compartment that is either filtered or sealed. If sealed, the electronics are well protected from insects and other vermin but become susceptible to the condensation of moisture. If filtered due to the need for cooling, a minimum of airflow must be maintained and they are susceptible to overheating as the filters load.

## 3.2. Present Manufacturing Barriers to a 10 Year MTTF

During the design phase of an inverter, calculations and tests are performed to achieve a theoretical MTTF goal. This effort will be thwarted unless the manufacturing process is carefully and continually monitored and optimized.

In addition to the failures that may be anticipated during the life-time of each inverter due to the inevitable component failures which have been identified by the MTTF calculations, variations in materials and workmanship along with unexpected combinations of operating conditions will **induce failures. Without efficient manufacturing techniques and active quality control measures**, these failures will ruin the reliability record of an otherwise excellent inverter.

### **3.2.1. Quantity**

The volume of inverters to be manufactured affects the cost of purchased components and the efficiency and accuracy of the production process.

#### **3.2.1.1. Purchasing**

For small lot manufacturing, components are also purchased in small quantities, often less than 100 pieces at a time. In order to keep costs down, it becomes necessary to competitively search for the best buy on these components. The result is that inverters will be built next month with components from different manufacturers and lot codes than those now being installed. While the design of an inverter is intended to accept the variations anticipated from one part to the next, the wider the variation of purchased components, the more frequently a new problem will surface, requiring action to maintain the required performance and reliability.

#### **3.2.1.2. Assembly**

As discussed in the section on resource limitation, fully trained assemblers are one key to maintaining integrity and reliability in the manufacture of inverters that have been carefully designed and documented. The highest possible reliability depends on consistent manufacturing. No test program or quality control program can completely weed out 100% of the defects created while manufacturing the inverters.

Even with thorough training, repetition will help to achieve consistent results. Each time a person prepares for a task that they haven't done for a while, they need to re-orient themselves to that task. This invites the opportunity for variations in the manufacturing process from one time to the next. It is only after the failures of units in test, burn-in, or end use due to unexpected variations that some of these details become apparent and may be documented, fully explained, and corrected. Of course, this documentation and corrective action may only be thoroughly achieved through a good quality control program.

Limited production runs also result in one workspace being utilized for a variety of tasks on a range of product. It becomes necessary to take down one setup to prepare for the next task, introducing another chance for unexpected variations.

### **3.2.2. Quality Control**

A thorough quality control program involves in-process inspection and documentation of failures. The result of a good quality control program, if not to totally eliminate all failures, is to advance the detection of problems from end-use

failures to detection at the factory, and to advance the detection of these factory failures from the latter stages of production, such as burn-in, to progressively earlier stages – final test, sub-assembly test, and inspection. The earlier these are detected, the lower the probability of inverter failure during end-use.

A common pitfall is that the success of inspection makes it appear as though inspection is unnecessary. When resources are limited and product quality is very good, inspection may be de-emphasized, only to regain attention when failures have escalated.

#### 3.2.2.1. Inspection

Some elements of manufacturing may cause failures during test or burn-in, or even worse, cause latent deficiencies in an inverter which may not surface during test and burn-in, only to result in failures after installation. When assemblies are inspected prior to testing, common errors can be identified, corrected, and avoided in the future, and the MTTF of the final product will be enhanced. Also, the root cause of potential failures can be determined and eliminated, for failures that might otherwise appear to be due only to random component failures.

#### 3.2.2.2. Failure Reporting

The documentation of all failures during test and field operation of the inverters is used to identify trends and to record corrective actions taken. No matter how comprehensive the design, documentation, and training program, there will be details, perhaps critical nuances of component requirements and the assembly process, which no one realized or thought to explain until these failures occur.

Frequently, when resources are limited, the first thing to be compromised is this documentation process. The question implied will be, “Our product is working fine. Why should we spend our time writing down what we did wrong?”

There are good reasons to maintain accurate and comprehensive failure documentation:

#### 3.2.2.3. Trend Identification

Identification of failure trends is a very useful tool for achieving the highest possible reliability. When failure reports are taken diligently, the data may be used to improve assembly and sub-assembly accuracy and quality, which will be seen in improved inspection and test results and reduced rework and burn-in failures. When a particular failure is noticed to occur repeatedly, Quality Control, Production and Engineering can work together to determine the root cause of the failures and take corrective action to prevent these failures from recurring.

#### 3.2.2.4. Field Returns

When field returns do occur, the records may be reviewed to determine what rework and failures have occurred previously on that same unit. In this manner, process errors and failures which are determined to increase the likelihood of future failures may be identified and eliminated.

#### 3.2.2.5. Cost of Quality

Limiting the scope of an inverter manufacturer's quality control program may appear to be a cost cutting measure. This is an illusion to be avoided. Inspection and failure reporting will provide a cost benefit:

- Reduce manufacturing rework
- Increase test throughput
- Improve inverter MTTF
- Reduce customer support time due to failures

### **3.2.3. Resource Limitation**

Excellent design, documentation, and production fixtures are imperative for the consistent manufacture of reliable inverters. But let us not forget another very important element – the people who build them. Emphasis must be placed on comprehensive training, and time and tools must be provided for each person to do his or her best while building and testing the inverters.

#### 3.2.3.1. Training

When a new product is ready for production and the sales force has customers waiting, there is great pressure to start shipping ASAP. All too often, the production process begins before the beta testing requirements are satisfied, and inverters are shipped before everyone has received adequate training. As the watchful eye of supervisors and engineers shifts to new programs, the assemblers and technicians, who have not been trained to identify some critical details of their jobs, begin to unknowingly deviate from the process which was intended.

#### 3.2.3.2. Personnel Rotation

Limited resources often lead to the rotation of personal from one task to another. This can result in the assignment of an assembler or technician to a task for which he or she has not been fully trained, or for which they have not had the experience to complete accurately without greater supervision. Quality is

compromised when less experienced workers perform operations without additional training, supervision, and inspection.

To fully appreciate the impact of limited resources, one may consider the impact of manufacturing small quantities as discussed elsewhere in this section. When resources are limited and personnel are shifted away from one product and back again later, that has the same impact as building the inverter in even smaller production runs.

### **3.2.4. Production Testing**

The design goal of achieving an MTTF of 10 years addresses the random failures and end-of-life failures of components within the inverter. However, the manufacturing process of both the components within the inverter, and the inverter itself, will inevitably produce some units with latent faults that only manifest after operation of the inverter. No matter how high the design MTTF may be, the actual performance of the inverter in use will achieve this MTTF only if these latent failures are precipitated during a thorough testing of all product before it leaves the factory. Production testing may be categorized into 3 distinct groups. These are circuit level test, final assembly level test, and burn-in.

The development of thorough production testing begins during beta testing of the inverter. However, the test development program must continue for the duration of product manufacturing. Just as Design for Manufacturability requires the monitoring of engineering progress by production personnel, and feedback from Production to Engineering, similar benefits are enjoyed when engineering and quality control personnel monitor the results of production tests in order to maintain an effective production testing program.

It is by this monitoring and improving process that the effect of production test is extended beyond just fixing broken parts. Ultimately, through this process, the factory personnel continually act together to eliminate failures even at the production test level, and also to extend the scope of this testing as failures appear in field use.

#### **3.2.4.1. Circuit Level Test**

Each individual sub-assembly, such as a circuit board, wire harness, etc., has the potential to cause a failure of the inverter. By testing these sub-assemblies and performing repairs as needed prior to assembly into an inverter, potential failures during final assembly level test may be greatly reduced. This is very important because failures of the inverter, even while the unit is still at the factory, have the potential to over-stress other components within the inverter, setting the stage for additional latent failures that may occur in field use.

#### 3.2.4.2. Final Assembly Level Test

These tests are designed to activate all of the circuits and features of the inverter. The results are both functional verification and parametric verification. At the conclusion of this test, a data sheet should be complete, which indicates that all of the inverter functions are performing correctly, and that all of the operating parameters of the inverter have been measured, compared to the required performance specifications, and are acceptable.

The required performance specifications may be the same as the published performance specifications. In many cases, the factory test specifications may include limits that are more stringent than the published specifications, in order to ensure adequate inverter performance for years to come.

#### 3.2.4.3. Burn-In

No test program is complete without adequate burn-in. During burn-in the inverter is operated continuously for a period of time so that any premature failures due to workmanship or materials will occur prior to field use. In the case of a failure during burn-in, the unit is repaired, re-tested, and submitted to burn-in again. It is very important for Quality Assurance and Engineering to monitor these failures. Detailed gleaned from this data may be applied to upgrade the circuit level and final assembly level tests to weed out problems before they cause burn-in failures.

Burn-in should be designed to stress all of the electronic components in the inverter to their maximum normal operating temperature. Power electronic components should be stressed to their maximum normal operating voltages and currents. Burn-in may be performed at conditions beyond normal operating conditions such as input voltage or output current in order to accelerate possible failures due to faulty materials or workmanship. In addition, the burn-in may be performed with cooling fans retarded or disabled in order to achieve maximum desirable component temperatures.

One of the greatest stresses on power electronic devices occurs during the start-up and shut-down of the inverter. Although it is often stated that burn-in should be a continuous operation of the inverter, it is best to cycle the inverter on and off after the maximum desired temperature is reached. The shut-off of an inverter during burn-in may be initiated through its own protection circuitry such as overvoltage, overcurrent, and overtemperature. The required automatic re-start of the inverter after each fault detection will then also be verified.

### **3.2.5. Beta Testing**

Beta testing is performed on engineering prototype units. This testing program is a major part of the design phase. Unlike production testing, where the product performance is essentially compared to that of a known good unit, beta testing begins with a prototype that inevitably has a variety of defects and design flaws. The beta test program involves many cycles of test, modification, and re-test.

Ideally, the beta test program continues until Engineering, Production, Quality Assurance, and Management are all in agreement that the product performance is acceptable and reliable, and that the product is manufacturable at a cost that supports the market pressure.

#### **3.2.5.1. Conflicting Goals**

- During beta testing, the following expectations are present:
- Performance Requirements
- Reliability Goals
- Cost Goals
- Deadlines

Each of these goals exerts pressure on the designers to compromise the attainment of the other goals. Some degree of compromise is always required. An atmosphere of open and clear communication of these goals at the onset of the design program will establish the best environment for compromise of various issues that arise, without compromising the inverter reliability.

The importance of honest discussion of the status of beta testing, and of flexibility in program demands, cannot be overemphasized.

### **3.2.6. Design for Manufacturability**

The ultimate goal of engineering is always to support manufacturing. The engineering design must be communicated accurately to Production, Production must accurately communicate any difficulties and anomalies to Engineering, and the design changes that arise out of these needs must then be communicated back to Production. Communication between Engineering and Production has been discussed under the headings of Beta Testing and Production Testing. How does this communication take place? During Beta Testing, informal discussions and meeting are sufficient. For production to commence, a written means of communication from Engineering to Production, and vice versa, is needed.

Once the design process has resulted in a comprehensive set of design documentation, Production and Engineering work together to complete the tooling, fixtures, test procedures, and workplace setting to efficiently and accurately manufacture the inverter. How these tasks are divided up may vary according to the skills and experience of people in these departments. It is imperative that these systems be documented in writing, and that changes are reviewed by both Production and Engineering.

#### 3.2.6.1. Engineering Changes

When Production experiences a problem that cannot be remedied with by attention to production processes only, they must communicate this problem to Engineering. This communication is best to be done in writing. An Engineering Change Request (ECR) form may be used for this process. This form should include information regarding the nature and extent of the problem, when it began, and any proposed solution that may be apparent.

Changes to the design should not be incorporated into the inverter until Engineering has reviewed them for possible conflicting effects on other performance parameters and reliability. When approved by Engineering, design changes may be communicated to Production by the use of and Engineering Change Order (ECO). This type of document indicates that the inverter will now be built with the specified change from the previous documentation. The ECO should detail the change to the design, and specify when to implement the change.

#### 3.2.6.2. Work Instructions

Often, during beta besting and pilot production, Manufacturing will generate work instructions for use in training assemblers and technicians how to build and test the inverter. Sometimes production problems arise that do not require engineering change, but rather, the manufacturing process may be modified. It is desirable for Engineering to review these changes to check for unexpected negative effects on other aspects of the inverter.

### **3.3. Candidate Technologies**

#### **3.3.1. DSP**

##### 3.3.1.1. History

Complex hybrid inverters are available today. These units typically utilize several conversions, with separate microprocessors, sensors, signal conditioning

components, and drivers for each function. These units can shift DC levels, charge batteries, regulate sine wave outputs, control operational states based on programmed and measured parameters, and perform data collection. PC interfaces may be included in such machines. Manufacturers build these machines to order, and variations from the manufacturer's standard system accommodations may be ordered, requiring additional engineering and design time and costs.

The desire for a low-cost inverter has led to the popularity of single-application inverters. These units operate over an input voltage range scaled for a particular technology, and in applications that are either grid-tied or stand-alone.

#### 3.3.1.2. The DSP Controller Approach

A DSP controller is the combination of a high-speed mathematical DSP core and memory and a set of peripheral devices on a single chip device. The more appropriate the set of peripherals for the application, the closer it is possible to reach a true single chip solution with no external interface components. Today's DSP controllers created for complex motor speed and servo control are also ideally suited for renewable energy inverter applications.

The creation of a universal inverter may be facilitated by the use of a DSP because these controllers can perform all of these complex functions of a hybrid inverter simultaneously, from a single chip. A single set of sensors, along with the DSP on-board signal processing, greatly reduces the component requirements to perform multiple functions within the inverter. Thus, the DSP can be utilized to create an inverter product line that has the versatility of the large hybrid inverters, while boasting the simplicity, reliability, and low cost of a single-purpose inverter.

In order to maximize the cost effectiveness of this approach, the inverter will be designed with a set of hardware and software building blocks that perform groups of functions. Several versions of the inverter will be built, with different groupings of functions. For instance, an inverter for installations without batteries will not include the battery charging hardware; however, the hardware included in such a unit will be the same as that used within the one built with the battery charging capability.

#### 3.3.1.3. Candidate DSP Functions

The DSP controller integrates the full set of functions required to build a single chip inverter system, including a high-speed DSP core, peripherals and both random access and read only memory (ROM). Not only can any combination of hardware functions be controlled from a common control circuit, the DSP can actually program the same hardware to perform different functions for different applications. For instance, a power bridge assembly may be programmed to

operate as a three-phase bridge for industrial grid support applications, or as a split-phase bridge and a charge controller for residential or commercial power availability enhancement.

#### **3.3.1.3.1. Pulse Width Modulation (PWM) Generator**

The power converter of choice for low to medium power inverter applications is a single-phase or three-phase IGBT or MOSFET bridge. The power device switching signals are usually fixed frequency PWM timing signals with frequencies ranging from a few kHz to 20 or 30KHz. A center based PWM controller with waveform symmetry has many advantages in stability and performance. The PWM generator on the DSP controller provides center based, dead time adjusted, PWM signals synchronized to the DSP clock signal. The PWM hardware includes both waveform calculation and timing functions so that up to three pairs of waveforms can be produced based on three register updates per PWM cycle.

Thus, the DSP will accommodate either a three-phase grid-tied configuration or a split-phase bridge with battery charge control or input voltage boost. The PWM generator includes additional configuration options such as individual output enable selection, a polarity control pin, and a gate drive feature. This means that the six outputs can be directly connected to the gate drive amplifiers of the power bridge IGBTs or MOSFETs without any additional external switching logic or power fault detection and protection circuitry.

The functions that the PWM generator will perform will include:

Half Bridge

Full Bridge

Three-Phase Bridge

Power Factor Correction (PFC) AC to DC converter

DC to DC Boost Converter

#### **3.3.1.3.2. Remote Communication**

The DSP controller includes on-board CAN bus and RS232 ports. The CAN bus will be used for communication with a remote dedicated user interface, in applications where the inverter location is not readily accessible, and for communication between inverters, in larger installations where several inverters are utilized to achieve high power levels.

The RS232 port will enable the direct interface of the inverter with a windows based PC program for inverter control and monitoring.

### **3.3.1.3.3. Data Acquisition Systems (DAS)**

The performance of the DSP analog-to-digital (A to D) and mathematical functions is sufficiently accurate that no additional sensors and hardware will be needed to perform DAS functions. The PC interface will enable any PC to be able to access and log the real-time inverter power performance statistics that many users request.

### **3.3.1.3.4. Power Circuitry Protection**

The DSP can perform a Multiply-and-Accumulate (MAC) function in 1 clock cycle. This speed allows the DSP to measure and react to power circuit over-voltage and over-current conditions in only several microseconds. Thus, device protection for most stress conditions can be safely performed without the need for external redundant sensors and analog circuitry. For harsh environments, simple external comparators may be used to set absolute maximum parameters for the device safe-operating-area (SOA) constraints of the power circuits. These comparators will connect to the DSP output enable pins to bypass the A to D and MAC functions of the DSP for absolutely fail-safe fault protection.

### **3.3.1.3.5. Maximum Power Tracking (MPT)**

For operation with photovoltaic (PV) power sources, an inverter must perform a continual search to maintain operation at the maximum power point of the PV circuit. The computing power of the DSP allows it to perform this as a background operation while performing the real-time power conversion operations.

### **3.3.1.3.6. Operation State Control**

An inverter utilized for renewable energy generation must respond to the power availability of the energy source, the demand of the load, and to user-programmed routines. These operations can easily be performed by the DSP, as background operations, with no additional sensors or circuitry.

## **Additional Advantages**

### **3.3.1.4.1. Lower Distortion**

In conventional inverters, including those with microprocessor control, the sine wave reference for the AC output may be digitally synthesized. However, this reference must be converted to a voltage signal which is then applied to the input of an operational amplifier (op-amp) with analog feedback, to control the output current of voltage waveform. Through the use of the DSP, the digital reference is

compared digitally to the output voltage or current data registers of the on-board A to D, resulting in lower total harmonic distortion.

#### **3.3.1.4.2. Adaptive Performance**

Inverters are designed to operate over a wide range of operating and environmental conditions. Switching frequency, cross-over times, control loop stability compensation, current limit points, and other parameters are set to compromise for performance over the full range of conditions. With DSP control, these parameters will be variable, and the DSP will perform real-time adjustments to adapt the inverter performance to external conditions such as power level, ambient temperature, input voltage, and others.

#### **3.3.1.4.3. Reduced Electromagnetic Interference (EMI)**

While PWM operation produces line frequency sine wave output power with exceptionally low harmonic distortion, the high speed switching of the power MOSFETs or IGBTs creates radio frequency (RF) interference, due to the harmonics of the power device switching. Filtering must be added to the inverter to maintain these signals below the limits of FCC Part 15. The DSP can be programmed to vary, or dither, the operational frequency of the PWM, which will reduce the generation of radio frequency harmonics, and reduce the need for additional hardware RF filter components.

### **3.3.2. Made-to-Order Power Electronics**

The concept of made-to-order power electronics is to involve the suppliers of the semiconductor power switches in the design of the power electronic system. Standard practice has been for the power electronic product designer to design with discrete power switching devices, in standard packages, chosen from a supplier's standard offerings. In the made-to-order model, the semiconductor power switches and their packaging are designed by the switch manufacturer to meet the needs of a specific application with the goals of:

- improving silicon utilization (lower cost)
- designing thermal interfaces for the expected thermal cycle life (reliability and cost improvement)
- increasing integration and reducing the number of components, interconnections, and thermal interfaces (size reduction, cost reduction, reliability improvement)
- including only the functionality required for the specific application (cost reduction).

The end result of this design process is usually an application specific power module that is manufactured by a semiconductor switch manufacturer, or by a

specialist module manufacturer. The module is sold to the power electronic product manufacturer who integrates it into the end product. The module typically contains more than one power switch and has separate, defined and characterized, interfaces for cooling, power, and control.

### 3.3.2.1. The Case for Development of a Made-to-Order Power Module

The typical manufacturing technology for a power module consists of an electrically insulating but thermally conductive substrate, such as a metallized ceramic, that attaches to a heat sink. The power semiconductor chips are mounted directly to the metallization of the ceramic on the opposite side from the heat sink. The metallization is etched to provide interconnection conductors among the chips. Topside connections to the chips are made with aluminum bonding wires. A molded plastic package encloses the chips and supports the external electrical interconnections, which may be solder pins, plugs, or screw terminals. [1,2]

Development of an entirely new module using this manufacturing technology can be expensive. Estimates from suppliers are on the order of \$500,000 for engineering and \$500,000 for tooling. In addition, the production equipment to manufacture these modules is very expensive and must be amortized over a large production volume. Development costs are much lower if a module package that is already in production is employed, and changes are restricted to changing the semiconductor chips used and the internal interconnections.

Lower volume applications use alternative fabrication techniques that require lower up-front costs and lower investment in manufacturing equipment. For example, semiconductor switches mounted in a standard surface mount package can be soldered to a metallized ceramic substrate, or an insulated metal substrate, using conventional surface mount or hybrid circuit techniques. The substrate is then mounted to a heat sink. Edge connections on the substrate, similar to those used for hybrid electronic circuits, are used to make electrical connections to a conventional printed circuit board that contains auxiliary circuits and the electrical interconnects for power and control.

Development of a module may be initiated by a product manufacturer seeking a competitive advantage or a solution to meet a particular cost or technical challenge. In this case the module usually remains a proprietary product, although the product manufacturer may grant permission to sell the module to other customers in order to reduce development and piece part costs. Alternatively, the semiconductor manufacturer may initiate development of a module that has potential for sale to a large customer base.

The technology trend is to add increased functional integration and intelligence to power modules. The hierarchy of increased integration and intelligence is:

- Single semiconductor switches in standard packages (e.g. TO220)
- Multiple semiconductor switches in a module package
- Modules incorporate the required semiconductor switch chips plus temperature and current sense devices.
- Switch gate drive circuits and switch protection circuits are added.
- Gate drive power supplies, control signal isolation and conditioning are added.
- Snubber circuits, power distribution bus structures, and bulk energy storage (capacitance) are added.
- Cooling system (heat sink) is added.
- Control electronics including the DSP and associated memory and signal conditioning electronics are added.
- Complete system is integrated into a module.

The level of integration and intelligence suitable for a particular application depends on a number of economic and technical factors and there is no straightforward metric to be applied to making the decision. Key factors to be considered include:

- A high level of integration narrows the customer base and increases the module supplier's costs for design, production, testing, and quality and reliability assurance. Therefore the value added for a highly integrated and intelligent module has to be high and the customer must be able to use a substantial quantity to justify the investment by the supplier.
- A highly application-specific design also narrows the customer base, so the application must have significant volume potential. In addition, for a highly application-specific design to have advantages over a general purpose design, the application must be well characterized and have aspects that can be exploited to achieve lower cost and improved performance.
- Up front design and tooling costs are typically higher for a highly integrated module, and component cost may appear to be the same or higher for an equivalent product designed using discrete components. The advantages of an integrated module are often in decreased labor input, decreased component count, improved reliability, smaller size, or increased ruggedness. There are also substantial advantages in reduced design cost and time to market if the module can be applied to other products.
- Design and tooling costs for integrated modules are high and design changes are expensive. The product application must be well defined and have sufficient stability to ensure that only one design cycle is required over the expected life of the module design. Also, the design teams involved must have the engineering processes, skills and discipline to ensure that the design is done right the first time.

The product manufacturer usually purchases highly integrated or application specific modules from a single source since the cost to set up multiple sources is usually prohibitive. This creates a number of issues with regard to security of supply and competitive pricing that must be overcome.

Modules are not easily repaired. The typical service procedure for a failed module is to discard it and replace it with a new module. Product service plans and budgets must take this into account.

From a technical perspective, applications that use multiple semiconductor switches that can be interconnected in a simple fashion within the module are preferable. Therefore, topologies with multiple parallel devices, bridge configurations, common power distribution buses, and no isolation barriers are preferred.

Examples of applications where integrated power modules have high usage include automotive power converters (actuator drivers, integrated starter/alternator controllers, HID lamp drivers, etc.), motor drives and actuator controls in white goods such as washing machines and air conditioners, low-power packaged variable frequency motor drives for factory automation applications, and dc-dc converters used in telecommunications systems.

These applications have the requisite high production volumes and well defined product requirements. Less highly integrated power modules are applied in medium-power variable frequency motor drives and medium and high power uninterruptible power supplies.

Renewable energy inverters for higher power applications (three phase output, >10kW) already employ power modules. Typically, modules at the 2<sup>nd</sup> through 5<sup>th</sup> level of integration are purchased as standard components from module manufacturers such as Semikron, Eupec, or Powerex. These modules, which contain IGBT or diode bridge assemblies, are also employed in variable frequency motor drives, industrial power conversion equipment, and higher power UPS.

Strictly speaking, these modules are not made to order, since the semiconductor chips and internal topologies within the modules are not customized for the renewable energy applications. However, the circuit topologies and operating voltages of renewable energy inverters are sufficiently similar to those of variable frequency motor drives and large UPS to allow the use of standard modules without a significant penalty in performance or cost.

A more “made to order” approach is used in the next level of integration, which is usually performed by the inverter manufacturer. In this level, the purchased power modules are combined with laminated power distribution buses, snubber components, bulk energy storage components, and heat sinks to create

assemblies at the 6<sup>th</sup> or 7<sup>th</sup> level of integration. These assemblies are “made to order” for the needs of renewable energy applications and are used as standard system elements when designing new power converters.

Given that production volumes of any single family of renewable energy inverters at power levels above 10 kW are unlikely to exceed 10,000 units per year in the next five years, the opportunities for a made-to-order approach at the semiconductor switch level are probably limited, particularly since standard components also used for motor drive and UPS applications are a reasonable fit. However there are substantial opportunities to use the made-to-order approach to improve current power electronic assemblies based on standard modules and to create highly optimized intelligent assemblies at the 8<sup>th</sup> and 9<sup>th</sup> levels of integration.

Currently, renewable energy inverters for lower power applications (single phase, < 10 kW) appear to be designed at the lowest level of integration. There are a number of reasons for this situation. Key to this is that there are a number of competing product architectures and circuit topologies in the market and overall production volumes are still relatively low – typically less than 10,000 units per year for any single product platform. Therefore it is difficult to identify a made-to-order module opportunity with sufficient volume to justify the development cost and capital equipment required.

#### 3.3.2.2. Opportunities to Increase Made-to-Order Modules

Current product architectures often have technical requirements that are difficult to meet at reasonable cost with available module technology. Examples include

- High current (100’s of amperes) low voltage MOSFET H-bridge circuits.
- Mixed technology circuits employing high current low voltage MOSFETs and high voltage lower current IGBTs.

Modules at these power levels developed for other markets, such as automotive, white goods, and low power packaged drives are very application specific. Many are not made available for sale to other customers and those that are sold as catalog products are not necessarily a good fit to the needs of the present generation of renewable energy inverters.

Manufacturers of renewable energy inverters have been small companies with limited technical and capital resources and they have been faced with a risky infant market for their products. The contrast between their situation and that of industries that have made successful use of made-to-order modules, such as the automotive industry and the white goods (household appliance) industry, is marked, and results in different conclusions about the risks and rewards of investing in a made-to-order module.

Looking ahead, there are opportunities to increase the use of the made-to-order approach in low power renewable energy systems. The renewable energy market is growing and it is possible to identify some specific product opportunities with high volume potential. For example, the world market for grid-tie residential PV systems is growing rapidly and presents an opportunity for an optimized high volume product. Other distributed energy applications and power quality applications can further expand the volume potential.

Newer technology, and a different view of product architecture, provides the opportunity to consolidate product platforms and circuit topologies, again resulting in higher volume potential. Finally, some of the technical barriers are also disappearing. For example, the need for high current, low voltage starter/alternator controllers in automotive applications is driving made-to-order module technology that will result in lower cost high current MOSFET modules suitable for renewable energy applications.

There are several paths to investigate and pursue to implement made-to-order concepts and higher levels of integration in the next generation of low power renewable energy inverters.

Develop inverter circuit topologies that are more closely aligned with available highly integrated modules developed for other markets. As an example, power modules developed for motor drives in washing machines and air conditioners [3,4] have a high level of integration and are designed for low cost. They could be very suitable for grid-tie inverters in the 0.5 kW to 3 kW range, particularly if a non-isolated, high voltage PV array topology was selected.

Employ module fabrication techniques that require investments in development and manufacturing equipment that fits the volume forecasts and risk profile of the renewable distributed energy industry. For example, pursue techniques that combine standard surface mount power devices with high performance thermal substrates, integrated heat sinks, and conventional printed circuit board technology for control and interface circuits. This approach could deliver many of the reliability, integration, and component count reduction advances sought, without the high investment and high volumes required for semiconductor chip based modules.

Investigate a semi-custom approach using a standard module assembly already in volume production for another application. Changes could be made to the semiconductors used, and interconnections made, inside the module without incurring the high costs of a fully custom module. For example, the low cost modules used for appliance and industrial motor drive applications are configured as six switch bridge circuits designed to drive three phase electrical machines. Residential renewable energy inverters are designed for single phase, or split phase (120V/240V), applications. Reconfiguration of the six switches in these modules to meet the needs of a single-phase application should be possible without too much difficulty.

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[4] "Application Note 9018 - Smart Power Module User's Guide," Fairchild Semiconductor, 2001.

### 3.3.3. Soft Switching

The action of the power switching semiconductor devices may be characterized as *Hard Switching* or *Soft Switching*. With hard switching, the switching devices are turned on and off abruptly, forcing the semiconductor to switch the full output current with the bus voltage present on the device.

Resonant circuits may be divided into two categories: zero-voltage switching and zero-current switching. The zero-voltage method is used to a considerable degree in motor control applications, and this paper will address the applicability of this kind of soft switching to the new inverter for renewable energy. To achieve zero-voltage soft switching, a set of resonant L-C components is added to the circuit. The resonant behavior of this circuit causes the voltage on the semiconductor switch be reduced to zero prior to turning it on.

#### 3.3.3.1. Zero-Voltage Resonant Switching

There have been many variations of the resonant switching inverter proposed to date. Two of the more common methods are described below.

One of the earliest soft switching topologies proposed for dc-to-ac inverters is the resonant pole inverter. A single-phase leg of a resonant pole inverter is shown below.

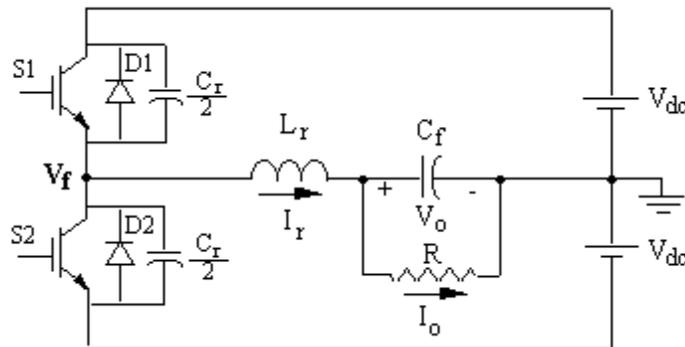


Figure 3.1. Simplified Resonant Pole Inverter Circuit

In the resonant pole inverter, an inverter pole consisting of switches S1 and S2 is configured. In order to achieve zero voltage switching, a resonant inductor is placed in series with a capacitor, across which the load is placed. The inverter phase voltage, V<sub>f</sub>, can be modulated to generate the desired low frequency voltage waveform. The resulting switching waveforms are shown in Figure 3.2.

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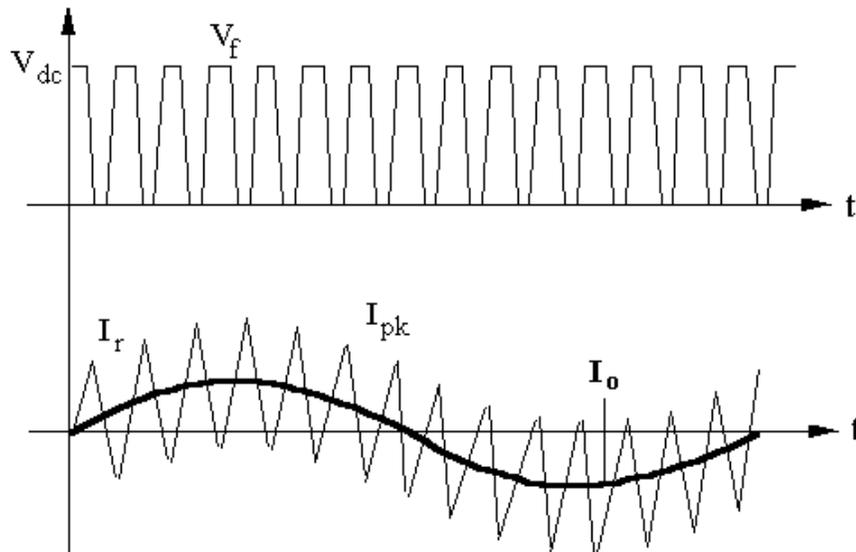


Figure 3.2. Resonant Pole Inverter Waveforms

Figures 3.1 and 3.2 demonstrate four drawbacks to this soft-switching configuration as applied to the new inverter.

- Additional inductive and capacitive components are required, adding complexity to the circuit.
- The slower transition times reduce the effective duty cycle, requiring a higher voltage on the DC buss.
- The peak currents in the semiconductor switches and the output inductor are much higher than the average output current, by a factor of 2 or more.
- Resonant circuit controllers operate best under heavy continuous loads. They do not respond well to light loads and load changes.

To overcome the complexity and high currents of the resonant pole inverter, another soft switching inverter topology, the resonant link inverter, has also been developed.

The resonant link inverter makes use of only one set of resonant components. The voltage across the resonant capacitor is also impressed across the six power devices. This voltage has an average or dc value which is equal to the dc bus,  $V_{dc}$ , and an oscillating or resonant component. Switching of the devices is synchronized to the link zero crossings.

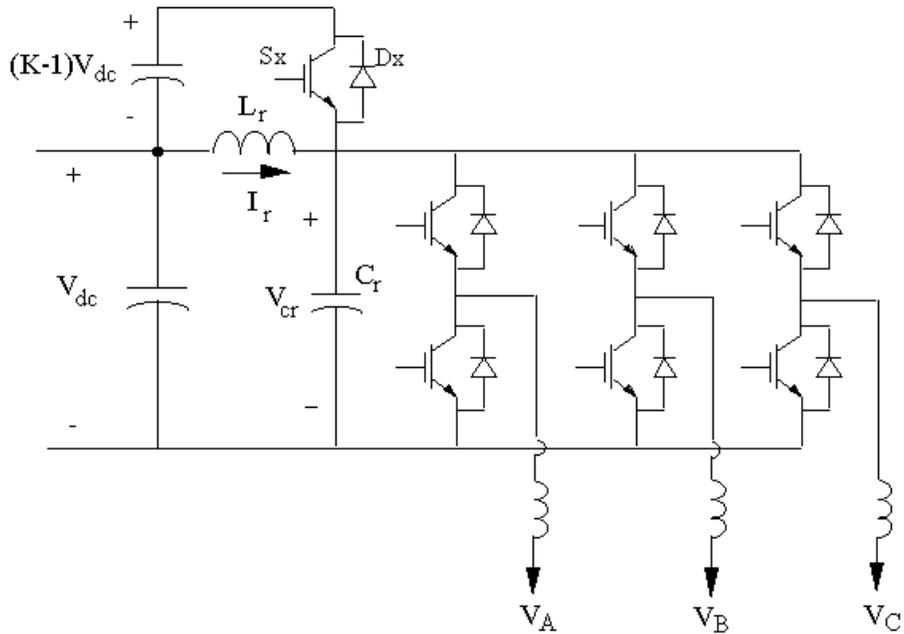


Figure 3.3. Resonant Link Inverter Circuit With Active Clamping

As devices are switched, the L-C resonant circuit excitation initial conditions are changed. This can result in high peak voltage stresses. In a resonant link inverter the IGBTs will have to operate at a peak voltage of two times the input voltage. To reduce the voltage stress, an additional voltage clamp may be added. This voltage clamp circuit is shown as in Figure 3.3, across the resonant inductor  $L_r$ .

The desired low frequency output voltage is generated in this inverter by using discrete resonant pulses, using a discrete pulse modulation (DPM) strategy. Typical low voltage synthesis is shown in Figure 3.4.

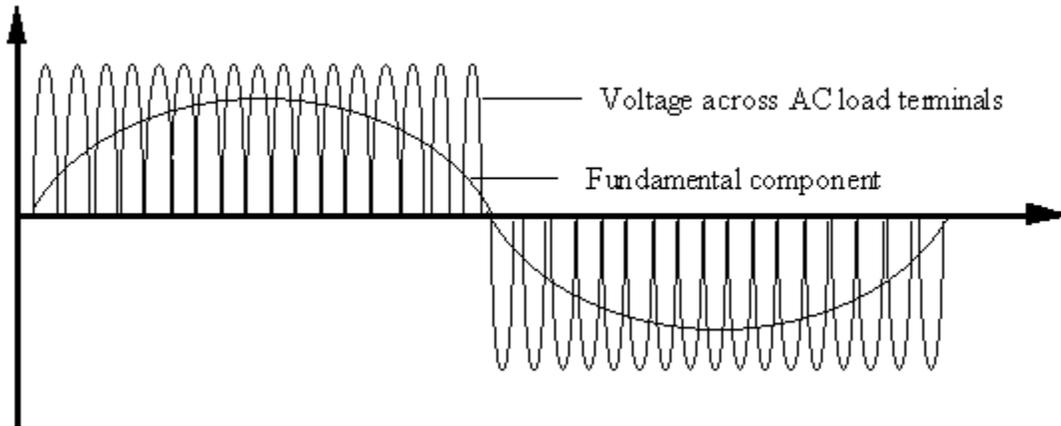


Figure 3.4. Resonant Link Voltage Synthesis

Drawbacks to the application of the resonant link inverter are:

- The voltage stress on the IGBTs is up to double the bus voltage.
- The control circuit must function at a variable frequency to maintain resonance.
- The additional voltage clamp circuit adds complexity.
- Resonant circuit controllers operate best under heavy continuous loads. They do not respond well to light loads and load changes.

### 3.3.3.2. Quasi-Resonant Inverters

Quasi-resonant inverters utilize additional semiconductor switches to excite the resonant circuit components on demand. This allows for pulse-width modulation control, although the control is a much more complex version than that needed for hard switching, due to the need to activate additional active components to control the resonant components and correctly time the main IGBT switching.

These circuits have the advantage that the resonant components do not carry the load current, and therefore are smaller and can operate at a higher frequency. This may allow the quasi-resonant circuit to perform under dynamic load conditions that are not supported by resonant inverters.

### 3.3.3.3. Hard Switching

In comparison to soft switching, hard switching imposes greater transient switching current on the semiconductor switching devices, and generates higher frequency harmonics that must then be filtered out. The effects of these

transients must be accounted for in designing for the SOA of the switching devices, while the higher harmonics must be filtered out.

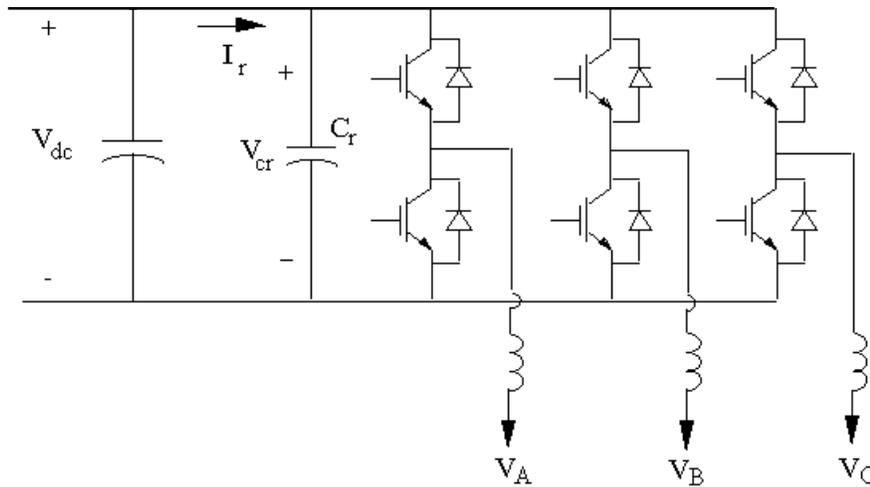


Figure 3.5. Hard Switching Inverter Circuit

### 3.3.4. Technology Approach Summary and Conclusions

Of the resonant inverter techniques, the fully resonant techniques are not ideally suited for use in an inverter designed for multiple applications due to their limitations in the ability to drive a diverse variety of loads.

The quasi-resonant inverter may prove valuable for use in the low to mid-power inverters. It offers these advantages:

- A quasi-resonant bridge generates fewer harmonics and less EMI, reducing the filtering requirements within the inverter.
- The SOA requirements of the semiconductor switching devices are lower.
- Reduced losses in the switching devices may be realized.

However, these potential advantages may be offset in low power inverters because:

- Present IGBT modules are designed with an SOA that easily accommodates the switching transients of hard switching.
- The harmonic and EMI filtering required for hard switching may be accomplished at a low cost.

- PWM algorithms for hard-switching are readily available for today's DSP devices. Development of quasi-resonant algorithms may be time consuming.
- IGBT dissipation due to hard switching is typically only one to two percent of the inverter output power. While an efficiency increase of up to one percent may be accomplished at heavy loads, there may actually be more losses at low loads.
- For hard switching in low power inverters, only one IGBT module is required for each power phase. Additional semiconductor switching devices are required to achieve quasi-resonant switching.

### **3.4. Universal Software Modules**

Each new generation of power electronics technology makes increasing use of software operating on embedded microcomputers. In early generations, software was used for status monitoring, high-level control and external communications functions. Today, software is critical to protective relaying functions required for grid interactive operation. In the next generation, software running on high speed digital signal processors will perform closed loop feedback control and will directly control the switching of the power devices (e.g., FETs and IGBTs ). With this increase in software's importance there is an increase in its size and complexity. Unfortunately, much of the current software suffers from reliability problems and it is difficult to maintain. These problems stem from the fact that much of software is written by power electronics engineers or control system engineers who have limited training and background in modern software engineering practices.

#### **3.4.1. Reusing Software Designs**

In addition to the reliability and maintenance problems associated with current software design practices, there is also a lack of design reuse. In some cases the software for a new power electronic converter is designed without reference to previous designs. In other cases an attempt is made to build upon previous software but the structure (or more accurately, lack of structure) of the software makes this a time consuming and error prone process. In many cases, the new software is initially less reliable than the software it was based on. In some cases key algorithms become corrupted because changes are made which affect undocumented, but critical, functions of the software implementing the algorithm. Part of the solution to these issues is to adopt modern software engineering practices based on modular software.

Modular software design practices require that the software be divided into a number of pieces that work together to provide the software's complete functionality. This top-down approach of dividing the software into modules is iterative and continues until the modules are sufficiently small and there are no

more opportunities for division. The essence of modular software design is logical division of the design according to criteria for setting the boundaries and functionality of the modules. There are two major criteria used to determine the module boundaries: by function hiding and by information hiding.

Parts of the software that work together to provide a particular function may be grouped into a single module. For example, consider a microcontroller that has a serial peripheral for communicating with other devices. In order for the software to use this peripheral, functions will be required to initialize, read and write to it. These functions would all be part of the same module. This module encapsulates or hides the functionality of the serial peripheral. If the functions are properly documented, then the module may be reused for other projects.

Information hiding is similar in concept but applies to the data that the software uses or produces. An example of information hiding is a software module that implements a database. The rest of the software needs access to the data in the database but it does not need to know how or where that data is stored. It could be stored in memory, on disk or on a tape. It could be compressed or encrypted. The database software module provides functions that allow other modules to access the data regardless of how or where it is stored. These functions form the interface to that module and the module hides the rest.

The benefits of designing modular software are well documented and known throughout the software industry. The benefits include:

- easier software reuse
- improved software documentation
- easier “porting”
- the ability to “build-up” a system from small “chunks” of code rather than monoliths
- easier and faster debugging
- easier and faster development
- software standardization.

### **3.4.2. Modular Software**

Easier software reuse means that subsequent software projects should proceed more quickly because engineers can combine already coded modules with new application modules thereby reducing development costs and hastening time to market.

The external software documentation of modular designs is better because the modules themselves have clear functional responsibilities and interfaces. Better

documentation will persuade software engineers to make use of the code because they will be more likely to understand and trust it. This will also reduce costs and time to market.

With modular software, porting to other hardware platforms (targets) becomes faster and easier because of the clear distinction (modularity) between target-specific and general purpose code. For example, consider two different microcontrollers that both include an A/D converter peripheral. Each one provides a different way to access it. The first one uses a register-based interface while the second uses a memory-mapped interface. Clearly, the code for accessing the A/D will be different for each processor but the function of the A/D is the same as far as the higher-level code is concerned. By providing a low-level A/D access module that presents the same interface to the higher-level code, the software engineer is able to port his software from one processor to the other by modifying or swapping out only one module instead of many. This, in turn, means that changes in the target hardware do not obsolete a lot of software development work. This saves time and money.

For systems that are very complex with large amounts of code (>500k lines), modularity allows the software to be assembled slowly and in a controlled way. This progressive, step-wise approach means that subsystems may be tested and verified a little at a time. The results are more robust and reliable code causing fewer problems “down the road.” Fewer problems lead to lower support costs.

Debugging is also easier with modular code as the interfaces between the modules provide well defined “test points” when using a debugger. The test points are places where the results of calculations and peripheral operations can be viewed, verified and altered in order to exercise the software. Easier debugging means lower development and future support costs.

The time required to develop software is drastically reduced using a modular approach. Multiple engineers can each work on a different module in parallel because the interfaces between the modules are well documented and understood. Faster development means faster time to market, which is important in today’s economy.

The ultimate goal of modular software is standardization. This includes:  
a standard requirements specification process:

- a standard design process and techniques
- a standard set of document templates
- a standard high-level language (i.e., ANSI C)
- a standard coding style and naming conventions
- a standard set of algorithm implementations.

All of these standards work together to increase design/code reuse, robustness and reliability and reduce development effort, costs and time to market.

Many organizations (i.e., companies, institutions, etc.) have realized the benefits of modular software design. Some of their software modularity efforts have extended “beyond their walls” and become guidelines/rules for developing modular software.

### **3.4.3. DSP Modules**

Of particular relevance to next-generation power electronics systems is the work of Texas Instruments. The Digital Control Systems Group at Texas Instruments (TI) is working towards providing their customers with software modules for their DSPs [0]. These modules include the low-level modules for accessing the on-chip peripherals like A/D converters, but they also include application specific modules for power electronics. Currently, the application modules developed by TI are limited to digital motor control. However, application modules for power electronic converters used in renewable energy and photovoltaic (PV) applications could be developed according to TI’s standards and methodology by TI, third party software vendors, or by the developers of the power electronic systems. TI’s vision is that, eventually, engineers will be able to develop control software using a standard set of software modules that “plug” together much like the blocks in a control system diagram.

In fact, there are already tools available (e.g., Matrix X and Real-time Workshop) that provide this high-level functionality and generate code from control system block diagrams. Unfortunately, the code still needs to be interfaced to the low-level routines of the particular target processor. In addition the code generated is sometimes somewhat inefficient when compared to code that is developed at lower level. However improvements in code generator performance and functionality and increases in embedded processor speed are expected reduce or eliminate these disadvantages. Proposals to adopt a third party code module library (such as TI’s) or a code generator can encounter organizational resistance.

From an engineering perspective there are concerns regarding:

- the reliability and robustness of the code
- performance when compared to software developed using lower level techniques
- the potential lack of support
- conflict in coding standards.

In addition to these valid concerns, the possibility of an organizational “not invented here” syndrome must be acknowledged and overcome.

From a corporate perspective there are concerns regarding:

- cost of license fees and development tools
- intellectual property (IP) ownership
- product liability issues.

Within an organization there are also issues to be overcome if a modular approach to software design is to become standard. Appropriate software-engineering processes and design standards must be put in place. Suitable development tools must be purchased. Software engineering skills must be developed through training and recruitment of experienced software designers. An appropriate balance must be found between the desire of the organization and its software designers to seek novelty, differentiation and design improvements and the need for discipline, standards, and design reuse.

#### **3.4.4. A Vision for Future Software**

If this can be achieved, then the software vision for next generation power electronics includes:

- Products as “black boxes” with well-defined and documented external interfaces. These interfaces will be based on “open” standards and protocols. This will allow customers to easily integrate products into their systems.
- Incorporation of TI’s modular DSP software methodologies and libraries into the software development process in order to improve reliability and reduce costs. Standard algorithms for functions such as maximum power point tracking, anti-islanding protection, power and energy metering, power system protective relaying, and so forth will be developed as well documented reusable software modules compliant with the TI standards.
- Greater use of high level languages, such as C or C++, and design tools such as MatrixX or Matlab Real-time Workshop so that more design is performed at the systems level.
- Adoption of modern revision/version control systems to control access and modification to the source code and documentation.
- Comprehensive software testing to ensure that software modules are correct and robust.

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### **3.5. Universal Functional Block Architecture**

A new inverter will be developed to be highly reliable and efficient. We then require that this inverter be versatile; that it be capable of interfacing with multiple technologies in multiple applications and at a minimum cost.

This new inverter will be initially launched as a multi-platform product. The majority of components within the inverter will be utilized regardless of the power level (2 to 10 kilowatts), the energy technology (PV, Fuel Cell, Storage, etc.), or the application (grid-tied, off-grid, UPS).

While the result of this project will be the creation of a multi-functional inverter, we must avoid forcing the user to pay for functions that will not be utilized. An inverter for a very simple application such as a high voltage PV source for single-phase grid-tied use will include only a sub-set of the same exact technology, circuits, and assemblies to be found within the most powerful inverter with bi-directional operation, energy storage, charge control and low-voltage renewable energy input. In this manner the economy and enhanced reliability of large-scale manufacturing may be maintained while achieving even greater economy when less functionality is demanded.

There are many functions that are performed by every inverter, regardless of the power level, the energy technology, or the application. These functions will be developed as functional blocks. Some of the blocks will be present in every inverter. Others will be used on a mix-and-match basis. The universal functional blocks are:

- Control Assembly
- Low Voltage Power Supply
- Half Bridge
- 3-Phase Bridge
- DC-DC Isolated Boost Converter
- DC-DC Isolated Buck Converter
- EMI Filter
- Remote Display
- DAS with Modem and GUI

The use of these functional blocks allows a uniform production and quality control plan. All of the assembly, testing and quality control of functional blocks may be performed in a large-scale factory setting. These blocks may then be assembled in a separate area, into a final inverter of any desired configuration for final test

and burn-in. Final tests for the various configurations will have a uniform appearance and procedure.

### **3.5.1. Control Assembly**

The exceptional versatility of Digital Signal Processing (DSP) devices will allow us to create a control assembly capable of controlling, from one processor, both the supervision of all inverter functions and the actual power conversion. One inexpensive DSP has the capability to support an inverter of any desired configuration, with only the software varying from one unit to another.

Specific program versions assembled from a library of software modules may be loaded into a controller after it is assembled into an inverter. The development of these software modules will reduce the development time for a multifunctional inverter, as will the need for only one control assembly regardless of the application.

### **3.5.2. Low Voltage Power Supply**

Regardless of the input and output voltages, certain voltages are required within the inverter for operation. All of the electronic circuits within the inverter operate on low voltage DC. The digital circuits, including the DSP, operate at +5 volts DC. Separate DC sources will power analog electronic circuits, isolated power switch gate drive, contactors and fans. All of these voltages will be derived from a common low voltage power supply.

### **3.5.3. Half-Bridge**

The primary function of an inverter, by definition, is the conversion of electrical DC power to AC. The circuit where this is accomplished is called a power bridge. The basic functional block of a bridge is a half-bridge. This circuit may utilize either FETs, for low voltage operation, or IGBTs for high voltage operation. Some inverters will operate from a low voltage source and other from a high voltage source. However, only one half-bridge is desired for this new inverter.

The use of IGBT modules is widespread in the motor control industry, which is geared to support the industrial user with high reliability requirements. It is proposed that this new inverter will operate with a high voltage bridge utilizing IGBTs, and that a boost assembly will be incorporated into inverters that must operate from a low voltage source.

### **3.5.4. 3-Phase Power Bridge**

For inverters operating into a three-phase utility, a three-phase bridge will be required. It is preferable to have a dedicated three-phase bridge assembly, rather than to use 3 separate single-phase assemblies, even though a three-phase bridge electrically includes three separate half-bridge circuits

Three-phase operation has the advantage of the cancellation of 60-Hz ripple, and therefore does not have the energy storage requirement of single-phase operation. The use of separate half-bridge assemblies would also duplicate some voltage and current sensing components. The use of a dedicated three-phase bridge assembly will reduce interconnections and component count for three-phase applications.

This assembly will be inhabited by three half-bridge circuits of the same electrical configuration as the half-bridge assembly, and will have common DC voltage bus, voltage and current sensing, and power distribution components.

These two bridge assemblies may be loaded with 100A, 200A, or 300A IGBT modules, depending on the output power of the inverter. The assemblies, prior to loading the IGBTs, may be produced in high volume.

The use of high volume assembly for the bridge assembly prior to installation of the IGBT modules, coupled with the use of the rugged IGBT module technology, maximizes the probability of meeting the DOE reliability and cost goals.

### **3.5.5. Universal DC-DC Isolated Boost Converter**

The DC-DC isolated boost converter is needed where the inverter will operate from any low voltage source, which can be fuel cells, PV, or batteries, to name a few. Incorporating isolation at this stage will allow the low voltage equipment to be grounded separately from the AC line ground, helping to eliminate the need for a large 60-Hertz transformer, and assuring compliance with any safety rules.

A boost converter is an efficient, reliable, and economical method of raising the voltage of a DC power source. This type of converter can accept an input from any energy storage or generation source and raise that voltage for use by a high voltage IGBT power bridge.

Although no power bridge can operate from both low voltage and high voltage sources, this universal functional block will facilitate the use of the same power bridge components within inverters operating from either high or low voltage sources.

### **3.5.6. DC-DC Isolated Buck Converter**

The power bridge is bi-directional, that is, it can operate with the power flowing from the high voltage DC bus to the AC line, or from the AC line to the DC bus. However, the power bridge cannot charge low voltage batteries directly. In order to charge the low voltage batteries from the high-voltage bus output from the power bridge, this isolated buck converter is used.

The DC-DC isolated buck converter is required only for applications with a low voltage battery bank where it is desirable to charge the batteries from the AC line. By having a module for this purpose that is only installed when needed, and yet is controlled by the central DSP when installed, the installed cost of both simple and complex systems is kept to a minimum.

### **3.5.7. EMI Filter**

The power bridge and the DC-DC converters utilize inductors to smooth out the current created by the switching of the IGBTs and the FETs. After this process, some unwanted high frequency ripple remains in the inductor. EMI filtering prevents this high frequency ripple from leaving the inverter on the input or output power lines.

Often, the EMI filter is added to an inverter design after it is tested. By designing in an AC and a DC EMI filter that will connect the power switching assemblies and the user interface of the inverter, the extra time and expense of creating and installing an add-on EMI filter to each unit configuration will be eliminated.

### **3.5.8. Remote Display**

Currently, every inverter product line has a display that indicates some inverter operational parameters. These displays vary considerably. The universal inverter design will include an optional remote display that will be driven by the DSP on the Control assembly. This same display assembly will be available for use with the inverter in any of its many application scenarios.

By utilizing the power of the DSP for the remote display, a single, low-cost universal remote display may access the inverter regardless of the inverter power level or the application.

### **3.5.9. DAS with Modem and Graphical User Interface**

Where the remote display is not sufficient, a remote DAS is required.

An integrated DAS will reduce the cost and installation time for systems that require a DAS. By having a DAS assembly which communicates to the DSP within the inverter, all of the daily and real-time operating conditions will be available for display and logging without the need to design a DAS for each installation.

### **3.6. High Reliability Manufacturing Considerations**

As the power electronics industry for PV systems matures, some of the biggest changes will be in the area of high reliability manufacturing. This shift will be driven by two key elements: requirements of the marketplace, expansion of volumes, and competition.

The maturation of the marketplace requirements will be reflected in both a greater level of standardization of product performance expectations as well as a general demand for high quality and reliability. As the rate the PV systems are installed is growing substantially (25%+ per year), the requirements associated with quality and reliability will be emphasized. This will be in true from an economic basis as the cost of low quality and poor reliability increase (i.e. warranty costs). The greater sophistication of the more experienced customer will also cause the power electronics manufacturers to focus even more on quality and reliability enhancements.

The standardization of product performance expectations will reflect the fact that the marketplace has gained experience about what is technically required of the power electronics for a given PV application. This will greatly reduce the number of customer issues that are related to a mismatch between expectations and the actual product performance. One example of this is the required performance in overload conditions, which are not presently well defined and can lead to customer disappointment even in the cases where the equipment is meeting the specification. While these issues are not directly related to manufacturing considerations, this maturation of expectations will result in a greater level of customer satisfaction, which is often presently expressed as a quality or reliability complaint.

The increase in the volume of equipment that is built for the PV application will drive the equipment manufacturers to more advanced manufacturing processes. This has been seen in a number of comparable industries. The expected benefits of the move to proven high volume manufacturing practices will certainly

enhance the quality and reliability of power electronics systems for PV applications. These changes include a formalization of the processes that are used (ISO 9000), the use of accelerated product life testing, and increased use of automated assembly.

As the market size increases and the customer expectations become more mature, this will certainly lead to increased level of competition. This is presently being seen in the power electronics for PV systems area with the recent expansion of European and Asian manufacturers into the US market and US manufacturers into overseas markets. This competition will push all manufacturers to achieve higher quality and reliability performance.

### 3.6.1. Comparable Industries

Substantial insight into high quality and reliability manufacturing considerations can be obtained by examining several comparable industries. For this report, information has been gathered from manufacturers of uninterruptible power supplies (UPS), adjustable speed motor drives (ASD), and telecom rectifiers. There are some significant similarities in the power electronics for these systems with those required for PV systems as noted below along with some of the “World Class” manufacturers that were investigated for this report:

Industry	Technical Similarities	Selected “World Class” Manufacturers
UPS	DC to AC inversion Battery management	American Power Conversion, Best Power, Toshiba, Liebert
ASD	DC to AC inversion Connection to utility grid	Emerson Electric, Toshiba, ABB, General Electric, Siemens
Telecom Rectifier	DC to DC conversion Interface to utility grid	Lucent Technologies, Power-One, Artesyn, Delta Electronics

All of the companies included are substantial suppliers of equipment to their industries and are in a position to provide insight into high quality and reliability power electronics systems. There are certainly other “World Class” companies that were not included for various reasons. The data was gathered through interviews, published information and the Internet. Additionally, valuable information was obtained from Motorola. The summarized information in this report does not include any confidential material.

For the purpose of this section of this report, quality is defined as the conformance to requirements. The elements of the materials and manufacturing

process are key elements to ensuring product quality. Reliability is related to the performance of the equipment in the intended application. The following sections present a summary of the activities of the leading manufactures in the identified comparable industries.

#### 3.6.1.1. Quality

From the manufacturing perspective, quality is typically perceived as implementing the materials, assembly, and test processes in an accurate and repeatable manner. While it is assumed that the engineering design is correct and properly documented, feedback is given to engineering to improve the quality of the design. The processes that were identified by the companies surveyed in the manufacturing process that are key to affecting quality are summarized as:

- Materials – Incoming materials from suppliers meeting requirements
- Assembly Process – Processes for product assembly are correct and accurately followed
- Test – Test procedures and fixtures are sufficient and give repeatable results
- Feedback Systems – Processes to measure and improve the above processes

These steps for ensuring that the end product is of high quality (conforms completely to requirements) are expanded upon in the following sections.

##### **3.6.1.1.1. Materials**

The use of high quality materials is obviously a key to providing a high quality end product. Power electronics manufacturers typically operate in a mode of doing final assembly and test in-house. Key system sub-assemblies are either built in-house or outsourced. The message received in this study was that the decisions concerning sub-assembly make/buy decisions were highly specific to the exact assembly concerned. The make/buy decision was indicated to be typically made on economic considerations. The quality system used for individual components is used to ensure that the subassembly suppliers provide quality components. A common example of this is the printed circuit boards (PCB). While there are many contract manufacturers (fabrication and stuffing), all of the companies reviewed did some assembly of key boards in-house. Most of the companies also used outsourcing for some PCB's.

A key material management trend that was identified is the implementation of close partnership between the power electronic equipment manufacturer and their component and subassembly suppliers. The use of a limited number of suppliers that are put through a detailed qualification process is viewed to be the

optimal materials management approach. This is typically implemented through the use of a strict Approved Vendor List (AVL). Approved vendors typically go through a company specific qualification process that reviews the quality systems of the supplier and delves fairly deeply into their operational details. The quality of the supplied components is measured and feedback, in the form of a “report card” is provided on a regular basis. There are also usually vendor audit procedures in place. A process of competitive checks is used to ensure the component cost targets are reached and these are typically reduced from year to year. By working closely with a limited group of approved vendors, systems cost reductions are often made through joint design changes where the benefits are shared by the supplier and the customer. The typical benchmark for this item is shown in the company procurement goals of reducing the number of vendors.

Another materials trend is the goal of reducing inventory levels. This involves implementing vendor relationships that support delivery of components more frequently and in smaller batches. The drivers for this are primarily economic, although quality and reliability benefit from limiting the exposure to “bad batch” type of problems with components. All manufacturers also have benchmark goals of reducing inventory levels throughout the manufacturing process.

All of the companies reviewed have some form of incoming material inspection process. This ranged from 100% to a statistical sampling. The statistical sampling rate would be adjusted based on experience and history with the specific component and vendor. The tone of the ideal approach was to limit the level of incoming material inspection and work closely with the vendors to ensure that the vendor sends quality material. The specifics are identified in their ISO procedures. The volumes of materials are typically high enough that inspection fixtures that gave relatively quick clear pass/fail criteria are used.

#### **3.6.1.1.2. Assembly Process**

The key aspect of the assembly process for quality is that each process is completed in an accurate and repeatable manner. This is implemented through the generation and use of assembly procedures. The conformance to these procedures is the key audit measure for the assembly process. Feedback is provided over time to improve the assembly procedures.

In addition to the general answer of properly following the assembly procedure, there were some specific manufacturing approaches that were cited to increase the quality of the end product.

Cell Based Manufacturing - This approach is to structure the manufacturing facility in such a manner that the people that assemble a product are focused on one (or a limited number) of products and are very familiar with that product. They are very aware of the processes that they do as well as the preceding and following processes to give a better ability to spot problems earlier in the

assembly process. Very often, the complete materials, assembly, and test processes are all contained in a focused cell. This results in having a team that is very familiar with all of the issues with a particular product that is well positioned to work together to improve quality and reliability. They are also focused in such a way that they are particularly aware of the issues that are associated with the materials and assembly procedures and are empowered to implement improvements.

Lean Manufacturing – This indicates an approach that is focused on maintaining as small of an inventory level at each point of the manufacturing process as possible. This includes the receiving of incoming materials from vendors. The lean approach is an extension of the Just In Time (JIT) approach where materials are delivered to their point of use at the time they are needed. The lean approach also often focuses on relatively small batch sizes. This limits the possibility of having a significant problem based on a “bad batch.”

Kaizen - This is a manufacturing approach that is focused on continual improvements to achieve improved results. It is a process adopted from Japanese manufacturers (obvious from the name that has achieved a bit of “buzzword” status among electronics systems manufacturers). There are two main thrusts of the Kaizen approach. The first is “Flow Kaizen.” This involves what is referred to as “value stream mapping” where each process is evaluated for the value that is added at that step. The second is “Process Kaizen” in which the focus is the elimination of waste at each step in the production process. Many of the ideas put forward in Kaizen are part of the Lean and Cell Based approaches. Kaizen comes up with power electronics manufacturers as something that is being looked at, implemented, or parts are being implemented. A company that is doing a Kaizen implementation is clearly focused on restructuring it’s manufacturing process.

Six Sigma – This term indicates a quality level of not more than 3.4 defects per million opportunities. Popularized by General Electric, it is an overall approach to quality measurements that is not limited to the manufacturing process. There are six key concepts at the core of Six Sigma (information source: GE Web Page):

1. Critical to Quality – Attributes most important to the customer
2. Defect – Failing to deliver what the customer wants
3. Process Capability – What the process can deliver
4. Variation – What the customer sees and feels
5. Stable Operation – Ensuring consistent, predictable processes to improve what the customer sees and feels
6. Design for Six Sigma – Designing to meet customer needs and process capabilities

This is implemented by adjusting the meaning of the word “customer” to cover a broad range. For example in manufacturing, the “customer” could be the next step in a series of processes. Some feedback was received that a common interpretation of “Six Sigma” was to have a very high threshold for the definition of meeting requirements more so than the specific number.

### **3.6.1.1.3. Manufacturing Test**

The use of testing during the manufacturing process to validate the proper operation of the power electronic systems is a key to providing high quality products. This testing typically covers key individual components, subassemblies, and the final system testing. The placement of the testing in the process is typically determined by examining the cost and effort to repair a defect if it is found later in the assembly process. This is a key area for continual improvement efforts to raise the quality level of the final product.

The most common tests of incoming components are on the power semiconductor devices, magnetics, and capacitors. This is to validate the functionality of the part as well as measure key performance characteristics that may be important in the selection process (from the Engineering requirements). The semiconductor devices are typically tested for proper operation and in some cases, this is done at elevated device temperature. Inductors and Transformers may be tested to verify their proper parameters. Capacitors are tested for their capacitance and may be measured on in limited surge conditions. Typically, these measurements are made if there is a history of an issue with a particular component or particularly tight parametric requirements.

Subassembly tests most commonly involve printed circuit boards and power assemblies (devices, capacitors, and interconnects). Printed circuit boards have a bed of nails test for a basic check of proper wiring and component installation. This test is typically done as the final step of the PCB manufacturing process. This is commonly followed by a functional test that takes place in a fixture that provides simulated signals to exercise the board as much as is possible outside the entire system. Power assemblies are almost always tested in large systems (above 5kW) before they are installed in the system due to the cost of making a repair outside of the final system (this may not be the case for smaller power level systems).

Final test is a key to confirming the proper performance of the power electronics system. This can be particularly challenging for power electronics systems because of the test equipment that may be required to completely exercise the system. This equipment typically includes power supplies, passive loads (resistive and reactive) and electronic test equipment that may need to be specially constructed for their designated purpose. Interestingly, resistive loads

that just burn the power are commonly used to raise the power level instead of active loads that could recover the power back to the utility grid.

In general, due to the relatively high manufacturing volumes and the need for repeatability, the tests implemented by UPS, ASD, and Telecom Rectifiers are implemented using automated test equipment. This removes the variations that may be found from having different technicians execute the test. Typically, the automated test equipment generates a pass/fail output. On larger systems, the test report may contain specific performance results that are kept on file or sent to the customer with the system. This can be used for future process optimization as well as for customer service.

The typical benchmark for manufacturing test is the measurement of First Pass Yield. This can be for components, subassemblies, or in final tests. All of the “World Class” customers who provided this data targeted First Pass Yields of 95% -99.5%.

#### **3.6.1.1.4. Feedback Systems**

To continually validate and optimize the performance of the manufacturing process, data is gathered and analyzed. This data is used throughout the manufacturing process and is tailored for the specific product and process that is being evaluated. In the high volume manufacturers examined, the data gathering process is very formal. This information can be (and usually is) also presented in a format that is used to communicate the performance of the system to the employees implementing the system. This information can be presented in the form of histograms that visibly show the trends and performance related to a specific goal such as First Pass Yield.

Commonly, an In Process Audit program is implemented for high volume power electronics manufacturing. This process involves auditing (inspection) of all aspects of a particular manufacturing process. This can include: bill of materials (BOM) audit, manufacturing documentation audit, process documentation, tool and test equipment calibration checks, and review of workmanship standards. This fits into the often-stated plan to have continuous improvement.

Formal corrective action systems are used to implement changes and improvement to the manufacturing process (as well as pass product information back to engineering). The details of this process are documented as part of the companies’ ISO processes. There is typically a Process Failure Modes and Effects Analysis system that involves cross functional teams that focus on product quality and reliability (that complement the Engineering FMEA process). A key process that is used in the case of an identified process failure is a Root Cause Analysis (also similar to that used for product failures).

This feedback is key to maintaining and improving the manufacturing process. It is highly dependent on the specific product and process being examined.

### 3.6.1.2. Reliability

The common definition of reliability is the ability of an item to perform a required function under stated conditions for a stated period of time. Power electronic systems are typically required by the customers to have a high level of reliability as they are employed in key functions. Reliability of these systems is related to the quality (meeting the requirements), engineering design for reliability, and the manufacturing processes that enhance the reliability in the end user application.

Before a piece of equipment reaches the manufacturing state, the engineering process must take into account the reliability goals of the system. This is especially true for power electronic systems, as there are clear design trade-offs that affect reliability. One key example of this is the junction temperature at which the devices are operated. The rule of thumb is that the lifetime of a semiconductor device drops by a factor of two for every ten degrees C that the operating temperature is increased. The selection of devices and the cooling system must take this into account. An additional important aspect of design is the use of Type Testing to validate a design. This places extreme conditions on a unit that is being designed to determine exactly the failure modes and give the engineer the opportunity to improve the design.

One common measure of reliability is the Mean Time Between Failure (MTBF). Research into competing industries did not give detailed MTBF numbers for the various applications. However, the following chart shows the standard warranties for those areas, (which is a good translation of the MTBF into economic terms).

Industry	Standard Warranty
UPS	2 years
ASD	18 months (Analog controls) 5 years (Digital controls)
Telecom Rectifier	2 years

The environmental conditions that a piece of equipment is operated in can dramatically affect its reliability. This is especially true for power electronic systems such as ASD's which are typically installed in a factory environment. This is less true for UPS systems and Telecom rectifiers that are often located in climate controlled environments. However, this is one area where the comparison to the power electronics for PV systems is a bit misleading. The

converters for the solar applications are typically installed outdoors and in a generally more hostile environment than these other applications. This fact needs to be considered in the design and manufacturing test process.

### **3.6.1.2.1. Burn-In Testing**

The principal method of increasing the end use application reliability through the manufacturing process is the use of environmental testing. This is typically referred to as the “Burn-In” test. The purpose of the test is to have any infant mortalities occur at the factory instead of at the end user. This moves the state of the product from past “early failure” range of the famous “Bathtub” curve of electronics reliability.

All of the manufacturers reviewed did some level of environmental testing as part of the manufacturing process. This involved typically operating at high temperature for an extended period of time. The time information varied from 2 hours to 48 hours depending on the system and there were some references to operating at rated maximum temperature and some tests were done at above the specified value. Some of the systems were put through temperature cycling, which increases the stress on the power electronic system. The details from the manufacturers of the testing were limited.

Interestingly, Motorola has a group that provides for environmental testing. They list the following as possible tests:

- Air-to-Air Thermal Shock
- Temperature/Humidity
- Falling Rain
- Wind and Rain
- Dust Laden Environment
- Electrodynamic Vibration (Sine, Random, Shock)
- Mechanical Shock
- Precision & Random Drop
- Package Testing
- Tension/Compression
- Electrical Variation Testing (Brown-Out, Frequency Sensitivity, etc.)
- Electrostatic Discharge Sensitivity per IEC guidelines
- Dimensional Verification
- Battery/Cell Capacity Measurement

While some of these are clearly of the Type Test nature, it seems likely that some of these tests could be used to further eliminate infant mortality failures in power electronics systems.

### 3.6.2. ISO Compliance

**Specifically define the importance of ISO compliance in maintaining a disciplined manufacturing doctrine.**

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The ISO 9001:1994(E) standard is one of three International Standards dealing with quality system requirements that can be used for external quality assurance purposes. The standard consists of 20 elements, each with compliance requirements. The elements address Management responsibility (policy, objectives, planning, quality management system, and management review), Resource management (human resources, training), Process management (customer satisfaction, design, purchasing, production), Measurement, analysis and improvement (audit, process control, continual improvement). Compliance to these requirements provides objective evidence suitable for assessment by a certified third party Registrar, which issues a Certificate of Registration to the particular ISO standard being assessed. Xantrex individual business units have demonstrated compliance to, and maintain Certificates of Registration to ISO 9001.

ISO Compliance, in itself, will not guarantee product quality or maintenance of a disciplined manufacturing doctrine. The guidelines set forth in the standard must be embraced and adhered to by the individuals affecting quality if any positive outcome is to be expected.

Xantrex Technologies exists in a regulated environment, as do all power electronic companies. Xantrex processes have been documented and written procedures were created to ensure consistent and repeatable results and provide a basis for continual improvement. The Xantrex quality system is in compliance with ISO standards, not as a result of the standards. Internal and third party audits are used as methods to improve overall business practices. Xantrex's products must meet UL (Underwriter's Laboratory) requirements, and are now also regulated by the CE mark and IEEE (519, 929) in the European markets. In this environment, Xantrex Technologies has chosen to commit itself to quality by its own definition, knowing that "doing the right things right" will result not only in a high quality product, but also will meet any reasonable standards that may be established by outside regulators. Xantrex has taken a proactive approach to these certifications, as evidenced by our current efforts to integrate the requirements of the CE mark with United States standards as defined by UL.

The timing of the formation of Xantrex Technologies coincided with a philosophical shift in thinking towards quality and quality systems. Instead of the quality staff being perceived as "cops" within the organization, Xantrex Technologies emphasized that quality was everyone's responsibility. Xantrex Technologies perceives ISO registration as a process that forces us to look at how we do business and provides a method to ensure correct and consistent performance as well as identifying opportunities for improvement. ISO standards

are a guideline on a good way to do business. As quality becomes an elementary principle in our approach to doing business, ISO registration and compliance consumes very few resources, for the requirements of ISO registration become inherent in establishing good business practices. Indeed, in an industry subject to certification by the Underwriter's Laboratory (UL) in the United States, and now the CE mark in Europe, Xantrex Technologies has adopted a very constructive attitude towards certification procedures and third party inspections. Xantrex welcomes UL product inspections and quality system audits as opportunities for third party feedback secure in our commitment to quality, Xantrex welcomes suggestions for quality improvement.

### **3.6.3. Quality Assurance**

Xantrex Technologies employs various quality assurance methods, depending on the task specified. For example, the Quality Manual states that all "designs are verified using analysis, tests, or comparison to existing proven designs." Xantrex maintains supplier evaluation records. For suppliers who have a history of excellent products, testing is not required at the time of delivery. Product verification in this instance is generally done at the point of use. However, for suppliers who are unproven or who have a history of nonconformance, their products are either subjected to initial testing upon delivery or are terminated as suppliers if the nonconformances are either severe enough or too frequent. Xantrex also clearly identifies all products for all stages of production to allow for error free assembly and accurate recognition of various parts and assemblies. Xantrex uses workmanship standards to ensure consistency and excellence in production and assembly. These standards are published and used regularly. Equipment is calibrated regularly, as required.

Employee involvement, morale and commitment to the values of the organization contribute to overall quality and maintenance of a disciplined manufacturing doctrine.

### **3.6.4. Accelerated Product Life Testing**

Research and quantify the benefits of HALT and HASS testing. Define the timing of applicable tests during the development cycle.

Highly Accelerated Life Testing (HALT) and Highly Accelerated Stress Screening (HASS) are processes used to predict and improve reliability, and verify those predictions.

**Basic Design Stage and Planning.** HALT testing with reliability analysis software assesses basic designs and allows for improvements

prior to building the first prototype. It also indicates how often something is likely to fail, which allows understanding of how warranty and support costs would be affected, and to make sure it can be fixed if it breaks. Propose the best service scenarios and design for serviceability. Develop preventive maintenance schedules, identify mean time to repair and maximum corrective maintenance time, mean down time and compare on-site versus depot repair. Provides information needed to determine what accelerated stress tests would properly test the potential failure modes and what sample size and test time would be necessary to prove-in a robust design.

Additional activities could include determining failure rate requirements (parametric and catastrophic), system level requirements, system life requirements and component life requirements. Root cause and failure mode analysis (RCFMA) and corrective action (CA).

**Prototype Stage.** HALT testing and Data Analysis based on information and predictions determined in the previous stage, using the reliability analysis software and published component reliability data. Testing and Accelerated Testing Data Analysis may include: Temperature-Step-Stress, Isothermal Aging, Pressure-Temperature-Humidity-Bias Testing, ESD-Electrostatic Discharge Classification Tests. Mechanical Testing: Shock & Vibration, and Temperature Cycle/Shock. The information that is gathered during this stage would allow better definition of the requirements for packaging, shipping containers, transportation from the OEM to site installation, and the installation environment. The preceding information was gathered from: Litton-TASC, QualMark Corp., Sandia-Center for System Reliability, and Systems Effectiveness Associates, Inc.

### **3.6.5. Automated Assembly**

Define which manufacturing processes could be automated and at what production volumes these processes become effective.

Automation, with proper planning, can increase factory productivity as well as benefit product quality in several ways:

- Automation can eliminate some of the monotony or fatigue tasks that cause errors by human beings.
- Process variation can be reduced by automatic monitoring and continuous adjustment of process variables.
- An important source of process troubles, i.e. the number of machine setups, can be reduced.
- Machines cannot only automatically measure product but can record, summarize, and display the data for the line production operators and staff

personnel. Feedback to the worker can be immediate, thus providing an early warning of impending troubles. (J.M.Juran, Frank M. Gryna 1993).

During the Design Study and Planning Phase, many Make / Buy decisions will be Made, as well as determining implementation of automated techniques. Addressing the following will arrive at these decisions:

- What process will be involved?
- Can the process be simplified?
- What is the process capability?
- What technologies are being used?
- Are there new technologies available?
- Do new forms of automation provide ROI, cost, quality, and flexibility?
- Where does the greatest ROI exist?
- Determine the type of automation.
- Flowchart the process.
- Can the process be simplified again?
- What training will be required?
- Purchase equipment.
- Train operators

For purchased parts, evaluate suppliers for ability to provide desired results, using their own manufacturing methods.

It would be very difficult to state which processes would be automated without evaluation of the specifics of each process and a clear understanding of projected production volumes. Circuit board fabrication and assembly is the obvious process, using Pick and Place, Auto-insertion, vapor phase and flow soldering techniques. Additional automation could be applied to circuit board testing, sub-system and system testing as well as enclosure fabrication.

## **Section 4. University of Minnesota Inputs**

### **4.1. Required Ratings of DC Energy Sources**

The present section analyzes various DC distributed energy sources to determine the required ratings of the input characteristics of a DC-AC inverter system that would convert the DC power available from these sources into 60 Hz AC power. The section also analyzes the various types of loads to determine the most commonly used output type in the medium power range of 2 kW to 10 kW. Finally, two configurations for the DC-AC inverter system are proposed which can be easily adapted for different types of sources and could potentially reduce the cost of the inverter system while achieving a very high reliability.

#### **4.1.1. Background**

Utility deregulation has increased the possibilities for distributed energy generation. The market for distributed generation is growing and is expected to reach between 25 and 50 GW by 2010 [1]. On-site generation of electricity using distributed energy sources is on the increase. The on-site generation capability is used in both grid-tied and off-grid modes in order to supplement the utility power and to provide power during outages. Sources like photovoltaic (PV) arrays, fuel cells and batteries are attractive options to be used as they are clean sources of power.

The above-mentioned sources are, in general, DC sources which generate power at low voltage and high current. An DC-AC inverter system is required to convert the DC voltage to the more commonly used 120 V AC single-phase, 240 V AC two-phase or 210 V three-phase systems.

Additionally, the above-mentioned distributed sources are currently not very cost effective. A major component of the cost of the system is the inverter. In order to make the entire system cost effective, the cost of the inverter has to be reduced. The inverter systems that are currently available in the market are built specifically for the source (PV arrays or fuel cells) and cost anywhere between \$1.7/watt for low power applications (1 kVA) to \$0.8/watt for high power applications (10 kVA) [2].

In order to achieve a lower cost for the inverter, it will be necessary to design an inverter that can work with different input sources (PV arrays, fuel cells and batteries) and can be used in different applications (grid-tied, off-grid, backup). The broad market for this inverter will ensure a large volume production and thereby a lower cost per watt.

This report focuses on the different requirements of the source and the load, to determine the type of inverter that would meet the above-mentioned objectives. The

report is divided into two sections. The first section analyzes the various available sources and loads to determine the ratings of the inverter. This will ensure the widest possible market for the product in the power range of 2 kW to 10 kW. The second section describes a couple of possible inverter configurations, which could be used to obtain the required goals of a 10-year mean time to first failure (MTFF) and low production costs.

#### **4.1.2. Energy Sources**

Most of the distributed energy sources produce low voltage and high current. Typical voltages of these sources (PV arrays, fuel cells and batteries) for power ratings from 2 to 10 kW are from 12 to 600 Vdc. These types of systems are generally limited to less than 600 volts by the voltage classification of components. Switchgear and other components for DC circuits in excess of 600 V are much more expensive. Fuel Cells, like batteries, consist of stacks of cells, each of which generate a nominal voltage of 0.75 V. The most commonly available fuel cells at power outputs of 7 to 10 kW operate at 48 V nominal, but are capable of generating power in the voltage range of 45 to 90 V [3].

PV arrays also generate power at low voltage, typically at a voltage of 20 to 25 Vdc open circuit. A 24 V, 120 W array can generate power in the voltage range from near 0 to 42 V (the PV array, being a current source, can generate power even at very low voltages). PV arrays are, however, most commonly configured in strings of up to 600 Vdc.

Batteries have a much smaller voltage variation, although for the same required output power it is possible to find batteries with different nominal voltages. Batteries for storage power are also generally configured in strings with voltages up to 600 Vdc being common.

Thus, it can be seen, that from the viewpoint of the source, it is necessary to have a converter which will be able to function efficiently and reliably over a large input voltage range.

#### **4.1.3. Anticipated Inverter Output Configurations**

In order to maximize the market for the DC-AC inverter system, it is necessary that the type output chosen have the greatest potential market in the medium power range. Three different types of outputs are most common – 120 V, 60 Hz single-phase system, 240 V, 60 Hz 3-wire system and three-phase 4-wire system. In the medium power range of 2 to 10 kW, the 240 V, 60 Hz 3-wire system has been found to have a

significant market. Typical applications of such systems are residential buildings (grid-tied and off-grid) and recreational vehicles (RVs).

#### 4.1.4. Proposed Inverter Configuration

From the above section, it can be seen that, in general, the input voltage for the inverter varies between the voltages of 12 V and 600 Vdc, depending on the application. Moreover, the DC sources are extremely non-linear and can generate power in a large voltage range around the nominal voltage, depending on the power drawn by the load. The preferred output for the system is a 240 V, 60 Hz 3-wire system. Thus, the inverter designed should be able to function efficiently for a wide range of input voltages and generate the desired output.

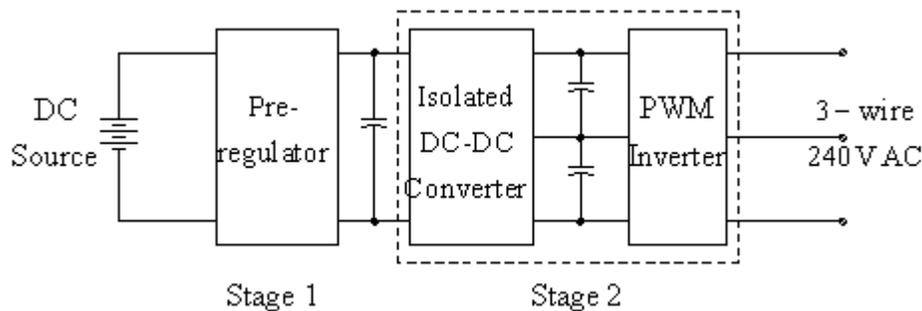


Figure 4.1. Proposed Inverter Configuration

The block diagram of the proposed inverter configuration is shown in Figure 4.1. The first stage of the inverter system is a DC-DC converter, which acts as a pre-regulator to convert the varying DC voltage of the source into a regulated DC voltage. The main task of this converter is not to boost up the voltage of source to the high levels required (as this would cause a lot of switching stresses in the converter), but to provide a reasonable regulation of its output. This stage would be a unique element, whose rating and design would vary based on the type of the source. This, in effect, isolates the rest of the system from the voltage variations of the source, making the design of the rest of the system independent of the type of the source.

The second stage consists of two parts - an isolated DC-DC converter and a pulse width modulation (PWM) inverter. The isolated converter ensures electrical isolation between the source and the load and helps in voltage matching by stepping up the ???DC voltage provided by the pre-regulator to the high levels required by the PWM inverter. It also provides a split DC link at its output, which is required for producing the

3-wire 240 VAC output. The four-switch PWM inverter utilizes the split DC link to produce the required output.

The instantaneous power drawn by the PWM inverter will have a 120 Hz component on the DC side. Since it is desired to draw constant current from the DC source, the instantaneous input power will be a constant. Thus, a storage element (like a capacitor), which is capable of absorbing the 120 Hz ripple in the current, is required within the system.

Two different topologies and control logic can be used for the isolation stage. The first configuration involves using an uncontrolled full bridge phase modulated converter (PMC) to boost up the voltage at the output of the pre-regulator. The PMC can be designed to ensure zero-voltage switching (ZVS) for the four switches under all load conditions without a significant conduction loss penalty. Thus, the switching losses in this stage can be minimized. This converter can thus be designed for very high efficiency operation. In this case, since the isolated converter is uncontrolled, all the 120 Hz ripple current will pass through the converter and thereby have to be absorbed by the capacitor at the output of the pre-regulator.

The second approach is to use a controlled, isolated DC-DC converter. The converter chosen is the six-switch hybrid converter [4], which is capable of achieving ZVS for its six switches under all load conditions. This converter has the added advantages of low filter requirements as compared to the PMC, without any increase in the total VA ratings of the switches or the transformers as compared to the PMC, at the cost of increased number of components. In this case, since the isolated converter is controlled, the 120 Hz ripple current is absorbed by the DC link capacitors, reducing the burden on the pre-regulator stage.

#### **References for 4.1.**

Friedman, Richard, "What the Future Holds for Utilities and Distributed Generation", Utility Automation, Vol. 4.9, November 1999.

Price list of inverters for PV arrays from Trace Engineering.  
( <http://www.traceengineering.com/products/prices.html#sw>)

Schweber, Bill, "Inverter is Key to Fuel-Cell Success", EDN Magazine, July 6, 2000.

R. Ayyanar and N.Mohan, "Full-Load-Range-ZVS Hybrid DC-DC Converter with Two Full-Bridges for High-Power Battery Charging", Proc. International Telecommunications Energy Conference (INTELEC '99), 1999, pp. 20-22.

## **4.2. DC Converter Topology**

This section presents a topology which could be used to convert DC power available from distributed energy sources (like PV arrays and fuel cells) to 60 Hz AC power. The proposed configuration is modular, can be easily configured for single-phase or split single-phase and can be easily paralleled for higher power requirements. A digital signal processing (DSP) controller is proposed which would enable the system to be configured according to the specific requirements of the customer at no additional cost.

### **4.2.1. Converter Features**

Paragraph 4.1 describes the chosen topology, along with the voltage ranges at different parts of the circuit. The voltages are chosen based on the specifications obtained for commercially available PV arrays. The flexibility of the proposed approach in obtaining various output power levels and different types of outputs is also described. This section describes the control structure for the proposed power stage and the modularity of the entire unit.

The features of the proposed topology are:

- **Modular:** By paralleling inverter systems, which are designed for a specific power rating, the system can be configured for output power ratings in the range of 2 to 10 kW. This modular approach would also reduce cost by increasing the volume of production.
- **Flexible:** The system can be easily wired to obtain either single-phase or split single-phase output, utilizing the maximum VA rating of the system.
- **Adaptable:** A smart controller using DSP would allow the controller to adjust to the power rating and the type of output. It would also provide all the protection features required to ensure safe operation of the system.
- **Efficient:** The proposed system has low conduction and switching losses and can thus achieve very high efficiencies.
- **Reliable:** The modular design increases the reliability of the system by providing redundancy.

#### **4.2.1.1. Proposed Inverter Configuration**

The block diagram of the proposed inverter system is shown in Figure four-1. Commercially available PV arrays generally operate at a nominal voltage of 12 Vdc, with a voltage variation window of 10to 16 V. However, at these voltage levels, the output power of the PV arrays is limited to about 100 W [1]. In order to obtain higher output powers, on the order of a couple of kW, many PV arrays have to be connected together.

Connecting twenty such arrays in series would enable a peak output power of 2 kW, and would give a nominal operating DC voltage of 240 V with a voltage variation from 200 to 320 V. Inverter modules rated for 2 kW each could then be used to obtain output power levels in the range of 2 to 10 kW.

### **Maximum Power Tracker**

The first stage is a boost converter, which acts as a maximum power tracker and a voltage regulator (Figure 4.2). The boost converter is controlled to ensure a semi-regulated 450 V DC at its output, which is then used by the isolation stage and the PWM inverter to generate the required AC output. This enables the high frequency isolator and the PWM inverter to be designed for a specified voltage rating and eliminates the need to have multiple ratings based on the type of source. Most of the distributed energy sources also have a limited ripple current capability, so the smooth input current characteristic of the boost converter would be ideally suited for this application.

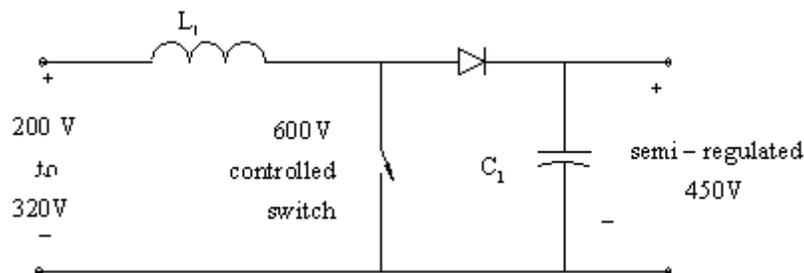


Figure 4.2. Proposed First Stage

The boost converter is also controlled to act as a maximum power tracker to ensure maximum possible power output from the PV arrays at all times. Soft switching in the boost converter would help to reduce the switching losses in the circuit and improve its efficiency [2]. This feature will be discussed in next month's report.

### **High Frequency Isolator**

The high frequency isolator is an uncontrolled full-bridge converter, as shown in Figure 4.3. This stage isolates the PV array from the grid and prevents damage to the PV array due to disturbances on the grid.

The primary side of the converter consists of four switches forming a full bridge configuration, operating at 50 % duty cycle. The switches produce a high-frequency, square-wave voltage waveform across the primary of the transformer. The full-wave diode bridge rectifies the square-wave voltage to produce the DC bus voltage.

Since the four primary side switches are operated at 50 % duty cycle, it is very easy to obtain zero-voltage switching for all four switches from full-load to no-load, by adjusting the magnetizing current of the transformer. Due to the 50 % duty cycle, the magnetizing current will not significantly increase the rms current flowing through the switches (and hence increase the conduction losses) as in the case of the conventional phase modulated converter [3]. Thus, with zero-voltage switching and low conduction losses, the primary side can be operated at high efficiencies.

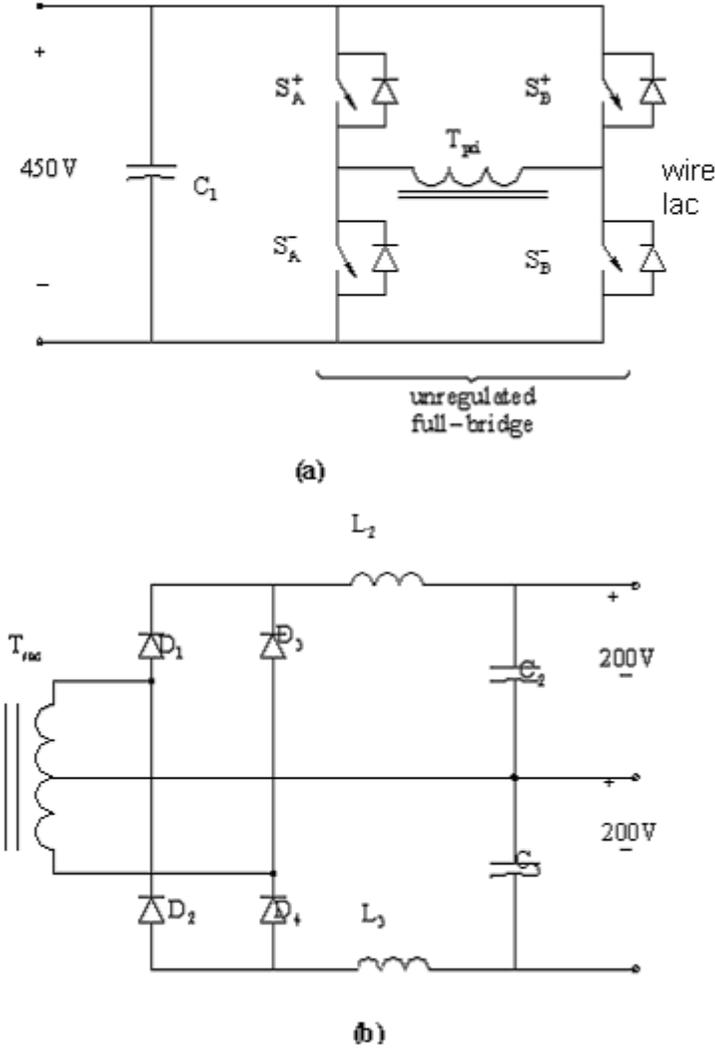


Figure 4.3. Topology of the Isolated DC-DC Converter  
 (a) primary (low-voltage) side, (b) secondary (high-voltage) side

The transformer “T” provides electrical isolation between the source and load. For the input voltage of 450 V, this is a 1:2 transformer with a center tap output. The center tap point is connected to the split capacitor at the output as shown in Figure 4.3(b). This connection is essential to prevent the voltage at the split capacitor from shifting when

the output currents are non-ideal. The split capacitor is also necessary to facilitate the operation of the inverter, since the inverter utilizes the split DC bus to generate the split single-phase AC output desired.

In the case of single-phase or split single-phase loads, the instantaneous output power will have a 120 Hz component. The corresponding 120 Hz component of the load current has to be absorbed in either the input capacitor  $C_1$  or the output capacitors  $C_2$  and  $C_3$ , to prevent the 120 Hz ripple from flowing into the DC source. If this ripple current is absorbed by the input capacitor, then the ripple current will have to flow through the isolated DC-DC converter, increasing the ratings of all the components. Thus, it will be preferable to have the ripple current absorbed by the output capacitors. The inductors  $L_1$  and  $L_2$  in Fig. 3 are used to prevent the 120 Hz ripple in the output current from flowing into the input capacitor  $C_1$ .

### **PWM Inverter**

The topology of the PWM inverter is shown in Figure 4.4. The inverter generates the required single-phase or the split single-phase, 60 Hz AC output utilizing the split DC link.

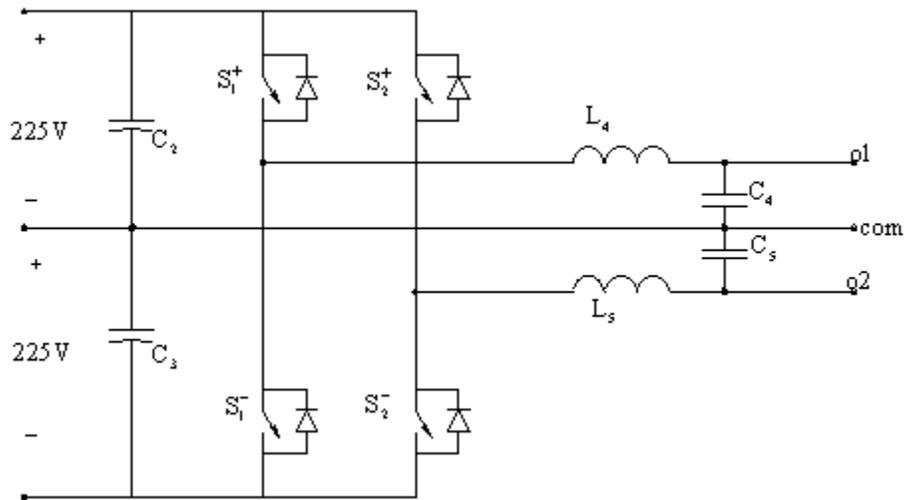


Figure 4.4. Topology of the PWM Inverter

Each inverter leg forms a half bridge inverter that can produce a 60 Hz, 120 VAC (ANSI C84.1) by suitable sinusoidal switch modulation. If these voltages are in phase, the outputs, o1 and o2, can be externally tied together to produce a single 60 Hz, 120 VAC output, utilizing the entire VA rating of the system. On the other hand, if the voltages are 180° out of phase, the outputs would be left unconnected to produce a 120/240

VAC split-phase output, again utilizing the entire VA rating of the system. Thus, this configuration can easily be adapted to give both single-phase and split single-phase outputs with no additional components. A minor change in the control loop would be all the change required, which could be easily implemented using a Digital Signal Processor.

## **CONTROL STRUCTURE**

This section describes the proposed modular configuration of the entire system with its unified DSP controller, which would make the system adaptable for any required VA rating.

A single 2 kW DC-AC inverter system will be designed as previously described. Several of these DC-AC inverter systems could then be interleaved to obtain higher power ratings, in multiples of 2 kW. Interleaving the modules, by phase shifting the switching waveforms appropriately, would help to meet the electromagnetic interference (EMI) requirements with reduced filter size at higher power levels.

The inverter system could be mounted in a cabinet along with a DSP controller motherboard. The cabinet would be built to have expansion slots to parallel the inverter systems to obtain higher power up to a maximum of 10 kW. This flexibility would enable expanding the capability of the inverter easily, when required. Each inverter system would send a single-bit signal to the controller, which would help the controller identify the number of inverter systems being interleaved. The DSP controller, programmed to detect the number of boards in the cabinet, would send the appropriate control signals to each of the inverter systems and would adjust its control algorithm accordingly. The type of the output (single or split phase) can be easily programmed into the DSP controller by means of a DIP switch, whose setting would determine the type of output. The DSP controller would also be programmed to handle all the protection features required by the system to meet the specifications set by IEEE Std. 929.

The modular approach would also increase the reliability of the entire system due to its in-built redundancy. Failure of one module would only decrease the maximum output power capability, but would not interrupt the operation of the system.

Thus, the proposed configuration would result in a very adaptable inverter system, which would maximize the market for the system.

## **References for 4.2.**

PV Components Database (<http://www.nmrc.ie/projects/remspv/pvcomp.html#modules>)

Jim Noon, "Analysis and Design of a 250 kHz, 500 W Power Factor Correction Circuit Employing Zero Voltage Transitions", High Frequency Power Conversion Conference, 1995.

R. Ayyanar, "A Novel Class of Hybrid, Soft-Switching DC-DC Converters with High-Power Density, High-Efficiency, and Low EMI", Ph.D. Thesis, University of Minnesota, June 2000.

### **4.3. A Detailed Description of the Power Stage**

This section presents a detailed description of the power stage of the proposed DC-AC inverter system. The analytical design of the power stage is carried out and the results are presented. The report details the various components chosen for the system, specifically the semiconductor devices. A breakdown of the losses in the system and the efficiencies of the individual stages of the system are tabulated. The system designed is capable of achieving an overall efficiency of 90 %.

The proposed topology is described –vis-à-vis the PWM inverter, the high frequency isolator and the maximum power tracker – individually. The final part of the report summarizes the performance characteristics of the system and the future tasks that have to be carried out.

Each part of the report, dealing with the individual stages of the system, describes the following details:

- The values and ratings of the inductors and capacitors used for filtering.
- The ratings of the semiconductor switches.
- Commercially available devices meeting the required switch ratings. (The parameters of these devices are used for computing losses in the system.)
- Breakdown of losses in the stage under consideration.

This report gives the general principles followed in the design procedure, but does not detail all the aspects of the design. The complete design, with all the relevant equations, will be presented in the final report at the end of the project.

#### **4.3.1. Design of the Power Stage**

The power stage configuration of the proposed DC-AC inverter system is shown in Figure 4.1. The ratings (of a single unit) are decided based on the voltage and power levels of commercially available photovoltaic (PV) arrays.

Connecting 20 twelve-volt PV arrays in series would result in a DC source voltage of 200 to 320 V and enable a peak output power of 2 kW. The relatively high voltages in the system would result in currents of the order of 10 A throughout the circuit. The low current values would reduce the cost of the entire system by reducing copper costs as compared to low voltage, high current systems.

Thus, the ratings of the system chosen for the purpose of design are:

<i>Input Voltage</i>	: 200Vdc–320Vdc nominal voltage = 240Vdc
<i>Output Voltage (rms)</i>	: 110 / 220V, 60Hz split – single – phase
<i>Output Power (<math>S_{output}</math>)</i>	: 2.5 kVA, 1.25kVA per phase
<i>Maximum Output current</i>	: 25 A

#### 4.3.2. PWM Inverter Design

The circuit diagram of the PWM inverter is shown in Figure 4.5. The nominal output current  $I_o$  is

$$I_o (rms) = \frac{S_{output}}{V_{o,rms}} = 11.36 A , \quad (1)$$

$$\hat{I}_o (peak) = \sqrt{2} I_{rms} \approx 16 A .$$

For the purpose of choosing the semiconductor devices, the peak output current is limited to 25 A.

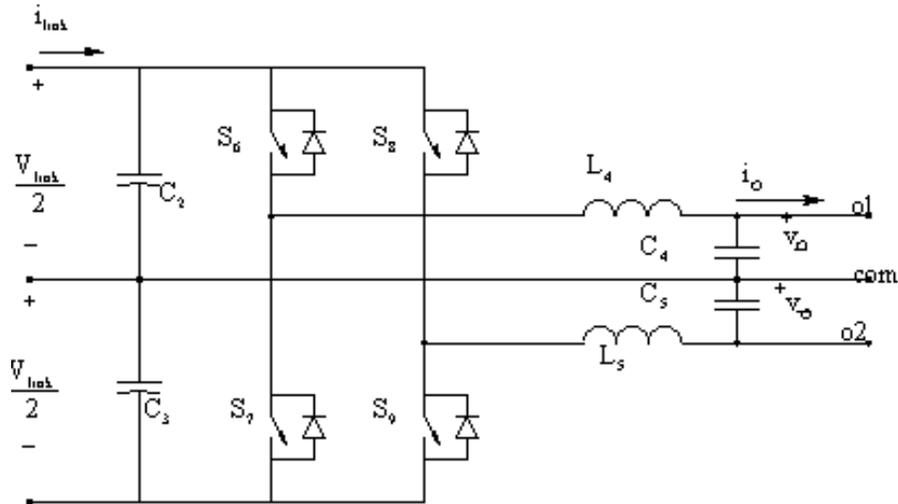


Figure 4.5. Circuit Topology of the PWM Inverter

### 4.3.3. Output Filter Design

Assuming a constant output voltage during a switching cycle (switching frequency  $f_s = 25\text{kHz}$ ), the worst-case peak-to-peak ripple current in the inductor can be expressed as,

$$\Delta i_{p-p, \text{worst case}} = \frac{I}{2} \left( \frac{V_{\text{link}}}{2L f_s} \right). \quad (2)$$

Assuming a peak current ripple equal to 10% of the maximum nominal output current,

$$\Delta i_{p-p, \text{worst case}} = \frac{I}{2} \left( \frac{450}{2 \times L \times 25,000} \right) = 1.6 \text{ A} \quad (3)$$

$$\Rightarrow L = 2.82 \text{ mH} .$$

The voltage ripple across the output capacitor, caused by the inductor ripple current can be expressed as,

$$\Delta v_{p-p} = \frac{I}{C} \int_{\frac{T_s}{4}}^{\frac{3T_s}{4}} i_{L,ripple} dt . \quad (4)$$

Choosing an output voltage ripple equal to 1 % of the maximum output voltage,

$$\Delta v_{p-p} = \frac{I}{2C} \left( \frac{\Delta i_L}{2f_s} \right) = 3.11 V \quad \Rightarrow C = 0.26 \mu F . \quad (5)$$

Splitting the output filter between the two phases,

$$\begin{aligned} L_4 = L_5 &= 2.82 mH, 20 A @ 60 Hz \\ C_4 = C_5 &= 0.52 \mu F, 220 VAC . \end{aligned} \quad (6)$$

#### 4.3.4. Switch Ratings

The maximum voltage across any switch of the PWM inverter is 450 V and the rms current through it is approximately 10 A. A 600 V, 44 A switch is chosen so that:

- It can withstand voltage spikes due to stray inductances.
- It can carry the peak output current after being derated for the increased temperature of operation.
- MOSFETs are found to be better than IGBTs for the present application, since the large turn-off times of the IGBTs would increase the switching losses at the chosen frequency of operation. The MOSFET chosen is IXFX44N60 from IXYS, which has a continuous current rating of 30 A at 100° C.

The total conduction and switching power loss in the switches, using the parameters of the chosen MOSFET is

$$P_{loss,switches} = \underbrace{52W}_{conduction\ losses} + \underbrace{22W}_{switching\ losses} = 74W .$$

#### 4.3.5. High Frequency Isolator Design

The circuit diagram of the high frequency inverter is shown in Figure 4.6.

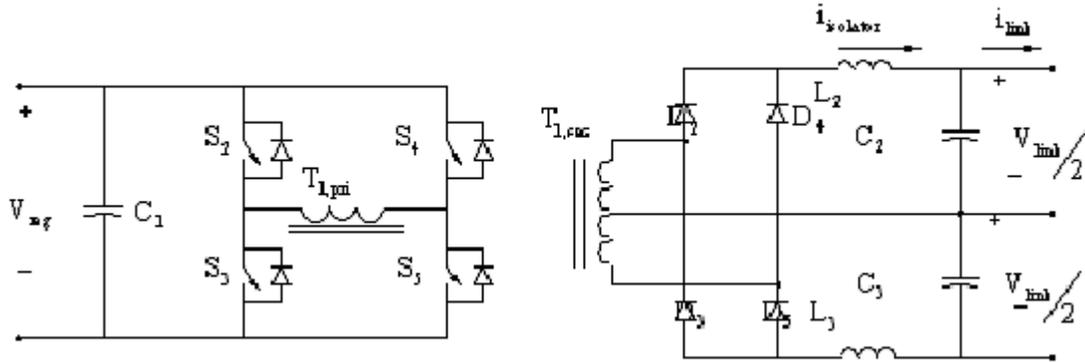


Figure 4.6. Circuit Topology of the High Frequency Inverter

#### 4.3.5.1. Output Filter of the Isolator

The output filter of the isolator serves two purposes: The filter capacitors  $C_2$  and  $C_3$  absorb the switching frequency ripple from the PWM inverter. The inductor ( $L_2, L_3$ )-capacitor ( $C_2, C_3$ ) combination prevents the 120 Hz ripple in the dc-link current from flowing into the isolator.

To achieve the above objectives,  $C_2$  and  $C_3$  are chosen much larger than  $C_1$ . In this case, the 120 Hz ripple current dominates the choice of the filter components. The equivalent circuit of the isolator for the lower frequency components of the dc-link current (DC and 120 Hz components) is shown in Figure 4.7. In this case, since the half-bridge converter operates at 50 % duty cycle, without any closed loop control, the input capacitor  $C_1$  is reflected to the secondary side of the transformer.

Assuming a constant DC link voltage of 450 V and a loss-less inverter, the dc-link current can be obtained by equating the instantaneous input and output powers of the inverter as follows:

$$P_o = (\hat{V}_o \sin((2\pi \times 60)t)) (\hat{I}_o \sin((2\pi \times 60)t)) = V_{link} i_{link} \quad (8)$$

Substituting the values for the output voltage, output current and the dc-link voltage, the dc-link current can be obtained from Eq. (8) as

$$i_{link} = 5.86 (1 - \cos((2\pi \times 120)t)) \quad (9)$$

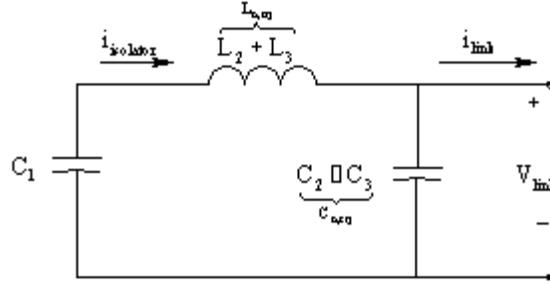


Figure 4.7. Low Frequency Equivalent Circuit of the Isolator

The filter is designed to allow 1 % of the 120 Hz ripple into the isolator. From Fig. 4, the transfer function of the system can be written as

$$\frac{i_{isolator}}{i_{link}} = \frac{I}{I + \frac{C_{o,eq}}{C_1} + s^2 L_{o,eq} C_{o,eq}} \quad (10)$$

The output capacitor selection is dominated by the required 120 Hz ripple current capability. A 315 V, 680  $\mu F$  electrolytic capacitor has a 1.7 A 120 Hz ripple current capability [1]. A parallel combination of three capacitors, in each half of the DC link, will give a 5.1 A ripple current capability, which is about the required current rating of 4.2 A.

Thus, the total capacitor value is

$$C_{o,eq} = \frac{3C}{2} = \frac{3 \times 680 \mu F}{2} = 1020 \mu F \quad (11)$$

It will be shown in the next section that  $C_1 = 16 \mu F$ .

With  $C_{o,eq} = 1020 \mu F$ ,  $C_1 = 16 \mu F$ , a nominal inductance  $L_{o,eq} = 1 \mu H$  will give the required 1 % division in the 120 Hz ripple component of the dc-link current.

#### 4.3.5.2. Switch and Diode Ratings

From Eq. (9), the average dc current flowing out of the isolator is about 5 A. Thus, at 50 % duty cycle the rms currents through the switch and diodes are 3.8 A (the currents in the switches and diodes are identical since the transformer is 1:1).

Six hundred (600) V, 15 A devices are chosen for the switches and diodes (the current rating is chosen higher than required to compensate for the derating due to the high temperature of operation). The specific devices chosen are

Diode: 15ETH06S from IRF

Switch: IXFH15N60 from IXYS (MOSFET)

#### 4.3.5.3. Zero-Voltage Switching (ZVS) of the MOSFETs

The chosen frequency of operation is  $f_s = 100kHz$ . The high frequency of operation reduces the size of the transformer and thus improves the power density.

ZVS for the primary side, for the full load range, can easily be achieved by introducing a 548.8  $\mu H$  magnetizing inductance in the high frequency transformer and 1 nF capacitors across the switches (the 1 nF capacitors minimize the losses across the switches during turn-off).

This magnetizing inductance increases the rms current through the switches by about 0.5 A from 3.5 A to 4 A. Thus, ZVS can be achieved up to no load with only a marginal increase in conduction losses.

The total power loss in the semiconductor devices (MOSFETs and diodes combined) is

$$P_{loss} = \underbrace{32W}_{MOSFET\ cond.\ losses} + \underbrace{2W}_{MOSFET\ switch.\ losses} + \underbrace{21W}_{diode\ cond.\ losses} + \underbrace{27W}_{diode\ switch.\ losses} = 82W \quad (12)$$

The transformer consists of 40 turns of 520/42 Litz wire for each winding, wound on a 46016-EC core. The total power loss in the transformer is

$$P_{loss} = \underbrace{3.5W}_{core\ loss} + \underbrace{3.5W}_{copper\ loss} = 7W \quad (13)$$

Thus, the total power loss in the isolator is 89 W.

#### 4.3.6. Voltage Regulator Design

The circuit diagram of the voltage regulator (and maximum power point tracker) is shown in Figure 4.8. The converter shown is the standard boost converter with additional components to achieve zero-voltage switching [2].

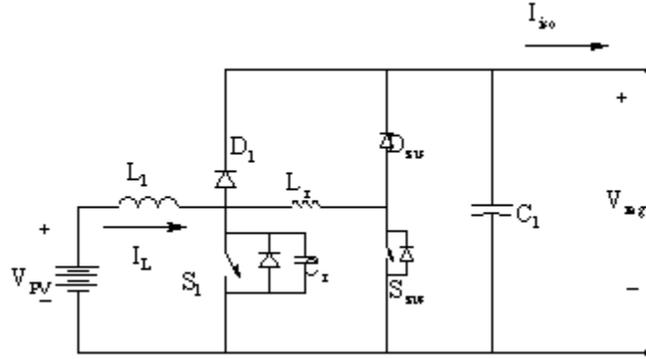


Figure 4.8. Circuit Topology of the Zero Voltage-Switched Boost

The average input current  $I_L$  varies between 7 A and 11.25 A for the given input voltage variation and output power rating (assuming an overall efficiency of 90 %). The variation in the duty cycle (D) required to maintain a constant output voltage is between 0.29 and 0.56.

### Design of the Filter Components

Assuming the above stated limits for the average inductor current and the duty cycle, the worst case ripple in the inductor current occurs at  $D = 0.5$  and is given by

$$\Delta i_L = \frac{V_{reg} (1-D) D}{L_1 f_s} \quad (14)$$

For a switching frequency of 50 kHz, a regulated output voltage of 450 V and a worst case input current ripple of 5 % (of the maximum average input current),

$$L_1 = 4mH \quad (15)$$

The worst case output voltage ripple occurs at  $D = 0.6$  and is given by

$$\Delta v_{p-p} = \frac{I_{iso} (1-D) T_s}{C_1} \quad (17)$$

For a worst case voltage ripple of 4.5 V (1 % of the output voltage), the required capacitance value is

$$C_1 = 16\mu F \quad (18)$$

### Switch Ratings

The maximum rms current through the switch ( $S_1$ ) is 8.5 A and the maximum rms current through the diode ( $D_1$ ) is 8 A. The voltage ratings of both these devices have to be at least 600 V (to have a sufficient safety margin). The components chosen are

$S_1$ : IXFT26N60Q from IXYS (600 V, 26 A MOSFET)

$D_1$ : 30ETH06S from IRF (600 V, 30 A diode)

### 4.3.7. ZVS of the MOSFET

Zero voltage turn-on of the main switch is achieved by resonating the capacitor  $C_{r,l}$  across the switch with the inductance  $L_r$ . Capacitor  $C_r$  is chosen to reduce the switching loss during turn-off by limiting the rate of rise of voltage across the switch. During turn-on, the auxiliary switch  $S_{zvs}$  is turned on first. The resonant inductor ( $L_r$ ) current ramps up and provides zero current switching for the main diode  $D_l$ . Once the main diode has turned off,  $L_r$  and  $C_r$  resonate to reduce the voltage across the main switch  $S_l$  to zero, at which point the main switch can be turned on, providing zero voltage switching for the diode. The zero switching losses come at the cost of conduction and switching losses in the auxiliary switch, but the overall efficiency of the system is improved significantly as compared to the hard switched converter.  $C_r$  is chosen to be 680 pF, which would reduce the turn-off losses to 0.5 W. A resonant inductor value of 2  $\mu$ H ensures a total blanking time of 125 ns. The rms current through the auxiliary switch is very small, but the device must be chosen based on its high peak pulsed current rating and small turn-off time. The devices chosen for the auxiliary switch and diode are:

$S_{zvs}$  : IRFBC40S/L from IRF (MOSFET)

$D_{zvs}$  : 15ETH06S from IRF

The total losses in the system, using these components are

$$P_{loss} = \underbrace{0.5W}_{\text{turn-off loss in } S_l} + \underbrace{4W}_{\text{loss in } S_{zvs}} + \underbrace{18W}_{\text{conduction loss in } S_l} + \underbrace{10W}_{\text{conduction loss in } D_l} = 32.5W \quad (19)$$

which is a 30 % reduction in losses as compared to the hard-switched converter.

### 4.3.8. Power Stage Design Conclusions

The design of the power stage of the proposed DC-AC inverter system has been described. Appropriate semiconductor devices have been chosen to meet the required ratings and the efficiencies of the individual stages have been computed. The system is found to achieve an overall efficiency of 90 %. The breakdown of losses in the system is summarized in Table 1.

Table 1. Split-Up of Losses in the System

	Switching losses	Conduction losses	Total Losses	% losses
Voltage Regulator	4.5 W	28 W	32.5 W	1.65 %
High Frequency Isolator	29 W	60 W	89.0 W	4.45 %
PWM Inverter	22 W	52 W	74.0 W	3.70 %
<b>Total Losses for the System</b> (except inductor losses, capacitor losses and control circuit losses)			<b>195.5 W</b>	
<b>Efficiency</b>			<b>90 %</b>	

The above design demonstrates that an overall efficiency of 90 % is achievable with the proposed topology, using off-the-shelf parts. The efficiency could be further improved by choosing better components.

### References for 4.3.

Cornell-Dubilier Catalog ([www.cornell-dubilier.com](http://www.cornell-dubilier.com))

Jim Noon, "Analysis and Design of a 250 kHz, 500 W Power Factor Correction Circuit Employing Zero Voltage Transitions", High Frequency Power Conversion Conference, 1995.

### 4.4. Simulation Results

This report presents the simulation results for the individual stages of the proposed DC-AC inverter system. The three stages are simulated individually in SABER™ to demonstrate the operation of the stages and to verify the analytical design described in the March report. Waveforms obtained from the simulation are presented and the results are discussed.

The three stages of the power system are simulated individually in open loop configuration. Each part of the report, dealing with the individual stages of the system, describes the following details:

- Circuit diagram as implemented in SABER
- Waveforms obtained from the simulation
- Comparison of the simulation results to the prediction from the analytical design

### 4.4.1. Voltage Regulator

Figure 4.9 shows the circuit diagram of the boost converter, which is being used as a voltage regulator and a maximum power point tracker. The values used in the simulation are identical to the values obtained in the analytical design. The switch and diode models used emulate the chosen semiconductor devices as far as their characteristics are concerned ( $r_{ds,on}$ ,  $t_{on}$ ,  $t_{off}$  and  $v_{on}$ ). The logic clocks provide the appropriate switching patterns to the main and auxiliary switches. The 0.1 nH inductor in series with the main diode is used to overcome convergence problems during simulations.

The simulation was carried out at three input voltage levels – 200 V (minimum input voltage), 240 V (nominal input voltage) and 320 V (maximum input voltage). The duty ratio was manually adjusted to obtain 450 V at the output. Figure 4.10 shows the input current and output voltage waveforms at the three input voltage levels.

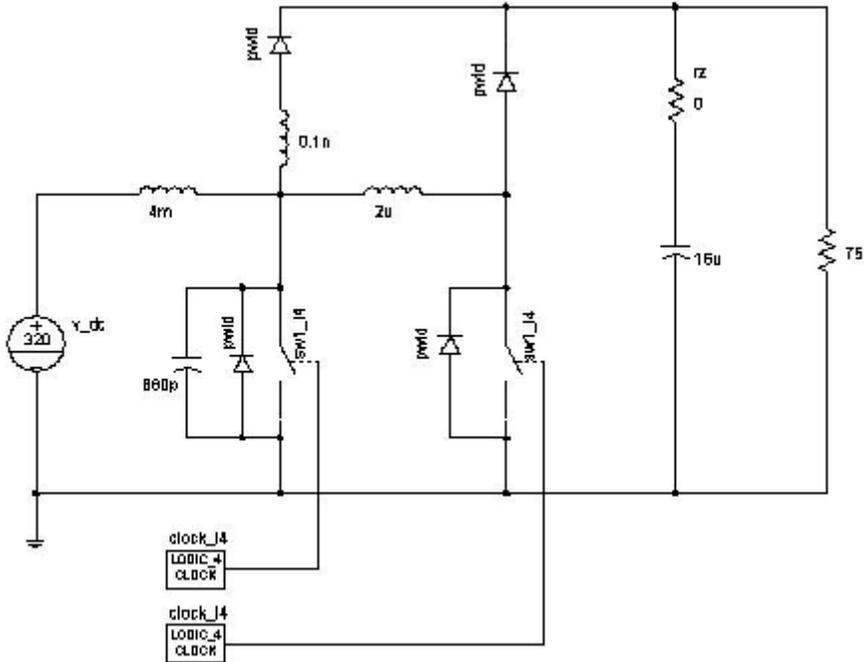


Figure 4.9. SABER Implementation of the Boost Converter

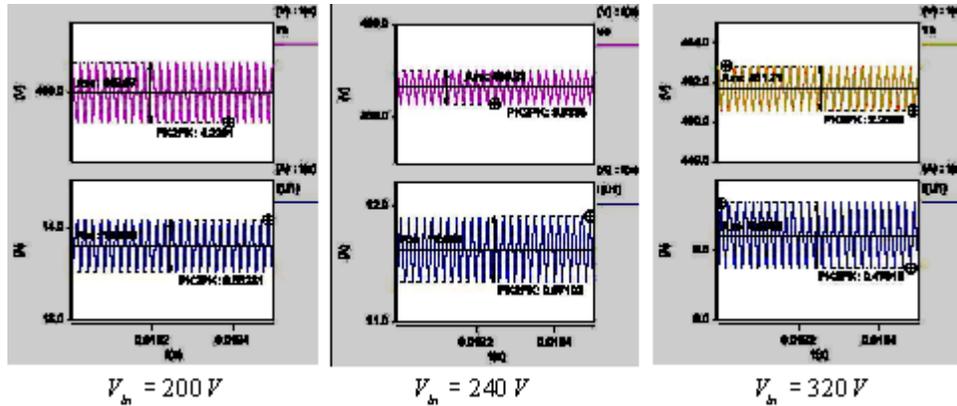


Figure 4.10. Input Current and Output Voltage Waveforms for the Boost Converter

As can be seen, the worst case input current ripple is about 0.57 A and the worst case output voltage ripple is about 4.3 V, both of which are within the required tolerances.

#### 4.4.2. ZVS Operation

For the circuit of Figure 4.9, the zero voltage turn-on of the main switch (sw1\_I4) depends on the output current and is independent of the input voltage. Hence the ZVS operation was tested at the nominal input voltage and three values of output current – full load, half-load and 10 % load. Figure 4.11 shows the drain-source voltage and the gate-source voltage for the three cases considered. The circuit is found to achieve ZVS under all load conditions.

The resonant circuit waveforms ( $i_{aux\_switch}$ ,  $i_{Lr}$  and  $i_{aux\_diode}$ ) are plotted in Figure 4.12. The rms values of these waveforms are computed in SABER and are shown in Figure 4.13. The auxiliary components are found to have high peak currents but very small rms currents.

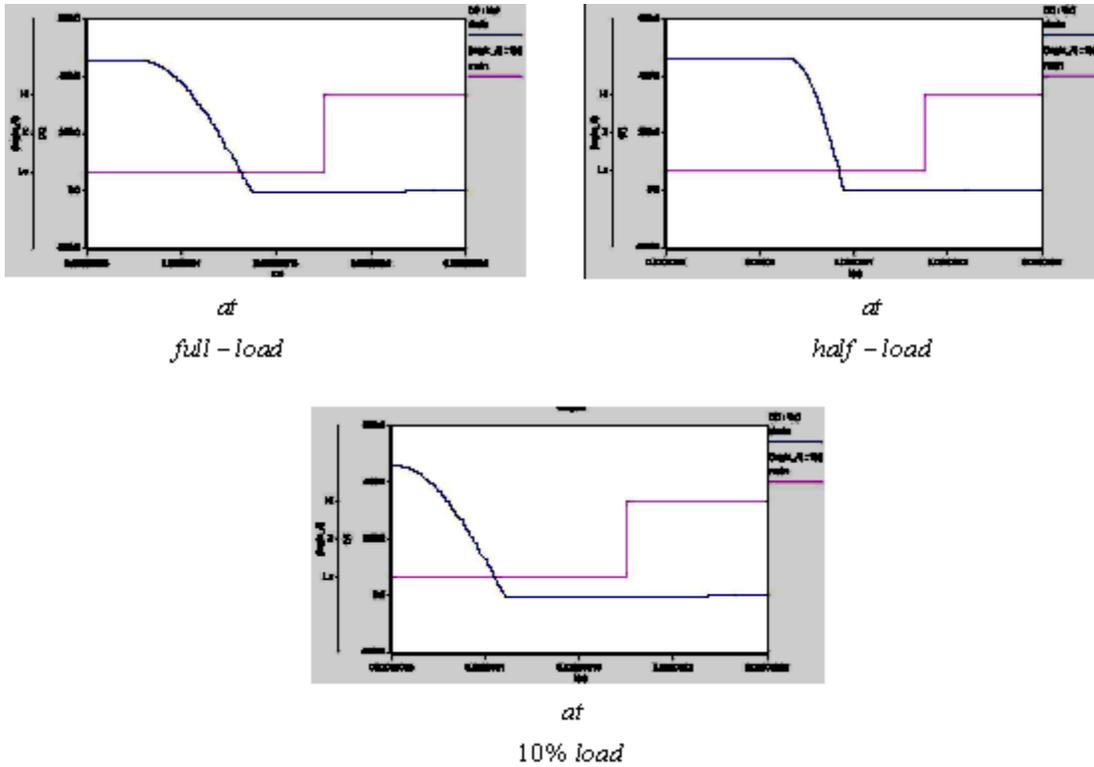


Figure 4.11. ZVS Operation at Different Load Currents

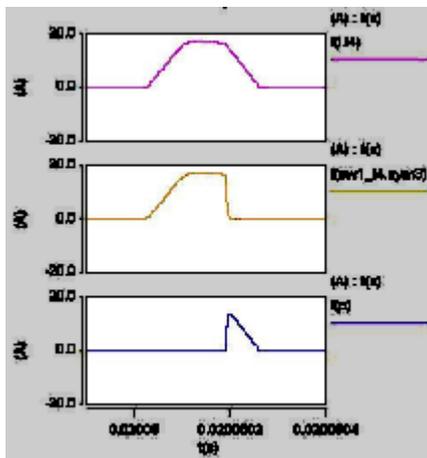


Figure 4.12. Resonant Circuit (left)

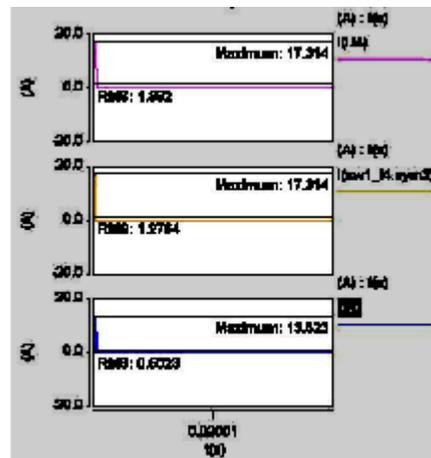


Figure 4.13. Resonant Circuit Current Measurements (right)

#### 4.4.3. High Frequency Isolator

The circuit diagram of the high frequency isolator as implemented in SABER is shown in Figure 4.14.

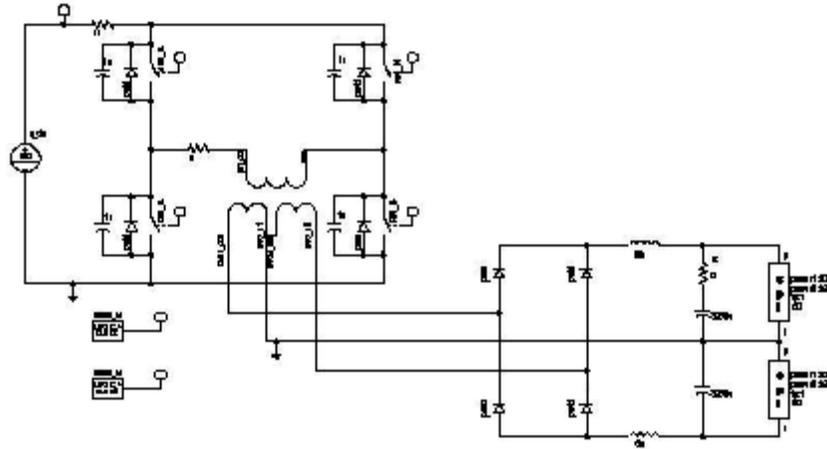


Figure 4.14. SABER Implementation of the High Frequency

The input to the isolator stage would be the output voltage of the voltage regulator, which provides a regulated 450 V. Thus, the input is represented by a 450 V voltage source. The switches are modeled (as in the case of the voltage regulator) using the values given in their data sheets.

The transformer is modeled using ( $R_{core}$ ) g circuit elements as shown in Figure 4.15. The core losses are modeled as a resistor and the magnetizing current is obtained by the magnetizing inductance  $L_m$ . The copper losses and the leakage fluxes are represented on the secondary side. The values for the resistances are chosen based on the loss computation presented in the March report. The leakage inductance is chosen based on a 2 % reactance drop in the transformer.

It is found in the simulation that the previously computed value of the output inductor is not sufficient to filter the 120 Hz ripple component of the output current, since a small voltage ripple at the output capacitor causes a large current ripple in the inductor. Hence the output filter inductor and capacitor values were changed to 6 mH and 3236  $\mu$ F respectively.

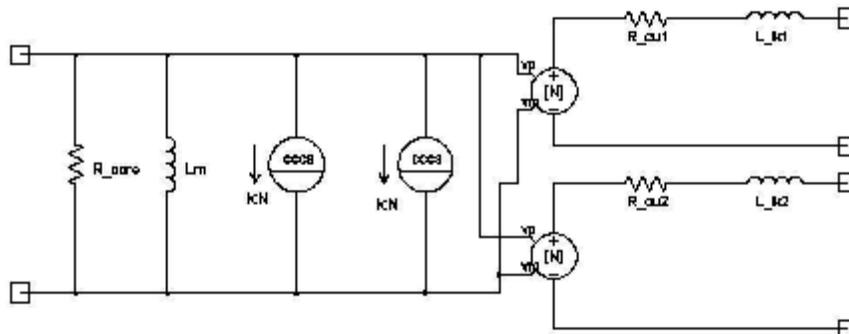


Figure 4.15. Transformer Model Used in Simulation

The output load is represented as a power source which draws an average power  $P_o$  and an instantaneous power in the form  $P_o + P_o \sin(2\omega t)$ , where  $\omega = 2\pi(60)$ . This is the load model chosen since it represents the power drawn by a controlled PWM inverter.

Figure 4.15 shows the output voltage and inductor current waveforms at full load. The inductor current is found to have a 10 % 120 Hz ripple and the voltage a 1 % 120 Hz ripple. The voltage also decreased from the designed value of 225 V to 220 V because of the 2 % leakage inductance in the circuit. However, since 220 V is sufficient to generate the required 110 V rms AC voltage, the turns ratio of the transformer need not be adjusted.

Figure 4.16 shows the drain-source and gate-source voltages across both the left-leg and right-leg MOSFETs. In both cases, the gate pulse is applied after the drain-source voltage drops to zero, indicating zero-voltage turn-on.

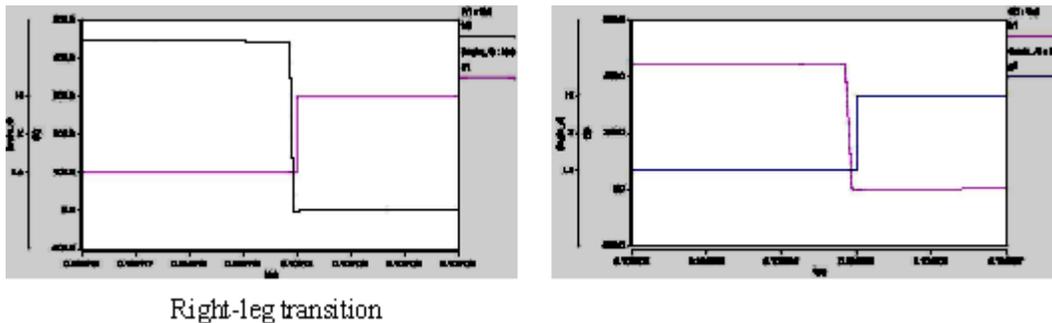


Figure 4.16. Zero-voltage Turn-on of the MOSFETs

Figure 4.17 shows the transformer primary current and its measured rms value. The increase in the rms value of the current due to the presence of the magnetizing inductance is found to be about 0.5 A.

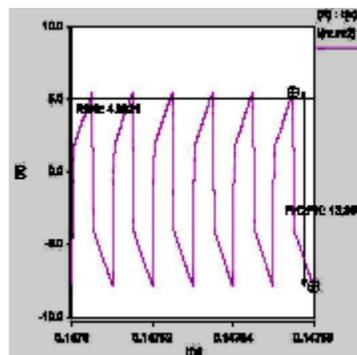


Figure 4.17. Primary Current of the Transformer

#### 4.4.4. PWM Inverter

The circuit diagram of the PWM inverter is shown in Figure 4.18.

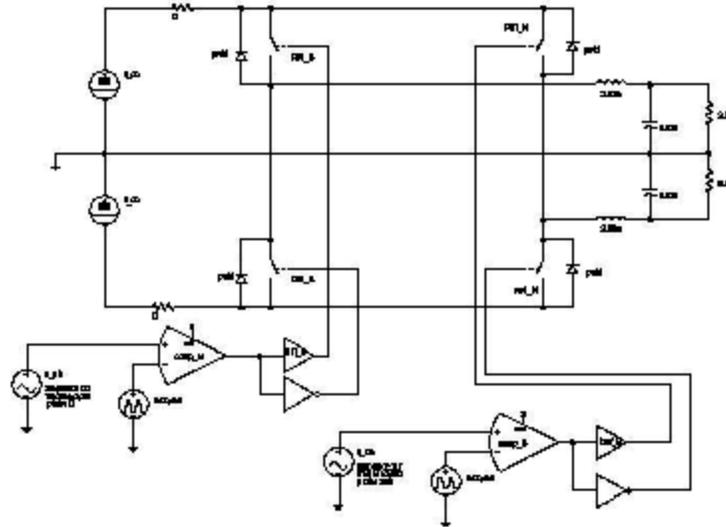


Figure 4.18. SABER Implementation of the PWM Inverter

The 1 %, 120 Hz ripple is ignored for now as the closed loop control system of the inverter would take care of any variations in the DC bus. Thus, the source of the inverter is modeled as two 225 V voltage sources. Since the two legs of the inverter are independent of each other, the MOSFETs are driven from two different sources. The reference sine waves are phase shifted by  $180^\circ$  to generate the split single-phase output required. Figure 4.19 shows the output voltage and inductor currents for both legs of the inverter. The two output voltages are found to be out of phase as expected.

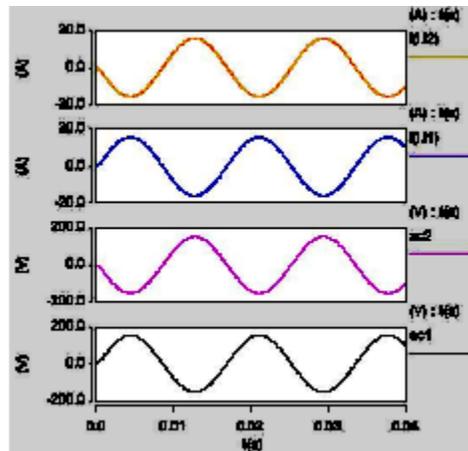


Figure 4.19. Output Voltage and Inductor Currents of the PWM Inverter

Figures 4.20 and 4.21 show the output voltage and inductor current ripples respectively. The ripple values are found to match the values computed from the analysis of the inverter.

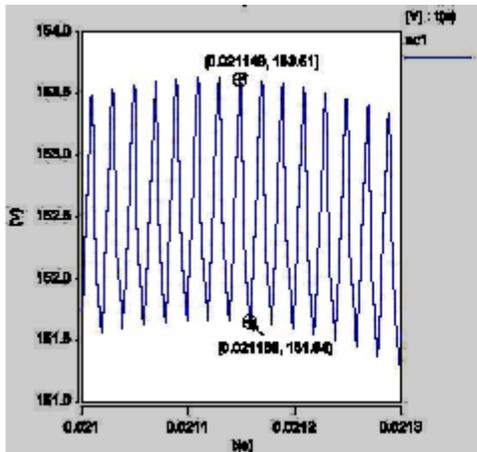


Figure 4.20. Output Voltage Ripple (left)

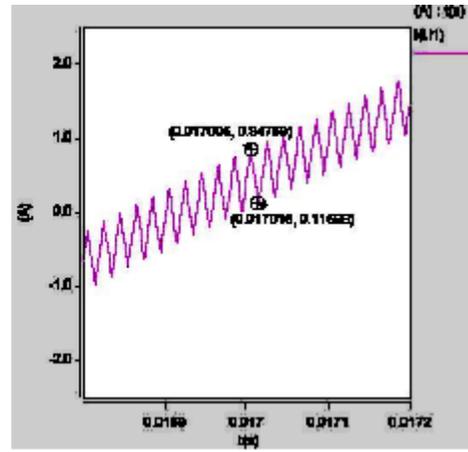


Figure 4.21. Inductor Current Ripple (right)

#### 4.4.5. Simulation Conclusions

The analytical design of the DC-AC inverter system is found to operate as expected. Barring the change in the output filter of the high frequency isolator, the analytical design produced the required results.

This report describes the design of the closed loop controller for utility interactive applications. The simulation results for the controller are presented. The maximum power point tracking algorithm is also developed and tested by simulation. Both the controllers are found to work satisfactorily under varying conditions.

#### 4.5. PWM Controllers

This report describes the design of the controllers for the PWM inverter stage of the proposed system for grid-tied applications and presents simulation results verifying the performance of the controller.

The report is divided into three parts. The first part of the report discusses the structure of the control system for utility interactive applications. The second part of the report presents the current control loop required to inject power into the grid at unity power

factor. The final part of the report describes the maximum power point tracking algorithm and its implementation.

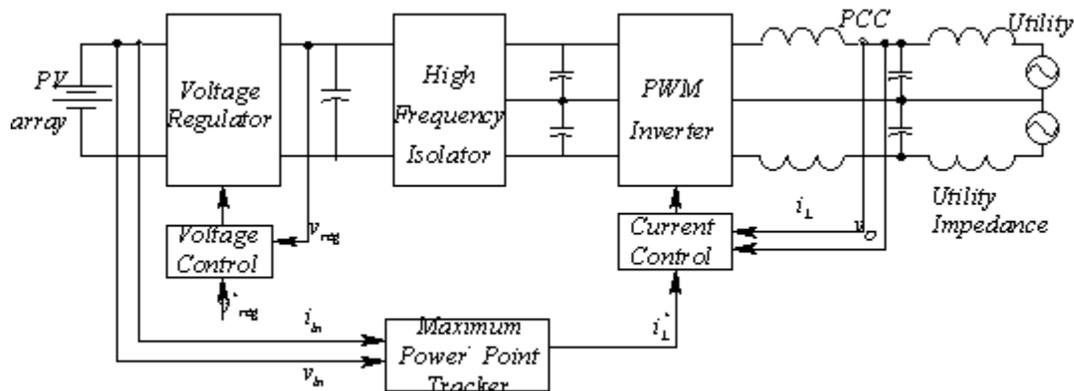


Figure 4.22. Basic Structure of the Utility Interactive System

This report discusses power injection into the grid at unity power factor only. The reactive power capability of the system and injection of reactive power into the grid to stabilize the bus voltage will be discussed in the next month's report.

#### 4.5.1. Structure of the Utility Interactive System

The basic structure of the utility interactive system, with the main control loops is shown in Figure 4.22. The system consists of three closed loops – two inner loops and one outer loops. The voltage regulator has an output voltage control loop, which regulates its output voltage irrespective of the input voltage variations. The design of this loop was discussed in the May report. Since the proposed system has independent control loops for the regulator and the PWM inverter, this loop need not be changed for utility interactive applications.

The control loop for the PWM inverter is modified, by removing the output voltage regulation and synchronizing to the utility, to inject the required power into the grid. Since the output voltage of the PWM inverter is already set by the utility, the inverter is current controlled to ensure power injection into the grid. The control loop is similar to the one discussed in the May report. The loop consists of an inductor current feedback loop, with an output voltage feedforward. The voltage at the Point of Common Coupling (PCC; the point where the load would be connected in parallel to the two sources), is measured and the current reference waveshape is derived from it. This ensures that the inverter is always synchronized to the grid. Since the two legs of the PWM inverter are controlled independently, the system can also handle an unbalance in the utility. In this case, each leg of the inverter would be synchronized to the voltage at its output, independent of the other phase.

The magnitude of the current reference to the PWM inverter is derived from the maximum power point tracker. Since the power drawn from the PV array is equal to the load power plus losses in the system, injecting more current into the grid would draw more power from the array. Thus, by measuring the power drawn from the array and adjusting the PWM inverter current reference, the maximum power point tracker ensures that the array is always supplying the maximum possible power at all times. This loop would be implemented using a DSP.

#### 4.5.2. Current Loop Design for the PWM Inverter

Figure 4.23 shows the block diagram representation of the current loop of the PWM inverter.

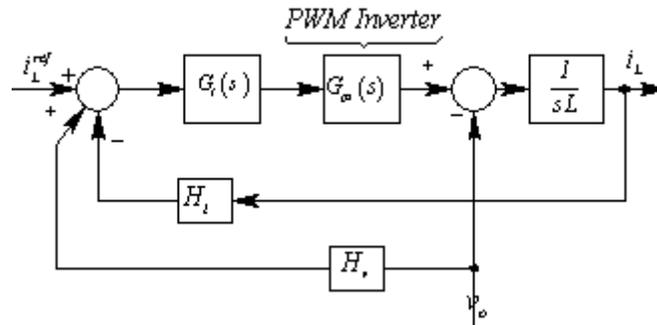


Figure 4.23. Block Diagram of the Current Loop Controller

The use of a feed forward controller to eliminate the effect of the output voltage on the output current would simplify the control loop design for the PWM inverter. The transfer function of the system shown above is

$$i_L \left( 1 + \frac{H_i G_i G_{ps}}{sL} \right) = i_L^{ref} \frac{G_i G_{ps}}{sL} + v_o \left( \frac{H_v G_i G_{ps}}{sL} - \frac{I}{sL} \right). \quad (1)$$

From (1), it can be seen that by properly choosing the feedforward transfer function  $H_v$ , it is possible to eliminate the effect of the output voltage on the inductor current, because the coefficient of  $v_o$  in (1) can be eliminated. Thus, choosing

$$H_v(s) = \frac{I}{G_i G_{ps}}, \quad (2)$$

the output voltage transfer function reduces to

$$\frac{i_L}{i_L^{ref}} = \frac{1/H_i}{1 + \frac{sL}{H_i G_i G_{ps}}} \quad (3)$$

The power stage transfer function  $G_{ps}$  can be considered to be a pure gain, since the response time of the power electronic circuitry is much smaller than the response time of the output LC filter. Eqn. 3 indicates that choosing simple gains for the voltage and the current controllers would be sufficient to achieve the required performance. The feedback gain  $H_i$  gives the flexibility of being able to choose both the location of the pole and the gain. Choosing pure gains for the transfer functions ensures that the feedforward transfer function is also a pure gain.

Choosing a bandwidth of 2.5kHz for the output current loop (a crossover frequency of  $f_s / 10$ ) and a condition that the low frequency closed loop gain of the system is 1 gives

$$\begin{aligned} G_i &= 0.4027 \\ H_i &= 1 \\ H_v &= 0.0226 \end{aligned} \quad (4)$$

## Synchronizing to the Voltage Grid

The reference to this current loop is a sinusoidal voltage that is synchronized to the grid and has the required magnitude. In order to generate a sine wave synchronized to the grid, a phase-locked-loop (PLL) is used which generates a sine wave synchronized to the grid and leading the grid voltage by 90°. Since the PLL incorporates a low pass filter within it, it ensures that high frequency switching noise present in the measured voltage signal does not pass through to the controller.

This sine wave is then multiplied by the required amplitude signal (obtained from the maximum power point tracker) and is used as the reference to the current loop of the PWM inverter.

## Simulation Results

Figure 4.24 shows the SABER schematic of the averaged system model used to test the current controller. The amplitude of the reference current is changed from 10A to 5A at 0.2s. The current is injected at unity power factor. Figure 4.25 shows the injected current and voltage at the PCC. The injected current is found to follow the reference at all times.

Thus, the simple feed forward control of Figure 4.23, with pure gains for the controllers is able to achieve the required response characteristics for the current loop of the PWM inverter.

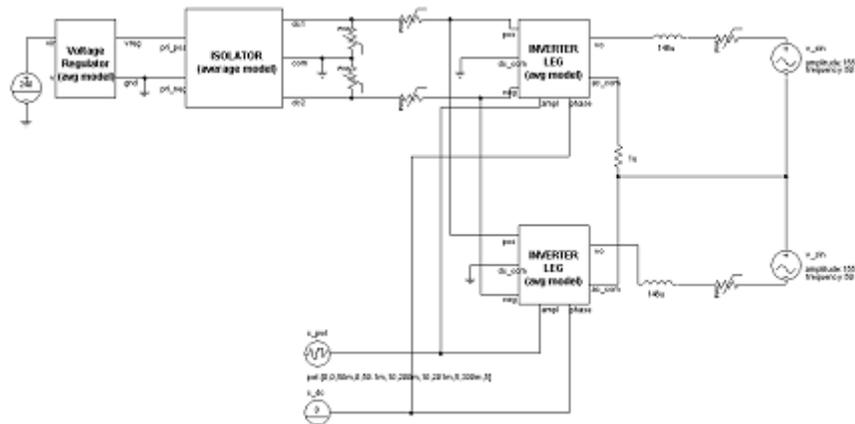


Figure 4.24. Average Model of the System Used for Testing the Current Loop

### 4.5.3. Maximum Power Point Tracker

The V-I characteristics of a solar cell have non-linear characteristics. Maximum power can be drawn from the cell at only one operating condition. The duty of the maximum power point tracker (MPPT) is to determine the maximum power point and to operate the solar array close to that point at all times.

A typical V-I characteristic for a 2.2kW solar call is shown in Figure 4.26. Figure 4.27 plots the output power of the solar array as a function of the current drawn from the array. For the characteristics shown, the maximum power output occurs at an input voltage of about 250V and an input current of about 8.8A.

There are generally two types of maximum power point tracking algorithms [1].

- Perturbation and observation method
- Incremental conduction method

In the perturbation and observation method, the current drawn from the solar array is perturbed and the power change is observed. If the perturbation results in an increase in power, the subsequent perturbation is made in the same direction and vice versa. This algorithm is slow to respond, but has the advantage of being simple and robust.

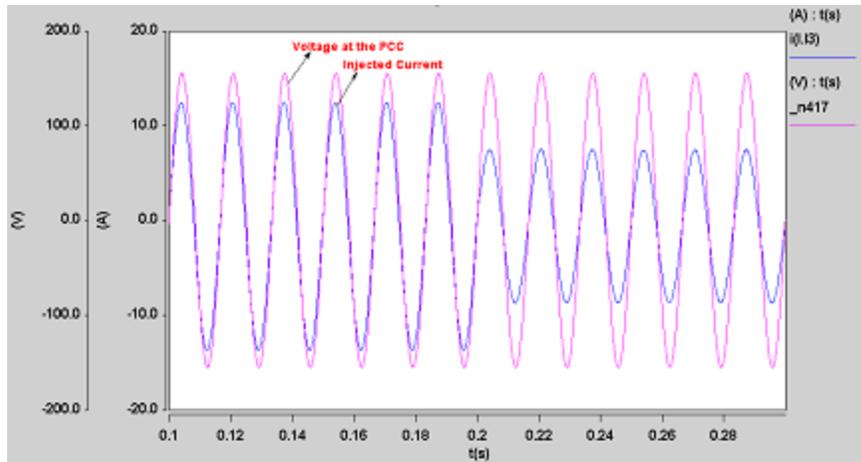


Figure 4.25. Simulation Results - Current Loop Response

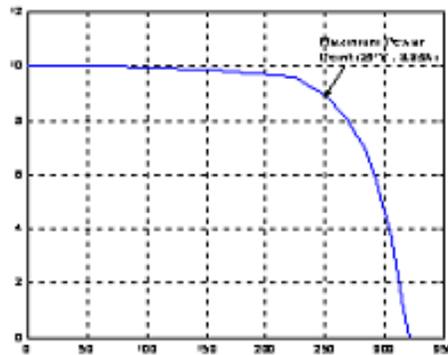


Figure 4.26. V-I Characteristic of the 2 kW Solar Array

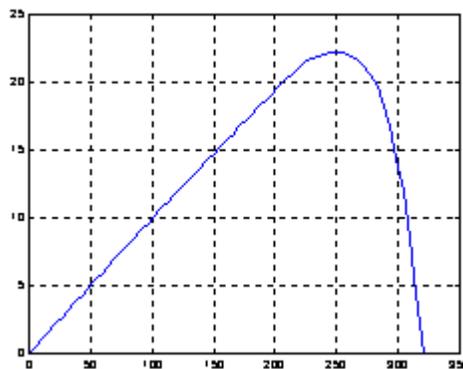


Figure 4.27. Power vs Current Plot for the Solar Array

In the incremental conduction method, the incremental and instantaneous array conductances are measured. The maximum power point is reached when both values

are equal. This algorithm is faster than the perturbation method, but requires more number of sensors.

In the case of the proposed system, the perturbation and observation method is preferred for its simplicity and robustness. The overall system response time in this case is found to be well within a second, which is not very slow compared to the dynamics of the atmosphere (on which the solar cell maximum power point is dependent).

The block diagram of the MPPT is shown in Figure 4.28.

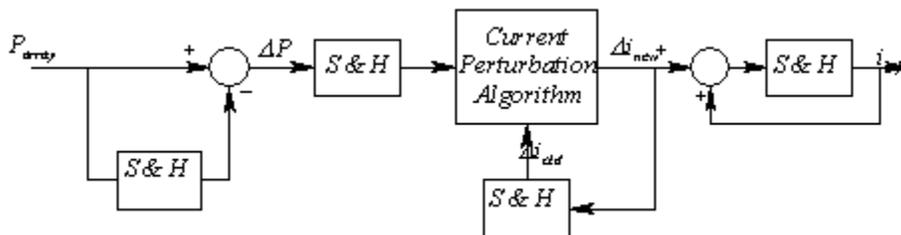


Figure 4.28. Maximum Power Point Tracker Algorithm

A change in current reference causes the output power of the solar array ( $P_{array}$ ) to change. The present power output of the system is measured and the change in power output ( $\Delta P$ ) is obtained by subtracting the earlier power output (stored by the sample and hold block) from it. This change in power is sampled when the  $P_{array}$  measurement settles down. The current perturbation algorithm determines the slope of the power curve and produces a new current perturbation ( $\Delta i_{new}$ ) based on the slope. The algorithm used is

$$\begin{aligned} \frac{dP}{di} > 0 &\Rightarrow \text{increase the reference current} \\ \frac{dP}{di} < 0 &\Rightarrow \text{decrease the reference current.} \end{aligned} \tag{5}$$

Thus, when the sample and hold block at the current reference is sampled, a new current reference generated by the algorithm is sent to the current controller and the process repeats. The sample rate used in the system is about 34 ms (two 60 Hz cycles).

## Simulation Results

The solar array characteristics shown in Figure 4.26 are used in the simulation carried out in SABER. Figure 4.29 shows the SABER schematic of the proposed system with a MPPT controller.

The output power of the solar array as well as the output current of the array are plotted in Figure 4.30. As it can be seen, the output power of the array nearly reaches the maximum power point (2200W). There is a noticeable dithering about the maximum power point in both the waveforms, which is characteristic of the algorithm used.

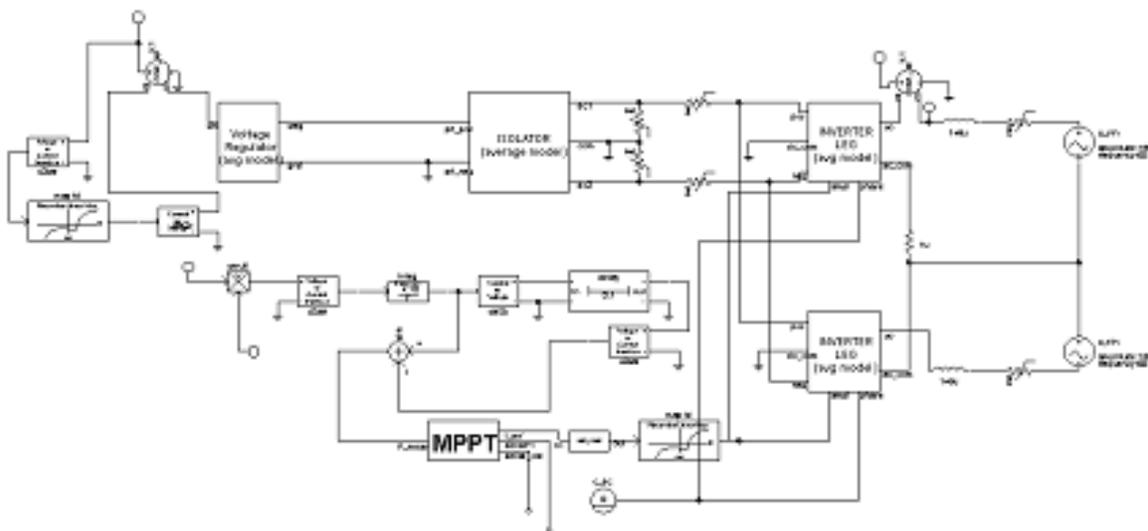


Figure 4.29. SABER Schematic of the Proposed System

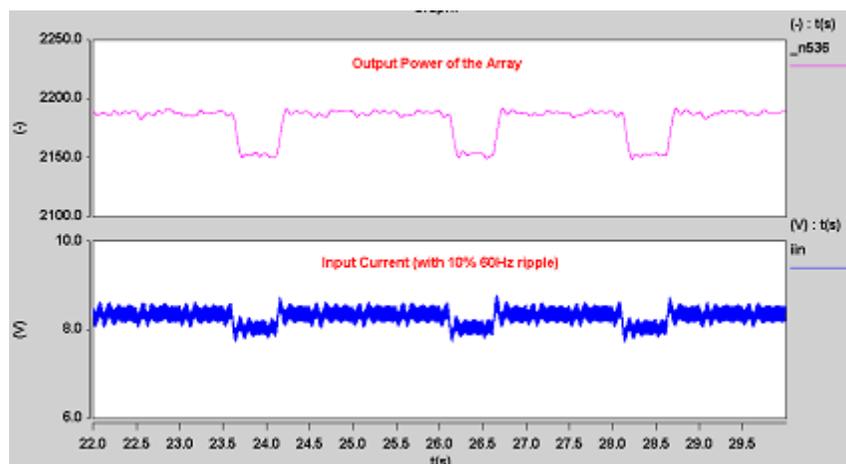


Figure 4.30. Output Power and Output Current of the Solar Array

Figure 4.31 shows the grid voltage at the PCC and the current injected into the grid. The current is found to be injected at unity power factor.

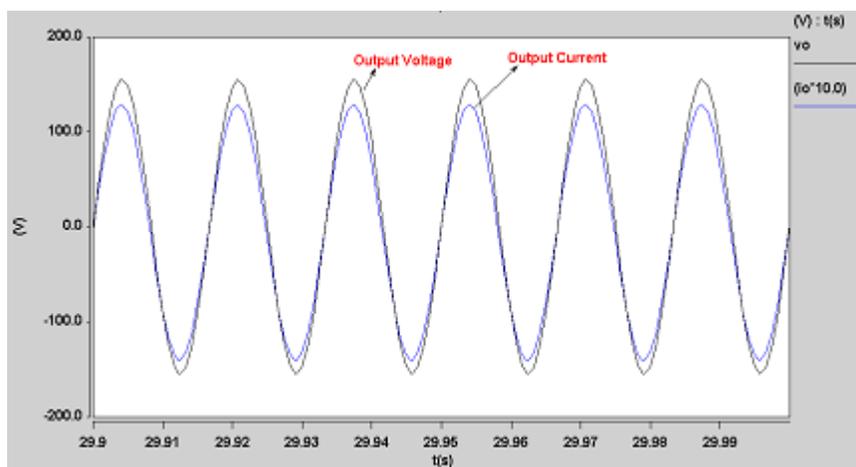


Figure 4.31. Grid Voltage and Current Injected into the Grid

#### 4.5.4. PWM Controller Conclusions

The grid-tied system is able to inject the required current into the grid at unity power factor. The maximum power point tracker is able to track the maximum power point of the array and maintain the operating point of the array close to the maximum power point.

#### Reference for 4.5.

Hua, C and Shen, C, "Comparative Study of Peak Power Tracking Techniques for Solar Storage Systems," Applied Power Electronics Conference 1998, vol. 2, pp679-85.

## **4.6. Inverter Protection Features**

This section discusses the protection schemes required for the proposed DC-AC inverter system. These schemes protect the system against external faults (like load short circuit, surges on the grid etc.) and internal faults (failure of a semiconductor device). The report is divided into three sections:

- The first section deals with the protection features required at the input side.
- The second section deals with the protection features required at the output side.
- The third section deals with over temperature faults.

### **4.6.1. Protection Schemes at the Input**

The input side protection of the converter system is designed to account for two types of faults:

- Failure of one of the input stages in the case of paralleled systems
- Reverse connection of the PV array at the input

The protection schemes designed to handle the above mentioned faults are described below.

#### **4.6.1.1. Failure of One of the Input Stages**

In case of paralleled systems, there is a possibility that one of the paralleled stages fails. This stage has to be isolated from the system, while the other converters operate uninterrupted. This can be easily implemented by inserting a MOSFET at the input of the boost converter as shown in Figure 4.32.

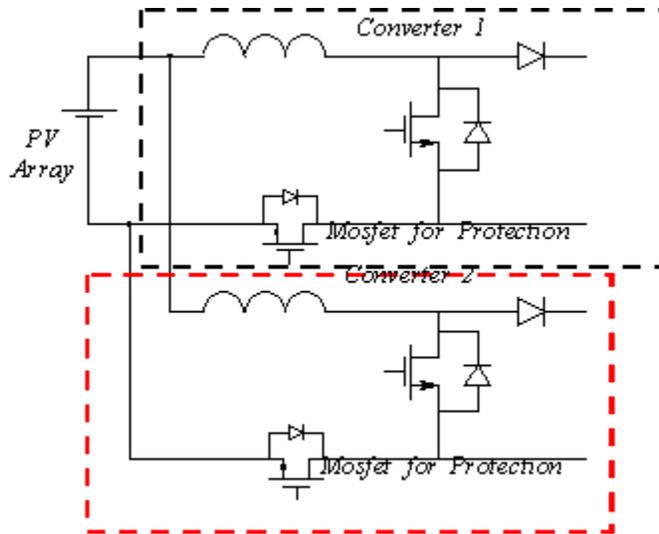


Figure 4.32. Input Side Protection Against Failure

If the boost stage power MOSFET in converter 1 fails (short circuits), then the input voltage falls to zero and the short circuit current of the array flows through the MOSFET. By detecting an undervoltage condition at the input, the fault condition can be detected. However, in order to isolate only the faulted stage, this signal is ANDED with a surge current detect through the inductor. Since only the faulted stage will have a surge in the inductor current, only that stage will be turned off. Thus, the implementation logic for the protection scheme is

$$\left. \begin{array}{l} \text{Undervoltage at Input} \\ \text{AND} \\ \text{Surge in the Input Current} \end{array} \right\} \Rightarrow \text{stage is faulted (turn off protection MOSFET)}$$

In order to prevent a stage from permanently shutting off due to temporary faults, logic could be implemented using a DSP that tries to start the stage by turning on the protection MOSFET at regular intervals of time, until the number of attempts reach a set limit.

### **Reverse Connection of the Input Source**

The PV array, when short-circuited, acts as a current source. It has a limited short circuit current capability and short circuiting the array will not destroy it. Thus, the reverse connection of the input source can be easily handled by putting a power diode in parallel with the source as shown in Figure 4.33.

When the source is connected properly, the diode is reverse biased and does not dissipate any power. When the source is connected in reverse, diode  $D_p$  will be

forward biased and the short circuit current will flow through it. The presence of two diodes in the secondary path as compared to a single diode in the primary path ensures that all the current flows in the primary path alone. Thus, the body diode of the power MOSFET does not conduct, preventing any damage to the MOSFET from over temperatures.

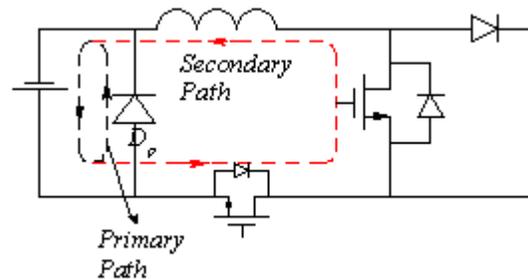


Figure 4.33. Protection Against Reverse Connection

#### 4.6.2. Protection Schemes at the Output

Three types of faults can commonly occur at the output side of the system:

- Voltage surges at the terminals of the inverter when it is connected to the grid
- Short-circuit fault at the load
- One of the paralleled stages fails due to the failure of a semiconductor device

The protection features to handle the above mentioned faults are described in this section.

##### Voltage Surge Protection

There are two ways to protect the system from lighting surges on the lines – Metal Oxide Varistors (MOVs) or a Silicon Avalanche Diode (Transorb).

The MOVs are cheap and can handle very high currents, but have a slow response time (as compared to Transorbs). Moreover, the effectiveness of the MOV decreases with repetitive activity.

The transorbs are more expensive compared to the MOVs, but have a faster response time and their effectiveness does not decrease with repeated application of surges.

They would be ideally suited for the present application.

### **Short-Circuit Fault**

Short-circuit fault protection consists of two types of protection – a fast acting active protection and a slow acting fuse.

The fast acting active protection system works on the principle of hysteresis control – if the output current exceeds a limit, the conducting switch in the inverter leg is turned off and the other switch is turned on. Thus, for a short circuit at the load, the inductor current would be alternating between the positive and negative limits. This would ensure that the system behaves as a current limited source in the event of a short circuit fault.

The slow acting fuse would disconnect the system from the load when it gets heated up due to the constant output current of the system in the case of a fault.

### **Failure of a Single Stage**

Figure 4.34 shows the parallel connection of two systems the output. If one of the MOSFETs were to fail (short-circuit), then that system would have to be isolated from the load and the other converters in the circuit.

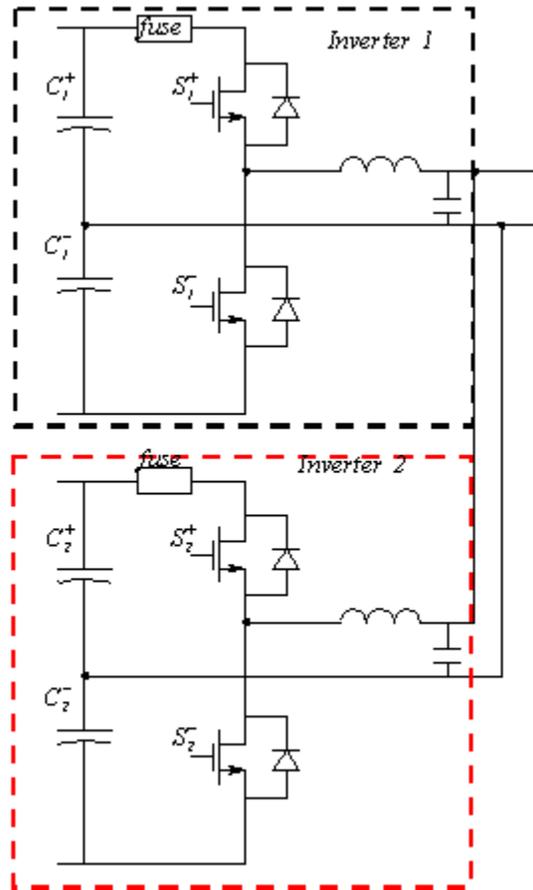


Figure 4.34. Protection for the Paralleled Inverter

If  $S_1^+$  were to short, capacitor  $C_1^+$ , would appear across the load. A surge of current would cause the fuse in the DC link to open. The DC link capacitor voltage would also reduce due to the surge of current. By implementing an under-voltage lockout on the inverter stage, the other switches of the inverter can be turned off once the capacitor voltage drops below a specified limit, preventing the stage from operating.

### 4.6.3. Over-Temperature Protection

Over-temperature protection for the entire circuit can be achieved by mounting all the semiconductor components on the same heat sink and using a thermocouple to measure the temperature. If the temperature of the heat sink goes beyond a particular value, the circuit can be shut down.

In the case of grid connected converters, if the over-temperature limit is reached, it will be possible to operate the system at lower current levels and bring the temperature within limits without having to shut the system down. Since the thermal time constants are very large, the loop will be very slow and can be easily implemented with a DSP.

#### **4.6.4. Summary of Protection Approaches**

The protection systems described in this report help to protect the system from both external and internal faults. Over-temperature protection ensures that the devices always operate within their normal temperature limits.