High Performance Electrical Modeling and Simulation Verification Test Suite - Tier I

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High Performance Electrical Modeling and Simulation Verification
Test Suite - Tier I

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Abstract

This document describes the High Performance Electrical Modeling and Simulation (HPEMS)
Global Verification Test Suite (VERTS). The VERTS is a regression test suite used for
verification of the electrical circuit simulation codes currently being developed by the HPEMS
code development team. This document contains descriptions of the Tier I test cases.
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1 Introduction

1.1 Purpose

This document describes the High Performance Electrical Modeling and Simulation (HPEMS) Global Verification Test Suite (VERTS). The VERTS is a regression test suite used for verification of the electrical circuit simulation codes currently being developed by the HPEMS code development team.

1.2 Scope

A software verification process is necessary to increase our confidence in the implementation of the required model equations and their numerical behavior. This includes the mathematical equations needed to correctly solve the physics and algorithms used by the code. Verification has been described in the Accelerated Strategic Computing Initiative (ASCI) V&V Guidelines as:
1. The process of determining that the equations are solved correctly.
2. The process of determining that a computational software implementation correctly represents the model of the physical process.

Acceptable performance of the simulation codes on the VERTS is the main factor that determines whether the code is ready for validation studies [ASCI V&V Guidelines].

This document outlines a Global VERTS that is used for verification of two electrical circuit simulation codes, ChileSPICE and Xyce. The Global VERTS was constructed during the initial development of the HPEMS ChileSPICE code. Test cases in the Xyce VERTS are extracted from the Global VERTS as functionality is added to the code. The VERTS structure, construction and assessment criteria are outlined in this document.

1.3 Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Abbreviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASCI</td>
<td>Accelerated Strategic Computing Initiative</td>
</tr>
<tr>
<td>DP</td>
<td>Defense Programs</td>
</tr>
<tr>
<td>HPEMS</td>
<td>High Performance Electrical Modeling and Simulation</td>
</tr>
<tr>
<td>PIRT</td>
<td>Phenomena Identification and Ranking Table</td>
</tr>
<tr>
<td>VERTS</td>
<td>Verification Test Suite</td>
</tr>
<tr>
<td>SNL</td>
<td>Sandia National Laboratories</td>
</tr>
</tbody>
</table>
2 Verification Test Suite (VERTS)

The VERTS is a regression test suite used to assess the performance of electrical circuit simulation codes, ChileSPICE and Xyce, which are currently being developed by the HPEMS team. Testing activities, including generating test cases, are done in parallel with code development activities. The VERTS is comprised of circuit netlists and their expected simulation outputs. A circuit netlist specifies the circuit components and their connections, the type of analysis to be performed, and the desired output. The simulation code parses the netlist, performs the desired analysis and generates an output file.

ChileSPICE is Sandia’s enhanced shared memory version of Spice3F5, which was originally developed at the University of California at Berkley. Xyce is a parallel electrical circuit simulation code that is being developed to support the simulation needs of the Sandia National Laboratories (SNL) electrical system designers. ChileSPICE is a development test bed for Xyce, which is intended to be the production simulator.

2.1 Key Areas

Three key areas will be addressed in describing the VERTS:
1. Structure: Why was the verification test suite chosen?
2. Construction: How was the verification test suite chosen?
3. Assessment: How is the VERTS executed? When are verification tests passed?

2.1.1 VERTS Structure

The structure of the VERTS is the logic by which the test suite is defined and applied to test the code [ASCI V&V Guidelines]. The HPEMS VERTS is structured according to the three-tier taxonomy first introduced in Version 1 of the ASCI V&V Guidelines.

- Tier I – tests with exact analytical solutions. These tests are designed to ensure that the basic devices are functional and are producing correct results when compared to exact analytical solutions (i.e., hand calculations).
- Tier II – tests with semi-analytical solutions. These tests are semi-analytical in nature. Hand calculations of these circuits are too complex for a reasonable evaluation of circuit performance. The results of these circuits are compared to experimental data to ensure performance, accuracy and convergence criteria are met.
- Tier III – idealized problems suitable for code comparison exercises. These tests are typically complex subcircuits and circuits. These tests are designed to ensure performance, accuracy and convergence criteria are met at the subcircuit and circuit level. Tier III tests are also designed to ensure that multiple component circuits are functional and are meeting performance, accuracy and convergence criteria. Code comparison exercises are the main method for evaluating Tier III tests.

While this structure is suitable for basic assessment of the code under development, it is vital that the VERTS structure reflects the requirements outlined by the Phenomena Identification Ranking Table (PIRT) for a particular stockpile driver. Specific VERTS will be developed for each stockpile driver. They will contain test cases from the global VERTS as well as circuit netlists.
that assess specific model or simulation requirements specified by the PIRT.

The PIRT is the methodology by which the key physical phenomena are defined. The PIRT ranks the importance of code activity associated with implementing the phenomena and provides the basis for gauging associated fidelity requirements. Electrical systems are constructed from many independent components. These components are hierarchically grouped into families based on technology, functionality and usage. Examples of family classes are transistors, resistors and capacitors. Within each class, there is a further division into related components. For example, a transistor can be categorized into a bipolar junction transistor, a junction field effect transistor and a metal oxide semiconductor field effect transistor. Each component may have a different response to the same external environmental stimuli. A BJT (bipolar junction transistor) reacts differently in a radiation field when compared to a resistor response in the same radiation field. The Global PIRT was constructed based on the hierarchy found in electronic components.

*This document addresses Tier I test cases. The Tier II and III tests will be documented in reports that will be released by September 2002.*

### 2.1.2 VERTS Construction

Discussion of the construction of the VERTS answers the basic question of how the VERTS is actually populated with the appropriate tests. In an electrical system design, the components are assembled into subsystems and the subsystems are assembled into systems [HPEMS V&V Plan]. The VERTS is similarly constructed. In accordance with the three-tier taxonomy outlined previously, Tier I circuits test the individual component device models to verify that the simulator produces accurate results. Tier II circuits consist of netlists that contain a variety of components that are integrated into subsystems. Tier III circuits are netlists that test large subsystems and will eventually include system level test cases.

Tier I test cases are designed to test the codes’:
- Basic Circuit Elements - transistors, resistors, capacitors, inductors, sources, etc.
- Simulation Analysis types - AC, DC, transient, transfer function, etc.
- Enhanced features - parameters, functions, look-up tables, analog behavioral modeling elements, etc.

These problems are small (2-3 components) and demonstrate that the circuit code can solve mathematical device model equations correctly when compared to exact analytical solutions. As device models, analysis types and enhanced features are added to the code, associated test cases are developed and added to the VERTS.

### 2.1.3 Execution of VERTS

The VERTS is organized in a directory tree with three main subdirectories: Netlists, Output Data, and Test Scripts. Each test case in the VERTS has a subdirectory containing the input and expected (or reference) output file in the Netlist and Output Data directories, respectively. The input file directory contains one input file and any necessary model library files. The output file directory contains the expected results in an output file. The Test Scripts directory contains the various scripts needed to perform an automated or manual regression test. This directory
structure allows for exercising VERTS regression testing automatically or manually, and is detailed in the [HPEMS/Xyce Test Plan].

For automated regression testing a set of scripts is used to build the executables, execute the regression testing, collect the output results, compare them to expected results and report the results to the code development team. A report containing the test results is generated. This report lists the test date, computational platform used, each test name with the associated pass/fail results for each executable (serial, parallel or both) that is used. Each regression test run issues an email message containing the test reports to each member of the HPEMS code development team. A cron job is used to schedule regression testing on a nightly basis.

Manual regression testing is useful for code developers testing code changes before committing them to the repository. They can run the test suite using the executables compiled in their working directory. The process for manual regression testing is similar to the automated test process. A developer checks out the test scripts from the CVS repository, runs the test script using their compiled serial or parallel executables and a test results file is created in the developer’s current directory.

### 2.1.4 VERTS Assessment

As new features are added to the code, VERTS regression testing is used to test these new features and verify that the changes to the code did not create any bugs. Code assessment by the VERTS is a simple pass or fail. For each test case in the VERTS, the current simulation output is recorded and compared to the reference output results. The reference output has been determined by the Test Specialist to be 'correct' based on hand calculations for Tier I tests. A compare program performs verification by comparing the reference and the current results and assuring that they are identical to within a specified tolerance of +/-2%. When the current results match the reference within 2%, then a pass is recorded in the test report; otherwise, fail is recorded in the test report. As detailed in [HPEMS Xyce Test Plan], the compare program allows a tolerance to be specified in both the independent and the dependent variables. Conceptually this corresponds to taking plots of the reference and test data and making sure that these are coincident within a certain distance by ‘fattening’ one of them and making sure that the other lies within the error margin of the fattened trace. As a practical matter it is insufficient to merely allow for errors in the dependent variable because many circuits have abrupt transitions that can be slightly miss-timed, but still are correct within acceptable tolerances. For this reason the reference traces are fattened in both the direction of the independent variable as well as the dependent variable. The specific amount of fattening in each direction is currently a relative amount of ±2%. Using time and voltage as the independent and dependent variables, respectively, the test value for comparison must meet the following criteria:

\[
(1 - \text{Tol}_V) \times V / V_{\text{REF}} \times (1 + \text{Tol}_V) \quad (1) \\
(1 - \text{Tol}_T) \times T / T_{\text{REF}} \times (1 + \text{Tol}_T) \quad (2)
\]

where,
- \( V, T \) = test voltage and time, respectively
- \( \text{Tol}_V, \text{Tol}_T \) = voltage and time tolerance, respectively
- \( V_{\text{REF}}, T_{\text{REF}} \) = reference voltage and time, respectively
Thus for a value of 1 volt in the reference plot, the test plot would need to lie within the range 0.98-1.02 volts. A transition like a fast rising edge would need to appear at a time within that observed in the reference plot. Thus a transition that occurs at 0.001 seconds would need to occur in the range 0.00098-0.00102 seconds in order to pass the test. For values near zero where the relative tolerance test is too restrictive, there is also a minimum absolute tolerance of 1 µvolt or 1 picoamp. For a value of 0 volts in the reference plot, the test value would need to be within 1 µvolt of zero. The choice of 2% tolerance is based on the accuracy that electrical circuit designers typically expect from simulation results, and was set by HPEMS Defense Program (DP) customers.
3 VERTS Netlists

3.1 Tier I Test Cases

The netlists contained in this section are Tier I test cases. A netlist file describes each test case. The first part of the file is a description that includes the circuit name, input and output voltages or currents, and equations used for a hand calculation of the expected results. The next section of the file defines the circuit elements, their connectivity, analysis type, and includes a print statement that defines the node voltages or branch currents to be recorded in the output file. Finally, a plot or a table of the ChileSPICE simulation results is shown.

Table 1. lists the basic circuit elements, test circuit name, description and analysis type for the Tier I test cases. Some of the circuit elements are tested using more than one test case. However, the purpose for each test case is unique as seen in the circuit description column.
<table>
<thead>
<tr>
<th>DEVICE TESTED</th>
<th>Circuit Name</th>
<th>Circuit Description</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>ABM_ABS</td>
<td>Test of ABM Absolute Value Function</td>
<td>DC*</td>
</tr>
<tr>
<td></td>
<td>ABM_ACOS_ASIN</td>
<td>Test of ABM Arccosine and Arcsine Functions</td>
<td>DC</td>
</tr>
<tr>
<td></td>
<td>ABM_ATAN_TAN</td>
<td>Test of ABM Arctangent and Tangent Functions</td>
<td>TRAN**</td>
</tr>
<tr>
<td></td>
<td>ABM_EXPLN</td>
<td>Test of ABM Exponential and Natural Log Functions</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>ABM_HYP</td>
<td>Test of ABM Hyperbolic Functions, .PARAM, .FUNC, IF Statements</td>
<td>DC</td>
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<tr>
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<td>ABM_LOG</td>
<td>Test of ABM Log Base 10 Function</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>ABM_SCT</td>
<td>Test of ABM Sine, Cosine and Tangent Functions</td>
<td>DC</td>
</tr>
<tr>
<td></td>
<td>ABM_SQRT</td>
<td>Test of ABM Square Root Function</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>ABM_TIME</td>
<td>Test of F(Y,T) Functionality</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>POLY</td>
<td>Test of Polynomial Function</td>
<td>DC</td>
</tr>
<tr>
<td>C</td>
<td>CAPACITOR</td>
<td>Test of Capacitor Model</td>
<td>TRANS</td>
</tr>
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<td>SEMIC_CAPACITOR</td>
<td>Test of Semiconductor Capacitor Model</td>
<td>TRANS</td>
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<tr>
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<td>DIODE</td>
<td>Test of Diode Model</td>
<td>DC</td>
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<td>E</td>
<td>VCVS</td>
<td>Test of Voltage-Controlled Voltage Source Model</td>
<td>DC</td>
</tr>
<tr>
<td>F</td>
<td>CCCS</td>
<td>Test of Current-Controlled Current Source Model</td>
<td>DC</td>
</tr>
<tr>
<td></td>
<td>VCCS</td>
<td>Test of Voltage-Controlled Current Source Model</td>
<td>DC</td>
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<td>G</td>
<td>CCVS</td>
<td>Test of Current-Controlled Voltage Source Model</td>
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<td>IEXP</td>
<td>Test of Exponential Current Source Model</td>
<td>TRANS</td>
</tr>
<tr>
<td>I</td>
<td>IPULSE</td>
<td>Test of Pulse Current Source Model</td>
<td>TRANS</td>
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<td>PWL</td>
<td>Test of Piecewise Linear Current Source Model</td>
<td>TRANS</td>
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<tr>
<td></td>
<td>ISFFM</td>
<td>Test of Single Frequency (FM) Current Source Model</td>
<td>TRANS</td>
</tr>
<tr>
<td></td>
<td>ISIN</td>
<td>Test of Sine Current Source Model</td>
<td>TRANS</td>
</tr>
<tr>
<td>J</td>
<td>NJFET</td>
<td>Test of N-Channel Junction Field Effect Transistor (JFET) Model</td>
<td>DC</td>
</tr>
<tr>
<td></td>
<td>PJFET</td>
<td>Test of P-Channel Junction Field Effect Transistor (JFET) Model</td>
<td>DC</td>
</tr>
<tr>
<td>K</td>
<td>MINDUCTORS</td>
<td>Test of Inductor Coupling Model</td>
<td>AC***</td>
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<td>TRANS</td>
</tr>
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<td>NMOS</td>
<td>Test of N-Channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) Model</td>
<td>DC</td>
</tr>
<tr>
<td>Column 1</td>
<td>Column 2</td>
<td>Description</td>
<td>Model</td>
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<tr>
<td>---------</td>
<td>----------</td>
<td>-----------------------------------------------------------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>Q</td>
<td>BJT</td>
<td>Test of NPN Bipolar Junction Transistor (BJT) Model</td>
<td>DC</td>
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<tr>
<td>R</td>
<td>Resistor</td>
<td>Test of Resistor Model</td>
<td>DC</td>
</tr>
<tr>
<td>S</td>
<td>Voltage Switch</td>
<td>Test of Voltage-Controlled Switch Model</td>
<td>TRAN</td>
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<td>T</td>
<td>Transmission Line</td>
<td>Test of Lossless Transmission Line Model</td>
<td>TRAN</td>
</tr>
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<td>.TF</td>
<td>TF Analysis</td>
<td>Test of Transfer Function Analysis</td>
<td>TF</td>
</tr>
<tr>
<td>V</td>
<td>EXP</td>
<td>Test of Exponential Voltage Source Model</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>PULSE</td>
<td>Test of Pulse Voltage Source Model</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>PWL</td>
<td>Test of Piecewise Linear Voltage Source Model</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>SFFM</td>
<td>Test of Single Frequency (FM) Voltage Source Model</td>
<td>TRAN</td>
</tr>
<tr>
<td></td>
<td>SIN</td>
<td>Test of Sine Voltage Source Model</td>
<td>TRAN</td>
</tr>
<tr>
<td>W</td>
<td>Current Switch</td>
<td>Test of Current Controlled Switch Model</td>
<td>DC</td>
</tr>
<tr>
<td>X</td>
<td>Digital Primitive Subcircuit</td>
<td>Test of AND Gate, NAND Gate, NOR Gate, OR Gate, XNOR Gate, XOR Gate</td>
<td>TRAN</td>
</tr>
<tr>
<td>Z</td>
<td>MESFET</td>
<td>Test of N-Channel MESFET Model</td>
<td>DC</td>
</tr>
</tbody>
</table>

* DC - DC sweep of an input voltage/current source
** TRAN - Transient analysis or behavior over time
*** AC - AC Analysis or small signal frequency response
3.1.1 Test Circuit for the Absolute Value Function

* Tier No.:  1
* Directory/Circuit Name: ABM_ABS/abs.cir
* Description: Test of the of analog behavioral modeling absolute value function.
* Input: VS
* Output: V(1), V(3)
* Analysis:
  * A DC input voltage, VS, is swept from -10V to 10V in 1V steps. A nonlinear
dependent voltage source, B1 or V(3), is defined as the negative of the absolute
value of the source voltage (VS=V(1)). A DC analysis is performed and the output
recorded, V(3), is the voltage defined by the input DC source voltage and the absolute
value function.
  *
  * This table is a set of hand calculations for the absolute value, ABS, of V(1):
  *
<table>
<thead>
<tr>
<th>V(1)</th>
<th>V(3)=ABS(V(1))</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1.00E+01</td>
<td>-1.00E+01</td>
</tr>
<tr>
<td>-5.00E+00</td>
<td>-5.00E+00</td>
</tr>
<tr>
<td>0.00E+00</td>
<td>0.00E+00</td>
</tr>
<tr>
<td>5.00E+00</td>
<td>-5.00E+00</td>
</tr>
<tr>
<td>1.00E+01</td>
<td>-1.00E+01</td>
</tr>
</tbody>
</table>

VS  1  0  0
RS  1  2  100
R1  2  0  100K
B1  3  0  V = {-(ABS(V(1,0)))}
R2  3  4  100
R3  4  0  100K
.DC VS -10 10 1
.PRINT DC V(1) V(3)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the ABS Circuit

VS = V(1) (Volts)

B1 = V(3) (Volts)

V(1)  V(3)
3.1.2 Test Circuit for the Arcsine and Arccosine Functions
******************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_ACOS_ASIN/acos_asin.cir
* Description:  Test of the analog behavioral modeling arcsine and arccosine functions.
* Input: V1
* Output: V(1), V(2), V(3)
* Analysis:
* The netlist contains an independent voltage source, V1 or V(1), which is swept from
* –0.99V to 0.99V in 0.1V steps. Two nonlinear dependent voltage sources are
* used to define the functions as follows:
* V(2)=B2=ASIN(V(1)) = inverse sine of V(1)
* V(3)=B3=ACOS(V(1)) = inverse cosine of V(1)
* A DC analysis is performed and the output recorded is voltages defined by the
* arcsine and arccosine functions.
* This table is a set of hand calculations for the functions of ACOS and ASIN of X
* X                      ACOS(X)                    ASIN(X)
* -1.0 3.14 -1.570
* -0.5 2.09 -0.524
*  0.0 1.57   0.000
*  0.5 1.05   0.524
*  1.0 0.00   1.570
******************************************************************************
V1 1 0 0
R1 1 0 1
B2 2 0 V = {ASIN(V(1,0))}
R2 2 0 1
B3 3 0 V = {ACOS(V(1,0))}
R3 3 0 1
.DC V1 -0.99 0.99 0.1
.PRINT DC V(1) V(2) V(3)
.OPTIONS ACCT LIST
.END
3.1.3 Test Circuit for the Tangent and Arctangent Functions

* Tier No.: 1
* Directory/Circuit Name: ABM_ATAN_TAN/atan_tan.cir
* Description: Test of analog behavioral modeling tangent and arctangent functions.
* Input: VS
* Output: V(1), V(2), V(3)
* Analysis:

A sinusoidal source voltage, VS or V(1), with a 1V amplitude and 1KHZ freq. is the input to the circuit. Two nonlinear dependent voltage sources are used to define the functions as follows:

V(2)=B2=TAN(V(1)) = tangent of input sine function = V(2)
V(3)=B3=ATAN(V(2)) = inverse tangent of B2 (or TAN(VS))=V(1)

= value of the input source VS

where,
V(1)=VS=SIN(0 1 1KHZ) = SIN(2*PI*(1KHZ)*(TIME))

A transient analysis is performed and the output recorded is the node voltages defined by the input source, V(1), the tangent, V(2), and arctangent, V(3), functions.

This table is a set of hand calculations for the TAN and ATAN functions

<table>
<thead>
<tr>
<th>TIME (Seconds)</th>
<th>V(1) (Volts)</th>
<th>V(2)=TAN(V(1)) (Volts)</th>
<th>V(3)=ATAN(TAN(V(1))) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>0.25E-3</td>
<td>1.00</td>
<td>1.55</td>
<td>1.00</td>
</tr>
<tr>
<td>0.5E-3</td>
<td>8.98E-11</td>
<td>8.98E-11</td>
<td>8.98E-11</td>
</tr>
<tr>
<td>0.75E-3</td>
<td>-1.00</td>
<td>-1.55</td>
<td>-1.00</td>
</tr>
<tr>
<td>1.0E-3</td>
<td>-1.8E-10</td>
<td>1.8E-10</td>
<td>1.8E-10</td>
</tr>
<tr>
<td>1.25E-3</td>
<td>1.00</td>
<td>1.55</td>
<td>1.00</td>
</tr>
<tr>
<td>1.5E-3</td>
<td>2.69E-10</td>
<td>2.69E-10</td>
<td>2.69E-10</td>
</tr>
<tr>
<td>1.75E-3</td>
<td>-1.00</td>
<td>-1.55</td>
<td>-1.00</td>
</tr>
<tr>
<td>2.00E-3</td>
<td>-3.59E-10</td>
<td>-3.59E-10</td>
<td>-3.59E-10</td>
</tr>
</tbody>
</table>

VS 1 0 SIN(0 1 1KHZ)
R1 1 0 1
B2 2 0 V={TAN(V(1,0))}
R2 2 0 1
B3 3 0 V={ATAN(V(2,0))}
R3 3 0 1
.TRAN 0.1MS 2MS
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the TAN & ATAN Circuit

![Graph showing simulation results for the TAN & ATAN Circuit]
3.1.4 Test Circuit for the Exponential and Natural Log Functions

* Tier No.: 1
* Directory/Circuit Name: ABM_EXPLN/exp_ln.cir
* Description: Test of analog behavioral modeling exponential and natural log functions
* Input: VS
* Output: V(1), V(2), V(3)
* Analysis:
  * The input voltage, VS, is a piece wise linear source with specified time and voltage pairs. Two nonlinear dependent voltage sources are used to define the functions as follows:
  * V(2)=B2=EXP(V(1)) = exponent of input voltage = EXP(V(1))
  * V(3)=B3=LN(V(2)) = ln of B2 (EXP function) = V(1)
  * A transient analysis is performed and the output recorded is the node voltages defined by the input source, V(1), the exponential, V(2), and natural log, V(3), functions.

* This table is a set of hand calculations for the EXP and LN functions:

<table>
<thead>
<tr>
<th>TIME (Seconds)</th>
<th>V(1) (Volts)</th>
<th>EXP(V(1)) (Volts)</th>
<th>LN(EXP(V(1))) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00E-3</td>
<td>2.5</td>
<td>12.182</td>
<td>2.5</td>
</tr>
<tr>
<td>0.50E-3</td>
<td>5.0</td>
<td>148.413</td>
<td>5.0</td>
</tr>
<tr>
<td>1.00E-3</td>
<td>7.5</td>
<td>1808.042</td>
<td>7.5</td>
</tr>
<tr>
<td>1.50E-3</td>
<td>10.0</td>
<td>22026.47</td>
<td>10.0</td>
</tr>
<tr>
<td>2.00E-3</td>
<td>7.5</td>
<td>1808.042</td>
<td>7.5</td>
</tr>
<tr>
<td>2.50E-3</td>
<td>7.5</td>
<td>1808.042</td>
<td>7.5</td>
</tr>
</tbody>
</table>

VS 1 0 PWL(0 2.5V 0.5MS 5V 1MS 7.5V 1.5MS 10V 2MS 7.5V)
R1 1 0 1
B2 2 0 V = {EXP(V(1,0))}
R2 2 0 1
B3 3 0 V = {LN(V(2,0))}
R3 3 0 1
.TRAN 0.02MS 2.5MS
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END
ChileSPICE Simulations Results for the EXP & LN Circuit

![Graph showing the Spice Simulation Results for the EXP & LN Circuit. The graph plots voltage (V) against time (in seconds). The x-axis represents time from 0.00E+00 to 1.20E+01 in increments of 5.00E-04, and the y-axis represents voltage from 0.00E+00 to 2.50E+04 in increments of 1.00E+00. The graph shows three different voltage levels: V(1), V(3), and V(2).]
3.1.5 Test Circuit for the Hyperbolic Functions

* Tier No.: 1
* Directory/Circuit Name: ABM_HYP/hyp.cir
* Description: Test of the analog behavioral modeling functions:
  * SINH, COSH, TANH, ASINH, ACOSH, ATANH
* Input: V(1)
  * V(12), V(13), V(14)
* Analysis:
  * Nonlinear dependent voltage sources are used to define the functions. See
    comments in netlist below for description of how functions are used
  * The following tables are hand calculations of the functions calculated in this netlist:
  *
<table>
<thead>
<tr>
<th>V(1)</th>
<th>V(2)=(-ABS(V(1)))</th>
<th>SINH(V(2))</th>
<th>COSH(V(2))</th>
<th>TANH(V(2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>-10</td>
<td>-10</td>
<td>-11013.23287</td>
<td>11013.23292</td>
<td>-0.999999996</td>
</tr>
<tr>
<td>-8</td>
<td>-8</td>
<td>-1490.478826</td>
<td>1490.479161</td>
<td>-0.999999775</td>
</tr>
<tr>
<td>-6</td>
<td>-6</td>
<td>-201.7131574</td>
<td>201.7156361</td>
<td>-0.999987712</td>
</tr>
<tr>
<td>-4</td>
<td>-4</td>
<td>-27.2899172</td>
<td>27.30823284</td>
<td>-0.9993293</td>
</tr>
<tr>
<td>-2</td>
<td>-2</td>
<td>-3.626860408</td>
<td>3.762195691</td>
<td>-0.96402758</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>-2</td>
<td>-3.626860408</td>
<td>3.762195691</td>
<td>-0.96402758</td>
</tr>
<tr>
<td>4</td>
<td>-4</td>
<td>-27.2899172</td>
<td>27.30823284</td>
<td>-0.9993293</td>
</tr>
<tr>
<td>6</td>
<td>-6</td>
<td>-201.7131574</td>
<td>201.7156361</td>
<td>-0.999987712</td>
</tr>
<tr>
<td>8</td>
<td>-8</td>
<td>-1490.478826</td>
<td>1490.479161</td>
<td>-0.999999775</td>
</tr>
<tr>
<td>10</td>
<td>-10</td>
<td>-11013.23287</td>
<td>11013.23292</td>
<td>-0.999999996</td>
</tr>
</tbody>
</table>
  *
<table>
<thead>
<tr>
<th>V(1)</th>
<th>V(2)/100=(-ABS(V(1)))/100</th>
<th>ASINH(V(2)/100)</th>
<th>ATANH(V(2)/100)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-10</td>
<td>0.1</td>
<td>-0.099834079</td>
<td>-0.100335348</td>
</tr>
<tr>
<td>-8</td>
<td>0.08</td>
<td>-0.079914911</td>
<td>-0.080171325</td>
</tr>
<tr>
<td>-6</td>
<td>0.06</td>
<td>-0.059964058</td>
<td>-0.060072156</td>
</tr>
<tr>
<td>-4</td>
<td>0.04</td>
<td>-0.039989341</td>
<td>-0.040021354</td>
</tr>
<tr>
<td>-2</td>
<td>0.02</td>
<td>-0.019998667</td>
<td>-0.020002667</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0.02</td>
<td>-0.019998667</td>
<td>-0.020002667</td>
</tr>
<tr>
<td>4</td>
<td>0.04</td>
<td>-0.039989341</td>
<td>-0.040021354</td>
</tr>
<tr>
<td>6</td>
<td>0.06</td>
<td>-0.059964058</td>
<td>-0.060072156</td>
</tr>
<tr>
<td>8</td>
<td>0.08</td>
<td>-0.079914911</td>
<td>-0.080171325</td>
</tr>
<tr>
<td>10</td>
<td>0.1</td>
<td>-0.099834079</td>
<td>-0.100335348</td>
</tr>
</tbody>
</table>
  *
<table>
<thead>
<tr>
<th>V(1)</th>
<th>ACOSH(V(1)) Note: ACOSH(V(1))=0 for V(1)&lt;=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>-10</td>
<td>0</td>
</tr>
<tr>
<td>-8</td>
<td>0</td>
</tr>
<tr>
<td>-6</td>
<td>0</td>
</tr>
<tr>
<td>-4</td>
<td>0</td>
</tr>
<tr>
<td>-2</td>
<td>0</td>
</tr>
</tbody>
</table>
* Declaration of parameters and functions

*.PARAM HALF=0.5
*.PARAM K=100

*.FUNC INVCOSH(A) {LN( A + SQRT((A**2 - 1)))}
*.FUNC INVTANH(A,B,C) {A * LN((1 + (B/C))/(1 - (B/C)))}

* DC source Whose VALUES are used to evaluate the function defined by
  * B2 (Voltage @ node * 2, V(2)=(-ABS(V(1))),
  * V1 is stepped from –10V to 10V as indicated on the .DC statement line
  V1 1 0 0
  R1 1 0 1
  * Absolute value function that uses V1 to produce a triangular waveform
  B2 2 0 V = {-(ABS(V(1,0)))}
  R2 2 0 1
  * Hyperbolic sine function: B3=V(3)={SINH(V(2))}
  B3 3 0 V={SINH(V(2))}
  R3 3 0 1
  * Mathematical expression for the hyperbolic sine function: B4=V(4); expected results identical
  to B3 results
  B4 4 0 V={(EXP(V(2)) - EXP(-(V(2))))/2}
  R4 4 0 1
  * Hyperbolic cosine function: B5=V(5)={COSH(V(2))}
  B5 5 0 V={COSH(V(2))}
  R5 5 0 1
  * Mathematical expression for the hyperbolic cosine function: B6=V(6); expected results
  identical to B5 results
  B6 6 0 V={(EXP(V(2)) + EXP(-(V(2))))/2}
  R6 6 0 1
  * Hyperbolic tangent function: B7=V(7)={TANH(V(2))}
  B7 7 0 V={TANH(V(2))}
  R7 7 0 1
  * Mathematical expression for the hyperbolic tangent function: B8=V(8); expected results
  identical to B7 results
  B8 8 0 V={(EXP(V(2)) - EXP(-(V(2))))/(EXP(V(2)) + EXP(-V(2))))}
  R8 8 0 1
  * Inverse Hyperbolic sine function: B9=V(9)={ASINH(V(2))}
  B9 9 0 V={ASINH(V(2))}
  R9 9 0 1
  * Mathematical expression for the inverse hyperbolic sine function: B10=V(10); expected results
  identical to B9 results
  B10 10 0 V={LN(V(2) + SQRT((V(2)**2 + 1)))}
R10 10 0 1
* Inverse Hyperbolic cosine function: B11=V(11)=ACOSH(V(1)) FOR V(1) >= 1
* Use if statement to eliminate computing values less than or equal to 1; function is chosen to be
* positive
B11 11 0 V={IF(V(1)<= 1, 0, ACOSH(V(1)))}
R11 11 0 1
* Mathematical expression for the inverse hyperbolic cosine:
* B12=V(12)
* Defined above by the .func INVCOSH Domain: x >= 1
* Use if statement to eliminate computing values less than or equal to 1; function is chosen to be
* positive expected results identical to B11
B12 12 0 V={IF(V(1)<= 1, 0, INVCOSH(V(1)))}
R12 12 0 1
* Inverse Hyperbolic tangent function: B13=V(13)=ATAN(V(2)/K)
* Use if statement to eliminate computation of positive values that are less than 1 (note: K
* parameter used to make V(2) less than 1)
B13 13 0 V={IF((ABS(V(2))/K) < 1, ATANH(V(2)/K), 0)}
R13 13 0 1
* Mathematical expression for the inverse hyperbolic tangent: B14=V(14)
* Defined above by the .func INVTANH
* Domain: |x| < 1
* Use if statement to eliminate computation of positive values that are less than 1 (note: K
* parameter used to make V(2) less than 1. The expected results should be identical to B13
B14 14 0 V={IF((ABS(V(2))/K) < 1, INVTANH(HALF,V(2),K), 0)}
R14 14 0 1
.DC V1 -10 10 1
.PRINT DC V(1) V(2) V(3) V(4) V(5) V(6) V(7)
+ V(8) V(9) V(10) V(11) V(12) V(13) V(14)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit

**SINH**

![Graph of SINH function](image)

**COSH**

![Graph of COSH function](image)
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit

**TANH**

\[
\begin{array}{c|c|c|c|c|c|c}
& V(1) & V(2) & V(7) & V(8) \\
\hline
V(2) & -1.1 & -0.9 & -0.7 & -0.5 & -0.3 & -0.1 & 0.1 \\
V(1) & -10 & -5 & 0 & 5 & 10 & & \\
\end{array}
\]

- $\times$ V(7)
- $\circ$ V(8)
- $\blacktriangleright$ V(2)

**ASINH**

\[
\begin{array}{c|c|c|c|c|c|c}
& V(1) & V(2) & V(7) & V(10) \\
\hline
V(10) & -3 & -2.5 & -2 & -1.5 & -1 & -0.5 & 0 \\
V(9) & -10 & -5 & 0 & 5 & 10 & & \\
\end{array}
\]

- $\circ$ V(9)
- $\times$ V(10)
- $\blacktriangleright$ V(2)
ChileSPICE Simulation Results for the Hyperbolic Functions Circuit

**ACOSH**

![ACOSH Graph]

V(1) Volts vs. V(1) Volts

ChileSPICE Simulation Results for the Hyperbolic Functions Circuit

**ATANH**

![ATANH Graph]

V(1) Volts vs. V(2) Volts
**3.1.6 Test Circuit for the Log Base 10 Function**

* Tier No.: 1
* Directory/Circuit Name: ABM_LOG/log.cir
* Description: Test of the analog behavioral modeling log function.
* Input: V1, V2
* Output: V(1), V(2), V(3), V(4)
* Analysis:
  * Two piece-wise linear sources are used to define voltages at various times.
  * These sources are defined as V1=V(1) and V2=V(2), respectively.
  * Two nonlinear dependent voltage sources are used to define the function as follows:
    * V(3)=B3=LOG(V(1))
    * V(4)=B4=LOG(V(2))
  * The values for the PWL sources are chosen such that the log functions are evaluated for both large [V1=V(1)] and small [V2=V(2)] values.
  * This table is a set of hand calculations for the Log10 function.
  * Note: The results are the given and expected values for the indicated node voltages.

<table>
<thead>
<tr>
<th>TIME(Seconds)</th>
<th>V(1) (Volts)</th>
<th>V(3)=LOG(V(1)) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1000</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>100000</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0.1</td>
<td>-1</td>
</tr>
<tr>
<td>5</td>
<td>0.1</td>
<td>-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TIME(Seconds)</th>
<th>V(2) (Volts)</th>
<th>V(4)=LOG(V(2)) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>0.301029996</td>
</tr>
<tr>
<td>2</td>
<td>3.77</td>
<td>0.57634135</td>
</tr>
<tr>
<td>3</td>
<td>6.49</td>
<td>0.812244697</td>
</tr>
<tr>
<td>4</td>
<td>13.1</td>
<td>1.117271296</td>
</tr>
<tr>
<td>5</td>
<td>13.1</td>
<td>1.117271296</td>
</tr>
</tbody>
</table>

V1 1 0 PWL(0S 100V 1S 1000V 2S 1E5V 3S 1V 4S 0.1V)
R1 1 0 1
V2 2 0 PWL(0S 1V 1S 2V 2S 3.77V 3S 6.49V 4S 13.1V)
R2 2 0 1
B3 3 0 V = {LOG(V(1))}
R3 3 0 1
B4 4 0 V = {LOG(V(2))}
R4 4 0 1
.TRAN 1S 5S 0 1S
.PRINT TRAN V(1) V(2) V(3) V(4)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the Log_{10} Circuit

![Graph showing simulation results for V(1), V(2), V(3), and V(4).]
3.1.7 Test Circuit for the Sine, Cosine and Tangent Functions

* Tier No.: 1
* Directory/Circuit Name: ABM_SCT/sct.cir
* Description: Test of the analog behavioral modeling sine, cosine and tangent functions.
* Input: VS
* Output: V(2), V(3), V(4), V(5)
* Analysis:
  * A DC voltage source, VS or V(1), is used as the circuit input. Four nonlinear dependent
    voltage sources are used to define the functions as follows:
  * V(2)=B2=SIN(V(1)) = sine of input source
  * V(3)=B3=COS(V(1)) = cosine of input source
  * V(4)=B4=TAN(V(1)) = tangent of input source
  * V(5)=B5=V(2)/V(3) = mathematical evaluation of the tangent function(SIN/COS)

* This table is a set of hand calculations for the SIN, COS and TAN functions

<table>
<thead>
<tr>
<th>X</th>
<th>SIN(X)</th>
<th>COS(X)</th>
<th>TAN(X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.0000000</td>
<td>1.0000000</td>
<td>0.0000000</td>
</tr>
<tr>
<td>0.5</td>
<td>0.479425539</td>
<td>0.877582562</td>
<td>0.54630249</td>
</tr>
<tr>
<td>1</td>
<td>0.841470985</td>
<td>0.540302306</td>
<td>1.557407725</td>
</tr>
<tr>
<td>1.5</td>
<td>0.997494987</td>
<td>0.070737202</td>
<td>14.10141995</td>
</tr>
<tr>
<td>1.6</td>
<td>0.999573603</td>
<td>-0.029199522</td>
<td>34.23253274</td>
</tr>
<tr>
<td>2</td>
<td>0.909297427</td>
<td>-0.416146837</td>
<td>-2.185039863</td>
</tr>
<tr>
<td>2.5</td>
<td>0.598472144</td>
<td>-0.801143616</td>
<td>-0.747022297</td>
</tr>
<tr>
<td>3</td>
<td>0.141120008</td>
<td>-0.989992497</td>
<td>-0.142546543</td>
</tr>
<tr>
<td>3.1</td>
<td>0.041580662</td>
<td>-0.99913515</td>
<td>-0.041616655</td>
</tr>
<tr>
<td>3.2</td>
<td>-0.058374143</td>
<td>-0.998294776</td>
<td>0.058473854</td>
</tr>
<tr>
<td>4</td>
<td>-0.756802495</td>
<td>-0.653643621</td>
<td>1.157821282</td>
</tr>
<tr>
<td>4.6</td>
<td>-0.993691004</td>
<td>-0.112152527</td>
<td>8.860174896</td>
</tr>
<tr>
<td>4.62</td>
<td>-0.995735173</td>
<td>-0.092257602</td>
<td>10.7929878</td>
</tr>
<tr>
<td>4.63</td>
<td>-0.996607947</td>
<td>-0.082295803</td>
<td>12.11007099</td>
</tr>
<tr>
<td>4.69</td>
<td>-0.999749377</td>
<td>-0.02238711</td>
<td>44.65736663</td>
</tr>
<tr>
<td>5</td>
<td>-0.958924275</td>
<td>0.283662185</td>
<td>-3.38051506</td>
</tr>
<tr>
<td>5.5</td>
<td>-0.705540326</td>
<td>0.708669774</td>
<td>-0.995584052</td>
</tr>
<tr>
<td>6</td>
<td>-0.279415498</td>
<td>0.960170287</td>
<td>-0.291006191</td>
</tr>
<tr>
<td>6.2</td>
<td>-0.083089403</td>
<td>0.996542097</td>
<td>-0.083377715</td>
</tr>
<tr>
<td>6.5</td>
<td>0.215119988</td>
<td>0.976587626</td>
<td>0.2202772</td>
</tr>
</tbody>
</table>

VS 1 0 0
R1 1 0 1
B2 2 0 V = {SIN(V(1,0))}
R2 2 0 1
B3 3 0 V = {COS(V(1,0))}
R3 3 0 1
B4 4 0 V = {TAN(V(1,0))}
R4 4 0 1
B5 5 0 V = {V(2)/V(3)}
ChileSPICE Simulation Results for the SIN, COS and TAN Circuit

VS (Volts)

V(2) & V(3) (Volts)

V(4) & V(5) (Volts)

V(2) V(3) V(4) V(5)
3.1.8 Test Circuit for the Square Root Function
******************************************************************************
* Tier No.:     1
* Directory/Circuit Name: ABM_SQRT/sqrt.cir
* Description: Test of the analog behavioral modeling square root function.
* Input: VS  
* Output: V(1), V(2), V(3)
* Analysis:
  * A piece-wise linear input voltage source, VS or V(1) is used to define various voltages in
    time.
  * Two nonlinear dependent voltage sources are used to define the functions as follows:
    * V(2)=B2=SQRT(V(1)) = square root of V1
    * V(3)=B3=(V(2)**2  = value of B2 source squared = V1
  *
  * This table shows hand calculations for the square root and square functions
  * The X values represent the values of VS
  *
  * | V(1) | SQRT(V(1)) | V(1)*V(1) |
  * |------|-----------|----------|
  * | 0    | 0         | 0        |
  * | 1    | 1         | 1        |
  * | 4    | 2         | 4        |
  * | 9    | 3         | 9        |
  * | 16   | 4         | 16       |
  * | 25   | 5         | 25       |
  * | 36   | 6         | 36       |
  * | 49   | 7         | 49       |
  * | 390625 | 625      | 3.91E05  |
  * | 998001 | 999      | 998001   |
  * | 1.00E+06 | 1000    | 1000000  |
  * | 1.00E+08 | 10000   | 10000000 |
  * | 1.00E+10 | 100000  | 100000000 |
  *
******************************************************************************
VS  1  0  PWL(0S 0V  1S 1V 2S 4V  3S 9V  4S 16V  5S 25V  6S 36V  7S 49V  8S 390625V
  +    9S 998001V 10S 1E6V 11S 1E8V 12S 1E10V)
R1  1  0  1
* SOURCE THAT TAKES THE SQUARE ROOT OF V1
B2  2  0  V = {SQRT(V(1))}
R2  2  0  1
* SOURCE THAT SQUARES THE VALUE OF B2
* RESULTING IN THE ORIGINAL VALUE OF V1
B3  3  0  V = {V(2) * *2}
R3  3  0  1
.TRAN 1S 12S 0 1S
.PRINT TRAN V(1) V(2) V(3)
.OPTIONS ACCT
.END

27
ChileSPICE Simulation Results for the Square Root Netlist

![Graph showing the relationship between Log(V(1)) and Log(V(2)) and Log(V(3)).]
3.1.9 Test Circuit for the F(Y,T) Functionality

* Tier No.: 1
* Directory/Circuit Name: ABM_TIME/time.cir
* Description: Test of the analog behavioral modeling function for using time as a variable
  * defining a nonlinear dependent voltage source
* Input: VS=V(1)
* Output: V(1), V(2)
* Analysis:
  * A piecewise linear voltage source, VS or V(1), is used as the circuit input.
  * Nonlinear dependent voltage sources are used to define the function as follows:
  * \[ V(2) = B2 = V(1) \times \text{TIME} \]
  * where, V(1) is the input voltage and time is the simulation time specified
  * on the .tran line. The resulting values for V(2) are the product of V(1),
  *
  * This table is a set of hand calculations for the B1=V(2) function:
  * \[
  \begin{array}{ccc}
  \text{TIME} & \text{VS=V(1)} & V(2)=V(1)\times\text{TIME} \\
  \hline
  0s & 0V & 0V \\
  1s & 5V & 5V \\
  2s & 10V & 20V \\
  3s & 10V & 30V \\
  4s & 5V & 20V \\
  5s & 0V & 0V \\
  6s & 0V & 0V \\
  \end{array}
  \]

VS 1 0 PWL(0S 0V 1S 5V 2S 10V 3S 10V 4S 5V 5S 0V 6S 0V)
R1 1 0 1K
B2 2 0 V=(V(1) * TIME)
R2 2 0 1K
.TRAN 0S 6S 0S 1S
.PRINT TRAN V(1) V(2)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the F(Y,T) Circuit
3.1.10 Test Circuit for the AND Gate

* Tier No.: 1
* Directory/Circuit Name: AND/and.cir
* Description: Test of the digital AND gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
* Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to an
* AND gate, which is defined internal to the code by a subcircuit. Parameters are defined
* in the netlist (by the .PARAMS statement) and passed into the AND subcircuit. The
* subcircuit uses the parameters to establish the following values of the output voltage:
* Rise Time = default_rise= rise/fall output voltage = 1ns
* Margin = default_margin = margin for output to exceed min/max logic levels = 0.5V
* High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
* Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
* The logic for the AND gate is the output is high if and only if both inputs are high; for all
* other combination, the output is low. This truth table shows the AND expected output
* for the given A and B time dependent inputs.
*
* TIME A(Volts) B(Volts) OUT(Volts)
* 0S 0 0 0
* 1S 0 0 0
* 2S 0 0 0
* 3S 0 5 0
* 4S 0 5 0
* 5S 5 0 0
* 6S 5 0 0
* 7S 5 5 5
* 8S 5 5 5
* 9S 5 5 5
* NOTE: Low = 0V High=5V

* Set digital default parameters
.PARAM default_rise=1ns
.PARAM default_delay=0
.PARAM default_low=0.5V
.PARAM default_high=4.5V
.PARAM default_margin=0.5V

* Gate Inputs
VA A 0 0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
VB B 0 0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)
X_AND A B OUT AND
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the AND Gate Circuit

![Graph showing simulation results for an AND gate circuit with voltage and time axes.]
3.1.11 Test Circuit for the Capacitor

* Tier No.: 1
* Directory/Circuit Name: CAPACITOR/capacitor.cir
* Description: Test of the capacitor model using a simple RC circuit configuration.
* Input: VIN
* Output: V(1), V(2)
* Analysis:
* A series RC circuit is connected to a pulsed voltage source that goes from
* 0V to 1V after a 10us delay, with rise and fall times of 1us. The capacitor
* voltage should reach 90% of its maximum value, 1V, in
*   time = (3*R*C) + rise + delay
*   = (3 * 1E3 * 20E-9) + 1E-6 + 10E-6
*   = 71us
* where R=1E3 and C=20E-9
* Therefore, at 71us, the capacitor voltage should be at least 0.9V.
* A transient analysis of the circuit voltage versus time is performed to determine
* the capacitor voltage, V(2).

VIN 1 0 PULSE(0 1 10U 1U 1U 80U)
R 1 2 1K
C 2 0 20N
.TRAN 5U 100U 0 5U
.PRINT TRAN V(1) V(2)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the Capacitor Circuit

Voltage (Volts)

Time (seconds)

V(1)  V(2)
3.1.12 Test Circuit for the Current Controlled Current Source (CCCS)

Tier No.: 1
* Directory/Circuit Name: CCCS/cccs.cir
* Description: Test of current controlled current source, CCCS, model using a simple resistor circuit. A DC operating point analysis is performed to obtain the transfer function characteristics of the circuit i.e., Rin, Rout, and voltage gain, Vout/Vin.
* Input: VS
* Output: V(2), V(3), Rin, Rout, V(3)/VS
* Analysis:
* The CCCS, F, is a current source that is controlled by the current through the input source, VS, and is defined as:
  * \( F = k \cdot I = -3 \cdot I(\text{VS}) \)
  * where
  * \( I(\text{VS}) = \frac{\text{VS}}{(R1 + R2)} = \frac{20}{(4000)} = 5\text{mA} \)
  * Therefore,
  * \( k \cdot I(\text{VS}) = -3 \cdot 5\text{mA} = -15\text{mA} \)
* The current through the dependent source is divided evenly through resistors R3 and R4 (which are in parallel) giving –7.5 mA through each resistor. The -7.5mA currents go from node 3 to node 0 (anode to cathode), making the voltage at node 3,
* \( V(3) = -(R3 \cdot 7.5\text{mA}) = -(500 \cdot 7.5\text{mA}) = -3.75V \)
* Additionally, the voltage at node 2, Rin, Rout and the voltage gain (V(3)/VS) are:
  * \( V(2) = I \cdot R2 = 5\text{mA} \cdot 2500 = 12.5V \)
  * \( \text{Rin} = R1 + R2 = 2500 + 1500 = 4\text{K Ohms} \)
  * \( \text{Rout} = R3 || R4 = 500 || 500 = 250 \text{ Ohms} \)
  * \( \text{GAIN} = V(3)/V1 = -3.75/20 = -0.1875 \)

VS 1 0 20V
F 3 0 VS -3
R1 1 2 1500
R2 2 0 2500
R3 3 0 500
R4 3 0 500
.DC VS 20 20 1
.PRINT DC V(1) V(2) V(3)
.OPTIONS ACCT
.TF V(3) VS
.END
**ChileSPICE Simulation Results for the CCCS Circuit:**

Current Controlled Current Source Circuit (CCCS)
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(1)</th>
<th>v(2)</th>
<th>v(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.000000E+01</td>
<td>2.000000E+01</td>
<td>1.250000E+01</td>
<td>-3.750000E+00</td>
</tr>
</tbody>
</table>

Transfer function information:
- **GAIN** = transfer function = -1.87500E-01
- **ROUT** = output impedance at v(3) = 2.500000E+02
- **RIN** = v_input impedance = 4.000000E+03
3.1.13 Test Circuit for the Current-Controlled Voltage Source (CCVS)

* Tier No.: 1
* Directory/Circuit Name: CCVS/ccvs.cir
* Description: Test of current controlled voltage source model using a simple resistor circuit.
  * A DC operating point analysis is performed to obtain the transfer function characteristics of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
* Input: VIN
* Output: V(2), V(3), V(4), I(VIN), Rin, Rout, V(4)/VIN
* Analysis:
  * The CCVS, H, is a voltage source controlled by the current through the input voltage source, VIN. H is defined as \( k \cdot I = -0.5 \cdot I \). The parameter k must have units of ohms for the product of k and I to be volts. Therefore,
  * \( H = V(3) = k \cdot I(VIN) = -0.5 \cdot I(VIN) \)
  * where,
    * \( I(VIN) = -VIN / (R1 + R2) = 15 / (5 + 10) = -1mA \)
  * Note: I(VIN) is referenced from the negative to positive node of VIN, which makes its value negative. The voltage of the dependent source is
    * \( H = V(3) = -0.5 \cdot -1mA = 0.5V \)
  * The voltages at nodes 2 and 4 are
    * \( V(2) = VIN \cdot R2/(R1+R2) = 15 \cdot 5 / (5 + 10) = 5V \)
    * \( V(4) = V(3) \cdot R4/(R3+R4) = 0.5V \cdot 25 / (25+25) = 0.25V \)
  * Additionally, Rin, Rout and the voltage gain are
    * \( Rin = R1 + R2 = 10 + 5 = 15 \) Ohms
    * \( Rout = R3||R4 = 25||25 = 12.5 \) Ohms
    * \( Gain = V(4)/VIN = 0.25/15 = 1.667E-2 \)

VIN 1 0 15V
H 3 0 VIN -0.5
R1 1 2 10
R2 2 0 5
R3 3 4 25
R4 4 0 25
.DC VIN 15 15 1
.PRINT DC V(2) V(3) V(4) I(VIN)
.OPTIONS ACCT
.TF V(4) VIN
.END
ChileSPICE Simulation Results for the CCVS Circuit:

Current-Controlled Voltage Source Circuit (CCVS)

DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(2)</th>
<th>v(3)</th>
<th>v(4)</th>
<th>vin_branch</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V(1) = VIN</td>
<td>I(VIN)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1.500000E+01</td>
<td>5.000000E+00</td>
<td>5.000000E-01</td>
<td>2.500000E-01</td>
<td>-1.000000e+00</td>
</tr>
</tbody>
</table>

Transfer function information:
- GAIN = transfer_function = 1.666667E-02
- ROUT = output_impedance_at_v(4) = 1.250000E+01
- RIN = vin_input_impedance = 1.500000E+01
### 3.1.14 Test Circuit for the Diode

**Tier No.:** 1  
**Directory/Circuit Name:** DIODE/DIODE.cir  
**Description:** Simple diode circuit to test the validity of the diode model.  
**Input:** VIN  
**Output:** V(3), I(VMON)  
**Analysis:**

A diode is forward biased with a 5V input source, VIN. With a 100fA saturation current, Is, the diode current, I(VMON) or Id, and voltage, Vd, are determined by the following equations:

1. \( I_d = I_s \left[ \exp\left(\frac{V_d}{V_t}\right) - 1 \right] \)
2. \( V_{in} = I_d R + V_d = I_s \left[ \exp\left(\frac{V_d}{V_t}\right) - 1 \right] R + V_d \)

where,

- \( V_t = 25.86 \text{mV} \)
- \( R = 2 \text{K} \)
- \( I_s = 100 \text{fA} \)
- \( V_{in} = 5 \text{V} \)

The diode voltage can be calculated by finding the value of Vd that makes equation (2) true. The diode current can be found by solving (1) after Vd is found.

Therefore,

- \( V_d = 0.6158 \text{V} \) and \( I_d = 2.19 \text{mA} \)

ChileSPICE Simulation Results for the DIODE Circuit:

```
VIN 1 0 DC 5V  
R1 1 2 2K  
D1 3 0 DMOD  
VMON 2 3 0  
.MODEL DMOD D (IS=100FA)  
.DC VIN 5 5 1  
.PRINT DC I(VMON) V(3)  
.OPTION ACCT  
.END
```

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon_branch</th>
<th>v(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>ID</td>
<td>VD</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>5.000000E+00</td>
<td>2.192078E-03</td>
<td>6.158450E-01</td>
</tr>
</tbody>
</table>
3.1.15 Test Circuit for the Exponential Current Source

* Tier No.: 1
* Directory/Circuit Name: IEXP/IEXP.cir
* Description: Test of model for an independent current source.
* Input: IEXP
* Output: I(VMON)
* Analysis:
  * The input is described as an exponential time dependent current source, IEXP, that has an initial value of 1A for the first 1s of the simulation. The current rises exponentially from 1A to 5A within 1s, with a 0.2s rise time constant. It then decays from 5A to 1A with a 0.5s fall time constant.
  * The general format for an exp voltage source is
    * EXP (I1 I2 TD1 TAU1 TD2 TAU2)
  * Where,
    * I1=initial value=1A  I2=pulsed value=5A  TD1=rise time delay=1s
    * TAU1=rise time constant=0.2s  TD2=fall delay time=2S  TAU2=fall time constant=0.5S
  * The current is described by the following equation:
    * for t between 0 and TD1
      * IEXP=I1
    * for t between TD1 and TD2
      * IEXP = i(t)=I1 + (I2-I1)*(1-EXP(-(TIME-TD1)/TAU1))
    * for t between TD2 and TSTOP
      * IEXP=i(t) + (I1-I2)*(1-EXP(-(TIME-TD2)/TAU2))
  * Therefore for given values of time, the expected current is:
    * T(seconds)       IEXP(T)
    * 01
    * 11
    * 1.5 4.67
    * 3 1.54
    * 51
  * A zero volt source, VMON, is used as an ammeter to measure the current from the IEXP source. A resistor is used to provide a closed loop for current flow.

IEXP 0 1 EXP(1A 5A 1S 0.2S 2S 0.5S)
R 2 0 500
VMON 1 2 0
.TRAN 1S 5S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END
ChileSPICE Simulation Results for the Exponential Current Source Circuit
3.1.16 Test Circuit for the Inductor
*****************************************************************************
* Tier No.:  1
* Directory/Circuit Name:  INDUCTOR/INDUCTOR.cir
* Description: Circuit netlist to test validity of the inductor model.
* Input: B1=I
* Output: I(VMON), V(3)
* Analysis:
* A small resistor and a zero volt source, VMON, is placed in series with the inductor.
* However, the inductor is essentially in parallel with the input current source, IS. The
* input current, defined by a nonlinear dependent source, B1, is:
* \[ B1 = I = 10t e^{-5t} \quad \text{for } t > 0 \]
* The voltage generated by the inductor is given by:
* \[ V(3) = L \frac{dI}{dt} = L \frac{d(10t e^{-5t})}{dt} = 10L e^{-5t} (1 - 5t) \]
* where \( L = \text{inductor value} = 10\text{mH} \)
* The table below shows calculated values of the inductor’s current and voltage, I and
* V(3), for given values time:
* Time (Seconds)    I (Amps)    V(3) (Volts)
* 0.001    0.009950125    0.099501248
* 0.002    0.019800997    0.098508719
* 0.003    0.029553358    0.097523615
* 0.004    0.039207947    0.096545887
* 0.005    0.048765496    0.095575487
* 0.006    0.058226732    0.094612364
* 0.007    0.067592379    0.093656471
* 0.008    0.076863155    0.09270776
* 0.009    0.086039773    0.091766182
* 0.01     0.095122942    0.090831691
* 0.011    0.104113366    0.089904238
* 0.012    0.113011744    0.088983778
* 0.013    0.12181877     0.088070262
* 0.014    0.130535135    0.087163645
* 0.015    0.139161523    0.086263882
* 0.016    0.147698615    0.085370925
* 0.017    0.156147088    0.084484729
* 0.018    0.164507613    0.08360525
* 0.019    0.172780858    0.082732442
* 0.02     0.180967484    0.081866261
*****************************************************************************
B1 0 1 I = (10 * TIME * EXP( - 5*TIME))
VMON 1 2 0
R1 2 3 0.000001
L1 3 0 10mH
.TRAN 0 20MS
.PRINT TRAN I(VMON) V(3)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the Inductor Circuit

![Graph showing simulation results for the inductor circuit. The graph plots current (Amps) against time (Seconds) and voltage (Volts) against time (Seconds). The legend indicates two curves: I(VMON) and V(3).]
3.1.17 Test Circuit for the Pulse Current Source

******************************************************************************

* Tier No.: 1
* Directory/Circuit Name: IPULSE/IPULSE.cir
* Description: Test of the model for an independent current source.
* Input: IPULSE
* Output: I(VMON)
* Analysis:
  * The current source is described as a pulse signal that starts at 1A and stays there for 1
  * second. Then the current increases linearly from 1A to 5A during the next 0.1s and stays
  * at 5A for 0.5s. It then decreases linearly from 5A to 1A in 0.4s. It stays at 1A for 1s.
  * The cycle is repeated (except for the initial delay) two more times between 3s and 7s.
  * A zero volt source, VMON, is used as an ammeter to measure the current from the
  * IPULSE source. A resistor is used to provide a closed loop for current flow.
******************************************************************************

IPULSE 0 1 PULSE(1A 5A 1S 0.1S 0.4S 0.5S 2S)
R 2 0 500
VMON 1 2 0
.TRAN 1S 7S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END

ChileSPICE Simulation Results for the IPULSE Current Source Circuit

[Graph showing the simulation results with a pulse current profile]

Time (Seconds)

Current (Amps)

ChileSPICE Simulation Results for the IPULSE Current Source Circuit
3.1.18 Test Circuit for the Piece Wise Linear Current Source

******************************************************************************
* Tier No.: 1
* Directory/Circuit Name: IPWL/IPWL.cir
* Description: Test of model for an independent pulse current source.
* Input: IPWL
* Output: I(VMON)
* Analysis:
  * A piece-wise linear current source, IPWL, which is a series of time and current pairs of
  * data points given by:
  *
<table>
<thead>
<tr>
<th>Index</th>
<th>Time(s), Current(amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(0.0 , 0.0)</td>
</tr>
<tr>
<td>2</td>
<td>(1.0, 0.0)</td>
</tr>
<tr>
<td>3</td>
<td>(1.2 , 5.0)</td>
</tr>
<tr>
<td>4</td>
<td>(1.4 , 2.0)</td>
</tr>
<tr>
<td>5</td>
<td>(2.0 , 4.0)</td>
</tr>
<tr>
<td>6</td>
<td>(3.0 , 1.0)</td>
</tr>
</tbody>
</table>
  *
  * A zero volt source, VMON, is used as an ammeter to measure the current from the IPWL
  * source. A resistor is used to provide a closed loop for current flow.
******************************************************************************
IPWL 0 1 PWL(0 0A 1S 0A 1.2S 5A 1.4S 2A 2S 4A 3S 1A)
R 2 0 500
VMON 1 2 0
.TRAN 1S 5S
.OPTIONS ACCT
.PRINT TRAN I(VMON)
.END
ChileSPICE Simulation Results for IPWL Current Source Circuit

![Graph showing current (Amps) over time (Seconds)]

Time (Seconds)

Current (Amps)

- vmon_branch
3.1.19 Test Circuit for the Single Frequency FM Source (ISFFM) Current Source

* Tier No.: 1
* Directory/Circuit Name: ISFFM/isffm.cir
* Description: Test of the model for single-frequency frequency modulated (SFFM) transient independent current source.
* Input: ISFFM
* Output: I(VMON)
* Analysis:
  * A single frequency frequency-modulation signal that has no initial current and a peak amplitude of 5A. It has a carrier frequency of 10KHz. For the 1ms transient analysis, 10 cycles of the carrier will be output in the 1ms time. The carrier is modulated at a rate determined by the single frequency (1KHz) and the modulation index (3).
  * The general format for a sffm transient function on a source statement is
    SFFM (IO IA FC MDI FS)
  * where,
    * IO=offset current = 0A   IA=amplitude = 5A
    * FC=carrier frequency = 10kHz  MDI=modulation index = 3
    * FS=signal frequency = 1kHz
  * The current is described by the following equation:
    * ISFFM(t)= IO + IA*sin(2*pi*FC*t + MDI*sin(2*pi*FS*t))
  * Therefore, at the given values of time, the current should be:

<table>
<thead>
<tr>
<th>T</th>
<th>ISFFM(T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000E+00</td>
<td>0.0000E+00</td>
</tr>
<tr>
<td>1.0000E-04</td>
<td>4.9076E+00</td>
</tr>
<tr>
<td>2.0000E-04</td>
<td>1.4222E+00</td>
</tr>
<tr>
<td>3.0000E-04</td>
<td>1.4222E+00</td>
</tr>
<tr>
<td>4.0000E-04</td>
<td>4.9076E+00</td>
</tr>
<tr>
<td>5.0000E-04</td>
<td>2.1244E-06</td>
</tr>
<tr>
<td>6.0000E-04</td>
<td>-4.9076E+00</td>
</tr>
<tr>
<td>7.0000E-04</td>
<td>-1.4222E+00</td>
</tr>
<tr>
<td>8.0000E-04</td>
<td>-1.4222E+00</td>
</tr>
<tr>
<td>9.0000E-04</td>
<td>-4.9076E+00</td>
</tr>
</tbody>
</table>

* A zero volt source, VMON, is used as an ammeter to measure the current from the ISFFM source. A resistor is used to provide a closed loop for current flow.

ISFFM 0 1 SFFM(0 5 10KHZ 3 1KHZ)
R1 2 0 1
VMON 1 2 0
.TRAN 5US 1MS 0 5US
.PRINT TRAN I(VMON)
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the ISFFM Circuit

![Graph showing current and time relationship for the ISFFM Circuit](image-url)
3.1.20 Test Circuit for the Sinusoidal Current Source

A time dependent current source that supplies a sinusoidal signal of 0.3A initial current, 1A amplitude and a 500Hz frequency with no initial time delay. The transient analysis of 6ms will give 3 cycles of a damped sine wave. The damping factor is 500.

The general format for the sinusoidal function in the current source is

\[ \text{SIN}(\text{IO} \text{ IA} \text{ FREQ} \text{ TD} \text{ THETA}) \]

where,

- \( \text{IO} \) = offset current = 0.3A
- \( \text{IA} \) = amplitude = 1A
- \( \text{FREQ} \) = frequency = 500Hz
- \( \text{TD} \) = time delay = 0
- \( \text{THETA} \) = damping factor = 500

The current is described by the following equation for time > TD:

\[ \text{ISIN}(t) = \text{IO} + \text{IA} \cdot \sin(2\pi \text{FREQ}(t - \text{TD})) \cdot \exp(-\text{THETA}(t - \text{TD})) \]

Therefore, at given values of time, the current should be:

<table>
<thead>
<tr>
<th>T</th>
<th>ISIN(T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.3</td>
</tr>
<tr>
<td>0.0005</td>
<td>1.078800783</td>
</tr>
<tr>
<td>0.001</td>
<td>0.299999972</td>
</tr>
<tr>
<td>0.0015</td>
<td>-0.172366553</td>
</tr>
<tr>
<td>0.002</td>
<td>0.300000034</td>
</tr>
<tr>
<td>0.0025</td>
<td>0.586504797</td>
</tr>
<tr>
<td>0.003</td>
<td>0.299999969</td>
</tr>
<tr>
<td>0.0035</td>
<td>0.126226057</td>
</tr>
<tr>
<td>0.004</td>
<td>0.300000025</td>
</tr>
<tr>
<td>0.0045</td>
<td>0.405399225</td>
</tr>
<tr>
<td>0.005</td>
<td>0.299999981</td>
</tr>
<tr>
<td>0.0055</td>
<td>0.236072139</td>
</tr>
<tr>
<td>0.006</td>
<td>0.300000014</td>
</tr>
</tbody>
</table>

A zero volt source, VMON, is used as an ammeter to measure the current from the ISIN source. A resistor is used to provide a closed loop for current flow.

\[ \text{ISIN 0 1 SIN(0.3A 1A 500HZ 0 500)} \]

\[ \text{R 2 0 1} \]

\[ \text{VMON 1 2 0} \]

\[ \text{.TRAN 0.06MS 6MS} \]

\[ \text{.PRINT TRAN I(VMON)} \]

\[ \text{.OPTIONS ACCT} \]

\[ \text{.END} \]
ChileSPICE Simulation Results for the ISIN Circuit

![Graph showing the simulation results of the ISIN Circuit. The x-axis represents time in seconds ranging from 0 to 0.006, and the y-axis represents current in amps ranging from -0.20 to 1.20. The graph plots the current through a branch labeled 'vmon_branch'.]
3.1.21 Test Circuit for the Current-Controlled Switch

Tier No.: 1
Directory/Circuit Name: ISWITCH/iswitch.cir
Description: Test of the model for a current controlled switch. The switch behaves like a resistor that toggles between a very small off resistance, and a very large on resistance which depends upon the controlling current.

Input: IS
Output: I(VMON), I(VMON1) Current through R1 and R2 (measured with 2 zero volt ammeters)

Analysis:
A DC current source, IS, is stepped from 0 to 2mA. The current in the switch, W, is controlled by the current through R1 (measured through VMON), supplied by the DC input source IS. The switch is initially open, thereby allowing no current to flow due to a large off resistance, ROFF=1E6 Ohms, of the switch. When the current through R1 reaches ION=10mA, the switch nears transition to the on state, and the switch resistance value is RON=1 Ohm. The current through R1 and R2 increase linearly from 15 to 40mA because the current is now split equally between the two 100 Ohm resistors.

The controlling current and the switch current are defined by the following equations:

\[ I_{\text{switch}} = I(VMON1) = IS - I(VMON1) \]
\[ I(VMON) = IS \times \left( \frac{R2 + Rs}{R1 + Rs + R2} \right) = \]

where,

\[ I(VMON1) = \text{switch current measure through a zero value voltage source}, \]
\[ VMON1 \]
\[ I(VMON) = \text{controlling current measured through a zero value voltage source}, \]
\[ VMON \]
\[ Rs = \text{switch resistance} \]

The switch resistance is defined by the following equations:

With ION > IOFF:

For \( Ic \leq ION \)
\[ Rs = ROFF \]
For \( IOFF < Ic < ION \)
\[ Rs = \exp(Lm + 3*Lr*(Ic-Im)/(2*Id) - 2*Lr*(Ic-Im)^3 / (Id)^3) \]
For \( Ic \geq ION \)
\[ Rs = RON \]

Where,
\[ Ic = \text{controlling current} = I(VMON) \]
\[ IOFF = \text{control current for the “off” state} = 0 \text{ ma} \]
\[ ION = \text{control current for the “on” state} = 10 \text{ ma} \]
\[ ROFF = \text{“Off” resistance} = 1 \text{ MOhm} \]
\[ RON = \text{“On” resistance} = 1 \text{ Ohm} \]
\[ Lm = \ln(SQRT(RON*ROFF)) = 6.908 \]
\[ Lr = \ln(RON/ROFF) = -13.816 \]
\[ Im = (ION+IOFF)/2 = .005 \]
\[ Id = (ION-IOFF)= 0.01 \]

The table below is a hand calculation of the switch resistance and the current,
I(VMON1), through the switch as a function of the controlling current.

<table>
<thead>
<tr>
<th>IS</th>
<th>I(VMON)</th>
<th>Rs</th>
<th>I(VMON1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00E+00</td>
<td>0.00000</td>
<td>1000000.00</td>
<td>0.00000</td>
</tr>
<tr>
<td>5.00E-03</td>
<td>0.00458</td>
<td>1000.24</td>
<td>0.00042</td>
</tr>
<tr>
<td>1.00E-02</td>
<td>0.00502</td>
<td>1.00</td>
<td>0.00498</td>
</tr>
<tr>
<td>1.50E-02</td>
<td>0.00754</td>
<td>1.00</td>
<td>0.00746</td>
</tr>
<tr>
<td>2.00E-02</td>
<td>0.01005</td>
<td>1.00</td>
<td>0.00995</td>
</tr>
<tr>
<td>2.50E-02</td>
<td>0.01256</td>
<td>1.00</td>
<td>0.01244</td>
</tr>
<tr>
<td>3.00E-02</td>
<td>0.01507</td>
<td>1.00</td>
<td>0.01493</td>
</tr>
<tr>
<td>3.50E-02</td>
<td>0.01759</td>
<td>1.00</td>
<td>0.01741</td>
</tr>
<tr>
<td>4.00E-02</td>
<td>0.02010</td>
<td>1.00</td>
<td>0.01990</td>
</tr>
</tbody>
</table>

*****************************************************************************
IS 0 1 DC 40mA
VMON 1 1A 0V
R1 1A 0 100
VMON1 2 3 0
R2 3 0 100
W 1 2 VMON W1 OFF
.MODEL W1 ISWITCH (ION=10mA IOFF=0mA RON=1 ROFF=1E6)
.DC IS 0 40mA 1mA
.PRINT DC I(VMON) I(VMON1)
.OPTIONS ACCT
.END

ChileSPICE Results for Current Controlled Switch Model

![Graph showing current as a function of controlling current]
3.1.22 Test Circuit for Mutually Coupled Inductors

* Tier No.: 1
* Directory/Circuit Name: MINDUCTORS/MINDUCTORS.cir
* Description: Test of mutually coupled inductors using coupling coefficient value of k=0.75
* Input: VS = V(1)
* Output: I(VS), V(2), V(3)
* Analysis:

  The circuit contains two coupled inductors, L1=1mH and L2=1mH, that form a transformer. The primary side of the transformer is connected to resistor R1 and the secondary is connected to resistor R2. The input signal, VS=V(1), is a 60Hz sinusoidal waveform with a peak voltage amplitude of 169.7 V. The rms value and radian frequency of the input signal are calculated as follows:

  V(1)rms = 0.707 * 169.7 = 119.98 V
  w = 2*π*frequency = 2 * 3.14159 * 60 Hz = 376.99 rads/s

  A voltage is induced across L2 from the current in L1. Using a coupling coefficient of k=0.75, the following calculations yield the current through the primary L1, I(VS), and the voltage across the primary and secondary inductors, V(2) and V(3), respectively:

  I1 = I(VS) = VS / SQRT (R1**2 + XL1**2)
  where,
  XL1 = inductive reactance of L1 = 2*π*frequency*L1= 376.99 * 1mH = 0.377 Ohms
  Therefore,
  I1 = 119.98 / SQRT (1000**2 + 0.377**2) = 0.1199 A rms
  = 0.1199/0.707 = 169.6 A peak
  V(2) = I * XL1 = 0.1199 * 0.377 = 0.0452 V rms
  = 0.0452/0.707= 63.9 V peak
  V(3) = k * V(2) = 0.75 * 0.0452 = 0.0339 V rms
  = 0.0339 * 0.707= 47.9 V rms

VS 1 0 SIN(0 169.7 60HZ)
R1 1 2 1K
R2 3 0 1K
L1 2 0 1mH
L2 3 0 1mH
K1 L1 L2 0.75
.TRAN 100US 25MS
.PRINT TRAN I(VS) V(2) V(3)
.OPTION ACCT
.END
ChileSPICE Simulation Results for MINDUCTORS Circuit

Time (seconds)

Voltage (Volts)

Current (Amps)

-8.00E-02
-6.00E-02
-4.00E-02
-2.00E-02
0.00E+00
2.00E-02
4.00E-02
6.00E-02
8.00E-02
0.00E+00 5.00E-03 1.00E-02 1.50E-02 2.00E-02 2.50E-02

V(2)  V(3)  I(VS)
3.1.23 Test Circuit for the NAND Gate

* Tier No.: 1
* Directory/Circuit Name: NAND/nand.cir
* Description: Test of the digital NAND gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
  * Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to an NAND gate, which is defined internal to the code by a subcircuit. Parameters are defined in the netlist (by the .PARAMS statement) and passed into the NAND subcircuit. The subcircuit uses the parameters to establish the following values of the output voltage:
  * Rise Time = default_rise = rise/fall output voltage = 1ns
  * Margin = default_margin = margin by which the output exceeds min/max logic levels
  * = 0.5V
  * High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
  * Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
  *
  * The logic for the NAND gate is the output is low if and only if both inputs are high, and for all other combination the output is high.
  * This truth table shows the NAND expected output for the given A and B time dependent inputs.

<table>
<thead>
<tr>
<th>TIME</th>
<th>A(Volts)</th>
<th>B(Volts)</th>
<th>OUT(Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>2S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>3S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>4S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>5S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>6S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>7S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>8S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>9S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
</tbody>
</table>

* NOTE: Low = 0V High=5V

Set digital default parameters
* .PARAM default_rise=1ns
* .PARAM default_delay=0
* .PARAM default_low=0.5V
* .PARAM default_high=4.5V
* .PARAM default_margin=0.5V

* Gate Inputs
  * VA A 0 0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
  * VB B 0 0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)

X_NAND A B OUT NAND
ChileSPICE Simulation Results for the NAND Gate Circuit
3.1.24 Test Circuit for the N-Channel JFET

* Tier No.: 1
* Directory/Circuit Name: NJFET/NJFET.cir
* Description: Circuit netlist to test current-voltage characteristics of the n-channel JFET model.
* Input: VDD
* Output: I(VMON), V(3,2), V(2)
* Analysis:
  * For the self-biased NJFET circuit the general algebraic solution for the bias point is:
  * \( ID = \frac{[-B - \sqrt{B^2 - 4*A*C}]}{2*A} \)
  * Where,
    * \( A = RS^2 = (600)^2 = 3.6E+5 \)
    * \( B = -\{2*|VP|*RS + (VP^2) / IDSS\} = -\{2 * 4 * 600 + 16/10.0E-3\} = -6.4E+3 \)
    * \( C = VP^2 = (-4)^2 = 16 \)
  * Therefore,
    * \( ID = \frac{[(-6.4E+3) - \sqrt{(-6.4E+3)^2 - 4 * 3.6E+5 * 16}]}{2 * 3.6E+5} = 3.009 \text{ mA} \)
    * \( VGS = ID*RS = 3.009E-3 * 600 = 1.806 \text{ V} \)
    * \( |VDS| = |VDD| - ID*(RD + RS) = 15 - 3.009E-3 * (1.5k + 600) = 8.7 \text{ V} \)
  * Note:
    * \( IDSS = BETA * VP**2 = 6.25E-4 * (-4)**2 = 10.0E-3 \text{ A} \)
    * \( VP = VTO = -4 \text{ V} \)
    * The circuit simulation should yield the following outputs:
      * \( I(VMON) = \text{Drain Current} \) \( Id = 3 \text{ mA} \)
      * \( V(3,2) = \text{Drain-Source Voltage} \) \( Vds= 8.7 \text{ V} \)
      * \( V(0,2) = \text{Gate-Source Voltage} \) \( Vgs= 1.8 \text{ V} \)

ChileSPICE Simulation Results for the NJFET Circuit:

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon_branch</th>
<th>v(3)-v(2)</th>
<th>v(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.500000E+01</td>
<td>3.009442E-03</td>
<td>8.680173E+00</td>
<td>1.805665E+00</td>
</tr>
</tbody>
</table>
**3.1.25 Test Circuit for the N-Channel MESFET**

************

* Tier No.: 1
* Directory/Circuit Name:
* Description: Test of a simple n channel MESFET circuit to examine the subthreshold characteristics of the device. Ideally, the drain current of a FET device should should reduce to zero when the device is biased below threshold. However, a residual subthreshold current exists in this regime. This circuit shows the turnoff properties of the ideal MESFET model.
* Input: Vgs and Vds
* Output: Ids
* Analysis:
  * This is a 1um NMESFET. The nominal threshold voltage is −1.3V. A DC transfer function analysis is described with Vgs swept from −1.75V to 0V in 50mV steps and Vds is stepped from 0.1V to 1.9V in 1.8V steps.
  * For the nonsaturation regime, where \( Vds \leq 3/\alpha \)
    \[
    Id = (1+\lambda*Vds)*\left\{\frac{\beta*(Vgs-Vto)^2}{1+B(Vgs-Vto)}\right\}*\left[1-(1-\alpha*Vds/3)^3\right]
    \]
  * For the saturation regime, where Vds>3/alpha,
    \[
    Id = (1+\lambda*VDS)*\left\{\frac{\beta*(Vgs-Vto)^2}{1+B(Vgs-Vto)}\right\}
    \]
  * \( \alpha = 3, \beta=1.4E-3, \lambda=0.03, Vto=-1.3, B=0.3 \) (default value)
  * for Vds = 0.1V, Vds which is less than 3/alpha or 1V,
    * @Vgs=-1.5V \( Id=-1.6E-12 \) A
    * @Vgs = -1V \( Id=4.4E-8 \) A
  * for Vds = 1.9V, which is greater than 3/alpha or 1V,
    * @Vgs=-1.5V \( Id=3.4E-12 \) A
    * @Vgs = 0.0V \( Id=1.8E-3 \) A
  * The drain current, Id, is measured through the VIDS zero volt source that acts as an ammeter.

************

```
VDS 1 0 0
VIDS 1 2 0
VGS 3 0 0
Z1 2 3 0 MESMOD AREA=1.4
.MODEL MESMOD NMF
+ RD=46 RS=46 VTO=-1.3 LAMBDA=0.03 ALPHA=3 BETA=1.4E-3
.DC VGS -1.75V 0 50MV VDS 0.1V 1.9V 1.8V
.PRINT DC I(VIDS)
.OPTIONS ACCT
.END
```
ChileSPICE Simulation Results for the NMESFET Circuit

![Graph showing the relationship between Ids (Amperes) and Vgs (Volts) for different Vds values (0.1V and 1.9V). The graph includes two curves, one for Ids@Vds=0.1V and another for Ids@Vds=1.9V. The y-axis represents Ids in logarithmic scale from 1.00E-12 to 1.00E-02, while the x-axis represents Vgs in linear scale from -1.80 to 0.20 Volts.]
3.1.26 Test Circuit for the N-Channel MOSFET

* Tier No.: 1
* Directory/Circuit Name: NMOS/NMOS1.cir
* Description: Circuit netlist to test current-voltage characteristics of the n-channel MOSFET model.
* Input: VDD
* Output: I(VMON) V(3,2) V(1,2)
* Analysis:

FOR THE NMOS CIRCUIT BIASED IN THE ACTIVE MODE OF OPERATION:

\[ \begin{align*}
 VG & = \frac{R_2}{R_1 + R_2} \cdot VDD = \frac{22 \times 10^6}{69 \times 10^6} \cdot 18 = 5.74V \\
 ID & = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \\
 & \text{Where,} \\
 A & = R_S^2 = (500)^2 = 2.5 \times 10^5 \\
 B & = -2 \{ (VG - VT) \cdot R_S + 1/KP \} = -2 \{ (5.74 - 2) \cdot 500 + 1/0.5 \times 10^{-3} \} = -7.74 \times 10^3 \\
 C & = (VG - VT)^2 = (5.74 - 2)^2 = 13.9876 \\
 & \text{Therefore,} \\
 ID & = \frac{-(-7.74 \times 10^3) - \sqrt{(-7.74 \times 10^3)^2 - 4 \cdot 2.5 \times 10^5 \cdot 2.5 \times 10^5 \cdot 13.9876}}{2 \cdot 2.5 \times 10^5} \\
 & = 1.927mA \\
 VGS & = VG - VS = VG - ID \cdot R_S = 5.74 - 1.927 \times 10^{-3} \cdot 500 = 4.78V \\
 VDS & = VDD - ID \cdot (R_D + R_S) = 18 - 1.927 \times 10^{-3} \cdot (2.7 \times 10^3) = 12.8V \\
 & \text{The circuit simulation should yield the following outputs:} \\
 & \text{I(VMON) = Drain Current} \quad \text{Id=1.927mA} \\
 & \text{V(3,2) = Drain-Source Voltage} \quad \text{Vds=12.8V} \\
 & \text{V(1,2) = Gate-Source Voltage} \quad \text{Vgs=4.776V} \\
\end{align*} \]

ChileSPICE Simulation Results for the NMOS Circuit:

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon_branch</th>
<th>v(3)-v(2)</th>
<th>v(1)-v(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.800000E+01</td>
<td>1.926428E-03</td>
<td>1.279864E+01</td>
<td>4.775916E+00</td>
</tr>
</tbody>
</table>
3.1.27 Test Circuit for the NOR Gate

* Tier No.: 1
* Directory/Circuit Name: NOR/nor.cir
* Description: Test of the digital NOR gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
  * Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to a
    NOR gate, which is defined internal to the code as a subcircuit. Parameters are defined
    in the netlist (by the .PARAMS statement) and passed into the NOR subcircuit. The
    subcircuit uses the parameters to establish the following values of the output voltage:
    * Rise Time = default_rise = rise/fall output voltage = 1ns
    * Margin = default_margin = margin by which the output exceeds min/max logic levels
    * = 0.5V
    * High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
    * Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
  * The logic for the NOR gate is the output is high if and only if both inputs are low; for any
    other combination the output is low.
  * This truth table shows the NOR expected output for the given A and B time dependent
    inputs.

<table>
<thead>
<tr>
<th>TIME</th>
<th>A(Volts)</th>
<th>B(Volts)</th>
<th>OUT(Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>2S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>3S</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>4S</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>5S</td>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6S</td>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>8S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>9S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
</tbody>
</table>

* NOTE: Low = 0V  High=5V

* Set digital default parameters
  .PARAM default_rise=1ns
  .PARAM default_delay=0
  .PARAM default_low=0.5V
  .PARAM default_high=4.5V
  .PARAM default_margin=0.5V
* Gate Inputs
  VA A 0 0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
  VB B 0 0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)
X_NOR A B OUT NOR
.TRAN 1S 9S
.PRINT TRAN V(A) V(B) V(OUT)
.OPTIONS ACCT
.END

ChileSPICE Simulation Results for the NOR Circuit

![Graph showing voltage over time for V(A), V(B), and V(OUT)]
3.1.28  Test Circuit for the NPN Bipolar Transistor

******************************************************************************
* Tier No.: 1
* Directory/Circuit Name: NPN/NPN1.cir
* Description: Circuit netlist to determine the current-voltage characteristics of the npn bipolar
*   transistor model. The circuit is configured as a common-emitter configuration.
* Input:  VCC
* Output: I(VMON1), I(VMON2), V(2)
* Analysis:
* FOR THE NPN CIRCUIT, DETERMINE:
*  IB = (VCC – VBE) / RB = (12 – 0.7) / 377E+3 = 29.9uA
*  IC = BETA * IB = 100 * 29.9E-6 = 2.99mA
*  VCE = VCC – IC*RC = 12 – (2.99E-3)*(2E+3) = 6.01V
* The circuit simulation should yield the following outputs:
*  I(VMON1) = Base Current     I_b = 29.7uA
*  I(VMON2) = Collector Current I_c = 2.97mA
*  V(2) = Emitter Collector Voltage V_{ce} = 6.06V
******************************************************************************

VCC  4 0 DC 12V
RC 3 4 2K
RB 4 5 377K
* ZERO VOLT SOURCES USED AS AMMETERS TO MEASURE THE
* BASE AND COLLECTOR CURRENTS, RESPECTIVELY
VMON1 5 1 0
VMON2 3 2 0
Q 2 1 0 NBJT
.MODEL NBJT NPN (BF=100)
.DC VCC 12 12 1
.PRINT DC I(VMON1) I(VMON2) V(2)
.OPTION ACCT
.END

ChileSPICE Simulation Results for the NPN Circuit:

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon1_branch</th>
<th>vmon2_branch</th>
<th>v(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.200000E+01</td>
<td>2.970195E-05</td>
<td>2.970196E-03</td>
<td>6.059609E+00</td>
</tr>
</tbody>
</table>
3.1.29 Test Circuit for the OR Gate

******************************************************************************
* Tier No.: 1
* Directory/Circuit Name: OR/or.cir
* Description: Test of the digital OR gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
  * Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to an OR gate, which is defined internal to the code by a subcircuit. Parameters are defined in the netlist (by the .PARAMS statement) and passed into the OR subcircuit. The subcircuit uses the parameters to establish the following values of the output voltage:
    * Rise Time = default_rise = rise/fall output voltage = 1ns
    * Margin = default_margin = margin which the output exceeds min/max logic levels = 0.5V
    * High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
    * Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
  * The logic for the OR gate is the output is high if and only if either one of the inputs is high. When both inputs are low, the output is low.
  * This truth table shows the OR expected output for the given A and B time dependent inputs.

<table>
<thead>
<tr>
<th>TIME</th>
<th>A(Volts)</th>
<th>B(Volts)</th>
<th>OUT(Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>4S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>5S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>6S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>7S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>8S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>9S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

* NOTE: Low = 0V  High=5V
******************************************************************************

* Set digital default parameters
  .PARAM default_rise=1ns
  .PARAM default_delay=0
  .PARAM default_low=0.5V
  .PARAM default_high=4.5V
  .PARAM default_margin=0.5V
* Gate Inputs
  VA A 0 0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
  VB B 0 0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)
  X_OR A B OUT OR
  .TRAN 1S 9S
  .PRINT TRAN V(A) V(B) V(OUT)
  .OPTIONS ACCT
  .END
ChileSPICE Simulation Results for the OR Gate Circuit
3.1.30 Test Circuit for the P-Channel Depletion Mode JFET

* Tier No.: 1
* Directory/Circuit Name: PJFET/PJFET.cir
* Description: Circuit netlist to test current-voltage characteristics of the p-channel JFET model.
* Input: VDD
* Output: I(VMON), V(3,2), V(1,2)
* Analysis:
* For determining the bias point of the PJFET circuit the general algebraic solution is:

\[
ID = \frac{[-B - \sqrt{B^2 - 4AC}]}{2A}
\]

* Where,

A = RS**2 = (1.65E3)**2 = 2.7225E+6
B = -{2*(|VP| + |VG|)*RS + (VP**2) / IDSS} = -{2 * (5 + 4) * 1.65E3 + 25/18.0E-3} = -31.09E+3
C = (|VP| + |VG|)**2 = (5 + 4)**2 = 81
Therefore,

ID = \frac{[-(-31.09E+3) - \sqrt{(-31.09E+3)^2 - 4 * 2.7225E+6 * 81}]}{2 * 2.7225E6} = 4.02mA

|VDS| = |VDD| – ID*(RD + RS) = 20 – 4.02E-3 * (1.85k + 1.65k) = 5.93V
* Since the JFET is P-channel, VDS is –5.93V
* VGS = |VG| - ID*RS
* = |R2 / (R2 + R1)| * VDD | - ID*RS
* = [47E3/(47E3 + 188E3)] * 20 – 4.02E-3*1.65E3
* = 2.63V
* Note:

IDSS = BETA * VP**2 = 7.2E-4 * (-5)**2 = 18.0E-3 A
* VP = VTO = -5V
* The circuit simulation should yield the following outputs:

* I(VMON) = Drain Current Id = 4.02mA
* V(3,2) = Drain-Source Voltage Vds= -5.93V
* V(1,2) = Gate-Source Voltage Vgs= 2.63V

J 3 1 2 JFET
R1 5 1 188K
R2 1 0 47K
RS 2 0 1.65K
RD 5 4 1.85K
VDD 0 5 20V
VMON 3 4 0
.MODELFET PJF BETA=7.2E-4 VTO=-5
.DC VDD 20 20 1
.PRINT DC I(VMON) V(3,2) V(1,2)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the PJFET Circuit:

P-Channel Depletion Mode JFET Circuit
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon_branch</th>
<th>v(3)-v(2)</th>
<th>v(1)-v(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD</td>
<td>ID</td>
<td>VDS</td>
<td>VGS</td>
</tr>
<tr>
<td>0</td>
<td>2.000000E+01</td>
<td>4.022105E-03</td>
<td>-5.922631E+00</td>
<td>2.636474E+00</td>
</tr>
</tbody>
</table>
3.1.31 Test Circuit for the P-Channel MOSFET

**************************************************************************
* Tier No.:  1
* Directory/Circuit Name: PMOS/PMOS1.cir
* Description: Circuit netlist to test current-voltage characteristics of the p-channel MOSFET model. The transistor is biased in nonsaturation region using resistors R1 and R2 to fix the gate voltage at half supply.
* Input: VDD
* Output: I(VMON), V(2,3), V(2,1)
* Analysis:
* FOR THE PMOS CIRCUIT BIASED IN THE NON-SATURATION REGION:
* $V_{SG} = VDD - VG = VDD - \{R2/(R1+R2)\} \times VDD = 5 - \{50/100\} \times 5 = 2.5V$
* $I_D = K_P \times [2 \times (V_{SG} + V_T) \times V_{SD} + V_{SD}^2]$
* $= 0.2E-3 \times [2 \times (2.5-0.8) \times (5 - 7.5E+3 \times I_D) - (5 - 7.5E+3 \times I_D)^2]$
* $= 0.515mA$
* $V_{SD} = VDD - I_D \times RD = 5 - (0.515E-3) \times (7.5E+3) = 1.14V$
* The circuit simulation should yield the following outputs:
* $I(VMON) = \text{Drain Current}$ $Id = 0.515mA$
* $V(2,3) = \text{Source-Drain Voltage}$ $Vsd= 1.14V$
* $V(2,1) = \text{Source-Gate Voltage}$ $Vsg= 2.5V$
**************************************************************************

VDD 2 0 DC 5V
R1 2 1 50K
R2 1 0 50K
RD 4 0 7.5K
VMON 3 4 0
M1 3 1 2 PFET L=10U W=160U
.Model PFET PMOS (KP=25U VTO=-0.8V)
.Dc VDD 5 5 1
.Print DC I(VMON) V(2,3) V(2,1)
.OPTION ACCT
.END

ChileSPICE Simulation Results for the PMOS Circuit:

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon_branch</th>
<th>v(2)-v(3)</th>
<th>v(2)-v(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD</td>
<td>ID</td>
<td>VSD</td>
<td>VSG</td>
</tr>
<tr>
<td>0</td>
<td>5.000000E+00</td>
<td>5.153525E-04</td>
<td>1.134856E+00</td>
<td>2.500000E+00</td>
</tr>
</tbody>
</table>
3.1.32 Test Circuit for the PNP Bipolar Transistor
****************************************************************************
* Tier No.: 1
* Directory/Circuit Name: PNP/PNP1.cir
* Description: Circuit netlist simulated in ChileSPICE to determine the validity of the
* current-voltage characteristics of the PNP bipolar transistor model. A common
* collector configuration is biased in the forward active mode.
* Input: VPOS, VBB
* Output: I(VMON1), I(VMON2), I(VMON3)
* Analysis:
* FOR THE PNP CIRCUIT DETERMINE:
* IE = (VCC – VEC)/RE = (5 – 2.5)/2E+3 = 1.25mA
* IC = [BETA/(1 + BETA)] * IE = 60/61 * 1.25E-3 = 1.23mA
* IB = IC/BETA = 1.23E-3/60 = 20.5uA
* RB = (VCC – VBB – VEB – IE*RE) / IB = (5 – (-2) –0.6 – (1.25E-3 * 2E3)) / 20.5E-6
* = 190.2K
* The circuit simulation should yield the following outputs:
* I(VMON1) = Base Current Ib = 20.5uA
* I(VMON2) = Collector Current Ic = 1.23mA
* I(VMON3) = Emitter Current Ie = 1.25mA
****************************************************************************
VCC 1 0 DC 5V
VBB 6 0 DC -2V
RE 1 2 2K
RB 3 4 190K
Q 5 3 7 PBJT
* ZERO VOLT SOURCES ACTING AS AN AMMETER TO MEASURE THE
* BASE, COLLECTOR, AND EMMITTER CURRENTS, RESPECTIVELY
VMON1 4 6 0
VMON2 5 0 0
VMON3 2 7 0
.DC VCC 5 5 1 VBB -2 -2 1
.PRINT DC I(VMON1) I(VMON2) I(VMON3)
.MODEL PBJT PNP (IS=100FA BF=60)
.OPTION ACCT
.END

ChileSPICE Simulation Results for the PNP Circuit:

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>vmon1_branch</th>
<th>vmon2_branch</th>
<th>vmon3_branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5.000000E+00</td>
<td>2.050980E-05</td>
<td>1.230588E-03</td>
<td>1.251098E-03</td>
</tr>
</tbody>
</table>
Test Circuit for the Polynomial Source

* Tier No.: 1
* Directory/Circuit Name: POLY/poly.cir
* Description: Test of polynomial function for describing a nonlinear dependent voltage source.
* Input: VINPUT = V(1)
* Output: V(2), V(3), V(4)
* Analysis:

A voltage source, VINPUT, supplies two equal resistors, R1=R2=1k. The nonlinear source, B, is dependent upon the voltage at node 2, V(2), by a given polynomial:

\[ B = V(3) = 3 + 2V(2) + V(2)^2 \]

V(2) is established by a voltage divider with Vinput. Additionally, V(4) is established by a voltage divider with V(3). The equations and expected output are as follows:

\[ (1) V(2) = VINPUT \times \frac{R2}{R1+R2} \]
\[ (2) V(3) = 3 + 2V(2) + V(2)^2 \]
\[ (3) V(4) = V(3) \times \frac{R4}{R3+R4} \]

VINPUT, or V(1), is described on the DC line as varying from -4V to 4V in 1V steps. Therefore, the following output, in volts, is expected:

<table>
<thead>
<tr>
<th>VINPUT</th>
<th>V(2)</th>
<th>V(3)</th>
<th>V(4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4.0</td>
<td>-2.0</td>
<td>3.00</td>
<td>1.50</td>
</tr>
<tr>
<td>-3.0</td>
<td>-1.5</td>
<td>2.25</td>
<td>1.125</td>
</tr>
<tr>
<td>-2.0</td>
<td>-1.0</td>
<td>2.00</td>
<td>1.000</td>
</tr>
<tr>
<td>-1.0</td>
<td>-0.5</td>
<td>2.25</td>
<td>1.125</td>
</tr>
<tr>
<td>0.0</td>
<td>0.0</td>
<td>3.00</td>
<td>1.50</td>
</tr>
<tr>
<td>1.0</td>
<td>0.5</td>
<td>4.25</td>
<td>2.125</td>
</tr>
<tr>
<td>2.0</td>
<td>1.0</td>
<td>6.00</td>
<td>3.000</td>
</tr>
<tr>
<td>3.0</td>
<td>1.5</td>
<td>8.25</td>
<td>4.125</td>
</tr>
<tr>
<td>4.0</td>
<td>2.0</td>
<td>1.10</td>
<td>5.500</td>
</tr>
</tbody>
</table>

VINPUT 1 0 1V
B 3 0 V = POLY(1) V(2) 3 2 1
R1 1 2 1K
R2 2 0 1K
R3 3 4 2K
R4 4 0 2K
.DC VINPUT -4 4 1
.PRINT DC V(2) V(3) V(4)
.OPTIONS ACCT
.END
## ChileSPICE Simulation Results for the Poly Circuit:

Polynomial Source Circuit
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(2)</th>
<th>v(3)</th>
<th>v(4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-4.000000e+00</td>
<td>-2.000000e+00</td>
<td>3.000000e+00</td>
<td>1.500000e+00</td>
</tr>
<tr>
<td>1</td>
<td>-3.000000e+00</td>
<td>-1.500000e+00</td>
<td>2.250000e+00</td>
<td>1.125000e+00</td>
</tr>
<tr>
<td>2</td>
<td>-2.000000e+00</td>
<td>-1.000000e+00</td>
<td>2.000000e+00</td>
<td>1.000000e+00</td>
</tr>
<tr>
<td>3</td>
<td>-1.000000e+00</td>
<td>-5.000000e-01</td>
<td>2.250000e+00</td>
<td>1.125000e+00</td>
</tr>
<tr>
<td>4</td>
<td>0.000000e+00</td>
<td>0.000000e+00</td>
<td>3.000000e+00</td>
<td>1.500000e+00</td>
</tr>
<tr>
<td>5</td>
<td>1.000000e+00</td>
<td>5.000000e-01</td>
<td>4.250000e+00</td>
<td>2.125000e+00</td>
</tr>
<tr>
<td>6</td>
<td>2.000000e+00</td>
<td>1.000000e+00</td>
<td>6.000000e+00</td>
<td>3.000000e+00</td>
</tr>
<tr>
<td>7</td>
<td>3.000000e+00</td>
<td>1.500000e+00</td>
<td>8.250000e+00</td>
<td>4.125000e+00</td>
</tr>
<tr>
<td>8</td>
<td>4.000000e+00</td>
<td>2.000000e+00</td>
<td>1.100000e+01</td>
<td>5.500000e+00</td>
</tr>
</tbody>
</table>
3.1.34 Test Circuit for the Resistor

* Tier No.: 1
* Directory/Circuit Name: RESISTOR/RESISTOR.cir
* Description: Circuit to demonstrate the validity of the linear resistor model.
* Input: VIN=0-5V DC
* Output: V(1), I(V1)
* Analysis:
* A DC voltage source, V1, in parallel with a 1K Ohm resistor, is swept from 0-5V in
* 1V increments. The measured output is the current, I(V1), through the resistor. This is
* calculated using Ohm's Law, which yields the linear I-V characteristic for a resistor.
* Voltage = Current * Resistance = I * R
* or
* I = V/R
* The netlist was simulated using a low (1E-9 Ohms), nominal (1E3 Ohms)
* and high (1E12 Ohms) values for the resistance.
* Therefore, for the given resistance and voltage values, I is:

<table>
<thead>
<tr>
<th>V(Volts)</th>
<th>R(Ohms)</th>
<th>I(Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1E-9/1E3/1E12</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1E-9/1E3/1E12</td>
<td>1E9/1E-3/1E-12</td>
</tr>
<tr>
<td>2</td>
<td>1E-9/1E3/1E12</td>
<td>2E9/2E-3/2E-12</td>
</tr>
<tr>
<td>3</td>
<td>1E-9/1E3/1E12</td>
<td>3E9/3E-3/3E-12</td>
</tr>
<tr>
<td>4</td>
<td>1E-9/1E3/1E12</td>
<td>4E9/4E-3/4E-12</td>
</tr>
<tr>
<td>5</td>
<td>1E-9/1E3/1E12</td>
<td>5E9/5E-3/5E-12</td>
</tr>
</tbody>
</table>

R1 1 0 1K
V1 1 0 5V
.DC V1 0 5V 1V
.PRINT DC V(1) I(V1)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the Resistor Circuit:

Resistor Circuit
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep V1</th>
<th>v(1)</th>
<th>v1_branch I(V1)=I(R1)</th>
</tr>
</thead>
</table>

**R = 1E-9 Ohms**

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep V1</th>
<th>v(1)</th>
<th>v1_branch I(V1)=I(R1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.000000e+00</td>
<td>0.000000e+00</td>
<td>0.000000e+00</td>
</tr>
<tr>
<td>1</td>
<td>1.000000e+00</td>
<td>1.000000e+00</td>
<td>1.000000e+09</td>
</tr>
<tr>
<td>2</td>
<td>2.000000e+00</td>
<td>2.000000e+00</td>
<td>2.000000e+09</td>
</tr>
<tr>
<td>3</td>
<td>3.000000e+00</td>
<td>3.000000e+00</td>
<td>3.000000e+09</td>
</tr>
<tr>
<td>4</td>
<td>4.000000e+00</td>
<td>4.000000e+00</td>
<td>4.000000e+09</td>
</tr>
<tr>
<td>5</td>
<td>5.000000e+00</td>
<td>5.000000e+00</td>
<td>5.000000e+09</td>
</tr>
</tbody>
</table>

**R = 1E3 Ohms**

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep V1</th>
<th>v(1)</th>
<th>v1_branch I(V1)=I(R1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
</tr>
<tr>
<td>1</td>
<td>1.000000E+00</td>
<td>1.000000E+00</td>
<td>1.000000E-03</td>
</tr>
<tr>
<td>2</td>
<td>2.000000E+00</td>
<td>2.000000E+00</td>
<td>2.000000E-03</td>
</tr>
<tr>
<td>3</td>
<td>3.000000E+00</td>
<td>3.000000E+00</td>
<td>3.000000E-03</td>
</tr>
<tr>
<td>4</td>
<td>4.000000E+00</td>
<td>4.000000E+00</td>
<td>4.000000E-03</td>
</tr>
<tr>
<td>5</td>
<td>5.000000E+00</td>
<td>5.000000E+00</td>
<td>5.000000E-03</td>
</tr>
</tbody>
</table>

**R = 1E12 Ohms**

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep V1</th>
<th>v(1)</th>
<th>v1_branch I(V1)=I(R1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
</tr>
<tr>
<td>1</td>
<td>1.000000E+00</td>
<td>1.000000E+00</td>
<td>1.000000E-12</td>
</tr>
<tr>
<td>2</td>
<td>2.000000E+00</td>
<td>2.000000E+00</td>
<td>2.000000E-12</td>
</tr>
<tr>
<td>3</td>
<td>3.000000E+00</td>
<td>3.000000E+00</td>
<td>3.000000E-12</td>
</tr>
<tr>
<td>4</td>
<td>4.000000E+00</td>
<td>4.000000E+00</td>
<td>4.000000E-12</td>
</tr>
<tr>
<td>5</td>
<td>5.000000E+00</td>
<td>5.000000E+00</td>
<td>5.000000E-12</td>
</tr>
</tbody>
</table>
3.1.35 Test Circuit for the Semiconductor Capacitor

* Tier No.: 1
* Directory/Circuit Name: SEMIC_CAPACITOR/SEMIC_CAPACITOR.cir
* Description: Test of semiconductor capacitor model using a simple RC circuit configuration
* Input: VIN
* Output: V(3)
* Analysis:
* A 20 pF capacitor is specified by a length, width and junction capacitance.
* A transient analysis of the circuit voltage versus time is performed to determine the
  capacitor voltage, V(3) and current, I(VMON). To obtain the capacitance value,
  integrate the capacitor current (wrt time) then divide by the capacitor voltage
  A series RC circuit is connected to pulse voltage source, which goes from 0V to 1V
  after a 10us delay, with rise and fall times of 1ns. The equation for a
  semiconductor capacitor's capacitance value is:

\[
C = CJ \times (L-NARROW) \times (W-NARROW) + 2 \times CJSW(L+W-2NARROW)
\]

where,
\[
CJ = 1 \text{ F/sq.meter, } L=20U, W=1U, NARROW=0, CJSW=0
\]
This gives a capacitance value of 20pF (20E-12F).
* The capacitor voltage should reach 90% of its maximum value, 1V, in
* time = (3*R*C) + rise + delay
* time
* = (3 * 1E3 * 20E-12) + 1E-9 + 10E-6
* = 10.06us
* Therefore, at 10.06us the capacitor voltage should be at least 0.9V. Using the common
* simulation data (csd) format for PSpice’s Probe, the 20pF capacitance value can be
* confirmed by dividing the integral of the capacitor current (vmon_branch) by the
* capacitor voltage (V(3)).

VIN 1 0 PULSE(0 1 10U 1N 1N 30U)
R 1 2 1K
C 3 0 CMODEL L=20U W=1U
VMON 2 3 0
.MODEL CMODEL C (CJ=1)
.TRAN 1N 20U
.PRINT TRAN V(3)
.OPTION ACCT
.END
ChileSPICE Simulation Results for the Semiconductor Capacitor Circuit
3.1.36 Test Circuit for the Semiconductor Resistor

The test circuit for the semiconductor resistor is designed to verify the validity of the semiconductor resistor model. The circuit consists of a DC voltage source, $V_{IN}$, in parallel with a semiconductor resistor, whose length, width, and sheet resistance are defined such that the resistance value is 1K ohm. The equation for a semiconductor resistor is:

$$R = R_{SH} \frac{(L-NARROW)}{(W-NARROW)}$$

where,

- $R_{SH}=1$, $L=1000\mu\text{m}$, $W=1\mu\text{m}$, $NARROW=0$
- $V_{IN}$ is swept from 0-5V in 1V increments. The measured output is the current through the resistor. The resistance is calculated using Ohm's Law:

$$\text{Voltage} = \text{Current} \times \text{Resistance} = I \times R$$

or, $$R = \frac{I}{V}$$

Therefore, for the given voltage and current values, $R$ is:

<table>
<thead>
<tr>
<th>$R$ (kOhm)</th>
<th>$I$ (mA)</th>
<th>$V$ (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

A zero volt source, $V_{MON}$, is used as an ammeter to measure the current through $R$ and resistor voltage is measured at node 2, $V(2)$. 

**Circuit Netlist**

```
R1 2 0 RMOD L=1000U W=1U
VIN 1 0 5V
VMON 1 2 0V
.DC VIN 0 5V 1V
.MODEL RMOD R (RSH=1)
.PRINT DC V(2) I(VMON)
.OPTION ACCT
.END
```
ChileSPICE Simulation Results for the SEMICONDUCTOR RESISTOR Circuit:
Semiconductor Resistor Circuit
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(2)</th>
<th>vmon_branch</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VIN=V(1)</td>
<td>I thru R1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
<td>0.000000E+00</td>
</tr>
<tr>
<td>1</td>
<td>1.000000E+00</td>
<td>1.000000E+00</td>
<td>1.000000E-03</td>
</tr>
<tr>
<td>2</td>
<td>2.000000E+00</td>
<td>2.000000E+00</td>
<td>2.000000E-03</td>
</tr>
<tr>
<td>3</td>
<td>3.000000E+00</td>
<td>3.000000E+00</td>
<td>3.000000E-03</td>
</tr>
<tr>
<td>4</td>
<td>4.000000E+00</td>
<td>4.000000E+00</td>
<td>4.000000E-03</td>
</tr>
<tr>
<td>5</td>
<td>5.000000E+00</td>
<td>5.000000E+00</td>
<td>5.000000E-03</td>
</tr>
</tbody>
</table>
3.1.37 Test Circuit for a the Transfer Function Analysis

* Tier No.: 1
* Directory/Circuit Name: TFANALY/tfanalysis.cir
* Description: Test of transfer function analysis using a simple BJT amplifier to find the small signal voltage gain, input and output impedance.
* Input: VBB, VCC, VS
* Output: V(2)/VS, Rin, Rout
* Analysis:
  * A simple bjt amplifier circuit is analyzed to determine the small signal transfer function characteristics. The voltage gain, input and output impedance, which are defined as:
  * Voltage Gain = Small Signal Input Voltage/Output Voltage
  * \[ Av = \frac{V(2)}{VS} = -\left(\frac{gm \cdot RC}{rpi + RB}\right) \]
  * Input Impedance = Rin = impedance as seen from the input source VS
    * \[ Rin = RB + rpi \]
  * Output Impedance = Rout = impedance as seen the output voltage location
    * or from the bjt collector to ground = RC
  * where,
    * \( gm = \) transconductance = ICQ/VT
    * ICQ = large signal quiescent collector current
      * \[ ICQ = \beta \cdot IB = 100 \cdot 10e-6 = 1mA \]
    * IBQ = large signal quiescent base current
      * \[ IBQ = \frac{(VBB - VBE(on))}{RB} = \frac{(1.2 - 0.7)}{50E3} = 10uA \]
    * VT=thermal voltage = 26mV
    * \[ gm = \frac{1E-3}{26E-3} = 38.46 \text{ mA/V} \]
  * NOTE: VBE, the base emitter turn on voltage is assumed to be 0.7V
  * \( \beta, \) the common emitter current gain, is 100*
  * \( rpi = \) diffusion resistance = \( \beta \cdot VT / IC = (\beta \cdot 0.7) / (1E-3) = 2.6 \text{ kOhms} \)
  * Therefore, the expected results are as follows:
    * \[ Av = \frac{V(2)}{VS} = -\left(\frac{gm \cdot RC}{rpi + RB}\right) \]
      * \[ Av = -\left(38.46E-3 \cdot 6E3\right) \cdot \left(\frac{2.6E3}{2.6E3 + 50E3}\right) = -11.4 \]
    * \( Rin = RB + rpi = 50E3 + 2.6E3 = 52.6 \text{ kOhms} \)
    * \( Rout = RC = 6 \text{ kOhms} \)
  * NOTE: The value used for Vbe may not be the exact value used by the simulator since Vbe is a calculated rather than user defined model parameter for a bjt transistor.

VCC 1 0 DC 12V
VBB 5 0 DC 1.2V
VS 4 5 SIN(0 0.3V 1khz)
RC 1 2 6K
RB 3 4 50K
Q 2 3 0 NBJT
.MMODEL NBJT NPN(IS=10FA BF=100)
.TF V(2) VS
.OPTIONS ACCT
.END
ChileSPICE Simulation Results for the Transfer Function Analysis Circuit:

Transfer function information:

\[ \text{GAIN} = \text{transfer\_function} = -1.14542e+01 \]

\[ \text{ROUT} = \text{output\_impedance\_at\_v(2)} = 5.999996e+03 \]

\[ \text{RIN} = \text{vs\_input\_impedance} = 5.238257e+04 \]
3.1.38 Test of the Transmission Line Circuit

* Tier No.: 1
* Directory/Circuit Name: TRANSLINE/TRANSLINE.cir
* Description: Test of Chilespice transmission line model using lossless circuit configuration.
* Input: VIN
* Output: V(2), V(3)
* Analysis:
  * The circuit contains a pulse voltage source (VIN), with a 50 ohm (RIN) output impedance, connected to a 50 ohm transmission line (TLINE) which is terminated in a 50 ohm (RL) matched load. The pulse goes from 0V to 5V with no delay, and has a pulse width of 25ns. The transmission line has a 10ns delay. Any change in the input voltage, V(2), of TLINE should occur 10ns later at the output (node 3).
  * Therefore, the input voltage rises from 0V to 2.5V in 1ns and remains at 2.5V for 5ns. The output voltage V(3), does the same as V(2) except that it is delayed by 10ns.
  * Note: V(2) is 2.5V due to the voltage drop across the 50 ohm RIN resistor.

VIN 1 0 PULSE(0 5 0.1N 0.1N 5N 25N)
RIN 1 2 50
TLINE 2 0 3 0 Z0=50 TD=10N
RL 3 0 50
.TRAN 0.25N 50N
.PRINT TRAN V(2) V(3)
.OPTION LIST ACCT
.END
ChileSPICE Simulation Results for the Transline Circuit
**3.1.39 Test Circuit for the Voltage Controlled Current Source (VCCS)**

* Tier No.: 1
* Directory/Circuit Name: VCCS/vccs.cir
* Description: Test of ChileSPICE voltage controlled current source, VCCS, model using a simple resistor circuit. A DC operating point analysis is performed to obtain the transfer function characteristics of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
* Input: VIN
* Output: V(2), V(3), Rin, Rout, V(3)/Vin
* Analysis:
  * The VCCS, G, is a function of the voltage, V(2), across R2 and is defined as
  * \[ G = k \cdot V = 0.02 \cdot V(2). \]
  * The k must have the unit of conductance (1/ohms) to make k and V equal amps.
  * The voltage V(2) found by voltage division is
  * \[ V(2) = \frac{VIN \cdot R2}{R1 + R2} = \frac{12 \cdot 900}{1200} = 9V \]
  * The current through the dependent source, G, is
  * \[ k \cdot V(2) = 0.02 \cdot 9V = 180mA \]
  * The current through the dependent source is divided evenly through resistors R3 and R4 (which are in parallel) giving 90mA through each resistor. The 90mA currents go from node 0 to node 3 (tail to tip), making the voltage at node 3
  * \[ V(3) = -(R3 \cdot 90mA) = -(200 \cdot 90mA) = -18V \]
  * Additionally, Rin, Rout and the voltage gain are:
    * Rin = R1 + R2 = 300 + 900 = 1200 Ohms
    * Rout = R3 || R4 = 200 || 200 = 100 Ohms
    * GAIN = V(3)/VIN = -18/12 = -1.5

```
VIN 1 0 DC 12V
G 3 0 2 0 0.02
R1 1 2 300
R2 2 0 900
R3 3 0 200
R4 3 0 200
.DC VIN 12 12 1
.PRINT DC V(2) V(3)
.OPTIONS ACCT
.TF V(3) VIN
.END
```
ChileSPICE Simulation Results for the VCCS Circuit:

Voltage Controlled Current Source (VCCS)
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(2)</th>
<th>v(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.200000E+01</td>
<td>9.000000E+00</td>
<td>-1.800000E+01</td>
</tr>
</tbody>
</table>

Transfer function information:
GAIN = transfer_function =  -1.500000E+00
ROUT = output_impedance_at_v(3) = 1.000000E+02
RIN = vin_input_impedance = 1.200000E+03
3.1.40 Test Circuit for the Voltage-Controlled Voltage Source Circuit (VCVS)

******************************************************************************
* Tier No.: 1
* Directory/Circuit Name: VCVS/vcvs.cir
* Description: Test of ChileSPICE voltage controlled voltage source model using a voltage
* amplifier circuit. A DC operating point analysis is performed to obtain the transfer function
* characteristics of the circuit (i.e., Rin, Rout, and voltage gain, Vout/Vin).
* Input: VIN
* Output: V(2), V(3), V(4), Rin, Rout, V(4)/VIN
* Analysis:
* The VCVS, E, is controlled by the independent source, VIN, in the circuit and is defined as:
*   \[ E = V(3) = k \times VIN = 2 \times 10V = 20V \]
*   The factor k is an amplification value of 2.
* The voltages at nodes 2 and 4 are
*   \[ V(2) = VIN \times R2/(R1+R2) = 10 \times 100K/(100K+250) = 9.975V \]
*   \[ V(4) = V(3) \times R4/(R3+R4) = 20 \times 1K/(40+1K) = 19.231V \]
* Additionally, Rin, Rout and the voltage gain are
*   \[ Rin = R1 + R2 = 100K + 250 = 100.25K \]
*   \[ Rout = R3||R4 = 40||1K = 38.46 \text{ Ohms} \]
*   \[ GAIN = V(4)/VIN = 19.231/10 = 1.923 \]
******************************************************************************

ChileSPICE Simulation Results for the VCVS Circuit:
Voltage-Controlled Voltage Source Circuit (VCVS)
DC transfer characteristic

<table>
<thead>
<tr>
<th>Index</th>
<th>voltage_sweep</th>
<th>v(2)</th>
<th>v(3)</th>
<th>v(4)</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td></td>
<td>9.975062E+00</td>
<td>2.000000E+01</td>
<td>1.923077E+01</td>
<td></td>
</tr>
</tbody>
</table>

Transfer function information:
GAIN= transfer_function = 1.923077E+00
ROUT = output_impedance_at_v(4) = 3.846154E+01
RIN = vin_input_impedance = 1.002500E+05

VIN 1 0 10V
E 3 0 1 0 2
R1 1 2 250
R2 2 0 100K
R3 3 4 40
R4 4 0 1K
.DC VIN 10 10 1
.PRINT DC V(2) V(3) V(4)
.OPTIONS ACCT
.TF V(4) VIN
.END
3.1.41 Test Circuit for the Exponential Voltage Source

* Tier No.: 1
* Directory/Circuit Name: VEXP/VEXP.cir
* Description: Test of the model for an exponential voltage source.
* Input: VEXP
* Output: V(1)
* Analysis:

- The voltage source, VEXP or V(1), is described as an exponential time dependent voltage signal that rises from 0 – 5V after a 1us delay time. The rise time constant is 1us. The signal does not decay until after 1s. Since the transient analysis is from 0 - 5us, the signal will stay at 5V for the duration of the simulation.

- The general format for an exp voltage source is
  
  EXP (V1 V2 TD1 TAU1 TD2 TAU2)

  Where,
  
  V1=initial value=0V  V2=pulsed value=5V  TD1=rise time delay=1us
  TAU1=rise time constant=1us  TD2=fall delay time=1s  TAU2=final time constant=0

- The voltage is described by the following equation:
  
  for t between 0 and TD1
  VEXP=V1
  for t between TD1 and TD2
  VEXP = v(t)=V1 + (V2-V1)*(1-EXP(-(TIME-TD1)/TAU1))
  for t between TD2 and TSTOP
  VEXP=v(t) + (V1-V2)*(1-EXP(-(TIME-TD2)/TAU2))

- Therefore for given values of time, the expected voltage is:

<table>
<thead>
<tr>
<th>T</th>
<th>VEXP(T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E-6</td>
<td>3.16</td>
</tr>
<tr>
<td>2E-6</td>
<td>4.32</td>
</tr>
<tr>
<td>3E-6</td>
<td>4.75</td>
</tr>
<tr>
<td>4E-6</td>
<td>4.91</td>
</tr>
<tr>
<td>5E-6</td>
<td>4.97</td>
</tr>
</tbody>
</table>

VEXP 1 0 EXP(0V 5V 1US 1US 1S)

R 1 0 500
.TRAN 1US 5US
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
ChileSPICE Results for Exponential Voltage Circuit

![Graph of exponential voltage circuit results with time in seconds on the x-axis and voltage in volts on the y-axis. The graph shows a curve representing the voltage over time, with the y-axis ranging from 0 to 5E+00 and the x-axis ranging from 0.00E+00 to 5.00E-06. The curve flatten at higher voltages.]

V(1)
3.1.42 Test Circuit for the Pulse Voltage Source

* Tier No.: 1
* Directory/Circuit Name: VPULSE/VPULSE.cir
* Description: Test of the pulse voltage source model
* Input: VPULSE
* Output: V(1)
* Analysis:
  * The voltage source, VPULSE or V(1), is described as time dependent voltage signal that
  * generates a sawtooth waveform. The signal rises linearly from 0V to 1V in 10us. The
  * voltage remains at its peak value of 1V for 0.1us then decrease back to zero volts in 10us.

VPULSE 1 0 PULSE(0V 1V 0S 10US 10US 0.1US 20.1US)
R 1 0 500
.TRAN 1US 20.1US
.OPTIONS ACCT
.PRINT TRAN V(1)
.END

ChileSPICE Simulation Results for the Pulse Voltage Circuit

![Graph showing the simulation results of the pulse voltage circuit. The graph plots voltage (Volts) against time (Seconds). The voltage signal is a sawtooth waveform with a peak value of 1V, rising linearly from 0V to 1V in 10us, and then decreasing back to zero volts in 10us. The signal remains at its peak for 0.1us.](image-url)
3.1.43 Test Circuit for the Piece Wise Linear Voltage Source

************************************************************

* Tier No.: 1
* Directory/Circuit Name: VPWL/VPWL.cir
* Description: Test of the piece-wise linear voltage source model
* Input: VPWL
* Output: V(1)
* Analysis:
* The source, VPWL or V(1), is as a piece wise linear voltage source which
* is described by a series of time and voltage pairs of data points, given by:

<table>
<thead>
<tr>
<th>index</th>
<th>time(s)</th>
<th>voltage(volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>2</td>
<td>2.0</td>
<td>3.0</td>
</tr>
<tr>
<td>3</td>
<td>3.0</td>
<td>2.0</td>
</tr>
<tr>
<td>4</td>
<td>4.01</td>
<td>5.0</td>
</tr>
<tr>
<td>5</td>
<td>4.51</td>
<td>-2.0</td>
</tr>
<tr>
<td>6</td>
<td>7.0</td>
<td>1.0</td>
</tr>
<tr>
<td>7</td>
<td>9.0</td>
<td>-1.0</td>
</tr>
<tr>
<td>8</td>
<td>9.01</td>
<td>4.0</td>
</tr>
<tr>
<td>9</td>
<td>10.0</td>
<td>3.0</td>
</tr>
<tr>
<td>10</td>
<td>11.0</td>
<td>3.0</td>
</tr>
</tbody>
</table>

************************************************************

VPWL 1 0 PWL(0S 0V  2S 3V  3S 2V  4S 2V  4.01V 5V  4.5S 5V
+ 4.51S -2V  7S 1V  9S -1V  9.01S 4V  10S 3V)
R 1 0 500
.TRAN 1S 11S
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
ChileSPICE Simulation Results for the Piece-Wise Linear Voltage Circuit

![Graph showing voltage over time for the piece-wise linear voltage circuit.](image)
### 3.1.44 Test Circuit for the Voltage Single Frequency FM Source (VSFFM)

*n Tier No.: 1*
*n Directory/Circuit Name: VSFFM/vsffm.cir*
*n Description: Test of Chilespice model for a single-frequency frequency-modulated (SFFM) transient voltage source.*
*n Input: VSFFM*
*n Output: V(1)*
*n Analysis:
* A single frequency - frequency modulation signal that has no initial voltage and a peak amplitude of 1V. It has a carrier frequency of 1MEG Hz. For the 10us transient analysis, 10 cycles of the carrier will be output in the 10us time. The carrier is modulated at a rate determined by the single frequency (250KHz) and the modulation index (2).*
*n The general format for a sffm transient function on a source statement is
* SFFM (VO  VA  FC  MDI  FS)
* where,
* VO=offset voltage = 0V  VA=amplitude = 5V
* FC=carrier frequency = 1MHz  MDI=modulation index = 2
* FS=signal frequency = 250kHz
* The current is described by the following equation:
* VSFFM(t)= VO + VA*sin(2*pi*FC*t + MDI*sin(2*pi*FS*t))
* Therefore, at the given values of time, the voltage should be:
*| T         | VSFFM(T) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000E+00</td>
<td>0.0000E+00</td>
</tr>
<tr>
<td>1.0000E-04</td>
<td>4.9076E+00</td>
</tr>
<tr>
<td>2.0000E-04</td>
<td>1.4222E+00</td>
</tr>
<tr>
<td>3.0000E-04</td>
<td>1.4222E+00</td>
</tr>
<tr>
<td>4.0000E-04</td>
<td>4.9076E+00</td>
</tr>
<tr>
<td>5.0000E-04</td>
<td>2.1244E-06</td>
</tr>
<tr>
<td>6.0000E-04</td>
<td>-4.9076E+00</td>
</tr>
<tr>
<td>7.0000E-04</td>
<td>-1.4222E+00</td>
</tr>
<tr>
<td>8.0000E-04</td>
<td>-1.4222E+00</td>
</tr>
<tr>
<td>9.0000E-04</td>
<td>-4.9076E+00</td>
</tr>
</tbody>
</table>

* VSFFM 1 0 SFFM(0 1 1MEG 2 250K)*
*R1 1 0 1*
*.TRAN 1US 10US 0 0.01US*
*.PRINT TRAN V(1)*
*.OPTIONS LIST ACCT*
*.END*
ChileSPICE Simulation Results for the SFFM Voltage Circuit

![Graph showing voltage over time](image-url)
3.1.45 Test Circuit for the Sinusoidal Voltage Source

* Tier No.: 1
* Directory/Circuit Name: VSIN/VSIN.cir
* Description: Test of the model for an independent sinusoidal voltage source.
* Input: VCOS
* Output: V(1)
* Analysis:

* The voltage source is described as a sinusoidal time dependent voltage signal that
  implements a cosine signal by specifying a negative delay equal to 2.5us, or a quarter of
  the period specified by the 10us in the transient analysis statement. The signal has a 5V
  peak value with a 100kHz frequency, or 10us period.
* The general format for the sinusoidal function in the voltage source is
  \( \text{SIN}(\text{VO VA FREQ TD THETA}) \)
  where,
  \( \text{VO}= \text{offset current} = 0A \quad \text{VA}=\text{amplitude} = 5A \)
  \( \text{FREQ}=\text{frequency} = 100kHz \quad \text{TD}=\text{time delay}= -2.5us \)
  \( \text{THETA}=\text{damping factor} = 0 \)
* The voltage is described by the following equation for time > TD:
  \( \text{VSIN}(t) = \text{VO} + \text{VA} \times \sin(2\pi \times \text{FREQ} \times (t - \text{TD})) \times \exp(-\text{THETA}(t-TD)) \)
* Therefore, at given values of time, the voltage should be:

<table>
<thead>
<tr>
<th>T(seconds)</th>
<th>Voltage(T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00E+00</td>
<td>5</td>
</tr>
<tr>
<td>2.00E-06</td>
<td>1.545084972</td>
</tr>
<tr>
<td>4.00E-06</td>
<td>-4.045084972</td>
</tr>
<tr>
<td>6.00E-06</td>
<td>-4.045084972</td>
</tr>
<tr>
<td>8.00E-06</td>
<td>1.545084972</td>
</tr>
<tr>
<td>1.00E-05</td>
<td>5</td>
</tr>
</tbody>
</table>

VCOS 1 0 SIN(0 5 100K -2.5U)
R 1 0 500
.TRAN 1US 10US
.OPTIONS ACCT
.PRINT TRAN V(1)
.END
ChileSPICE Simulation Results for the Sinusoidal Voltage Circuit

![Graph showing sinusoidal voltage over time]
3.1.46 Test Circuit for the Voltage Switch Implementation of a NOR Gate

* Tier No.: 1
* Directory/Circuit Name: VSWITCH/VSWITCH.cir
* Description: Test of voltage controlled switch model. The switch behaves like a resistor that toggles between a very small on resistance, and a very large off resistance which depends upon the controlling voltage.
* Input: VCC, V3, V4
* Output: V(1), V(3), V(4)
* Analysis:

  The circuit equivalent to the MOSFET implementation of a NOR gate with the transistors replaced by two switches, S1 and S2, and a load resistance connected to 5V, VCC or V(2). The controlling voltages at nodes 3 and 4 represent the two inputs to the NOR gate, which has the following logic table:

<table>
<thead>
<tr>
<th>InputA</th>
<th>InputB</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0(Low)</td>
<td>0(Low)</td>
<td>1(High)</td>
</tr>
<tr>
<td>0(Low)</td>
<td>1(High)</td>
<td>0(Low)</td>
</tr>
<tr>
<td>1(High)</td>
<td>0(Low)</td>
<td>0(Low)</td>
</tr>
<tr>
<td>1(High)</td>
<td>1(High)</td>
<td>0(Low)</td>
</tr>
</tbody>
</table>

The two input signals, V(3) and V(4), are a sequence of logic 0 and 1 described by two PWL voltage sources. A transient analysis of the circuit from 0 to 4us circuit from 0us to 4us yields the following expected output:

| V(3)=InputA | 0 | 5 | 0 | 5 | 5 |
| V(4)=InputB | 0 | 0 | 5 | 5 | 5 |
| V(1)=Output | 4.99 | .005 | .005 | .025 | .025 |

*Note: V(1)=0.005 and V(1)=0.025 are logic 0.

RL 2 1 1K
S1 1 0 3 0 SW
S2 1 0 4 0 SW
VCC 2 0 5
V3 3 0 PWL (0 0 1U 0 1.01U 5 2U 5 2.01U 0 3U 0 3.01U 5)
R3 3 0 1
V4 4 0 PWL (0 0 2U 0 2.01U 5)
R4 4 0 1
.MODEL SW VSWITCH(RON=1 ROFF=1MEG VON=1 VOFF=0)
.TRAN 0.02U 4U
.PRINT TRAN V(1) V(3) V(4)
.OPTIONS ACCT
.END
Test Circuit for the XNOR (Exclusive NOR) Gate

* Tier No.: 1
* Directory/Circuit Name: XNOR/xnor.cir
* Description: Test of the digital exclusive nor, XNOR, gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
  * Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to an XNOR gate, which is defined internal to the code as a subcircuit. Parameters are defined in the netlist (by the .PARAMS statement) and passed into the XNOR subcircuit.
  * The subcircuit uses the parameters to establish the following values of the output voltage:
    * Rise Time = default_rise = rise/fall output voltage = 1ns
    * Margin = default_margin = margin which the output exceeds min/max logic levels = 0.5V
    * High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
    * Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
  * The logic for the exclusive nor gate is the output is high if and only if both inputs are low or both inputs are high, for any other combination the output is low. This truth table shows the XNOR expected output for the given A and B time dependent inputs.

<table>
<thead>
<tr>
<th>TIME</th>
<th>A(Volts)</th>
<th>B(Volts)</th>
<th>OUT(Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>2S</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>3S</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>4S</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>5S</td>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6S</td>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>8S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>9S</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

NOTE: Low = 0V, High = 5V

* Set digital default parameters
  * .PARAM default_rise=1ns
  * .PARAM default_delay=0
  * .PARAM default_low=0.5V
  * .PARAM default_high=4.5V
  * .PARAM default_margin=0.5V
* Gate Inputs
  * VA A 0.0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
  * VB B 0.0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)
  * X_XNOR A B OUT XNOR
  * .TRAN 1S 9S
  * .PRINT TRAN V(A) V(B) V(OUT)
  * .OPTIONS ACCT
  * .END
ChileSPICE Simulation Results For the XNOR Circuit

![Graph showing simulation results for the XNOR circuit with axes labeled Voltage (Volts) on the y-axis and Time (Seconds) on the x-axis. The graph illustrates the voltages V(A), V(B), and V(OUT) over time.](image-url)
3.1.48 Test Circuit for the XOR (Exclusive Or) Gate

* Tier No.: 1
* Directory/Circuit Name: XOR/xor.cir
* Description: Test of the digital exclusive or, XOR, gate used for defining logic circuits.
* Input: VA=V(A), VB=V(B)
* Output: V(A), V(B), V(OUT)
* Analysis:
  * Two piecewise linear voltage sources, V(A) and V(B), are used as logic inputs to an XOR gate, which is defined internal to the code by a subcircuit. Parameters are defined in the netlist (by the .PARAMS statement) and passed into the XOR subcircuit. The subcircuit uses the parameters to establish the following values of the output voltage:
  * Rise Time = default_rise = rise/fall output voltage = 1ns
  * Margin = default_margin = margin which the output exceeds min/max logic levels = 0.5V
  * High = default_high + default_margin = logic high voltage = 4.5V + 0.5V = 5V
  * Low = default_low - default_margin = logic low voltage = 0.5V - 0.5V = 0V
  * The logic for the exclusive or gate is the output is high if and only if one input is low and one input is high; when both inputs are simultaneously high or low, the output is low.
  * This truth table shows the XOR expected output for the given A and B time dependent inputs.

<table>
<thead>
<tr>
<th>TIME</th>
<th>A(Volts)</th>
<th>B(Volts)</th>
<th>OUT(Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2S</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>4S</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>5S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>6S</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>7S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>8S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>9S</td>
<td>5</td>
<td>5</td>
<td>0</td>
</tr>
</tbody>
</table>

* NOTE: Low = 0V  High = 5V

* Set digital default parameters
  .PARAM default_rise=1ns
  .PARAM default_delay=0
  .PARAM default_low=0.5V
  .PARAM default_high=4.5V
  .PARAM default_margin=0.5V

* Gate Inputs
  VA A 0 0V PWL(0 0 1 0 2 0 3 0 4 0 5 5 6 5 7 5 8 5)
  VB B 0 0V PWL(0 0 1 0 2 0 3 5 4 5 5 0 6 0 7 5 8 5)
  X_XOR A B OUT XOR
  .TRAN 1S 9S
  .PRINT TRAN V(A) V(B) V(OUT)
  .OPTIONS ACCT
  .END
ChileSPICE Simulation Results for the XOR Gate Circuit

![Voltage vs Time Graph]

- **V(A)**
- **V(B)**
- **V(OUT)**
4 References


5 Distribution

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1  MS 0525  1734  L Waters
1  MS 0525  1734  T Russo
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