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Fundamental Understanding and Development of Low-Cost, High-Efficiency Silicon Solar Cells

Final Progress Report: September 1999 – June 2000

A. Rohatgi, A. Ebong, V. Yelundur, M. Hilali, J. Jeong, A. Ristow, B. Damiani, J. Brody,
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Abstract

The overall objectives of this program are to (1) develop rapid and low-cost processes for manufacturing that can improve yield, throughput, and performance of silicon photovoltaic devices, (2) design and fabricate high-efficiency solar cells on promising low-cost materials, and (3) improve the fundamental understanding of advanced photovoltaic devices. Several rapid and potentially low-cost technologies are described in this report that were developed and applied toward the fabrication of high-efficiency silicon solar cells.

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SUMMARY

SUMMARY

The overall objectives of this program are (1) to develop rapid and low-cost processes for manufacturing that can improve yield, throughput, and performance of silicon photovoltaic devices, (2) to design and fabricate high-efficiency solar cells on promising low-cost materials, and (3) to improve the fundamental understanding of advanced photovoltaic devices. Several rapid and potentially low-cost technologies are described in this report that were developed and applied toward the fabrication of high-efficiency silicon solar cells.

One of the most difficult aspects of large-scale solar cell production is forming high-quality front contacts. The metallization techniques used in laboratory settings (which involve vacuum evaporation, lift-off photolithography, and plating) are too time consuming and impractical for large-scale application. On the contrary, screen-printing (SP) offers a simple, cost-effective contact method that is consistent with the requirements for high-volume manufacturing. The problem with SP, however, is that the throughput gains are attained at the expense of device performance. The losses associated with SP metallization fall into three categories: 1) increased minority carrier recombination in the required heavily doped n^+ regions, 2) increased shading due to wide grid fingers ($> 100\mu\text{m}$), and 3) fill factor degradation due to poor contact quality. The purpose of this section is to provide a detailed study of the third issue: *contact quality*. This is important because contact quality determines the device fill factor, and therefore, affects the overall cell efficiency ($\eta = V_{oc} \cdot J_{sc} \cdot FF$). Though high fill factor performance has been demonstrated in the past with SP, most commercial solar cell processes, which implement this technology result in relatively low fill factors (≈ 0.750). No comprehensive study

has been conducted to isolate the causes for low fill factor in SP cells and relate them to specific process conditions. In chapter 1, the SP process is closely analyzed and developed so that high fill factors (≈ 0.785 - 0.790) can be reproducibly achieved on monocrystalline Si solar cells. The requirements on emitter junction depth and contact firing schedules are established in a systematic manner. For the first time, the beneficial effect of a *post-fire* forming gas anneal on contact resistance is demonstrated. By achieving high fill-factor response, device efficiencies of 17.0% (4 cm^2) are demonstrated for fully screen-printed, planar, single layer AR coated solar cells fabricated on FZ Si substrates.

Surface passivation or electrical confinement of carriers is crucial for high performance Si solar cells. A comprehensive and systematic investigation of low-cost surface passivation technologies for Si cells is presented in chapter 2. Most commercial solar cells today lack adequate surface passivation. In contrast, laboratory cells use conventional furnace oxides (CFO) for high-quality front and/or back surface passivation but at the expense of a lengthy, high-temperature step. This investigation tries to bridge the gap between commercial and laboratory cells by providing fast, low-cost methods for effective surface passivation. As an alternative to CFO, rapid thermal oxides (RTO) can give comparable passivation in a much shorter time. Additionally, plasma deposition of silicon nitride (SiN) has recently emerged as a low-temperature passivation technique, which simultaneously provides a good antireflection coating for silicon solar cells. In this chapter, we demonstrate, for the first time, the efficacy of TiO_2 , thin ($<10 \text{ nm}$) RTO, and PECVD SiN passivation individually and in combination for (diffused) emitter and (non-diffused) back surface passivation. The effects of emitter sheet resistance, surface texture, and three different SiN depositions (two using a direct PECVD

system and one using a remote system) were investigated. The impact of post-growth/deposition treatments such as forming gas anneal (FGA) and firing of screen-printed contacts was also examined. This study revealed that the optimum passivation scheme consisting of a thin RTO, SiN, and 730°C screen-printed contact firing can (a) reduce the emitter saturation current density, J_{oc} , by a factor of >15 for a 90 Ω /sq. emitter, (b) reduce J_{oc} by a factor of > 3 for a 40 Ω /sq. emitter, and (c) reduce S_{back} below 20 cm/s on 1.3 Ω -cm p-Si. Furthermore, this double-layer RTO+SiN passivation is independent of the deposition conditions (direct or remote) of the SiN film and is more stable under heat treatment than SiN or RTO alone. Model calculations are also performed to show that the RTO+SiN surface passivation scheme may lead to 17%-efficient thin screen-printed cells even with a low bulk lifetime of 20 μ s.

A passivation scheme involving plasma silicon nitride (PECVD SiN) deposition on top of SiO₂ grown by rapid thermal oxidation is developed in chapter 3 to attain a low surface recombination velocity (S) of nearly 10 cm/s on the undiffused 1.25 Ω -cm p-type (100) silicon surface. This is particularly important for bifacial screen-printed devices. Such low S values are achieved by the stack structure even when the rapid thermal oxide (RTO) or PECVD SiN films individually yield poorer surface passivation. It is found that the use of a short, moderate temperature anneal (in this study 730°C for 30 seconds) after the stack formation is critical to achieving low S by the RTO/PECVD SiN stack. This thermal treatment is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO₂ interface, thereby reducing the density of interface traps at the silicon surface. Compatibility with this post-deposition anneal makes the stack passivation scheme attractive for cost-effective solar cell production where a similar anneal is required to form screen-printed contacts.

Al back surface field is widely used and is critical for high efficiency devices. However, quality of BSF is a strong function of process conditions. In chapter four, screen-printing and rapid thermal annealing have been combined to achieve an aluminium-alloyed back surface field (Al-BSF) that lowers the effective back surface recombination velocity (S_{eff}) to approximately 200 cm/s for solar cells formed on 2.3 Ω -cm Si. Analysis and characterization of the BSF structures show that this process satisfies the two main requirements for achieving low S_{eff} : 1) deep p^+ region and 2) uniform junction. Screen-printing is ideally suited for fast deposition of thick Al films which, upon alloying, result in deep BSF regions. Use of a rapid alloying treatment is shown to significantly improve the BSF junction uniformity and reduce S_{eff} . The Al-BSF's formed by screen-printing and rapid alloying have been integrated into both laboratory and industrial cells with efficiency of 19.0 and 17.0%, respectively, on planar 2.3 Ω -cm float zone Si. For both process sequences, these cell efficiencies are 1-2% (absolute) higher than analogous cells made with un-optimized Al-BSF's or highly recombinative rear surfaces.

The U.S. Photovoltaic Industry Roadmap calls for an increase in low-cost Si PV cell efficiency to 16% by 2003, and 18% by 2010. Chapter five provides guidelines for achieving $\geq 18\%$ efficient industrial cells through an assessment of impact of individual cost-effective design features. This chapter also reviews recent progress in high-efficiency manufacturable and non-manufacturable mc-Si solar cell technologies with the aim of identifying which technologies are the most promising for the long term goal of silicon photovoltaics.

For widespread implementation of silicon PV, the module cost must be reduced by a factor of 2 to 4. This can be accomplished by lowering the cost of solar cell materials and processing without sacrificing cell efficiency. A combination of high throughput belt line processing, SP contacts and mc-Si material offers an opportunity for significant cost reduction. However, most cell manufacturers who use the above combination are only able to achieve fill factors in the range of 0.68-0.75 with cell efficiencies in the range of 10-14%. Thus throughput gains are attained at the expense of device performance. In addition, there is considerable scatter in the fill factor of the SP cells in the literature with no clear guidelines for achieving high fill factors. This chapter six shows that proper understanding of loss mechanisms and optimization of SP paste and firing cycle, can lead to fill factors approaching 0.77 and 0.79 on mc-Si and single crystal silicon, respectively, on a $45 \Omega/\square$ rapidly formed belt line emitter with a shallow junction depth of $\sim 0.27 \mu\text{m}$. It was observed that, deep and shallow emitters on mc-Si could lead to the same values of fill factors ~ 0.77 when the proper combination of paste and firing cycle is used. The peak firing temperature for deep emitter is higher than the shallow ones with superior value of junction leakage current. Rapid thermal anneal process has been optimized and applied to achieve 14+% efficiency on large area ($10 \times 10 \text{ cm}^2$) screen-printed EFG silicon solar cells. Large area EFG silicon cells were fabricated in collaboration with ASE Americas. The n+ emitter, PECVD SiN single layer AR coating, and printing of silver contacts on the front and Al on the back were done at ASE Americas. The RTP co-firing was done using a rapid thermal processor at Georgia Tech. During the RTP co-firing, PECVD silicon nitride on the front, aluminum paste on the back, and silver front contact metals were annealed simultaneously to achieve silicon nitride induced hydrogenation, aluminum back-surface-field, and ohmic contact of silver grids through the silicon nitride film. RTP co-firing produced $\sim 15\%$ screen-printed solar

cells on EFG as well as string ribbon from Evergreen Solar. A new silicon solar cell structure is developed on dendritic web silicon ribbon in which the p-n junction is formed by alloying aluminum with n-type web silicon, and where this p-n junction is located at the back (non-illuminated) surface of the cell. With a phosphorus front diffusion, the resultant n^+np^+ structure has on 100 μm thick web doped with antimony to 20 $\Omega\text{-cm}$. Such a structure eliminates shunting of the p-n junction, provides an effective front surface field, enables a high minority carrier lifetime in the base, and is immune to light-induced degradation. Using only production-worthy, high-throughput processes, aluminum alloy back junction dendritic web cells have been fabricated with efficiencies up to 14.2% and corresponding minority carrier (hole) lifetime in the base of 115 μs (diffusion length of 370 μm).

A novel device fabrication process called the **STAR** is developed and described in chapter seven. STAR process accomplishes, in a single high temperature step, a Simultaneously diffused emitter and Back Surface Field (BSF), on a Textured silicon wafer, with an *in-situ* thermal oxide for surface passivation and Anti-Reflection coating. In a single high-temperature step, the **STAR** process provides four important quality-enhancement features: (1) emitter oxide passivation, (2) back surface passivation via a boron back surface field, (3) a low reflectance (SiO_2) single layer AR coating and (4) a back surface reflector (BSR) for light trapping. The STAR process is implemented using a novel diffusion technique which can simultaneously form boron and phosphorus diffusions and grow an in-situ thermal oxide in a conventional diffusion furnace, without the deleterious effects of cross doping. Conversion efficiencies as high as 20.1 % have been obtained for this structure on 2.0 $\Omega\text{-cm}$ float zone silicon. This chapter presents a detailed characterization of the impact of each of the above quality enhancement features, using

a combination of an extended IQE analysis, minority carrier lifetime measurements and measurements of the emitter saturation current density, J_{oc} . It is found that the in-situ oxide provides very good front surface passivation, producing J_{oc} values as low as 29.2 fA/cm^2 for a $76 \text{ } \Omega/\square$ emitter. The boron BSF obtained by this approach gives an effective back surface recombination velocity (S_{eff}) of 390 cm/s , while the in-situ back oxide BSR greatly enhances the absorption of long wavelength radiation, providing an additional 1.3 mA/cm^2 in J_{sc} over an equivalent structure without a BSR. Computer simulations are used to improve the understanding of STAR cells and show that the STAR process is capable of producing device efficiencies over 19% on thin, relatively modest quality, solar grade silicon materials.

In chapter eight, a simple porous silicon texturing technique that is applicable to various kinds of silicon material, including multicrystalline and ribbon Si, of any doping type and level is used to fabricate solar cells. Acidic etching of Si leads to a homogeneous porous silicon (PS) surface layer with reflectance as low as 9%. Phosphorus diffusion and thermal oxidation are shown to produce very low emitter saturation current density, 128 fA/cm^2 , which is only slightly higher than values obtained on planar surfaces, but still capable of giving open-circuit voltages in excess of 650 mV. The dopant oxide solid source (DOSS) solar cell process with simultaneous formation of phosphorus emitter and in-situ surface oxide leads to an excellent surface passivation, while maintaining low reflectance on PS textured wafers. The fabricated solar cells gave efficiencies of up to 14.9% using the PS layer for anti-reflection coating (ARC) and surface passivation. This is the highest reported cell efficiency with this kind of texturing and without any additional ARC. The simplicity of the process makes it a very promising technology and easily transferable into industrial production.

Traditional Czochralski grown Si solar cells are known to suffer from light induced degradation (LID) which adversely affects the minority carrier lifetime. Recent methods that have been explored to reduce the effects of LID involve elimination of one of the constituents (Boron and Oxygen) responsible for the degradation via material growth or cell processing techniques. Chapter nine shows that the effects of LID can also be reduced substantially in traditional boron doped CZ silicon cells by using thinner wafers in conjunction with low back surface recombination velocity. A methodology is developed to determine the cell thickness that not only limits the LID but also maximizes the stabilized efficiency after LID. A combination of device modelling and experimental data is used to demonstrate that for a conventional CZ Si, which undergoes a light induced lifetime degradation from 75 μs to 20 μs , optimum cell thickness is $\sim 150 \mu\text{m}$ for a BSRV on the order of 10^4 cm/s . This thickness reduces the light induced efficiency degradation from 0.75% (for a 375 μm thick device) to 0.24% absolute and gives the highest stabilized CZ cell efficiency.

CHAPTER I

FUNDAMENTAL UNDERSTANDING AND DEVELOPMENT OF SCREEN- PRINTED METALLIZATION FOR MONOCRYSTALLINE SI SOLAR CELLS

1. Fundamental Understanding and Development of Screen-Printed Metallization for Monocrystalline Si Solar Cells

One of the most difficult aspects of large scale solar cell production is forming high-quality front contacts. The metallization techniques used in laboratory settings (which involve vacuum evaporation, lift-off photolithography, and plating) are too time consuming and impractical for large scale application. On the contrary, screen-printing (SP) offers a simple, cost-effective contact method that is consistent with the requirements for high-volume manufacturing. The problem with SP, however, is that the throughput gains are attained at the expense of device performance. The losses associated with SP metallization fall into three categories: 1) increased minority carrier recombination in the required heavily doped n^+ regions, 2) increased shading due to wide grid fingers ($> 100\mu\text{m}$), and 3) fill factor degradation due to poor contact quality. The purpose of this section is to provide a detailed study of the third issue: *contact quality*. This is important because contact quality determines the device fill factor, and therefore, affects the overall cell efficiency ($\eta = V_{OC} \cdot J_{SC} \cdot FF$). Though high fill factor performance has been demonstrated in the past with SP [1], most commercial solar cell processes which implement this technology result in relatively low fill factors (≈ 0.750) [2]. No comprehensive study has been conducted to isolate the causes for low fill factor in SP cells and relate them to specific process conditions.

In this chapter, the SP process is closely analyzed and developed so that high fill factors ($\approx 0.785\text{-}0.790$) can be reproducibly achieved on monocrystalline Si solar cells. The requirements on emitter junction depth and contact firing schedules are established in a systematic manner. For

the first time, the beneficial effect of a *post-fire* forming gas anneal on contact resistance is demonstrated. By achieving high fill-factor response, device efficiencies of 17.0% (4 cm²) are demonstrated for fully screen-printed, planar, single layer AR coated solar cells fabricated on FZ Si substrates.

1.1 Fill Factor Loss Mechanisms

The *primary* fill factor loss mechanisms associated with SP metallization are shown in Fig. 1.1. The losses arise from excess: 1) gridline resistivity, 2) contact resistance, and 3) junction leakage and shunting. The *gridline resistivity* and the *contact resistance* both depend on the contact firing cycle and the material qualities of the conductor paste. If the overall resistance becomes excessive, then the solar cell fill factor will be lowered. The *junction leakage* and *shunting behavior* depend primarily on the junction design and the contact firing cycle. If the junction is compromised during the firing cycle, the lowered shunt resistance and increased junction leakage will cause severe fill factor degradation.

The impact of series resistance (R_{series}), shunt resistance (R_{shunt}), and junction leakage (J_{02} and n_2) on device fill factor can be simulated numerically using the solar cell equivalent circuit model shown in Fig. 1.2. (The J_{02} diode and its corresponding ideality factor model the effect of junction leakage via depletion region recombination.) This equivalent circuit was employed together with a device simulator (*PCID-4*) to model the fill factor change as a function of R_{series} , R_{shunt} , and J_{02} . The results (Fig. 1.3-Fig. 1.5) can be used to formulate the following guidelines for attaining high fill factor: $R_{\text{shunt}} > 1000 \text{ } \Omega\text{-cm}^2$, $R_{\text{series}} < 0.50 \text{ } \Omega\text{-cm}^2$, and $J_{02} < 10^{-8} \text{ A/cm}^2$. In the following sections, the experimental behavior of screen printed metallization in the context of these parameters is presented. Different characterization techniques, such as diode (dark) IV,

solar cell lighted IV, contact resistance, and conductivity analysis, are used to extract the parameters which govern fill factor response.

1.2 Effect of SP Firing Treatment on Conductor Paste Resistivity

The conductor paste used in this work was made by Ferro Corporation (*3349 Ag Conductor*). After printing, the following procedure was used to form the contacts. First, the solvents were removed by baking on a hotplate at 150°C for 2 minutes. This was followed by firing in a 3-zone IR-belt furnace in which the lengths of zones 1,2, and 3 were 7.5", 15", and 7.5", respectively. The first two zones were set to 425°C and 580°C and used to burn off organic materials in the printed paste. The *hotzone* (zone 3) temperature was varied to suit the particular investigation. The overall firing time was determined by the beltspeed through the furnace. Beltspeeds of 15"/min and 40"/min were implemented in this study, which correspond to hotzone dwell times of 30 seconds and 11 seconds, respectively.

First, the Ag resistivity was determined so that basic model calculations could be performed. (It is instructive to note that the resistivity of pure Ag is 1.6 $\mu\Omega$ -cm.) As shown in Fig. 1.6, this parameter is a function of hotzone firing temperature. In fact, the resistivity changes by more than a factor of 2 (from 5.3 to 2.2 $\mu\Omega$ -cm) for a hotzone temperature swing of 300°C and a dwell time of 30 seconds. The data also shows the effect of varying the beltspeed through the furnace. Two points are important to note when considering the effects of beltspeed on a process. The first issue is obvious: a higher beltspeed reduces the overall process time. Additionally, for a fixed temperature setting, a higher beltspeed will result in the sample moving deeper into the furnace before it is brought to temperature. To compensate for these effects, the temperature

setpoints must be increased when a faster beltspeed is implemented. This behavior is evident in Fig. 1.6.

The data in Fig. 1.6 was used to model and compare the power loss expected for solar cells with pure Ag contacts ($1.6 \mu\Omega\text{-cm}$) and SP Ag contacts ($3.5 \mu\Omega\text{-cm}$, 700°C hotzone, 30 sec dwell time). The following device parameters were used for simulation purposes: solar cell active area of 2 cm by 2 cm, 8 grid fingers, a single tapered bus bar, and a $40 \Omega/\text{sq}$ emitter sheet resistance. The width and height of each finger were fixed at $130 \mu\text{m}$ and $8 \mu\text{m}$, respectively (typical values for screen-printed solar cells). The simulations show that the increased metal resistivity of SP Ag compared to pure Ag leads to an R_{series} increase of $0.12 \Omega\text{-cm}^2$ and an *additional* power loss of $0.14 \text{ mW}/\text{cm}^2$. In other words, SP fill factors are inherently lower than those of a pure Ag metallization by approximately 0.010 due to higher ρ_{metal} and R_{series} .

1.3 Effect of Junction Depth on the FF of Monocrystalline Si Solar Cells

As discussed in Section 2, most conductor pastes contain a small amount of glass frit. The frit serves to improve adhesion to the substrate by conforming to the surface topology. Additionally, for Si substrates, the frit *etches* a small distance into the Si material. If the firing process is too aggressive, the glass frit along with the metal particles will begin to encroach on the n^+p junction. This encroachment manifests itself as decreased R_{sh} and increased J_{o2} . As indicated by the modeling results in Fig. 1.2, low R_{sh} and high J_{o2} can destroy the device fill factor.

In this section, the importance of junction depth on the quality of SP contacts is explored. A set of phosphorus diffusions was carried out using cerium pentaphosphate solid sources. The diffusion time was fixed at 30 minutes, and in each case the peak temperature was varied. The

resulting sheet resistances were in the 40-90 Ω/sq range, and the junction depths are shown in Fig. 1.7.

Screen-printed solar cells were formed on each emitter. (Throughout this study, all devices were 4 cm^2 in area, and the front contact coverage was roughly 7%). To fire the contacts, an intermediate beltline firing cycle (hotzone temperature of 730°C and beltspeed of 15"/min) was selected based on Fig. 1.6. After firing, the contacts were annealed in forming gas at 400°C. (This FGA plays an important role in reducing contact resistance, and will be discussed in detail in a following section.) A histogram of fill factor versus emitter sheet resistance is shown in Fig. 1.8. For comparison, the high fill factor of a device formed with photolithography (PL) contacts is also shown. The same data is presented as a function of junction depth in Fig. 1.9.

As shown in Fig. 1.9, the highest fill factor was measured for the deepest junction (40 Ω/sq , x_j of 0.38 μm). Yet even for this case, there is a noticeable fill factor spread (0.740-0.780) which is unacceptable for reliable, high-efficiency devices. As the emitter junction depth decreases, the fill factor drops off sharply. This behavior suggests two possibilities: 1) with reduced junction depth the cells suffer from lowered R_{sh} and high J_{o_2} , or 2) with increased emitter sheet resistance the devices experience higher R_{series} from contact resistance effects. In order to precisely determine the cause for the fill factor drop, the non-illuminated I-V responses for the cells were measured and analyzed. Plots of these IV curves are shown in Fig. 1.10. For comparison, the IV response for a cell with contacts formed by lift-off PL is also shown. It is immediately evident that the lift-off PL cell has a large R_{sh} and low leakage current. Fitting this IV curve to the equivalent circuit model in Fig. 1.2 reveals in an $R_{\text{sh}}=6 \times 10^3 \Omega\text{-cm}^2$, $J_{\text{o}_2}=1 \times 10^{-8} \text{ A/cm}^2$ (with $n_2=2$), and $R_{\text{series}}=0.35 \Omega\text{-cm}^2$. These parameters are consistent with the high fill factor (0.792) exhibited by the cell. On the contrary, the R_{sh} behavior for all the screen-printed devices is significantly

worse. Analysis of these devices reveals R_{sh} values less than $1000 \Omega\text{-cm}^2$ in all cases and J_{o2} values greater than $0.5 \mu\text{A}/\text{cm}^2$ ($n_2=2.2$). Moreover, the junction leakage worsens with increasing emitter sheet resistance and decreasing junction depth. These effects are responsible for the fill factor degradation and scatter shown in Fig. 1.8 and Fig. 1.9.

It is interesting to note that for all the n^+ emitters shown in Fig. 1.10, which exhibit surface concentrations between 2×10^{20} - $5 \times 10^{20} \text{ cm}^{-3}$, the R_{series} for all SP contacts is essentially the same.

This observation is important because R_{series} is often presumed to be the cause of fill factor degradation when in fact the problem stems from the compromised junction.

1.4 Reducing Leakage and Shunting with Deeper n^+ Emitters

Deeper emitters were attained by diffusion from a POCl_3 liquid source at a diffusion temperature of 900°C . An appropriate gas flow condition and diffusion time were established so that a $35\text{-}40 \Omega/\text{sq}$ emitter with $0.5 \mu\text{m}$ junction depth was achieved. The n^+ region profile is shown in Fig. 1.11 along with the first set of emitters formed by solid source diffusion. Initial SP solar cells were fabricated on this new emitter using the same process detailed above (hotzone of 730°C and beltspeed of $15''/\text{min}$). Average fill factors of 0.785 were consistently achieved. It is evident from Fig. 1.12 that the problems of excess shunting and leakage are eliminated.

Table 1.1: Junction depth requirement for screen printed contact formation to monocrystalline Si solar cells.

Junction Depth	R_{shunt} Value	Junction/FF Quality
< 0.25 μm	low	Completely shunted/Low FF
0.30-0.40 μm	< 1000 $\Omega\text{-cm}^2$	Onset of leakage/Moderate FF
> 0.50 μm	\approx 10,000 $\Omega\text{-cm}^2$	No shunting or leakage/High FF

By consolidating the data in Fig. 1.8 through Fig. 1.12, the following guidelines for emitter junction depth are established for SP contact formation.

1.5 Effect of Firing Conditions and Post-Firing Forming Gas Anneal on the Contact Resistance and Fill Factor

In addition to R_{sh} and J_{o2} , the quality of SP contacts depends critically on the overall R_{series} . This was shown in the modeling results of Fig. 1.4 and Fig. 1.5. R_{series} is comprised of different resistance components (metal resistivity and contact resistance, among others). The metal resistivity issue is discussed in Section 4.2.2. In this section, the contact resistance (ρ_c) associated with SP metallization is investigated. In a novel application, a low-temperature FGA is shown to be effective in lowering ρ_c *after* the SP contacts have been fired in the IR-belt furnace.

The investigation of peak firing condition on fill factor was extended for large temperature variations. The response is shown in Fig. 1.13 for beltspeeds of 15"/min and 40"/min. Immediately after the firing treatment, the fill factors are prohibitively low (\approx 0.500-0.600). However, the fill factors drastically improve after the samples are annealed in forming gas at 400°C. For the hotzone dwell time of 30 sec (beltspeed of 15"/min), there exists at least a 60°C

range in acceptable peak firing temperature (690°C to 750°C) in which final fill factors of 0.785 are attained. For the 40"/min beltspeed, a similar range exists, though higher process temperatures are required to offset the reduced dwell time and increased ramp-up distance. These results indicate that, in contrast to conventional thinking on the topic, the range of acceptable firing temperatures is relatively broad.

In order to verify that the FGA specifically acts to improve ρ_c , non-illuminated IV measurements were conducted for a typical device before and after the FGA treatment. The result in Fig. 1.15 shows that after annealing, the curve changes in the high-current regime where the response is most sensitive to R_{series} . It was determined separately that the FGA has no effect on the gridline resistivity of the fired metal. This clearly shows that the only parameter altered by the FGA is ρ_c . Additionally, *transmission line model* (TLM) based contact resistance measurements were performed for the SP metallization (Fig. 1.14). These results also provide clear support of ρ_c reduction as a result of the FGA treatment.

It is believed that the FGA initiates an oxidation-reduction (redox) reaction at the interface between the printed metal and the Si surface. The question is why should such a reaction be important for SP contacts? The Ag paste used in this study contains a lead borosilicate glass frit. At the time of printing, the Ag and frit particles are packed together within the organic vehicle. When firing is initiated, the organic vehicle is burned away leaving behind the metal-frit combination. As the temperature is raised further, the metal particles begin to sinter which serves to expel or "squeeze out" the frit from the interior of the printed feature. (This process is also referred to as glass "bleedout" [3].) The glass frit is forced to migrate to the metal surface and the Si-metal interface. Since the firing is done in air, some of the lead content in the frit becomes oxidized. This creates an insulating layer and a large ρ_c at the metal-Si interface. The hydrogen in

the ensuing FGA is believed to reduce this species back to Pb, bringing about the measured improvement in the ρ_c .

In order to provide a degree of verification for this model, a similar contact anneal at 400°C was conducted in N₂ instead of forming gas. The results in Fig. 1.16 show that the N₂ anneal in *no way* improves the contact quality. However, subjecting the same samples to a subsequent FGA treatment improves the fill factor to a high level. This provides clear evidence that hydrogen is the active species in this process, and it supports the theory that a reduction reaction is occurring at the Si surface to lower ρ_c .

1.6 Effect of Peak Firing Temperature on Solar Cell Shunting Behavior and Fill Factor

It is instructive to analyze the results of Fig. 1.13 in greater detail to ascertain the effect of peak firing temperature on contact quality. As indicated in this figure, there is a relatively large firing window (>60°C) which can be implemented to form high quality contacts. The question arises as to precisely what effect (if any) the process temperature within this range has on the contact quality. The average dark IV responses for certain devices are shown in Fig. 1.17. The corresponding R_{sh} values, extracted from numerical analysis of the IV curves, are shown in Fig. 1.18. The analysis reveals that increasing the hotzone temperature by as little as 10°C results in a measurably reduced R_{sh} . A 60°C increase in hotzone temperature reduces R_{sh} by over one order of magnitude, from $2 \times 10^4 \Omega\text{-cm}^2$ at 690°C to $10^3 \Omega\text{-cm}^2$ at 750°C. However, as shown in Fig. 1.3, an R_{sh} value of $10^3 \Omega\text{-cm}^2$ essentially marks the cutoff between high and low fill factor

Table 1.2: Reproducibility of the SP process developed in this study. Each entry represents an average value over multiple (≈ 9) cells. All devices are planar, 4 cm^2 in area, with single layer AR coatings.

Run ID	Cell Type	Voc (mV)	Jsc (mA/cm ²)	Fill Factor	Eff. (%)
1	1.3Ω-cm Si (850°C beltline Al-BSF)	624	34.5	0.791	17.0
2	1.3Ω-cm Si (850°C beltline Al-BSF)	623	33.8	0.789	16.6
3	1.3Ω-cm Si (850°C RTP Al-BSF)	626	34.4	0.783	17.0
4	0.65Ω-cm Si (no BSF)	621	32.8	0.785	16.0
5	0.65Ω-cm Si (900°C beltline Al-BSF)	635	33.7	0.796	17.0

response for solar cells. Since all cases in Fig. 1.17 have R_{sh} values are higher than $10^3 \Omega\text{-cm}^2$, all devices exhibit high fill factors (≈ 0.785).

Fig. 1.6 and Fig. 1.17 illustrate the fundamental competition in the SP process. Higher temperatures are needed to achieve low gridline resistivity, whereas lower temperatures are desirable to avoid shunting. The highest fill factors are achieved only when both R_{series} and R_{shunt} values fall within acceptable ranges.

In order to determine the reproducibility of this contact formation method, many solar cells were fabricated with the above developed process. By implementing the $0.5 \mu\text{m}$ deep POCl_3 emitter, a hotzone temperature of 700°C - 730°C with a dwell time of 30 seconds, and a 10 min

FGA after firing, fill factors between 0.785-0.795 were achieved in a consistent manner on monocrystalline Si. Some of these results are listed in Table 1.2.

1.7 SP mc-Si Solar Cells

The SP process has been applied to various mc-Si substrates including Solarex, HEM, and Eurosolare. The fill factors as a function of junction depth are shown in Fig. 1.19. The results show that for highest FF response, deeper junctions are required for mc-Si substrates than for (100) single crystal Si. The increase in junction depth required, and the relative fill factors achieved, are material specific. It has been observed [4] that the etch reaction between the frit and Si is more aggressive for certain crystalline orientations (preference for $\langle 111 \rangle$ over $\langle 100 \rangle$). Since mc-Si grains exhibit random orientations across a wafer, the reaction of the frit with various grains will be different. Some regions will have a greater tendency to react, and therefore, decrease the R_{shunt} .

1.9. Fabrication and Characterization of Gridded-Back Contact Solar Cells

The RTO/SiN stack passivation scheme is applied to the fabrication of *gridded-back contact* (GBC) screen-printed solar cells. In order for these devices to be highly efficient, two important requirements must be met. First, the contact resistance (ρ_c) at the rear SP electrode must be low. Secondly, the area averaged S_b (with contact coverage effect) must be reduced to levels well below 500 cm/s. Both of these issues are investigated in this section. A methodology for accurately extracting ρ_c at the rear electrode is developed and applied in the analysis of GBC

cells. The effect of rear electrode coverage on the overall surface passivation quality is also analyzed. Model calculations are performed to demonstrate whether the stack passivation and GBC scheme can be applied to thinner substrates without sacrificing performance.

1.9.1 Impact of the Back Contact on GBC Cells

The GBC device (Fig. 1.20a) has the potential for high-efficiency and bifacial performance. The structure is attractive from a manufacturing standpoint because it can be formed completely using rapid process techniques. Two features of the cell processing are particularly noteworthy. First of all, front and rear contacts can be fired in the same thermal cycle (*co-firing*), which simplifies processing and reduces cost. In contrast, the Al-BSF cell described in this chapter requires a separate high-temperature (850°C) alloying step for p⁺ junction formation. Moreover, the stress created by this Al-BSF process can preclude application to thin wafers. Secondly, only a small quantity of metal paste is needed to form the back contact to the GBC structure. Simple calculations show that a gridded-back contact with a line height of 15 μm, line width of 200 μm, and line spacing of 2.5 cm requires ≈125 times *less* conductor paste than a full coverage BSF. Clearly, the GBC structure offers advantages from the standpoint of both process simplicity and material cost. The challenge, however, is to form a contact that reduces both resistance and recombination experienced at the rear side of the structure.

In order to maximize the efficiency of a GBC device, the contact resistance (ρ_c) at the back must be low. This requirement is complicated by three factors. First, the bulk doping level of PV substrates is relatively low ($<310^{16} \text{ cm}^{-3}$), which creates a barrier to current flow at the metal-Si

junction. Second, the printed lines must physically punch through the SiN layer before reaching and contacting the Si surface. Finally, to take advantage of the co-firing feature displayed in Fig.1.20b, the above obstacles must be overcome with the same firing cycle used to form the front contacts. Because of these issues, selection and application of an appropriate rear contact conductor paste is imperative for achieving effective device performance.

1.9.2 Quantitative Assessment of ρ_c for Rear Conductor Pastes

Two types of conductor paste (*Ferro Corp.*) were investigated for application to the back contact. The first was a pure Al paste and the second was a Ag paste mixed with a small fraction of Al additive. The pastes were printed in a special configuration known as the transfer length method (TLM), and fired in a beltline furnace using the 730°C/30 second SP firing cycle. A general TLM test structure is shown in Fig.1.21. It consists of a series of contacts separated by unequal distances.

Between any two adjacent pads, the resistance can be expressed as

$$R_T = \frac{\rho_s}{Z} \cdot d_i + 2R_c \quad (1)$$

where R_c is the total contact resistance and ρ_s is the semiconductor sheet resistance. Equation (1) represents a line with y-intercept equal to $2R_c$. Since ρ_c is embedded in R_c , determination of the y-intercept from the R_T versus d_i plot allows for the extraction of ρ_c [5]:

$$\rho_c = (R_c \cdot Z)^2 \sqrt{\rho_s} \quad (2)$$

It is important to realize that the semiconductor sheet thickness is assumed to be zero in the TLM technique. This is equivalent to saying the current flow in the diffused region is strictly one-dimensional. However, it is difficult to satisfy this requirement when attempting to measure ρ_c to p-Si with N_a of $\approx 10^{16} \text{ cm}^{-3}$ (typical for PV substrates). The problem is that substrate wafers are thick ($\approx 300 \text{ }\mu\text{m}$). This leads to two-dimensional current flow in the test structure. Clearly, the TLM technique is not ideally suited for thick wafers. More generally, simple techniques for determining ρ_c to PV substrates are not readily available. Therefore, accurate determination of ρ_c at the back contact is one of the challenges to developing the GBC structure.

In spite of this non-ideality, the TLM technique was applied as an initial characterization tool. Al and Ag pastes were printed onto p-Si wafers with varying N_a (between 5×10^{15} and $2.2 \times 10^{16} \text{ cm}^{-3}$) and different surface conditions. *Surface condition* refers to whether the Si wafer is bare or pre-coated with a SiN film. Again, this issue is particularly relevant for the GBC cell because the contacts must be fired through the passivating RTO/SiN stack (as shown in Fig.1.20.b). The TLM-extracted ρ_c values for each process are shown in Fig.1.22.

The lowest ρ_c values are attained for Al paste fired directly on bare Si. This is attributed to the alloying reaction between Al and Si at elevated temperatures. However, the same process is unsuccessful when the Al paste is fired through SiN. In this case, the SiN film serves as a diffusion barrier that prevents alloying between Al and Si. Since Al paste can not punch-through SiN at 730°C , ρ_c values for this process are not measurable.

It is important to note that while the Al punch-through process is unsuccessful at the 730°C condition, a more energetic thermal cycle can be applied to achieve low ρ_c with this paste. An example of this, where Al is fired through SiN at 850°C in two minutes, is shown in Fig. 1.22.

The ρ_c values for this process are nearly as low as those attained for Al fired on bare Si. However, it is important to remember that high-temperature can not be applied to a co-firing process because the front contacts would quickly diffuse through (shunt) the emitter junction and destroy the device. If such temperatures were required for back electrode formation, the front contacts would have to be fired separately. This would increase process complexity and fabrication time. For these reasons, the pure Al paste is essentially incompatible with the *co-fired* GBC structure. However, high-temperature firing could potentially be applied to form a local Al-BSF device.

The results are notably different for the Ag paste. When fired using the standard 730°C/30 second beltline condition, the Ag paste successfully punches-through the SiN layer. This punch-through ability is aided by the glass frit content in the mixture. A small amount of frit in the paste can induce etching of the underlying material (in this case SiN), which results in excellent adherence of the printed lines to the substrate. While the ability of the Ag paste to punch-through SiN is attractive, the ρ_c values for this process are approximately two times higher than for the same paste fired on bare Si, and approximately 10 times higher than for the Al paste fired on bare Si. In the next section, model calculations are performed to determine whether these ρ_c levels are acceptable for effective device operation.

While it is believed that the trends in Fig. 1..22 are representative of the ρ_c behavior, it is probable that the absolute ρ_c values are affected by the deviations from the ideal TLM setup. To further investigate this issue, an alternative ρ_c extraction methodology particularly suited for solar cell back contacts was developed. The details of this methodology and the results of its application are described below.

1.9.2.1 *Quantitative Assessment of ρ_c by a Combination of One Dimensional Power Loss Modeling and Cell Fabrication*

The ohmic losses associated with the contacts in a conventional cell (with full back coverage) are shown in Fig. 1.23. R1, R2, R3, R4, R5, and R6 represent the bus bar resistance, grid finger resistance, front contact resistance, emitter sheet resistance, substrate resistance, and rear contact resistance, respectively.

Expressions for the power loss associated with each resistive component are given in Equations (3)-(7) [6]. (The power loss at the rear contact is typically neglected because of the full area coverage.) All geometric variables used in these equations are defined in Fig.1.24

$$P_{lateral-sheet} = \frac{2}{3} J_L^2 nab^3 \rho_{sheet} \quad (3)$$

$$P_{contact-front} = 2J_L^2 nab^2 (\rho_c \cdot \rho_{sheet})^{1/2} \quad (4)$$

$$P_{finger} = \frac{4}{3} (J_L^2 na^3 b^2 \rho_{metal}) / (h \cdot w_{finger}) \quad (5)$$

$$P_{bus} = \frac{2}{3} (J_L^2 a^2 n^3 b^3 \rho_{metal}) / (h \cdot w_{bus}) \quad (6)$$

$$P_{bulk} = 2J_L^2 nab \rho_{bulk} t \quad (7)$$

The analysis of this conventional cell can be extended to account for a gridded-back contact by simply adding a *rear contact resistance* and a *lateral bulk (sheet) resistance*. The expressions for these two loss components are direct analogies of Equations (3) and (4) with the bulk semiconductor properties substituted for the emitter sheet resistance:

$$P_{\text{contact-back}} = 2J_L^2 nab^2 (\rho_c \cdot \rho_{\text{bulk}})^{1/2} \quad (8)$$

$$P_{\text{lateral-bulk}} = \frac{2}{3} J_L^2 nab^3 \rho_{\text{bulk}} \quad (9)$$

Together, Equations (7) and (9) represent a one-dimensional approximation to the two-dimensional problem at hand. The assumption is that the resistive losses created by the vertical and horizontal current flow in the base are independent and additive (a simplification that results in a “worst-case” resistance calculation). The validity of this assumption becomes evident later in this section. The overall solar cell series resistance can be calculated by summing all of the applicable power loss terms above and dividing by the *active area* current density J_L :

$$R_s = P_{\text{total}} / J_L^2 . \quad (10)$$

Equations (3)-(10) were incorporated into a computer model and used to simulate FF response for different back contact structures. The primary objective was to determine the effects of the back ρ_c and rear contact spacing (Δx) on R_s and FF in GBC devices. Simulated FFs for 0.65 and 1.3 Ω -cm p-Si substrates are shown in Fig.1.26 and Fig.1.27. Experimental values were generated with the test structure shown in Fig.1.25. The back contact to this test structure was formed by firing Ag paste through SiN at the standard 730°C/30 second condition. The measured data is also plotted in Fig. 1.26 and Fig.1.27.

The simulations reveal that ρ_c variation creates a shift in the FF versus Δx plot. By comparing the measured data with simulation, the true ρ_c value at the back electrode can be determined. Applying this methodology, ρ_c values of approximately 10 $\text{m}\Omega\text{-cm}^2$ and 1 $\text{m}\Omega\text{-cm}^2$

are attained for Ag contacts to 1.3 Ω -cm and 0.65 Ω -cm p-Si, respectively. These values are substantially lower than the ones determined by the TLM technique. The modeling also indicates that the TLM-extracted ρ_c values are inconsistent with the true device operation.

1.9.2.2 Fabrication and Analysis of GBC Solar Cells

In Table 1.3, GBC cells are compared to devices that lack an effective back surface treatment. (Here, *no passivation* refers to a fully SP Al co-fired with the front contact. This process results in poor S_{eff} .) The performance difference illustrates the stack's ability to effectively lower S_b . The Siemens CZ result is particularly noteworthy because it illustrates the importance of lowering S_b for currently used PV grade Si. The importance of lowering S_b will become more critical as PV substrates are cut (or grown) thinner. The 17% efficiency attained with the GBC structure on 0.65 Ω -cm FZ is essentially the same as the highest efficiency Al-BSF cell.

Bifacial devices with rear-illuminated efficiencies of 11.6% ($V_{\text{oc}}=624$ mV, $J_{\text{sc}}=25.1$ mA/cm², FF=0.743) were also achieved on 300 μ m thick 0.65 Ω -cm Si. The ratio of $J_{\text{sc}}(\text{rear})/J_{\text{sc}}(\text{front})$ for these devices was ≈ 0.75 .

As discussed previously, the effective S_b for GBC cells is a combination of the recombination activity at the dielectric/Si interface and the metal gridline/Si interface. For reduced gridline spacing, the area coverage of the rear metal increases, which increases the

effective S_b . This is clearly observed in Table 1.3. An IQE comparison for GBC devices with different Δx is shown in Fig. 1.28.

Table 1.3: Passivated rear SP solar cell performance. All cells contained rear metal overlays as in Fig.1.25. The PV grade CZ Si was grown by Siemens Corporation. (*Verified at Sandia National Laboratory, †Average value of nine cells measured at UCEP)

Material	Rear	Grid	V_{oc}	J_{sc}	FF	Eff
	Surface	Spacing	(mV)	(mA/cm²)		(%)
0.65 Ω -cm	GBC	2500 μm	641	33.4	0.792	17.0*
FZ-Si	GBC	1750 μm	637	32.5	0.782	16.2†
	No Pass	---	622	31.8	0.801	15.8*
1.3 Ω -cm	GBC	3000 μm	636	34.8	0.762	16.9†
FZ-Si	GBC	1750 μm	631	33.1	0.776	16.2†
	No Pass	---	609	32.8	0.786	15.7†
0.8 Ω -cm	GBC	2500 μm	622	32.0	0.776	15.5†
CZ-Si	No Pass	---	611	31.0	0.782	14.8†

It was shown in section 1.6 that for 0.65 Ω -cm Si without any metal coverage, the stack passivation results in an S of ≈ 20 cm/s. However, for the GBC cell with Δx of 2500 μm , the rear surface metal coverage is approximately 8.3%. The spatially averaged S_b for the device is expected to be considerably higher than the S of 20 cm/s measured for the stack passivation alone. A combination of rear-illuminated IQE measurements and model calculation was performed in order to accurately extract S_b for the cell.

The measured rear-illuminated IQE for the bifacial cell is shown in Fig.1.29. (A light bias of roughly 0.25 suns was applied during the measurement.) Also shown in Fig.1.29 is a

family of simulated curves for the same device structure. A comparison of measurement to simulation shows that the GBC device experiences an effective S_b of ≈ 340 cm/s near the J_{sc} bias condition, which is a factor of 17 higher than the S value measured for the stack alone. It is evident that the 8.3% metal coverage has a substantial impact on the effective recombination at the rear side of the device. Nonetheless, this effective S_b of 340 cm/s is within the target range established earlier by model calculations.

1.9.3 Modeling the Impact of the Stack Passivation for Thin Solar Cells

A primary advantage of the GBC structure is that it can be applied to thin substrates without causing breakage and yield problems. At the same time, however, the impact of S_b on device performance becomes more pronounced for thinner substrates. If S_b is high, the cell performance will suffer when substrate thickness is reduced. If S_b is low, the performance will either remain the same or improve when the cell thickness is reduced. Model simulations were performed to predict the effect of substrate thickness for the GBC structure with effective S_b of 340 cm/s on 0.65 Ω -cm Si. All other important input parameters (emitter profile, S_{front} , surface reflectance) were gathered from separate measurements.

The results in Fig.1.30 show that for the high S_b case (10^4 cm/s), the V_{oc} response falls significantly as substrate thickness is reduced. (This high S_b situation is analogous to the rear surface being fully covered by a metal layer or a poorly formed Al-BSF region.) On the contrary, for the stack passivated GBC structure (with S_{eff} of 340 cm/s), the V_{oc} remains the same even after the cell thickness is substantially reduced. Corresponding cell efficiencies in Fig.1.31 indicate that for thin ($\approx 100\mu\text{m}$) material, the passivated GBC structure can result in an efficiency

improvement of nearly 2% absolute over the non-passivated case. This compatibility with thin substrates makes the stack passivation scheme highly attractive for low-cost, high-efficiency commercial solar cell production.

1.10 Conclusions

An effective SP methodology has been developed which yields high-quality contacts and fill factors in the 0.785-0.795 range on single crystal Si solar cells. These values approach those achieved by intricate lift-off photolithography procedures. In achieving these results, multiple device related effects have been established. It has been shown that a critical junction depth (0.5 μm in the present case) is required to avoid fill factor degradation due to device shunting and excessive leakage. For this optimal emitter design, a relationship between peak firing temperature and the resulting R_{shunt} has been determined. Additionally, a novel post-firing FGA process has been shown to dramatically improve fill factor by lowering the contact resistance. It is believed that the hydrogen exposure during this treatment induces a redox reaction at the interface between Si and the SP contacts. This contact formation methodology has been used to achieve 17% efficient fully screen-printed, planar, single layer AR coated devices (4 cm^2 area) on FZ substrates.

Screen-printed GBC cells with efficiencies as high as 17% have been fabricated on 0.65 $\Omega\text{-cm}$ Si. These cells are approximately 1% absolute higher in efficiency than those formed with ineffective rear surface treatments (or high S_b), and essentially equivalent to cells formed with optimized Al-BSF regions. In addition, rear-illuminated efficiencies as high as 11.6% have been achieved for fully SP bifacial structures. An attractive feature of the GBC fabrication process is

that both front and rear contacts are co-fired together in the same thermal cycle. In this study, a methodology for accurately extracting the rear ρ_c for GBC cells was developed. Applying this technique to the analysis of different conductor pastes showed that a Ag paste (containing a small amount of glass frit and Al additive) is an appropriate material for a rear electrode. Rear-illuminated IQE measurements showed that the effective S_b for the GBC device with rear metallization coverage of 8.3% was approximately 340 cm/s. Model calculations reveal that this passivation scheme can be applied to thinner substrates without experiencing any V_{oc} degradation. This behavior, coupled with the fact that the RTO/SiN stack does not cause excess stress in thin substrates, demonstrates the strong potential of this GBC structure for future PV applications.

1.11 References

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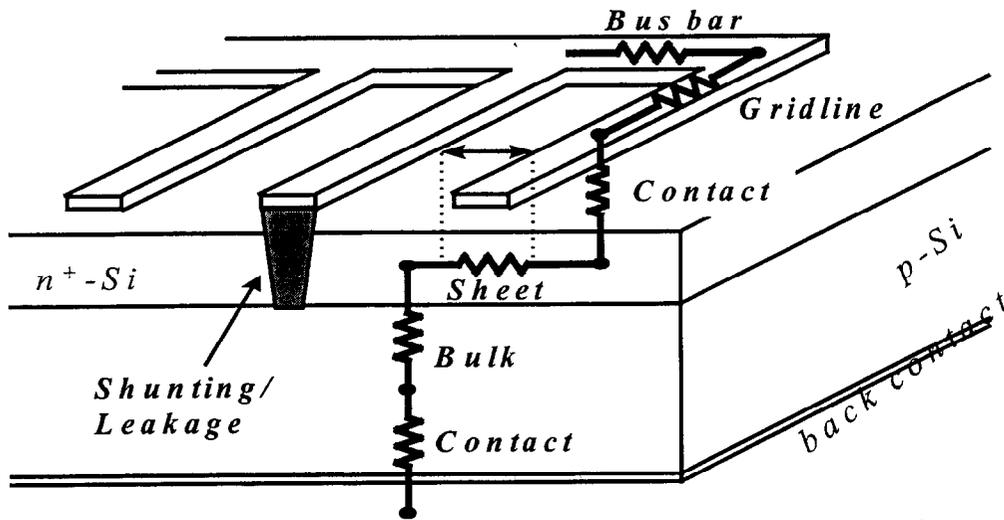


Fig. 1.1 Fill factor loss mechanisms associated with screen printing.

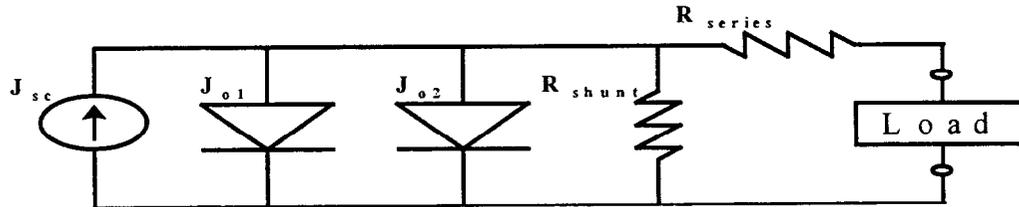


Fig. 1.2 Solar cell equivalent circuit. Fill factor is influenced by J_{o2} , R_{shunt} , and R_{series} .

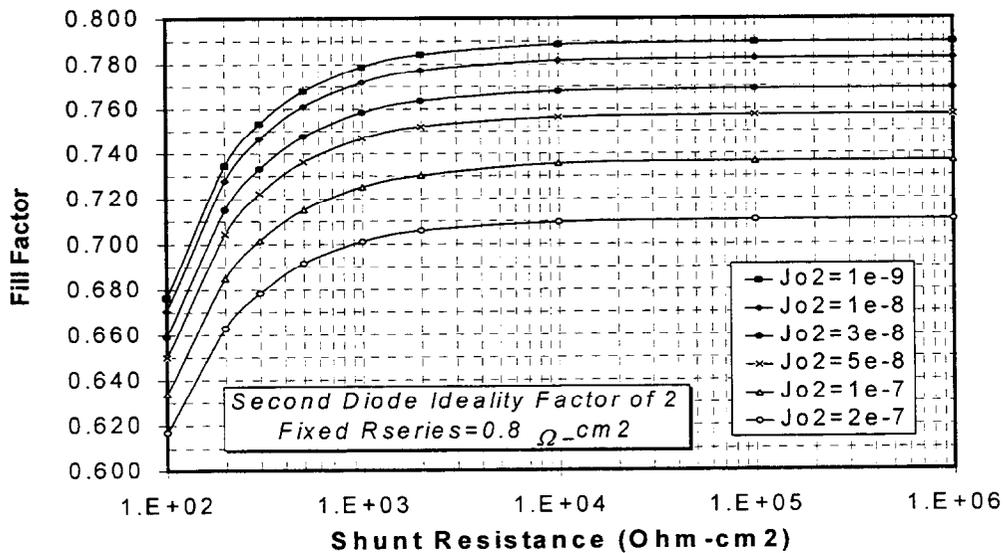


Fig. 1.3 Effect of R_{shunt} and J_{o2} on fill factor response. (R_{series} fixed at $0.8 \Omega\text{-cm}$)

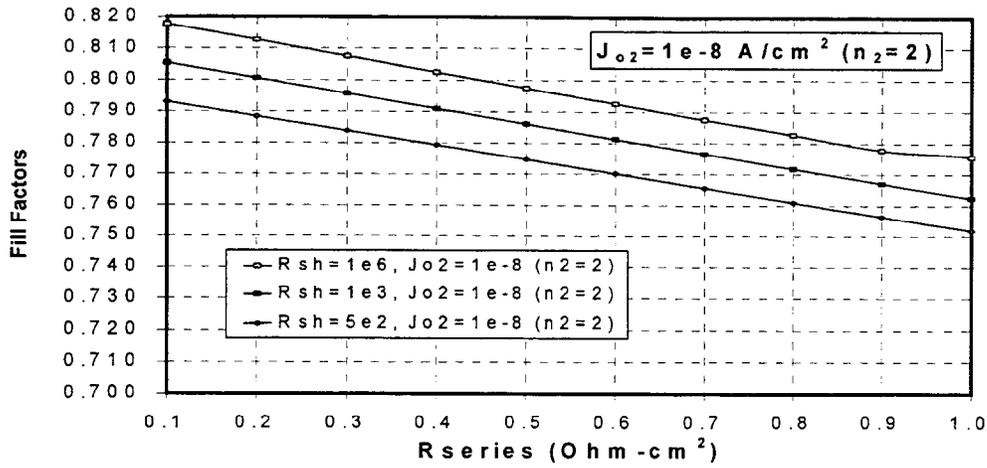


Fig. 1.4 Effect of R_{series} and R_{shunt} on fill factor response. (J_{o2} fixed at 10^{-8} A/cm^2)

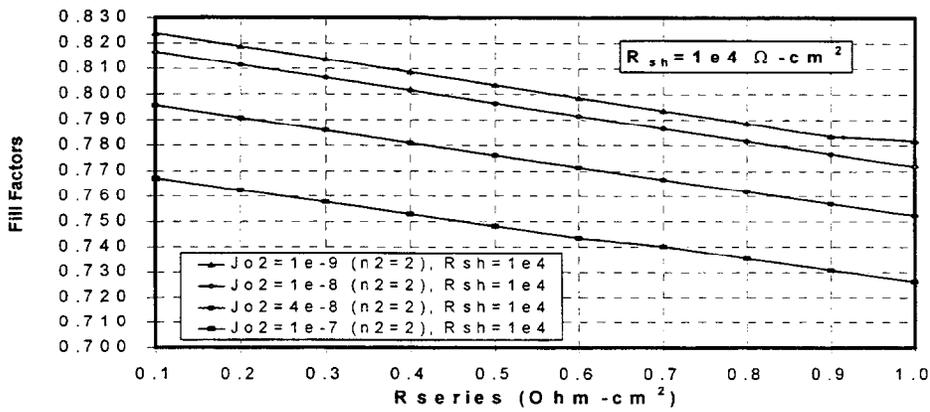


Fig. 1.5 Effect of R_{series} and R_{shunt} on fill factor response. (R_{shunt} fixed at $10^4 \Omega \cdot \text{cm}^2$)

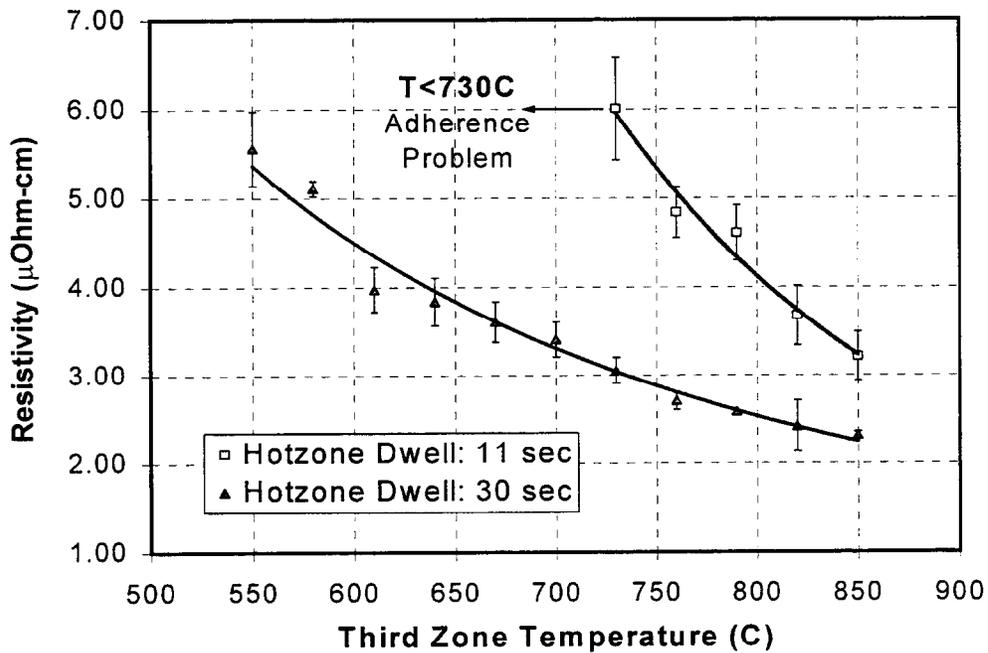


Fig. 1.6 Effect of beltline firing temperature and belt-speed on metal conductivity. The corresponding hot-zone dwell times are 30 sec (15"/min) and 11 sec (40"/min)

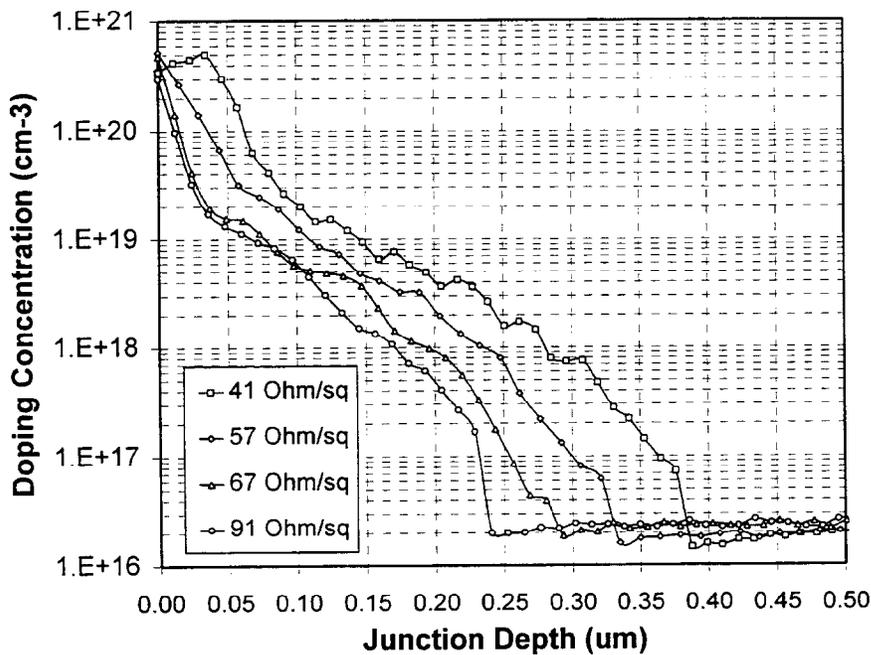


Fig. 1.7 Solid source diffusion profiles measured by the spreading resistance technique. The diffusion time was fixed at 30 min, and the highest temperature used was 850°C.

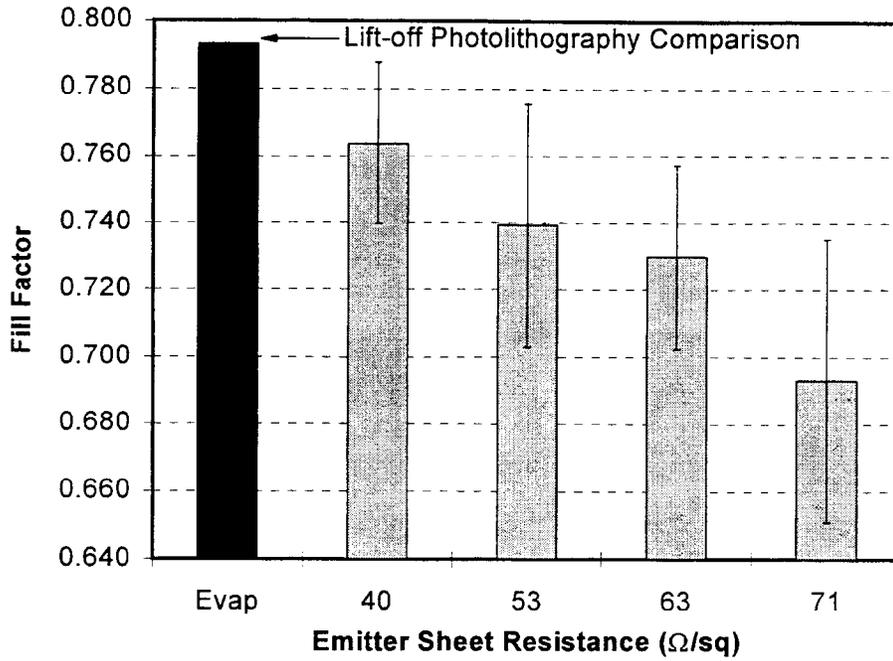


Fig. 1.8 Fill factor versus emitter sheet resistance

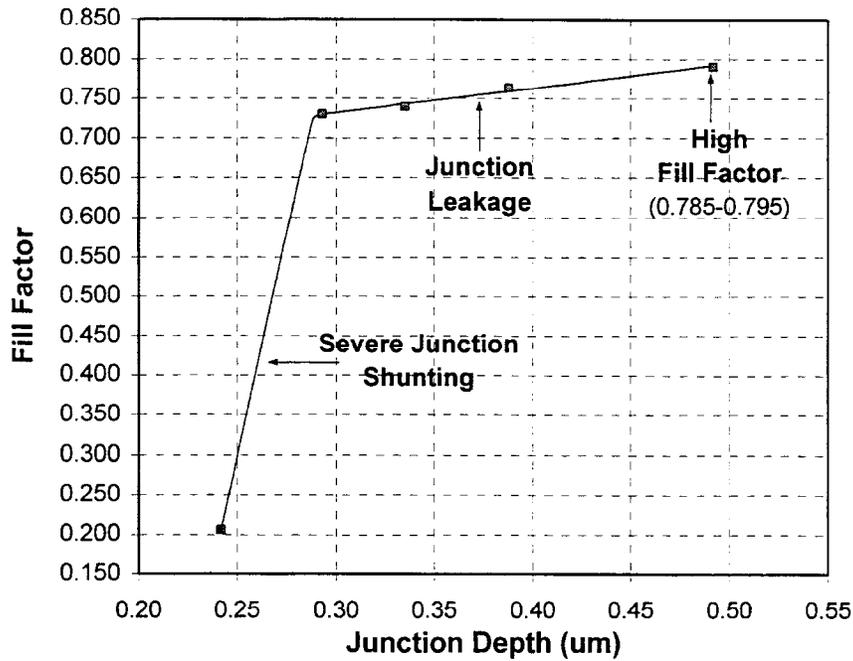


Fig. 1.9. Relationship between screen-printed fill factor and junction depth.

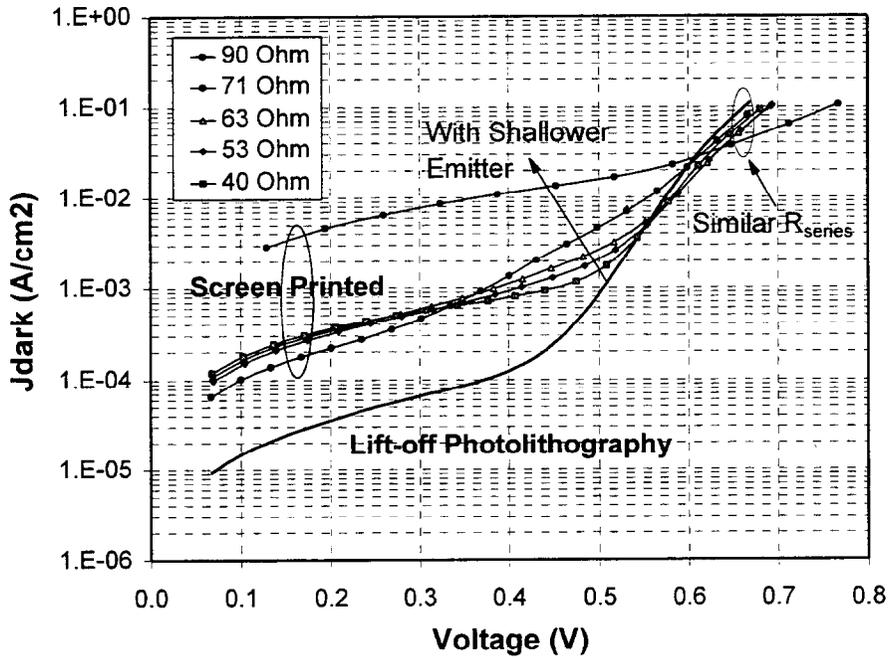


Fig. 1.10 Relationship between screen-printed fill factor and junction depth.

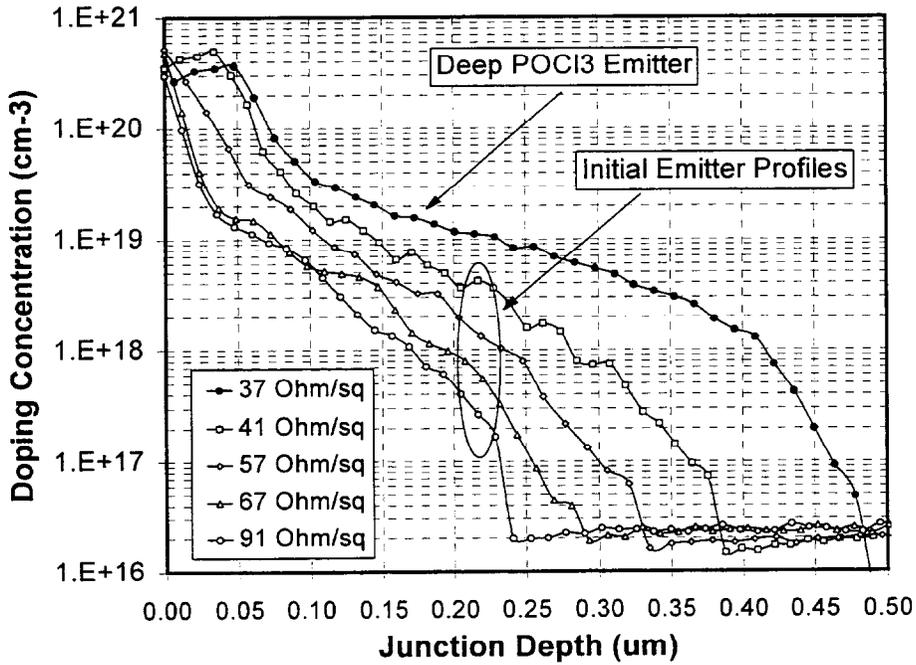


Fig. 1.11 Deeper $POCl_3$ emitter as compared to original solid source diffusion

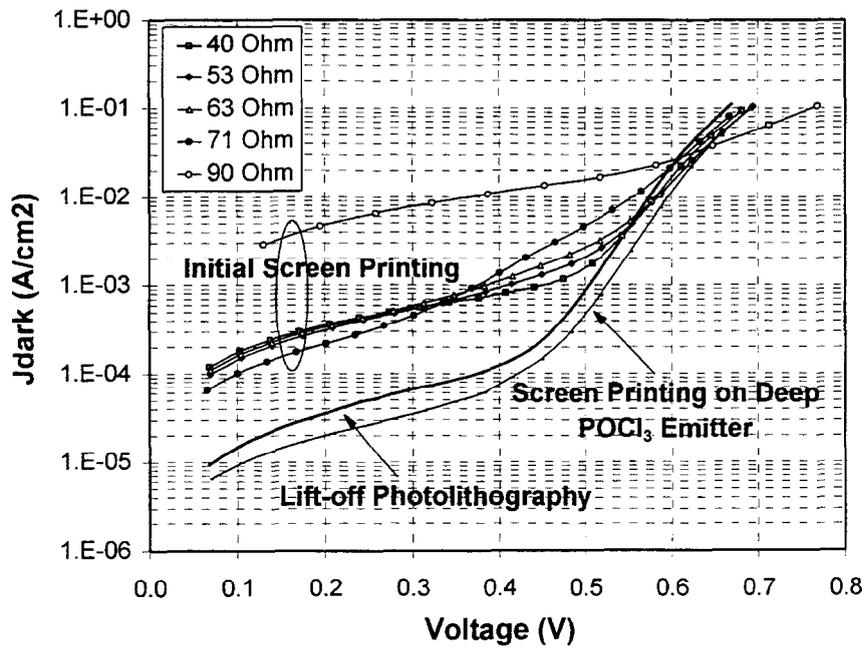


Fig. 1.12. Dark IV response when printing is done on deeper emitter.

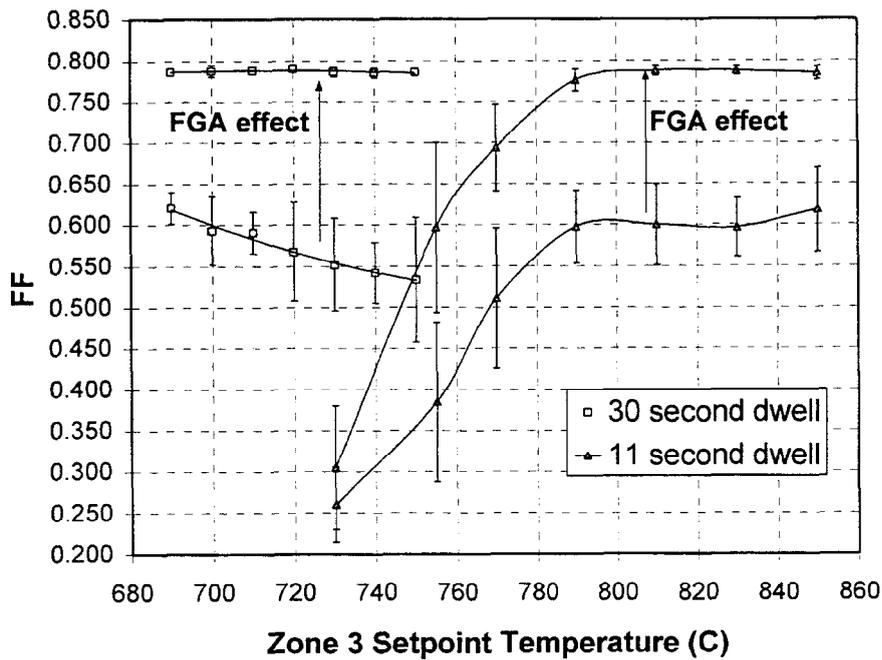


Fig. 1.13. Fill factor response as a function of hot-zone temperature and dwell time.

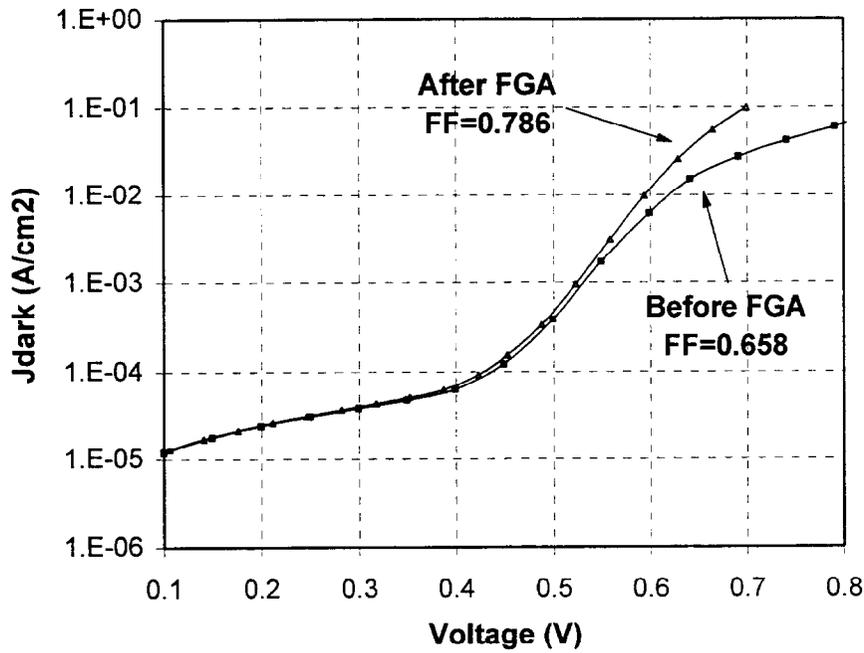


Fig. 1.14. The effect of a 400°C FGA on the series resistance of fired SP contacts.

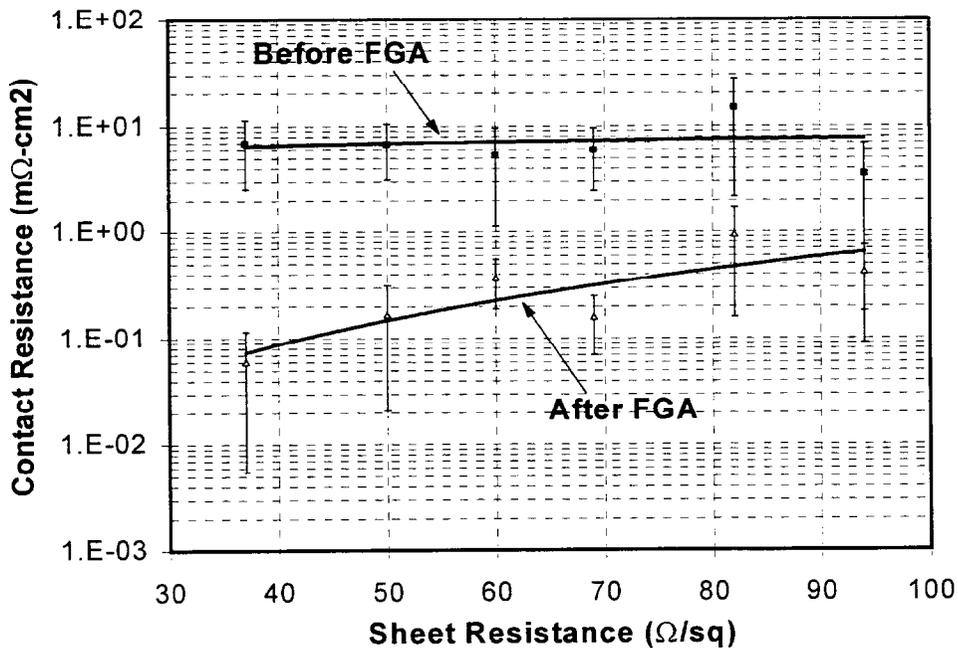


Fig. 1.15. The effect of the FGA on the ρ_c of SP contacts to n^+ emitter regions.

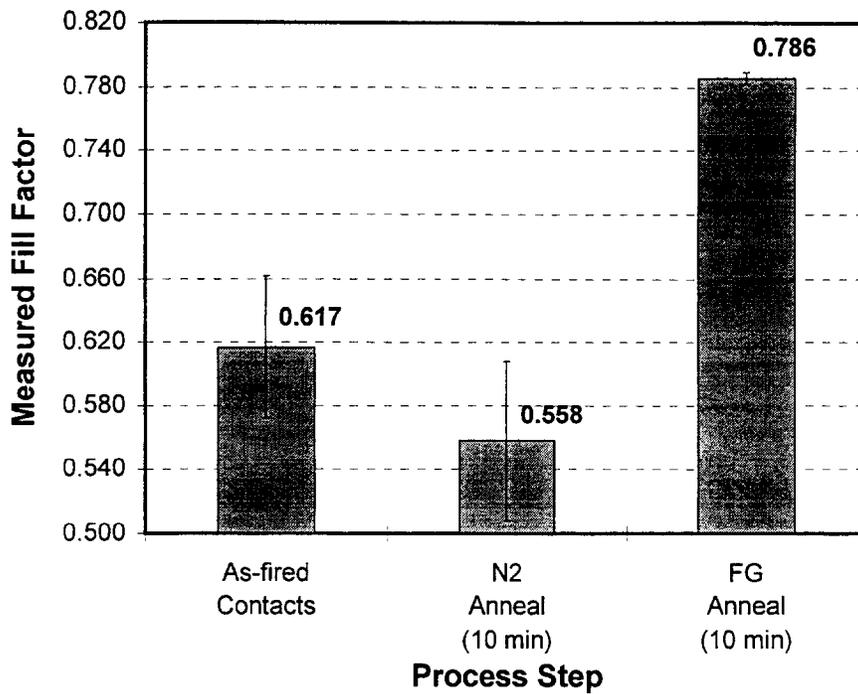


Fig. 1.16. Effect of post-firing contact anneal in non-reducing (N₂) and reducing (FG) ambient. The anneal temperature was 400°C.

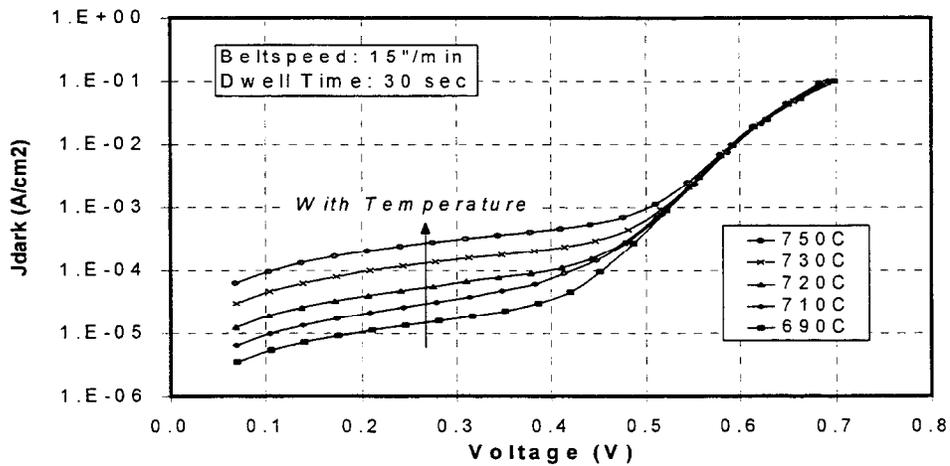


Fig. 1.17. Effect of hot-zone firing temperature on the ensuing dark I-V response of solar cells.

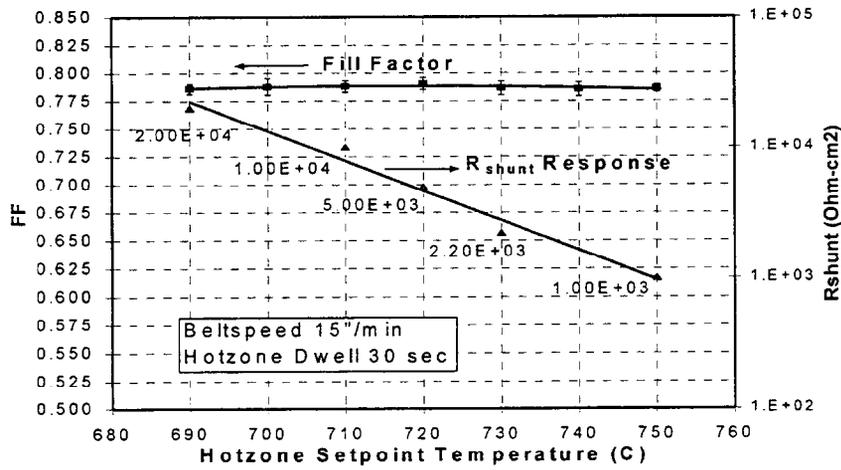


Fig. 1.18. Effect of hot-zone firing temperature on R_{sh} value.

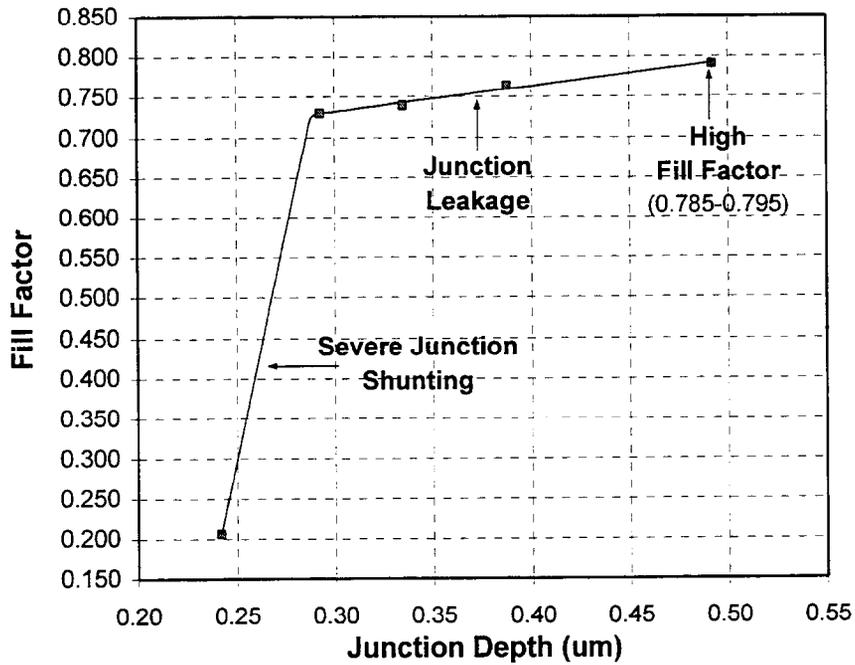


Fig. 1.19. Effect of junction depth on fill factor of a screen-printed solar cell.

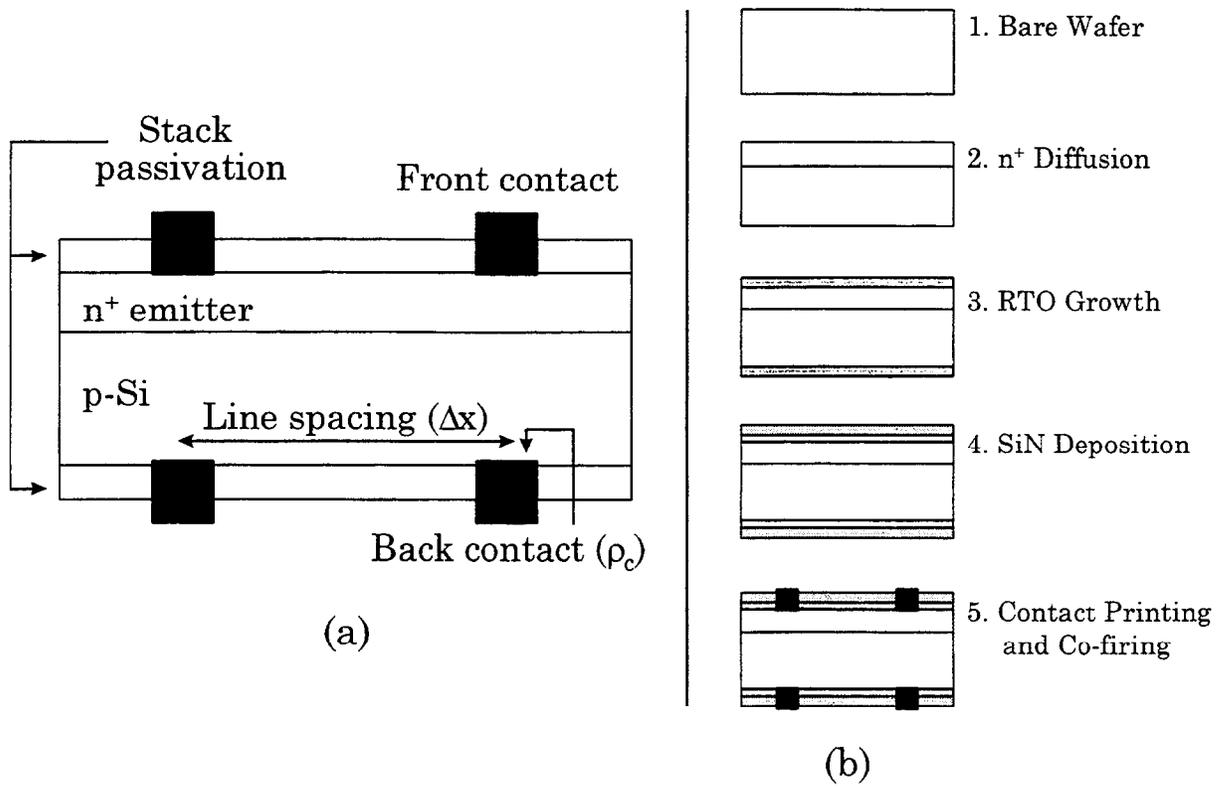


Fig.1.20. a) GBC solar cell structure. b) Simplified GBC process sequence.

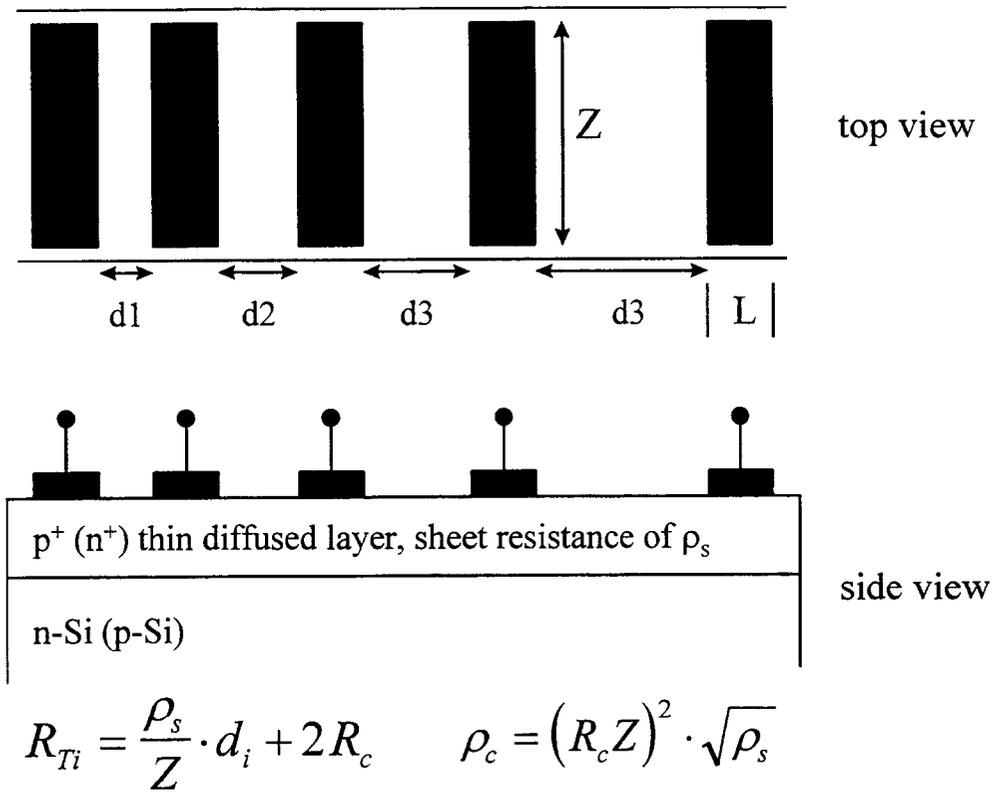


Fig. 1.21. The TLM measurement structure.

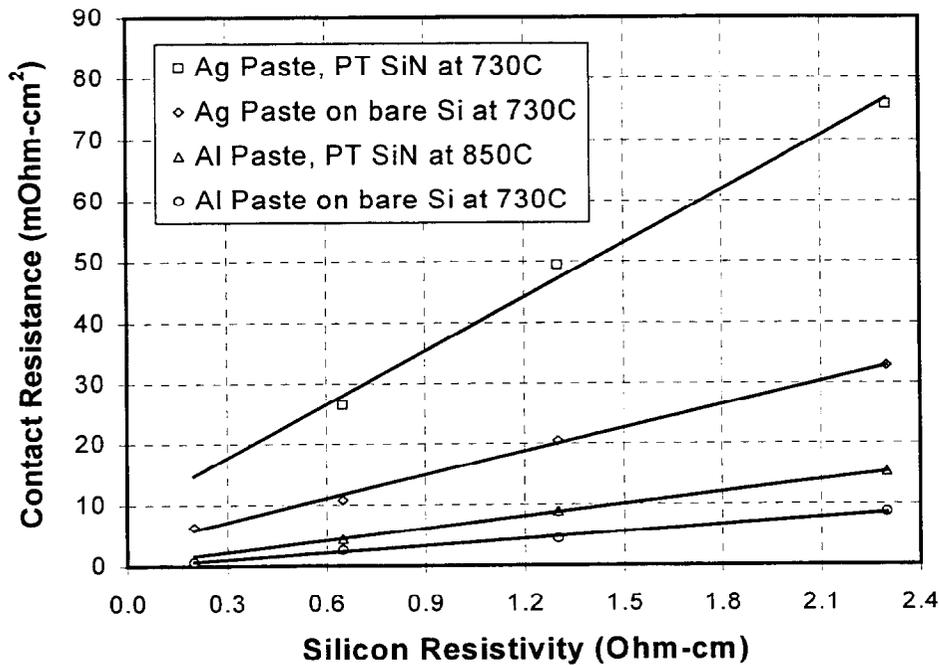


Fig. 1.22. Contact resistance for Ag and Al pastes on p-type Si. The hotzone firing temperature was set to 730°C. PT signifies a *punch-through* process.

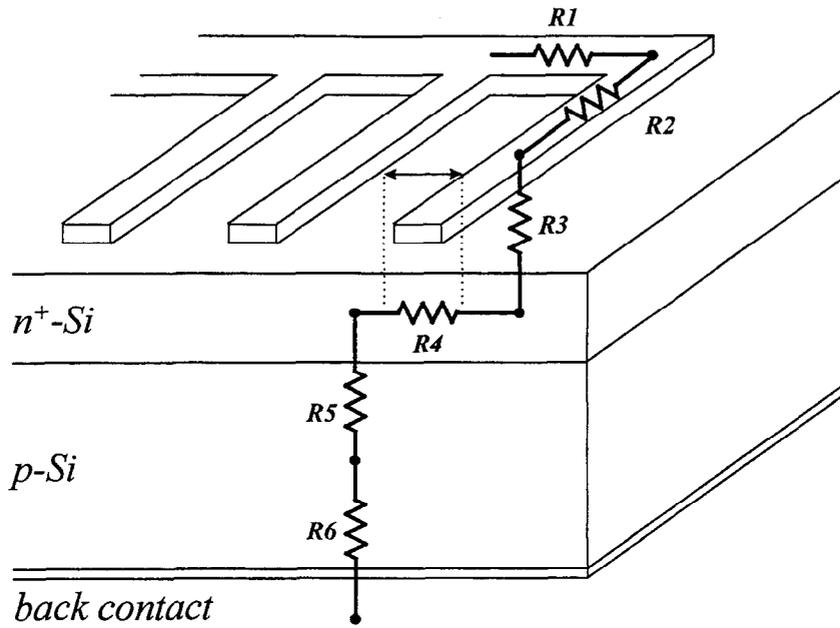


Fig.1.23. Solar cell resistances. R_1 , R_2 , R_3 , and R_4 exist for each gridline segment but are not shown in the figure.

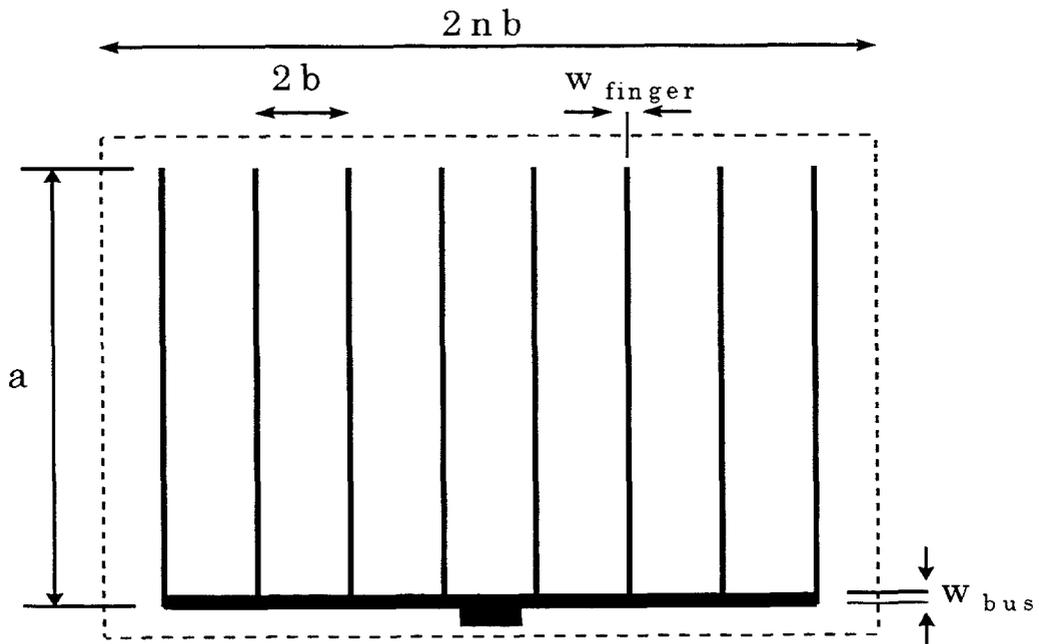


Fig. 1.24. Simple front contact pattern.

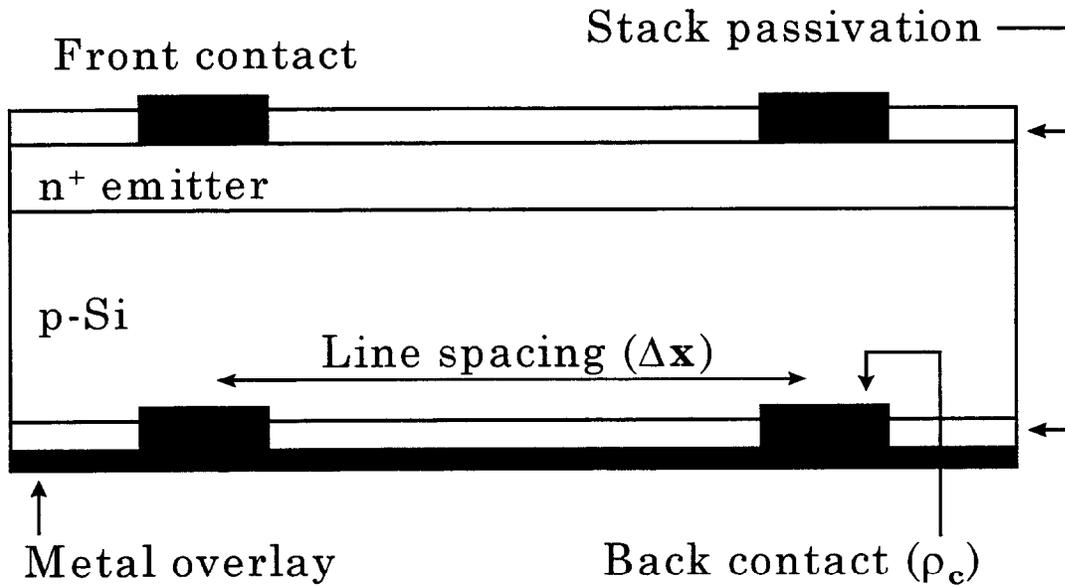


Fig. 1.25. Device structure used to study the effects of ρ_c and Δx on FF. The effects of P_{finger} and P_{bus} for the rear electrode were removed by the metal overlay.

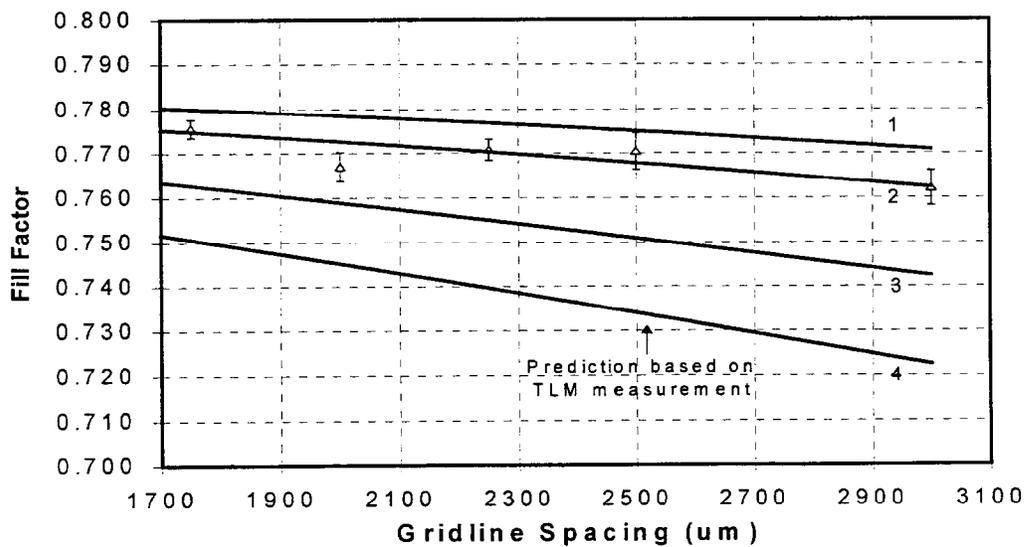


Fig. 1.26. Fill factor versus GBC rear line spacing for 1.3 $\Omega\text{-cm}$ substrate material. The solid lines are simulated values for rear ρ_c values of: 1) 1 $\text{m}\Omega\text{-cm}^2$, 2) 10 $\text{m}\Omega\text{-cm}^2$, 3) 30 $\text{m}\Omega\text{-cm}^2$, and 4) 50 $\text{m}\Omega\text{-cm}^2$. The triangles represent experimental data.

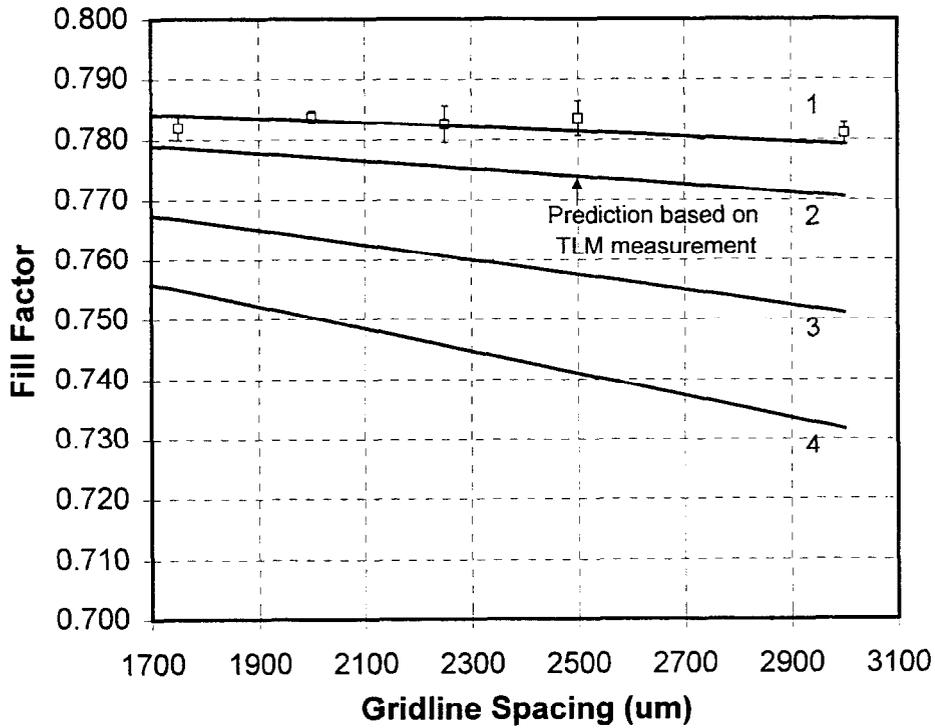


Fig. 1.27. Fill factor versus GBC rear line spacing for 0.65 Ω -cm substrate material. The solid lines are simulated values for rear ρ_c values of: 1) 1 $m\Omega$ - cm^2 , 2) 10 $m\Omega$ - cm^2 , 3) 30 $m\Omega$ - cm^2 , and 4) 50 $m\Omega$ - cm^2 . The squares represent experimental data.

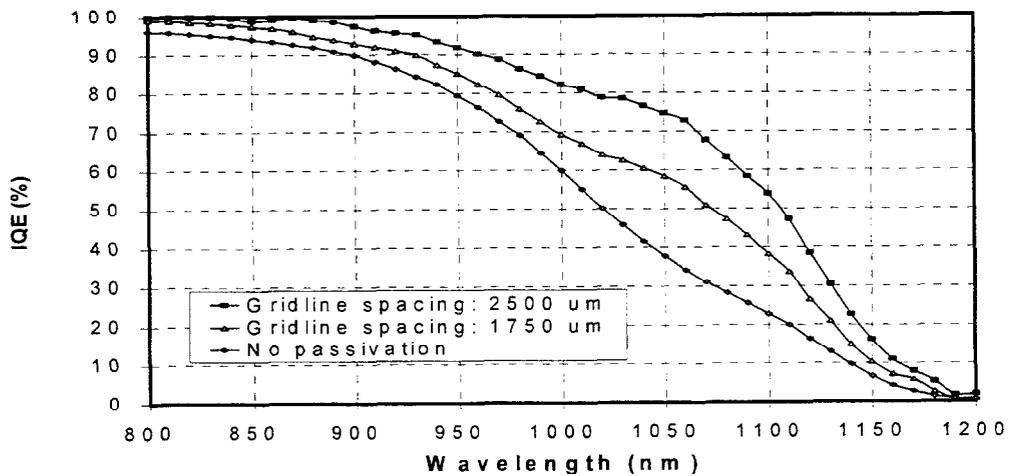


Fig.1.28. Effect of rear gridline spacing on the long-wavelength IQE.

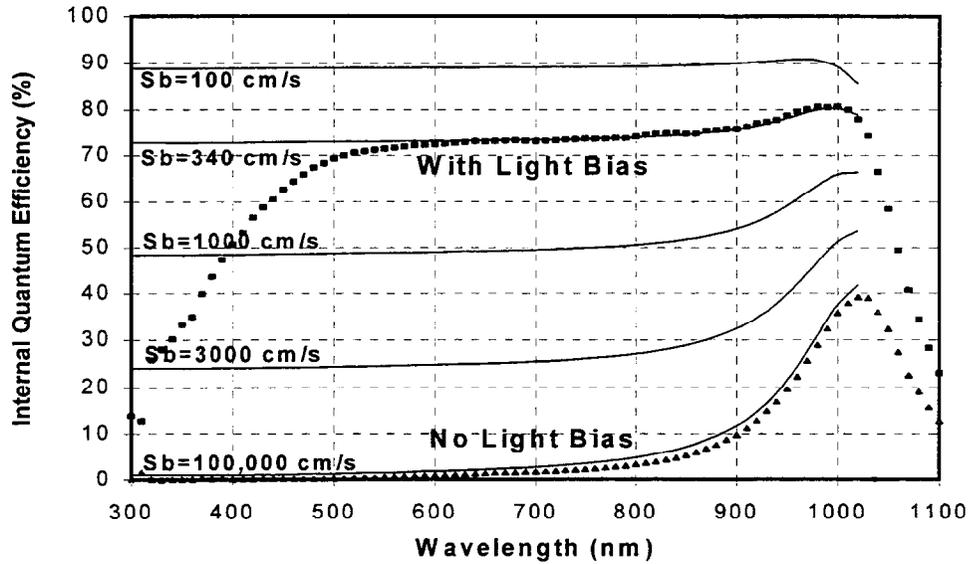


Fig. 1.29. Rear illuminated IQE of the bifacial solar cell. The solid lines represent simulation results. The dip in the measured IQE in the 300-500 nm range is caused by absorption in the SiN layer with index ≈ 2.25 .

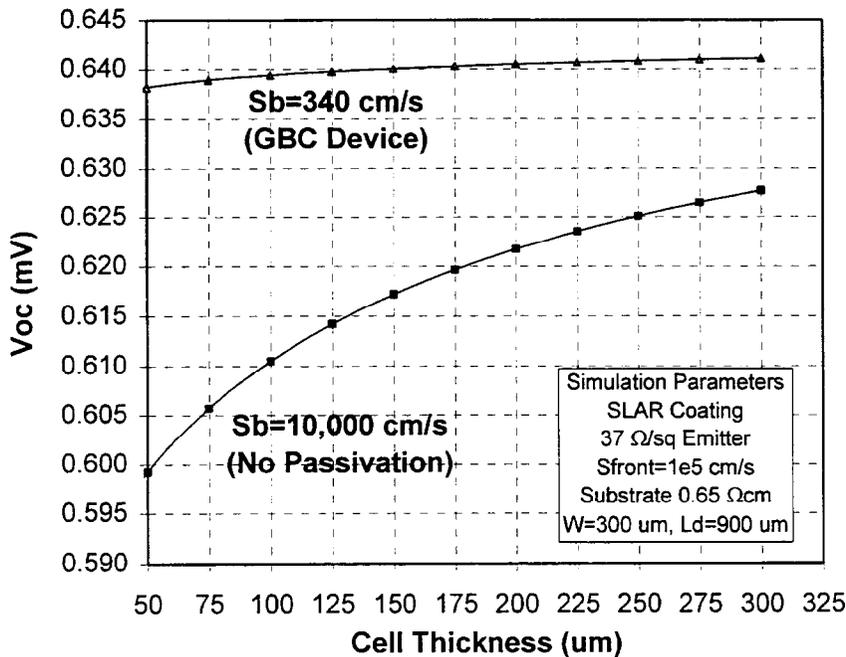


Fig. 1.30. Effect of reduced substrate thickness for S_b of 10^4 cm/s. L_d signifies the minority carrier diffusion length in the bulk Si.

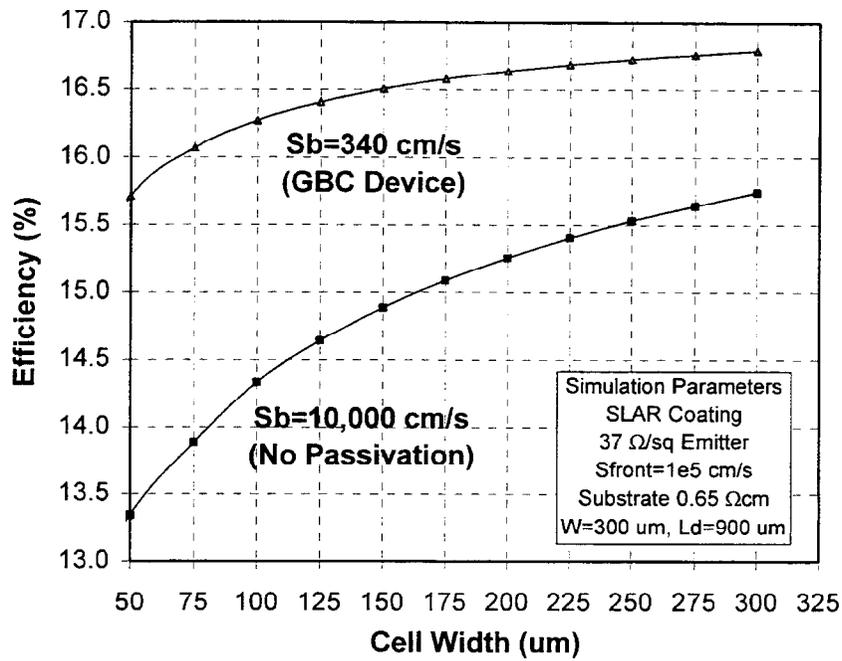


Fig. 1.31. Solar cell efficiency versus thickness for GBC and non-passivated cells. For the passivated rear device, the slight drop in efficiency for thin cells is caused by reduced light trapping quality and lower J_{sc} .

CHAPTER II

COMPREHENSIVE STUDY OF RAPID, LOW-COST SILICON SURFACE PASSIVATION TECHNOLOGIES

2. Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies

A comprehensive and systematic investigation of low-cost surface passivation technologies is presented for achieving high-performance silicon devices, in this case for photovoltaic devices. Most commercial solar cells today lack adequate surface passivation. In contrast, laboratory cells use conventional furnace oxides (CFO) for high-quality front and/or back surface passivation but at the expense of a lengthy, high-temperature step. This investigation tries to bridge the gap between commercial and laboratory cells by providing fast, low-cost methods for effective surface passivation. As an alternative to CFO, rapid thermal oxides (RTO) can give comparable passivation in a much shorter time. Additionally, plasma deposition of silicon nitride (SiN) has recently emerged as a low-temperature passivation technique, which simultaneously provides a good antireflection coating for silicon solar cells. In this chapter, we demonstrate, for the first time, the efficacy of TiO_2 , thin (<10 nm) RTO, and PECVD SiN passivation individually and in combination for (diffused) emitter and (non-diffused) back surface passivation. The effects of emitter sheet resistance, surface texture, and three different SiN depositions (two using a direct PECVD system and one using a remote system) were investigated. The impact of post-growth/deposition treatments such as forming gas anneal (FGA) and firing of screen-printed contacts was also examined. This study reveals that the optimum passivation scheme consisting of a thin RTO, SiN, and 730°C screen-printed contact firing anneal can (a) reduce the emitter saturation current density, J_{0e} , by a factor of >15 for a $90 \Omega/\text{sq}$. emitter, (b) reduce J_{0e} by a factor of > 3 for a $40 \Omega/\text{sq}$. emitter, and (c) reduce S_{back} below 20 cm/s on $1.3 \Omega\text{cm}$ p-Si. Furthermore, this double-layer RTO+SiN passivation is independent of the deposition conditions (direct or remote) of the SiN film and is more stable under heat treatment than SiN or RTO alone. Model calculations are also performed to show that

the RTO+SiN surface passivation scheme may lead to 17%-efficient thin screen-printed cells even with a low bulk lifetime of 20 μ s.

2.1 Introduction

Minimizing recombination of minority-carriers at the surfaces of silicon is crucial for the performance of many Si devices including solar cells, BJTs, CCDs, and power devices. The objective of this paper is to provide a comprehensive and systematic study of different surface passivation technologies available for diffused and non-diffused silicon, planar (flat) and chemically textured surfaces. The information is immediately applicable for junction devices such as solar cells, which typically have a n^+p structure. For such devices, surface passivation is the key to higher performance especially because the trend is towards thinner substrates, which bring the surface closer to the collecting junction.

The passivation schemes investigated include evaporated films of TiO_2 , thin SiO_2 films grown in a conventional furnace (CFO) and in a rapid thermal processor (RTO), plasma-deposited (PECVD) SiN, and selected combinations of RTO, TiO_2 , and SiN. RTO films are of particular interest because thin 8-10 nm films can be grown in an extremely short time. Films like TiO_2 and SiN are investigated because they provide silicon antireflection properties, which are essential for photovoltaic devices. Since SiN depends strongly upon deposition conditions and the type of PECVD equipment used, SiN films from three different sources were compared.

In this study, rapid, low-cost technologies like RTO and PECVD SiN are focused upon. These low-cost methods can provide effective surface passivation in a short time and with a much lower thermal budget than a CFO. Individually, their effectiveness for solar cell passivation has been demonstrated previously [1,2,3]. However, their combined effect and their ability to withstand subsequent thermal treatments necessary for complete solar cell fabrication has never

been studied. Therefore, the impact of solar cell fabrication steps such as forming gas anneal (FGA) and screen-printed contact firing on the surface passivation quality of individual and double-layer stacks of dielectrics has also been quantified.

2.2 Experimental

To assess the surface passivation of p-type silicon, effective minority carrier lifetime (τ_{eff}) measurements were performed on 1.3 Ωcm p-type $\langle 100 \rangle$ FZ silicon wafers coated with various passivating films. The investigation of n^+ -emitter passivation was performed by J_{oc} measurements by the photoconductance decay (PCD) technique on diffused, high-resistivity (750 Ωcm), high bulk lifetime (> 1 ms) FZ Si wafers. Some of the wafers were subjected to a chemical random surface texturing before processing. Surface texturing is commonly used for solar cells to help optically confine and antireflect more light. Samples for the emitter passivation experiment were diffused on both sides in an RTP system using spin-on dopant sources. We investigated emitters with sheet resistances of 40 and 90 $\Omega/\text{sq.}$, which correspond to emitters that can accommodate screen-printed and evaporated contacts, respectively. After removal of the residual phosphosilicate glass, part of the diffused and non-diffused p-type samples were oxidized in the same RTP system used for the diffusions. This rapid thermal oxidation at 900°C for 150 s resulted in an oxide thickness of approximately 6 nm. The oxidized low-resistivity samples were then annealed in forming gas at 400°C for 15 min. After this, depositions of passivating films were performed in three different laboratories. The thickness of these films was approximately that of a single-layer antireflection (AR) coating (~ 60 nm). The refractive indices of these films measured at 632.8nm were between 2.15 and 2.27, which is in the optimum range for single-layer AR coatings under glass, or the first film of double-layer AR coatings in air [4].

The deposition of TiO₂ was performed by evaporating titanium in an oxygen atmosphere under a low pressure of 15 mPa. For the deposition of SiN, three different PECVD systems were used. Two of these systems have a parallel plate reactor and high frequency excitation, with deposition temperatures of 300°C and 350°C, respectively. The third system is a remote PECVD system with microwave excitation and a deposition temperature of 400°C [5]. Table 2.1 summarizes the differences in key parameters of these systems. The plasma deposition systems vary in a number of other aspects, such as the reactor geometry, and the plasma power and pressure. However, all three SiN films are used as a standard in the respective laboratories.

After film deposition, the effective minority carrier lifetime (τ_{eff}) was measured on all samples. Subsequently, a forming gas anneal (FGA) at 400°C was performed on all samples. As a final step, the samples were subjected to a short temperature cycle with a maximum temperature of 730°C, which is typically used as a firing cycle for screen-printed contacts. This step was performed in a beltline furnace with tungsten-halogen lamp heating.

The minority carrier lifetime was measured after each step using a commercially available inductively-coupled PCD tester. From these data, the emitter saturation current J_{0e} (for diffused samples) and the surface recombination velocity S_{eff} were calculated. The PCD measurement of J_{0e} is discussed in Kane and Swanson [6] and S_{eff} was calculated using the following two equations [7]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \beta^2 \cdot D_n \quad (1)$$

$$\tan\left(\frac{\beta \cdot W}{2}\right) = \frac{S_{eff}}{\beta \cdot D_n} \quad (2)$$

In this study, an infinite bulk lifetime ($\tau_b \rightarrow \infty$) was assumed so the calculated S_{eff} actually represents the worst-case (maximum) value.

2.3 Results and Discussion

The passivation of solar cell front surfaces was investigated on both 40 $\Omega/\text{sq.}$ and 90 $\Omega/\text{sq.}$ emitters. On relatively opaque 40 $\Omega/\text{sq.}$ emitters (which is generally needed to accommodate screen-printed contacts), the surface is largely decoupled from the bulk, because of the high surface doping concentration and depth of the doping profile. Thus, the introduction of RTO or SiN passivation resulted in a moderate decrease in J_{0e} of about a factor of two to three, as can be seen from Fig. 2.1. While TiO_2 showed hardly any passivation, SiN 1 was clearly inferior to RTO or SiN 3, which, in combination, resulted in the best passivation. Note that the high-temperature treatment during RTO growth changed the doping profile and lead to a lower surface doping concentration, which allowed for better surface passivation. The J_{0e} values for textured samples were about 1.5 to 2 times higher than those for planar surfaces, which resembles the 1.73 times increase in surface area resulting from regular pyramidal texturing.

On the relatively transparent 90 $\Omega/\text{sq.}$ emitters, (which are generally used for evaporated contacts) the difference in the degree of passivation for various schemes was more apparent, as shown in Fig. 2.2. Again, TiO_2 does not provide any appreciable reduction in J_{0e} . For the planar surface, RTO growth reduced J_{0e} by more than a factor of ten to below 100 fA/cm^2 , as does the deposition of SiN 3. However, on the textured surface, RTO is not as effective, resulting in a moderate J_{0e} value of 400 fA/cm^2 . Here, SiN 3 and the RTO+SiN double layers were clearly superior.

As-deposited double layers of RTO and SiN were better than the nitrides alone in all cases, resulting in low J_{0e} values of 50 fA/cm² for planar and 100 fA/cm² for textured emitter surfaces (see Fig. 2.2). A subsequent forming gas anneal did not change the surface passivation appreciably. The same applies for the contact firing cycle on the 40 Ω /sq. emitters. This indicates that double layer passivation with a SiN cap preserves the passivation quality of heavily-doped silicon during contact firing. For comparison, thin conventional furnace oxides (CFOs) and double layers of CFO and SiN were grown on the same emitters. This passivation resulted in identical or only slightly lower J_{0e} values than the RTO-based schemes.

On the undiffused surface of 1.3 Ω cm silicon, the deposition of TiO₂ again did not give any measurable surface passivation, nor did the growth of RTO or the deposition of SiN 1 (see Fig. 2.3). (Please note that S_{eff} values above 10⁴ cm/s could not be measured reliably by the method used in this study.) However, both SiN 1 and RTO passivation improved considerably after FGA. While as-deposited SiN 3 already gave very good passivation, it tended to degrade slightly with the FGA. Double layers of RTO with all nitrides resulted in excellent S_{eff} values after FGA, possibly because of the release of hydrogen from the SiN which then reaches the interface, reducing the interface state density.

Fig. 2.4 shows that the same trend was observed for textured surfaces, with SiN 3 giving considerably better passivation than the other nitrides. After FGA, all RTO+SiN double layers showed good passivation, resulting in a very low S_{eff} value of 39 cm/s for RTO+SiN 3.

As a last step, the samples with SiN and RTO+SiN double layers were subjected to a screen-print contact firing cycle with a maximum temperature of 730°C. Fig. 2.5 indicates that the SiN passivation resulted in moderate to low S_{eff} values after this treatment, with SiN 1 and SiN 3 showing some degradation. This may be because of hydrogen escaping from the SiN films. In contrast, the RTO+SiN double layers provided exceptionally low S_{eff} values regardless of the type

of nitride used. After this treatment, the double layer with SiN 1 resulted in the lowest S_{eff} value of 12 cm/s on a planar surface. Note that this value gives the same value as the record low S_{eff} value of 4 cm/s resulting from SiN 3 passivation [5] which was calculated using a bulk lifetime of 1.7 ms. Since we used an infinite bulk lifetime in all of our calculations, we have reported the higher value of 12 cm/s corresponding to the *maximum* S_{eff} . Furthermore, Fig. 2.5 clearly shows the superior thermal stability of RTO+SiN in contrast to any of the SiN films alone, which degrade upon screen-printed contact firing.

2.4 Impact of Surface Passivation on Photovoltaic Device Performance

Model calculations were performed to predict the impact of the various promising surface passivation schemes on the performance of photovoltaic devices. For this, a one-dimensional modeling program, PC-1D version 5.1 was used to calculate the energy conversion efficiency. The results of these calculations can be seen in Fig. 2.6 which shows the calculated cell efficiencies as a function of front and/or back surface passivation and a two different values of cell thickness ($W = 100$ or $300 \mu\text{m}$) and bulk lifetime ($\tau_b = 20 \mu\text{s}$ or $200 \mu\text{s}$). The calculations were performed with a $40 \Omega/\text{sq}$. emitter, 6% grid shading factor, and fill factor of 0.77-0.78 to be consistent with typical commercial screen-printed solar cells. Highly-efficient commercial screen-printed cells are about 14-15% efficient today and do not usually have front or back surface passivation. Fig. 2.6 shows that up to about 0.5% (absolute) gain in efficiency can be derived from improving just the front surface passivation. A comparatively large improvement can be gained by employing high quality back surface passivation as well. The calculations show that 17-18%-efficient screen-printed cells are possible with RTO+SiN front and back surface passivation even on materials with a bulk

lifetime of only 20 μs . It is very important to note that the calculations assumed negligible contact recombination, which may not be valid especially for back contacts unless a highly effective local back surface field is employed. However, we, along with others, have demonstrated low S_{pp+} values of 200-300 cm/s using an optimized Al BSF [3,8,9]. Thus, the cells in Fig. 2.6 may be realized with the combination of high-quality RTO+SiN passivation and a gridded BSF. Fig. 2.6 also shows that thinner cells (with a bulk lifetime of only 20 μs), which consume less silicon and therefore reduce cost, actually improve in performance because of high-quality back surface passivation. These calculations are encouraging especially since cost limitations are forcing the trend to reduced cell thickness with lower qualities of silicon.

2.5 Conclusions

This study provides a thorough investigation of silicon surface passivation by RTO, TiO_2 , different PECVD silicon nitrides, and double-layer combinations of these films. The deposition or growth of these films can be performed in a matter of minutes, and all of the passivation schemes used provide or allow for near-optimum antireflection properties. Thus, they can enhance the performance of current industrial solar cells significantly. We have found that both a RTO film and three different silicon nitride films can individually reduce surface recombination substantially. Three PECVD SiN deposition systems, differing in various aspects, were used, and the resulting passivation was evaluated. This study demonstrated that the double-layer of RTO+SiN can improve the surface passivation even further, resulting in exceptionally low J_{0e} values below 50 fA/cm^2 on 90 Ω/sq . emitters, 200 fA/cm^2 on 90 Ω/sq . emitters, and maximum S_{eff} values below 20 cm/s on a planar 1.3 Ωcm Si surface. The combination of RTO and SiN also reduces the gap in passivation quality between the different nitrides allowing for a high degree of freedom in the SiN deposition

conditions. Furthermore, this combination has been shown to enhance the stability of the surface passivation under thermal treatments such as screen-printed contact firing. Textured surfaces revealed a similar trend as planar surfaces but showed a greater amount of surface recombination. Therefore, effective RTO+SiN passivation is even more essential for textured surfaces since surface recombination can frequently limit performance. Finally, model calculations show that the combination of RTO+SiN double-layer passivation and standard screen-printed contact firing anneal can result in significant improvement of current industrial cells. Calculations show that this passivation on the front and back may lead to 17%-efficient screen-printed cells on thinner substrates (100 μm) with low bulk lifetimes (20 μs), resulting in considerable cost reduction of photovoltaic cells.

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Table 2.1: Plasma depositions used in this investigation.

System No.	Excitation mode	Deposition Temp. [°C]	Gases
SiN 1	direct, HF (13.6 MHz)	300	SiH ₄ , N ₂ , NH ₃
SiN 2	direct, HF (13.6 MHz)	350	SiH ₄ (5%) in He, N ₂ , NH ₃
SiN 3	remote, 2.45 GHz	400	SiH ₄ , NH ₃

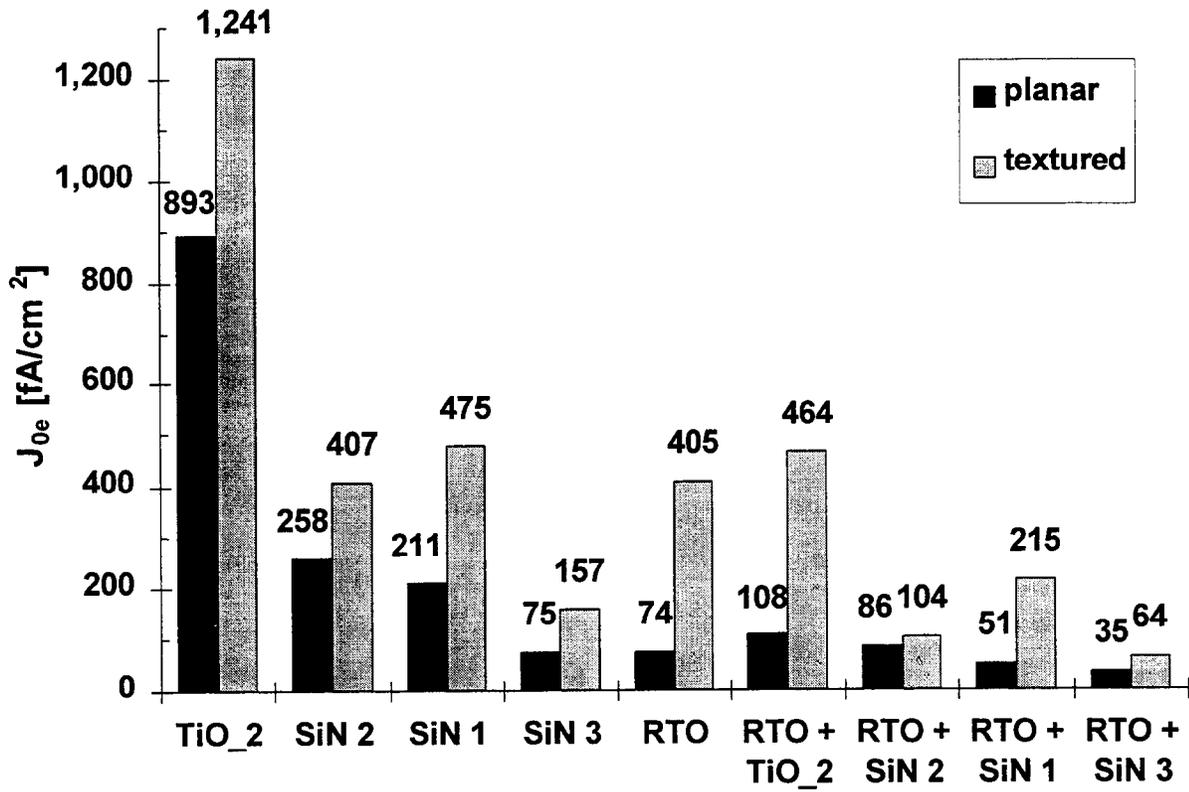


Fig. 2.1. Emitter saturation current densities for different passivation schemes on 40 Ω /sq. RTP emitters.

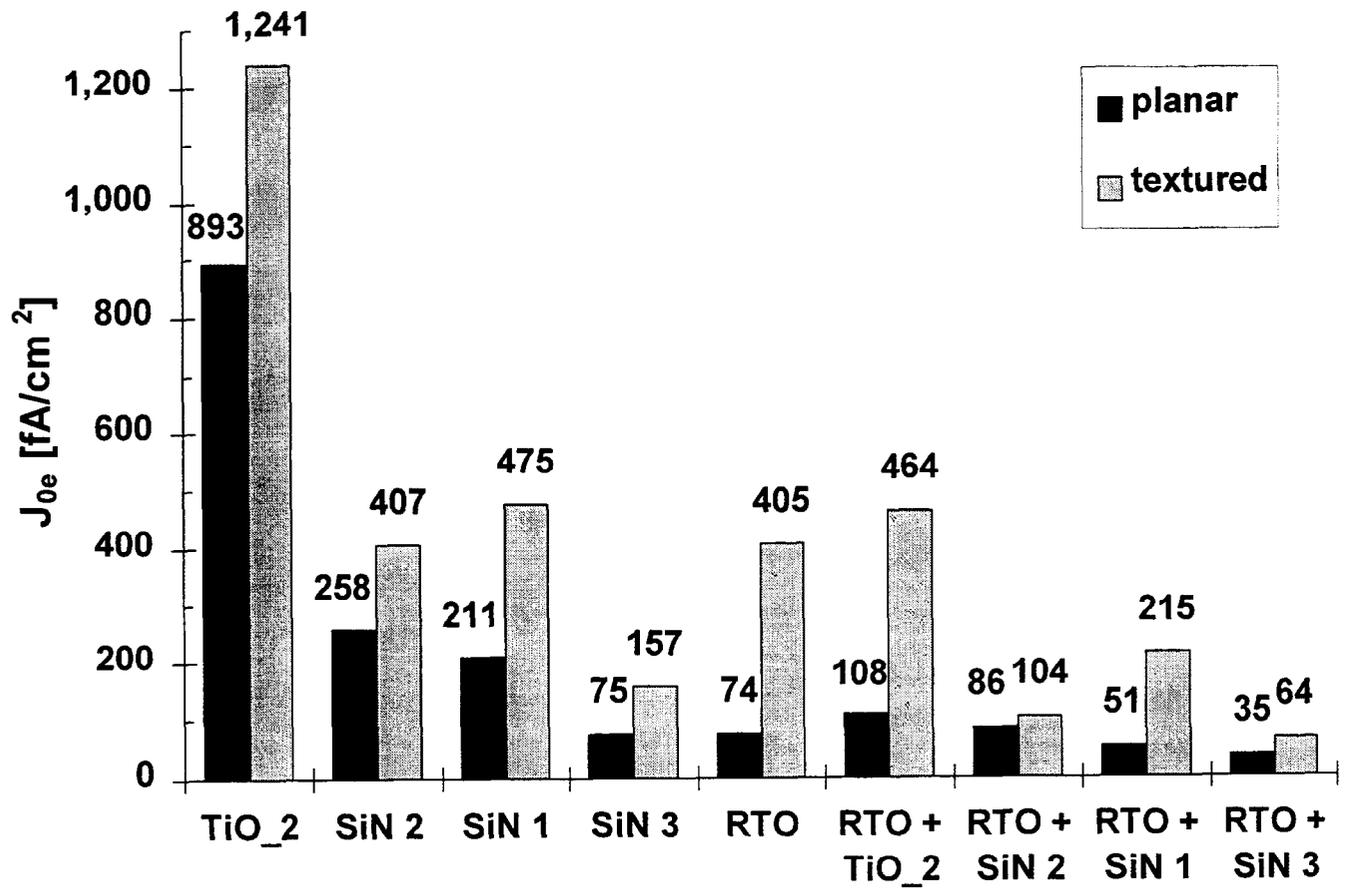


Fig. 2.2. Emitter saturation current densities for 90 Ω /sq. RTP emitters.

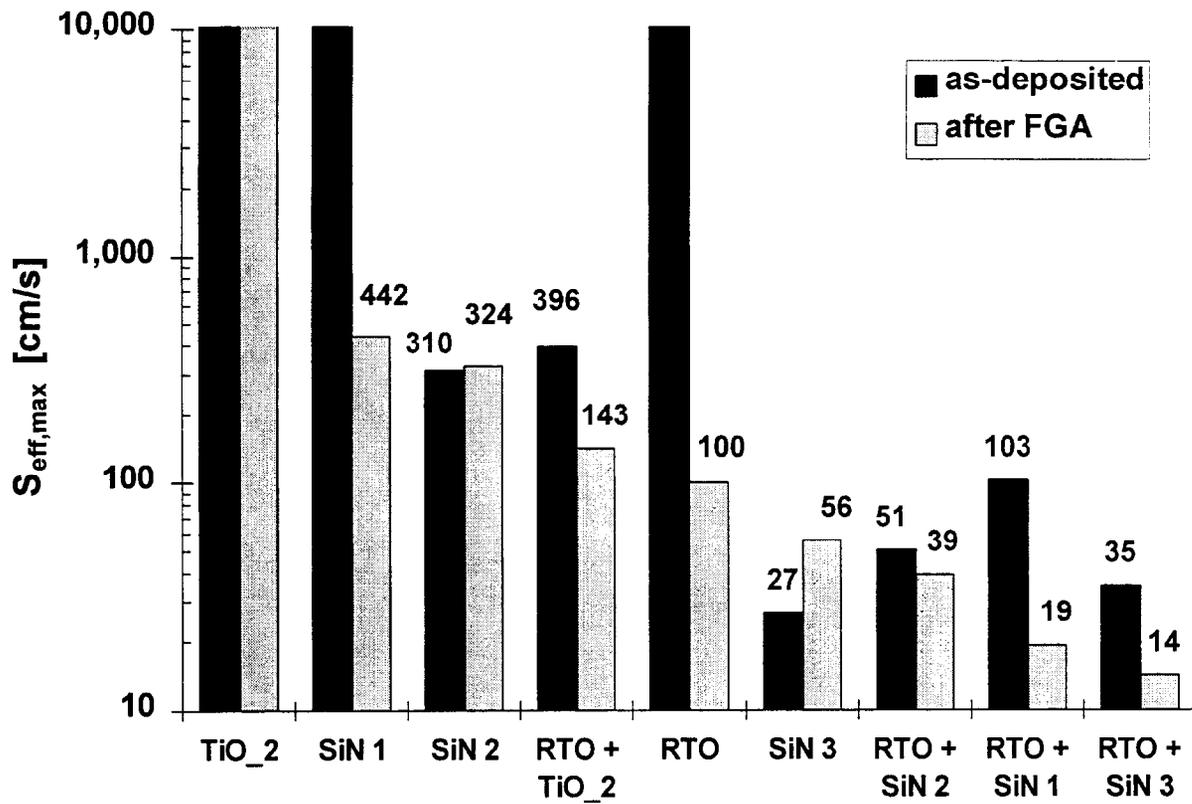


Fig. 2.3. Maximum surface recombination velocities for different passivation schemes on planar surfaces. S values above 10^4 cm/s cannot be resolved by the measurement technique used and are not shown.

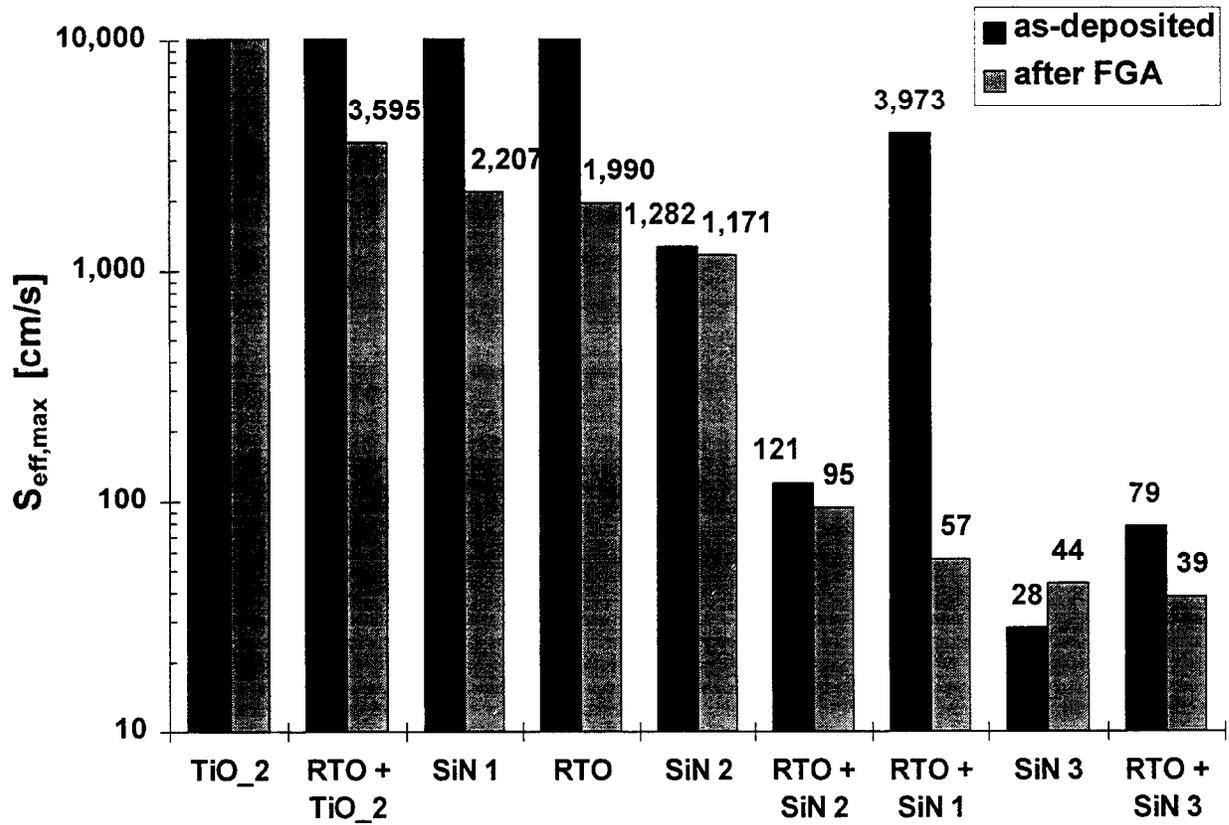


Fig. 2.4. Maximum surface recombination velocities for textured surfaces.

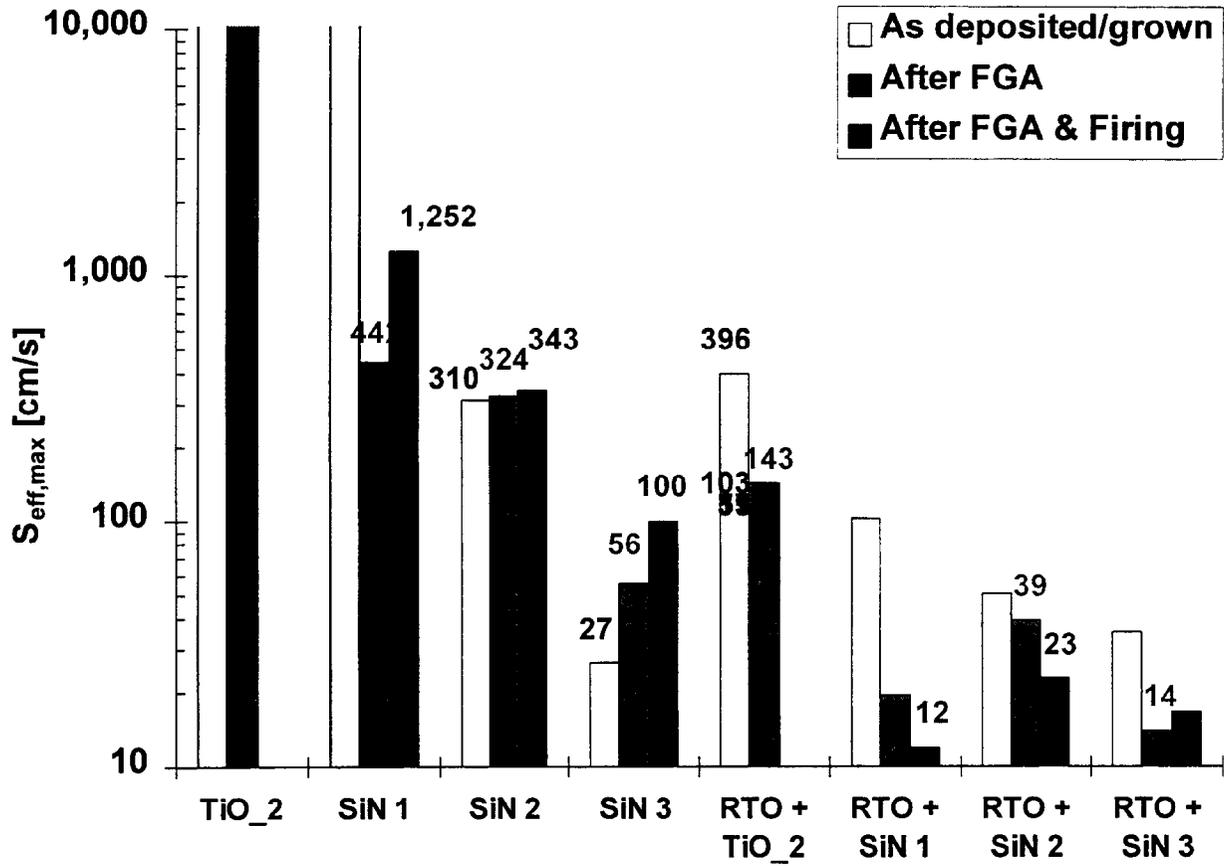


Fig. 2.5. Effect of heat treatment on the planar surface passivation. The combination of RTO+SiN is shown to withstand the 730°C screen-printed contact firing used to form contacts compatible with industrial cells.

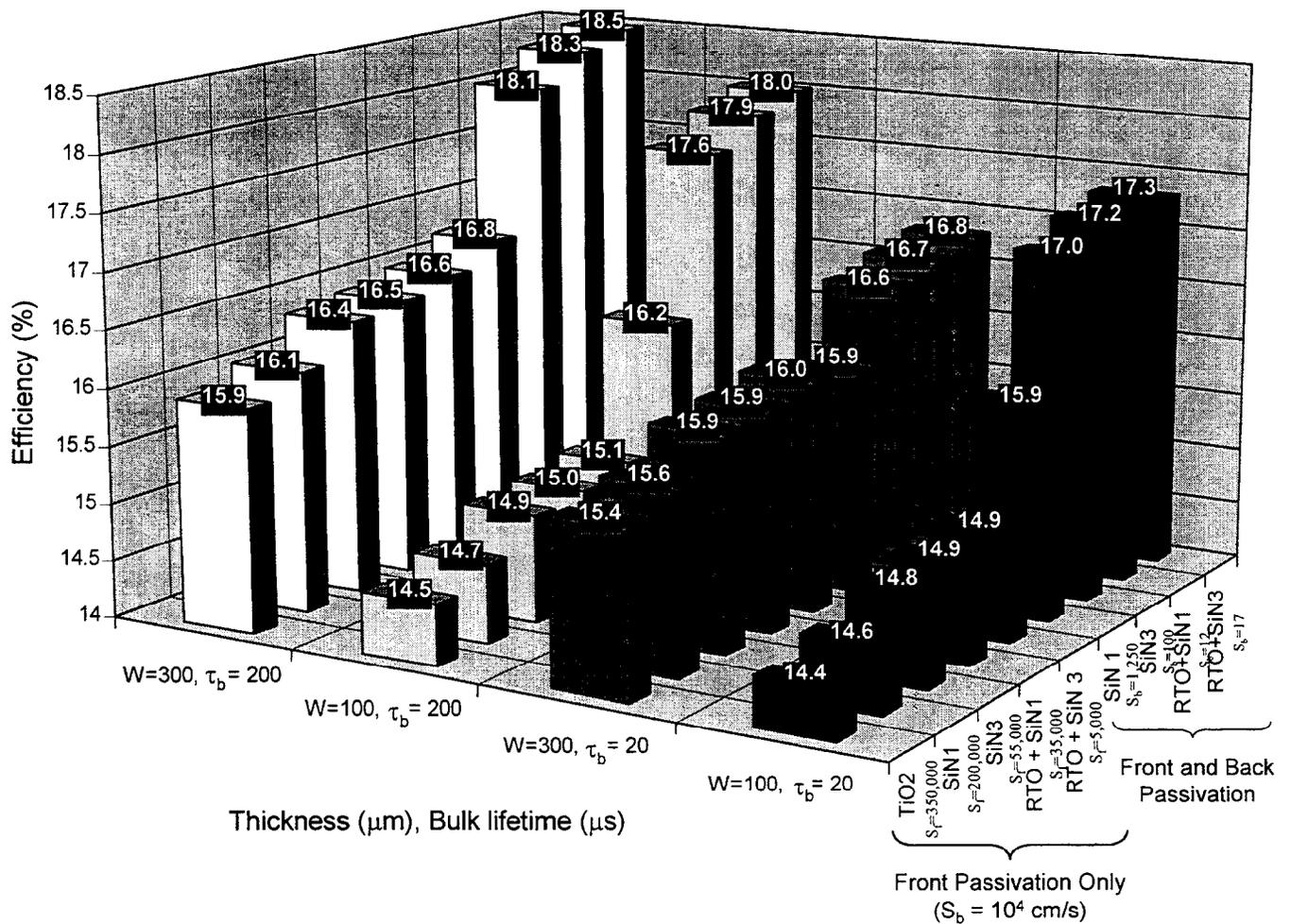


Fig. 2.6. Impact of front and/or back surface passivation on photovoltaic device performance. All calculations were performed with a $40 \Omega/\text{sq.}$ emitter, 6% grid shading factor, and fill factor of 0.77-0.78 to be consistent with screen-printed solar cells.

CHAPTER III

EFFECTIVE PASSIVATION OF THE LOW RESISTIVITY SILICON SURFACE BY A RAPID THERMAL OXIDE/PLASMA SILICON NITRIDE STACK

3. Effective Passivation of the Low Resistivity Silicon Surface by a Rapid Thermal Oxide/Plasma Silicon Nitride Stack

3.1 Introduction

Low surface recombination velocity (S) is an important requirement for the performance of many semiconductor devices. For silicon solar cells, the recombination velocity at the front and rear surfaces (S_f and S_b , respectively) must be reduced in order to achieve high-efficiency. Moreover, the techniques by which S_f and S_b are reduced should be compatible with high-throughput, low-cost fabrication. S_b reduction is generally accomplished for p-type substrates by forming an aluminum or boron back surface field (BSF). Even though such BSFs can lead to low S_b ,^{1,2} there are disadvantages associated with each. For example, stresses imparted to the Si substrate during aluminum BSF formation preclude application to thin wafers, and lengthy diffusion times required to form deep boron BSFs reduce compatibility with high throughput processing.

Surface passivation by a dielectric film provides an alternative to BSF design. However, traditional methods of growing a high quality thermal SiO_2 layer in a conventional furnace are not consistent with low-cost solar cell fabrication.³ Alternatively, silicon nitride (SiN) films deposited by plasma enhanced chemical vapor deposition (PECVD) have been shown to provide excellent passivation of the low resistivity p-type Si surface.⁴ However, the passivation quality of SiN films can vary greatly with deposition conditions, plasma reactor design, and post-deposition annealing. For example, reports show that high frequency direct PECVD SiN deposited on low-resistivity Si at 300°C can result in S values as low as 30 cm/s⁵ or as high as 20,000 cm/s.⁶ The former films showed an increase in S after a low temperature post-deposition anneal in forming gas, whereas the later films showed an improvement in passivation after a similar treatment. Since industrial solar

cells undergo a moderate thermal anneal in order to fire the screen-printed device contacts ($>700^{\circ}\text{C}$ and typically the final step in processing), it is imperative that a potential passivation scheme be compatible with this heat treatment.

In this work, we report the use of a dielectric stack comprised of SiO_2 grown by rapid thermal processing (RTP) and SiN deposited by the PECVD technique for effective passivation of the low resistivity p-type (100) Si surface. Not only does this passivation scheme withstand a moderate heat treatment ($>700^{\circ}\text{C}$), it relies on such a treatment to achieve very low S values. Compatibility with post deposition annealing makes this passivation scheme attractive for high-efficiency, high-throughput solar cell fabrication.

3.2 Experimental

P-type (100), $1.25\ \Omega\text{-cm}$, $300\ \mu\text{m}$ thick, float zone (FZ) wafers were used in this study to monitor surface passivation. The as-received wafers were chemically polished (*not* mirror-mechanically polished). Prior to rapid thermal oxide (RTO) growth and/or SiN deposition, the wafer surfaces were prepared with the following chemical treatment: dip in 2:1:1 $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4$ for 5 minutes, etch in 15:5:2 $\text{HNO}_3:\text{CH}_3\text{COOH}:\text{HF}$ for 2 minutes, dip in 2:1:1 $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$ for 5 minutes, and dip in 10:1 $\text{H}_2\text{O}:\text{HF}$ for 2 minutes. Between each step, the wafers were thoroughly rinsed in deionized water. The RTO layers were grown in an RTP unit (AG Associates 610) at 900°C in less than 5 minutes. PECVD SiN films were deposited in a direct, high-frequency (13.5 MHz), parallel-plate reactor (Plasma-Therm) at 300°C in 6-7 minutes. Ensuing thermal treatments (simulating screen-printed contact firing) were carried out in beltline furnace (Radiant Technology Corp.) in which samples are heated by tungsten-halogen lamps. The total anneal time in the beltline

was fixed at 2 minutes, and samples were exposed to a peak firing temperature of 730°C for only 30 seconds.

3.3 Results and Discussion

The passivation quality of each scheme was monitored by the transient photoconductance decay (PCD) technique. The effective lifetimes measured by PCD were converted to S values using a conventional analysis method.⁷ In this paper, all S values are calculated assuming an infinite minority carrier bulk lifetime. The resulting S values are therefore maximum or “worst-case” limits.

The passivation quality of an RTO layer grown at 900°C is shown in Figure 3.1 as a function of injection level in the 10^{14} - 10^{15} cm⁻³ range. The as-grown oxide results in S greater than 10,000 cm/s (not plotted in Figure 3.1) which is reduced to approximately 100 cm/s by an anneal in forming gas at 400°C. However, an ensuing 730°C beltline anneal degrades the passivation and increases S to greater than 1000 cm/s.

A similar trend is observed in this study for the PECVD SiN film *alone* (Figure 3.2). The as-deposited SiN results in S greater than 10,000 cm/s which is reduced to less than 200 cm/s by an ensuing anneal in forming gas at 400°C. (The high S value for the as-deposited film and the improvement after forming gas annealing are both consistent with the results of Refs. 6 and 8 in which a similar high-frequency, direct SiN was studied. However, there is a lack of agreement with the results of Ref. 5 in which the as-deposited SiN film results in very low S and subsequent low temperature forming gas annealing increases this value. Again, differences in the passivation behavior of seemingly analogous films are believed to arise from variations in reactor design and deposition conditions.) The effect of the 730°C beltline anneal is also shown in Figure 3.2. Again,

the heat treatment degrades the interface quality, and increases S by roughly one order of magnitude.

Clearly, the two passivation schemes shown above (RTO alone or PECVD SiN alone) are not compatible with high-throughput solar cell fabrication since neither can effectively withstand a screen-printed contact firing cycle without significant degradation in S. However, contrary to the response of the individual films, annealing the RTO/PECVD SiN *stack* actually enhances the passivation quality. The effect of stacking PECVD SiN on top of the RTO layer and then annealing at 730°C is shown in Figure 3.3. The S value attained after the final anneal (Step 3 in Figure 3) is clearly superior to the RTO growth (Step 1) or the SiN deposition on top of the oxide layer (Step 2). The 730°C anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO₂ interface, thus reducing the density of states at the surface. Also evident is the weak injection level dependence of S within the measurement range (10¹⁴-10¹⁵ cm⁻³). This behavior is quite different than that reported for the highest quality remote SiN films where S increases by a factor of 5 as the injection level falls from 10¹⁵ to 10¹⁴ cm⁻³.⁴

It is important to note that the final S value achieved after the 730°C firing of the stack is the same whether or not a forming gas anneal is used as an intermediate step following oxidation (Figure 3.4). This indicates that the SiN film is indeed supplying all the hydrogen needed to reduce S to such low levels. *Maximum* S values of 11 cm/s and 20 cm/s are achieved by the stack passivation on the surfaces of 1.25 Ω-cm and 0.65 Ω-cm material, respectively. These are among the lowest S values ever reported for solid film passivation of the low-resistivity Si surface. Moreover, these S values are significantly lower than those attained by either the RTO or PECVD SiN alone, even after the individual films are annealed in forming gas (Figures 3.1 and 3.2).

The initial RTO growth temperature is observed to have an effect on the final S value of the annealed stack. In Figure 3.5, the stack progression is shown for RTO layers grown at 850°C and 900°C. In both cases, low S values (<40 cm/s) are attained after the 730°C anneal. However, the initial 900°C RTO SiO₂ growth clearly results in lower S (aforementioned 10-20 cm/s). In the past, higher RTO growth temperatures have been observed to improve the SiO₂-Si interface quality by limiting the interface width⁹ and reducing the suboxide bonding arrangement.¹⁰

Dielectric passivation of undiffused surface is crucial for bifacial solar cells. Fig. 3.6 shows the effectiveness of several *individual*-passivating dielectrics. The dielectrics investigated include the 100 Å RTO alone, 100 Å thick conventional furnace oxide (CFO) alone, and 650 Å SiN alone. The individual layers result in S values in excess of 10,000 cm/s on 1.3 Ω-cm Si immediately after growth or deposition. This extremely poor S is reduced to lower levels (20-200 cm/s) if an additional FGA at 400°C is performed. However, a subsequent 730°C belt line anneal (simulating SP contact firing) degrades each passivation, increasing S above 1000 cm/s for the RTO and SiN films and above 175 cm/s for the CFO.

Contrary to the response of the individual films, annealing the RTO/SiN and CFO/SiN stacks clearly *enhances* the passivation quality. The stepwise effect of stacking SiN on top of the RTO or CFO layer and then annealing at 730°C is shown in Fig. 3.7. An S value of nearly 10 cm/s is attained at the 1.3 Ω-cm Si surfaces after the final anneal. This anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO₂ interface, thereby reducing the interface state density (D_{it}).

In conclusion, it is shown that an RTO/PECVD SiN stack, along with a short 730°C anneal, can be used to attain S values nearing 10 cm/s on the 1.25 Ω -cm p-type silicon surface. These S values are achieved by the stack even when passivation by the individual films degrades after annealing. Inability of the individual films to maintain low S values after moderate heat treatments precludes application to low-cost, high-efficiency solar cells which require effective surface passivation and screen-printed contact firing between 700°C-800°C. On the contrary, the stack passivation is ideally suited for high-throughput processing, and can be utilized to form cost-effective bifacial solar cells.

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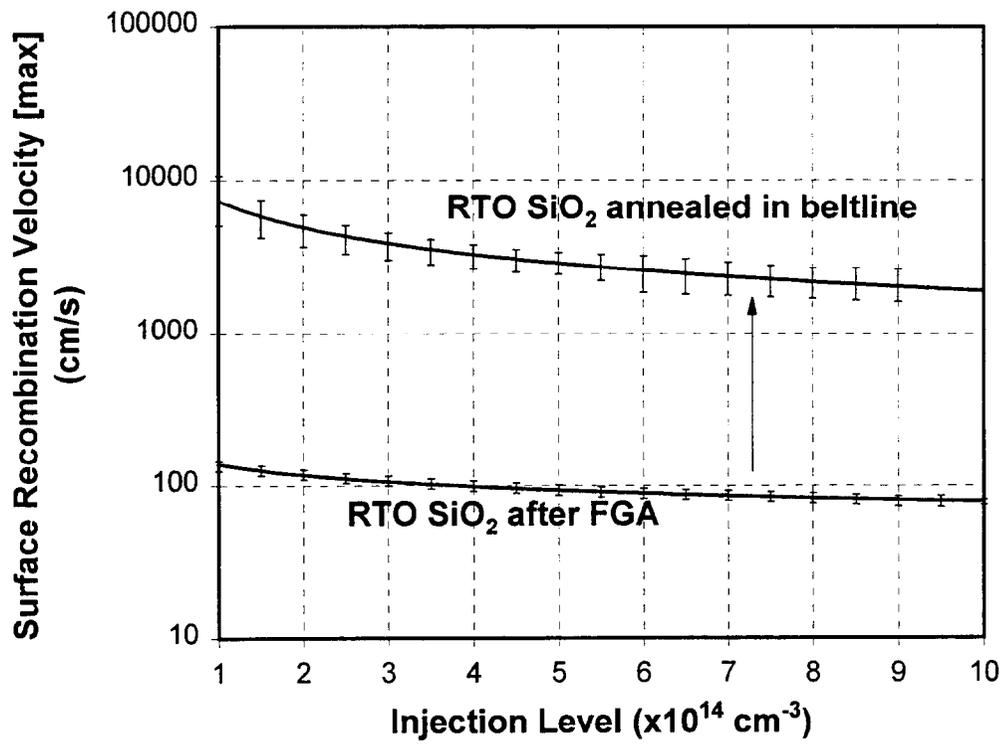


FIG 3.1. Passivation of the 1.25 Ω -cm p-type (100) Si surface by RTO SiO₂ alone. The RTO was done at 900°C in 5 minutes ($\approx 79\text{\AA}$), and the ensuing forming gas anneal (FGA) was done at 400°C in 15 minutes.

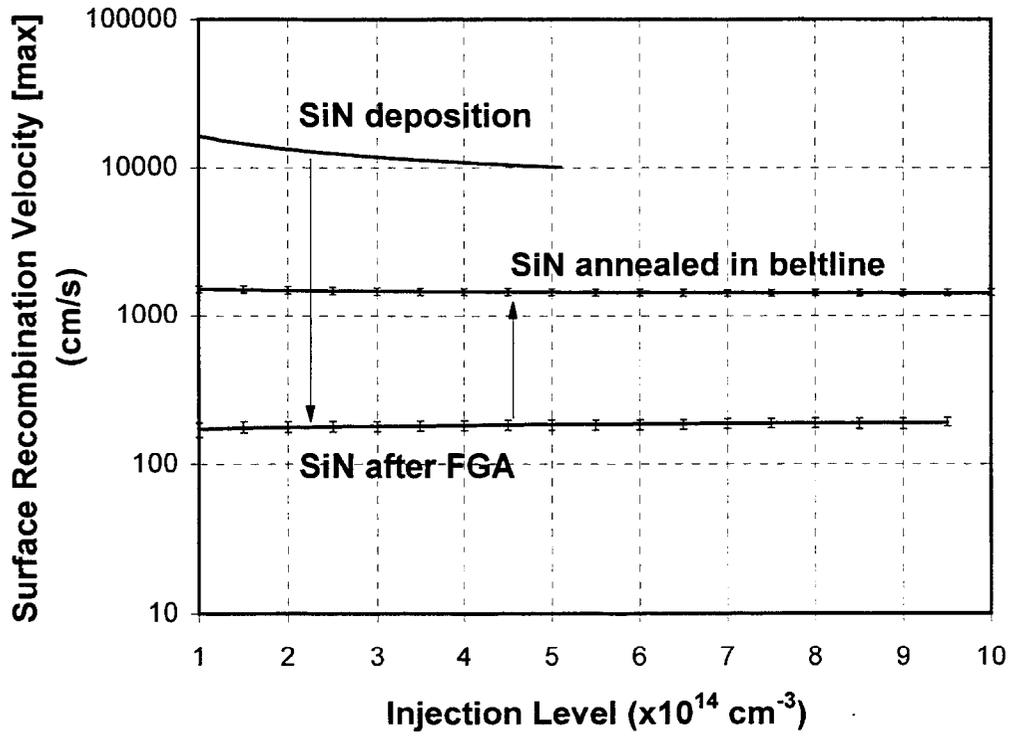


FIG 3.2. Passivation of the 1.25 Ω -cm p-type (100) Si surface by SiN alone. The FGA was done at 400°C in 30 minutes.

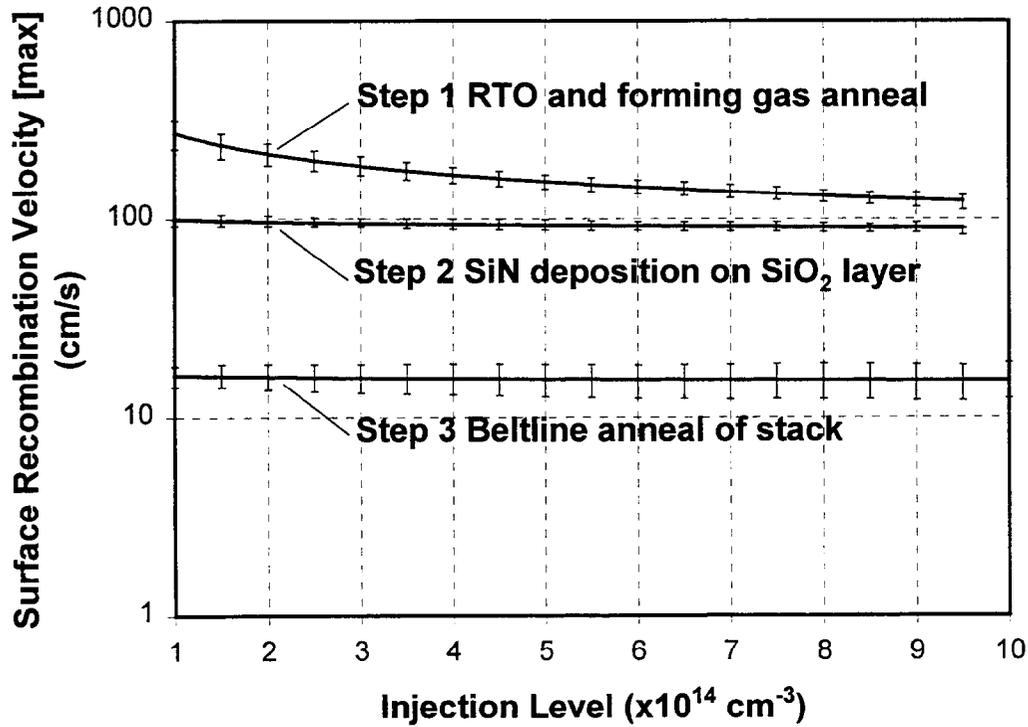


FIG 3.3. Progression of S values for passivation by the RTO SiO₂/PECVD SiN stack. SiO₂ films ($\approx 57\text{\AA}$) were grown at 900°C in 2 minutes, and the ensuing FGA was done at 400°C in 15 minutes.

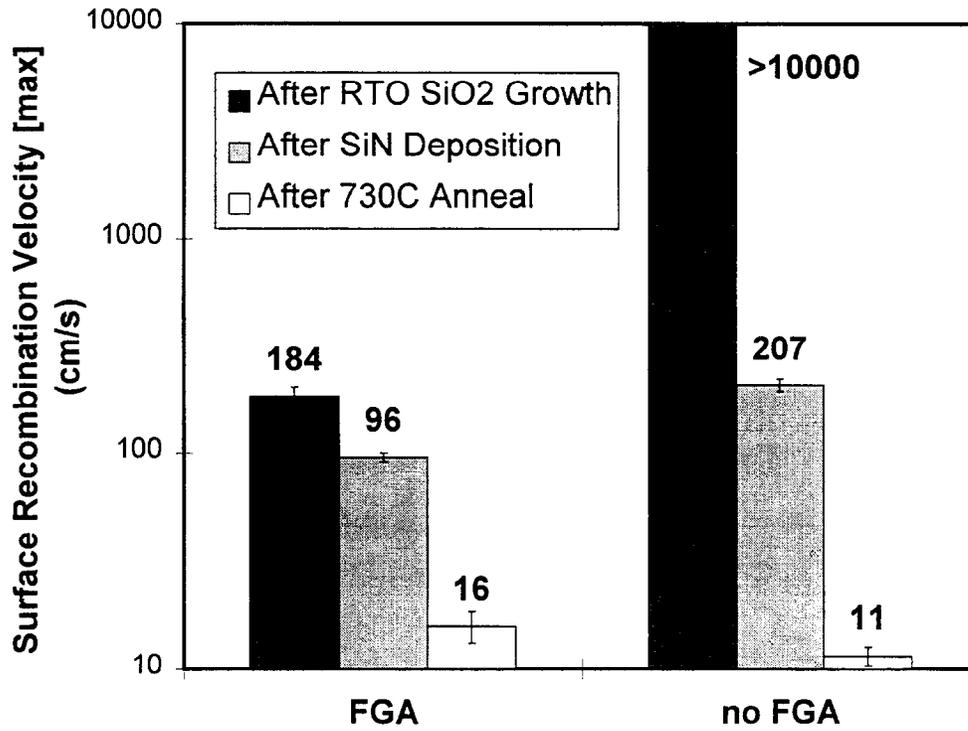


FIG 3.4. Effect of intermediate FGA (immediately after RTO growth) on the stack passivation. RTO films were grown at 900°C in 2 minutes, and the FGA was done at 400°C in 15 minutes.

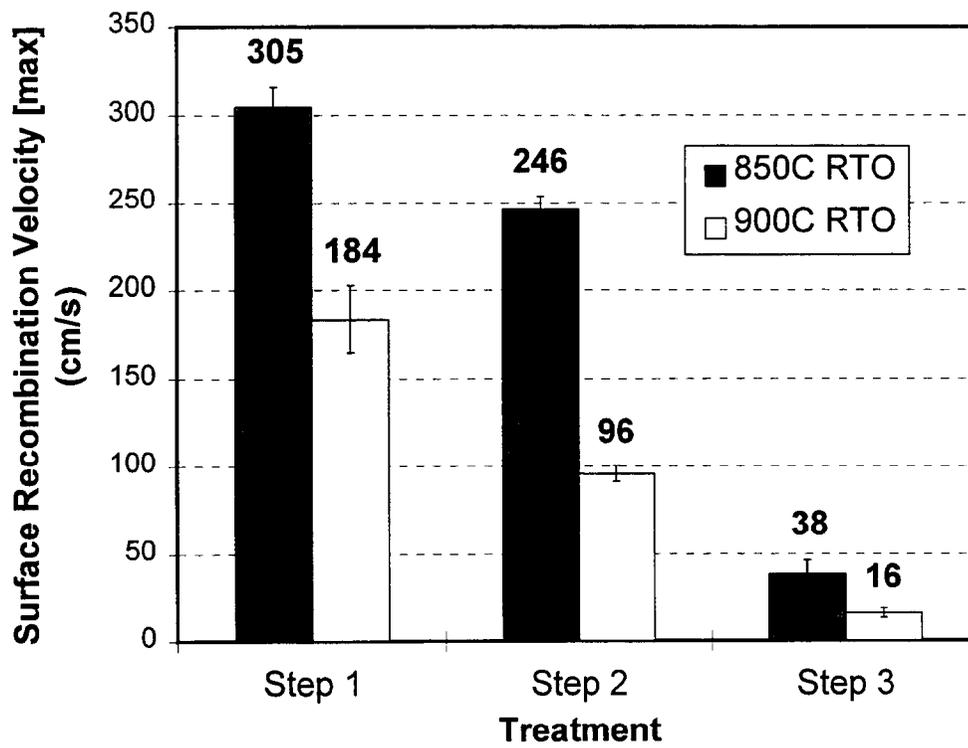


FIG 3.5. Effect of RTO temperature on the stack passivation. Step 1: 2 minute RTO growth ($\approx 43\text{\AA}$ at 850°C , $\approx 57\text{\AA}$ at 900°C) followed by FGA at 400°C in 15 minutes, Step 2: SiN deposition on RTO layer, Step 3: 730°C anneal of stack.

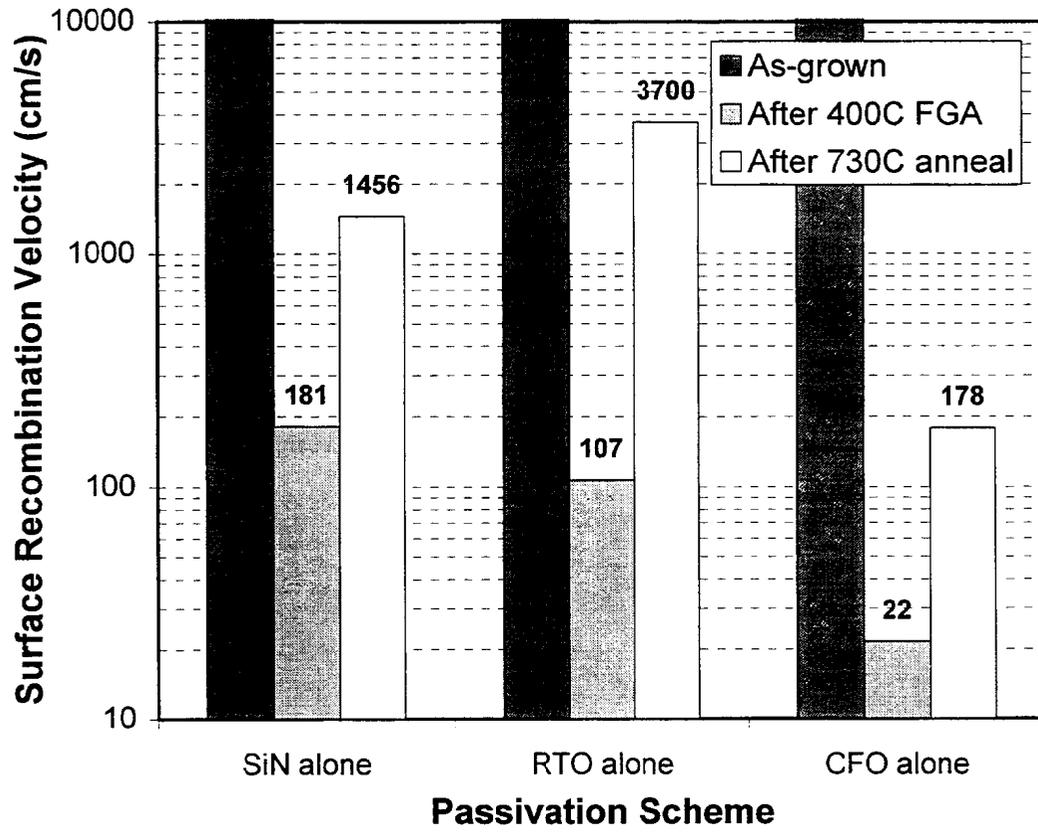


Fig. 3.6: The effect of belt line annealing on the S value of individual dielectric passivation schemes.

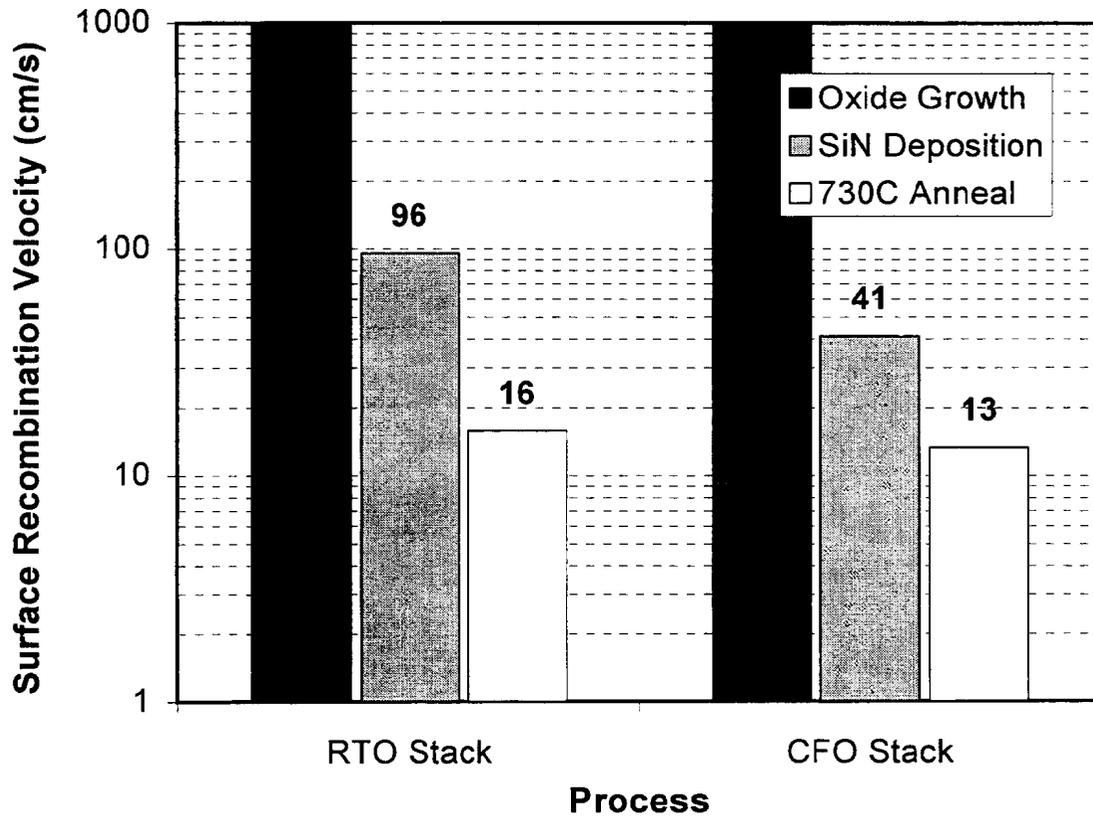


Fig. 3.7 Improvement in S of the stack passivation scheme after 730°C/30 sec annealing.

CHAPTER IV

AN OPTIMIZED RAPID ALUMINUM BACK SURFACE FIELD TECHNIQUE FOR SILICON SOLAR CELLS

4. An Optimized Rapid Aluminum Back Surface Field Technique for Silicon Solar Cells

4.1 Introduction

The back surface recombination velocity (S_b) begins to strongly influence solar cell performance when the ratio of minority carrier diffusion length to device thickness approaches or exceeds unity. Single crystalline Si typically falls into this category, and multicrystalline growth techniques have improved to the point where “cm-scale” grain sizes with long intragrain diffusion lengths are common. Furthermore, the cost-advantage associated with reduced Si consumption has led photovoltaic (PV) manufacturers to implement thinner substrates. When the solar cell thickness is reduced, the influence of S_b on device performance is felt more strongly. These observations emphasize the need to reduce S_b in commercially available solar cells.

A robust structure capable of reducing S_b is the back surface field (BSF), or high-low junction. This region acts to transform the true S_b into an effective recombination velocity (S_{eff}) at the BSF junction edge [1,2,3,4,5,6,7,8]. Commonly implemented on p-type substrates is the aluminum-alloyed BSF (Al-BSF). The Al-BSF is attractive because the p^+ region is formed by metal-Si alloying instead of dopant diffusion. As a result, BSF formation can be accomplished very quickly (within seconds or minutes) and at moderate temperatures ($<900^\circ\text{C}$). This provides a distinct advantage over, for example, a deep p^+ boron BSF that requires a lengthy (≈ 1 hour), high-temperature ($\approx 1000^\circ\text{C}$) diffusion step in order to achieve low S_{eff} [9,10].

In general, BSF action improves with increasing junction depth and doping level. A theoretical treatment of the Al-BSF based on the Al-Si phase diagram reveals that: 1) the junction depth is primarily determined by the amount of Al initially deposited onto the Si substrate, and 2) the doping

level is determined by the peak alloying temperature [11]. The greater the thickness of deposited Al, the deeper the resulting BSF junction. Similarly, the higher the alloying temperature, the more heavily doped the p^+ region.

A limited number of experimental studies have attempted to quantify these theoretically expected relationships. In [11], del Alamo et. al. investigated the effect of peak alloying temperature (in the range of 650°C-825°C) on Al-BSF quality. While a weak relationship between S_{eff} and alloying temperature was observed, the lowest S_{eff} 's attained were not consistent with the requirements for high-efficiency solar cells. The authors indicated that the limitation was due mainly to the deposition of thin Al films ($\approx 1\ \mu\text{m}$) prior to BSF alloying. In [12], Amick et. al. investigated the effect of the initial Al thickness on BSF action. Screen printing was used to deposit thick and (relatively) thin Al films onto solar cell samples. After alloying, the resulting BSF junction depths were measured by the spreading resistance technique to be in excess of 10 μm . However, the impact of these deep p^+ regions on solar cell V_{oc} was minimal, increasing V_{oc} by only $\approx 5\text{mV}$ for 2 $\Omega\text{-cm}$ substrate Si. Moreover, the cells were not characterized to determine the impact of the Al thickness on S_{eff} . In [13], Lolgen et. al. used photoconductance decay analysis to measure S_{eff} values below 200 cm^2/s (on 3 $\Omega\text{-cm}$ Si) for screen-printed Al layers alloyed in a belt furnace. However, when the same Al-BSFs were applied to cells, efficiency improvements concomitant with the expected S_{eff} reductions were not evident [14]. This was partly attributed to the use of substrates with low minority carrier diffusion lengths. It is evident from these studies that the effects of basic BSF formation conditions have not been established to a high degree of confidence.

Another important factor that affects Al-BSF electrical quality, one that is not considered in the studies mentioned above, is junction uniformity. In [15,16], Roberts and Wilkinson discussed the factors that influence the uniformity of alloyed metal-Si junctions. They indicated that the ramp-rate

used to reach the peak alloying temperature should have a significant impact on the resulting smoothness of the interface. This effect was later observed, in qualitative terms, for the Al-Si system in [17]. However, no study has analyzed the effect of junction uniformity on Al-BSF electrical quality and the resulting solar cell efficiency.

The goal of this work is therefore to: 1) understand the impact of Al-BSF uniformity on S_{eff} and cell performance, and develop processes that suppress junction non-uniformity, 2) establish from fundamental considerations an effective, high-throughput Al-BSF formation process, and 3) integrate this optimized Al-BSF into solar cell formation sequences to demonstrate high-efficiency. The main Al-BSF formation parameters (Al deposition quantity, alloying temperature, and furnace ramp-rate) are considered in detail. Industrially viable process techniques such as screen-printing, rapid thermal processing (RTP), and beltline alloying are analyzed in terms of their impact on BSF quality and cell performance.

4.1 Al-BSF Formation Issues

4.1.1 Theoretical Modeling: Effects of Temperature and Al Deposition Quantity

Al-BSF formation occurs in four steps: 1) Al deposition onto the rear Si surface, 2) alloying above the Al-Si eutectic temperature (577°C), 3) cooldown and epitaxial regrowth of the p^+ BSF, and 4) final solidification at the eutectic temperature. In general, the *opacity* of a BSF can be improved by increasing the junction depth and/or the p^+ doping level. A rudimentary analysis of the Al-Si binary phase diagram reveals that the Al-BSF *junction depth* is increased by either depositing thicker layers of Al onto the Si substrate or by alloying at higher temperatures, and the *doping level* is increased solely by raising the alloying temperature. The expected junction depth can be written explicitly in terms of process parameters:

$$W_{BSF} = \frac{t \cdot \rho_{Al}}{\rho_{Si}} \left(\frac{F(T)}{1 - F(T)} - \frac{F(T_o)}{1 - F(T_o)} \right) \quad (1)$$

where t represents the thickness of the deposited Al layer, ρ_{Si} and ρ_{Al} are the densities of Si and Al, $F(T)$ represents the Si atomic weight percentage of the molten phase at the peak alloying temperature, and $F(T_o)$ represents the Si atomic weight percentage at the eutectic temperature ($\approx 12.2\%$ for the Al-Si binary system) [11]. Applying this phase diagram analysis, the characteristic retrograde profile of an Al-BSF can be constructed and analyzed numerically to determine the change in S_{eff} expected for variations in Al deposition quantity and alloying temperature. The results of such an analysis are plotted in Fig. 4.1 for Al-BSFs on 2.3 Ω -cm Si. The model predicts that increasing the alloying temperature in intervals of 50°C (between 800°C-1000°C) should only reduce S_{eff} by a modest factor of 1.5 per interval. In contrast, increasing the Al deposition quantity from 1 to 10 μm should reduce S_{eff} by nearly one order of magnitude. Clearly, S_{eff} reduction can be achieved more readily by going to thicker Al deposition instead of higher alloying temperatures. It must be noted, however, that this simplistic treatment offers only general guidelines for Al-BSF design. It fails to consider another aspect of the BSF structure that has a significant impact on the electrical performance: *junction uniformity*.

4.1.2 Effect of Ramp-Rate on Al-BSF Uniformity

The uniformity of an Al-BSF is controlled to a large extent by the ramp-up rate used to reach the alloying temperature. Under slow ramp conditions, alloying between Al and Si can occur at certain sites before others (a form of *local wetting*), which leads to non-uniformities in the resulting Al-BSF [15]. These non-uniformities can include variations in junction depth, loss of surface planarity, spiking, and even non-formation of the p^+ region. Under fast ramp conditions, the sample goes through the eutectic point and reaches the process temperature very quickly. At typical process

temperatures ($\approx 800\text{-}900^\circ\text{C}$), the Al layer becomes molten and readily wets the entire Si surface. This promotes uniform alloying, and in turn, leads to more uniform Al-BSF regions.

Fig. 4.2 shows SEM micrographs of Al-alloyed p^+ junctions formed under slow ramp and fast ramp conditions. In both cases, $10\ \mu\text{m}$ of Al was thermally evaporated onto the Si substrates before alloying at 850°C . The sample undergoing the slow ramp process was pushed into a conventional furnace below the Al-Si eutectic temperature and ramped-up at a rate of $5^\circ\text{C}/\text{min}$. The sample undergoing the fast ramp procedure was processed in an RTP unit (AG Associates 610) and ramped-up at a rate of $1200^\circ\text{C}/\text{min}$. After processing, the p^+ regions were delineated by etching the samples in an acid solution [18].

As evident from Fig. 4.2, the slow ramp process results in an extremely non-uniform, discontinuous p^+ junction. On the contrary, the sample alloyed under fast ramp conditions shows a higher degree of junction uniformity and planarity. It is important to note, however, that while BSF uniformity is promoted by fast ramp alloying, the creation of non-uniformities can not be totally suppressed. Even under fast ramp conditions, Al-BSF junction depth variation can be significant (as high as 50% across the wafer). This effect has also been observed in a previous study on rapid Al-Si alloying [17]. Furthermore, it has been suggested that junction uniformity can be influenced by the type of heating element (halogen lamp versus graphite heater) used in the RTP unit [19]. These observations call into question the accuracy of relying on measured p^+ junction profiles to calculate S_{eff} . A more accurate method would be to analyze a finished solar cell and extract S_{eff} by a combination of internal quantum efficiency (IQE) measurements and device simulation.

The effects shown in Fig. 4.2 have a profound impact on the performance of solar cells formed on materials in which the minority carrier diffusion length exceeds the cell thickness. Fig. 4.3 shows the resulting V_{oc} change for solar cells fabricated on $2.3\ \Omega\text{-cm}$ FZ Si with Al-BSFs formed under

slow and fast ramp conditions. For each case except the *baseline* cell, 10 μm of Al was evaporated onto the back of the sample prior to alloying at 850°C. (The baseline BSF process refers to evaporation of 0.5 μm of Al followed by fast ramp alloying at 850°C. As a result of this thin deposition, an ineffectual BSF is formed, and the V_{oc} approaches the value limited by high S_b .) Each data point in Fig. 4.3 represents the average of nine 4 cm^2 cells fabricated from a 100 mm diameter wafer. All wafers were selected from the same ingot of float zone (FZ) Si. In order to minimize experimental variation, non-comparative process steps (i.e. emitter formation, emitter surface passivation, contact formation, and AR coating application) were done simultaneously. A detailed process sequence for these high-efficiency laboratory cells is given in Section 4.1.

Predictions based solely on the Al-Si phase diagram would require all cells in Fig. 4.3 to exhibit the same S_{eff} (and therefore the same V_{oc}) since the Al deposition quantity and peak alloying temperature are the same for each. Clearly this is not the case as Al-BSFs formed with differing ramp-rates exhibit significantly different device performance. IQE plots in Fig. 4.4 reveal that the change in V_{oc} observed for varying ramp-rates is indeed due to differences in S_{eff} . Long wavelength IQE in this spectral range (800-1100 nm) is a function of both bulk lifetime (τ_b) and S_{eff} . For high-lifetime material, such as the 2.3 $\Omega\text{-cm}$ FZ Si used in this study, the IQE is invariant to small perturbations in τ_b and responds only to changes in S_{eff} . Also shown in Fig. 4.4 are long wavelength IQE simulations generated using *PCID-4* [20] for an analogous device with S_{eff} values ranging from 10^4 cm/s to 10^2 cm/s . By simple comparison, it is clear that the S_{eff} of the Al-BSF is reduced by nearly one order of magnitude by changing from slow to fast ramp process conditions.

4.1.3 Effect of Al Deposition Thickness and Alloying Temperature on Al-BSF Quality

Fig. 4.5 shows that the positive effect of increased Al deposition thickness on BSF quality (predicted theoretically by Al-Si phase diagram analysis) occurs only when fast-ramp alloying is implemented. Under such conditions, V_{oc} improvements in excess of 25 mV can be achieved by increasing the Al deposition thickness from 1 to 10 μm for 2.3 $\Omega\text{-cm}$ FZ Si. Under slow ramp alloying conditions, the same correlation between deposition quantity and BSF action is severely diminished.

The other variable in the Al-BSF formation process is the alloying temperature. As the BSF alloying temperature is increased, it is expected that both the p^+ region doping level and junction depth also increase. Again, the analysis in Fig. 4.1 indicates that S_{eff} should drop by a factor of 1.5 for every 50°C increase in alloying temperature between 800°C and 1000°C. To verify this prediction, p^+ Al alloyed junctions were formed and profiled using the electrochemical CV measurement technique. The junctions were formed by thermally evaporating 10 μm of Al onto p-type Si and then alloying by RTP at temperatures between 800-1000°C. The results (Fig. 4.6) are consistent with the theoretical *trend* expected for the alloying temperature effect.

To determine whether the same trend is observed for solar cells, a series of devices was fabricated with Al-BSFs alloyed at 850°C, 900°C, and 950°C in the RTP unit. The results show that the temperature variation actually has little effect on cell performance. Furthermore, IQE measurements of the same devices reveal almost no variation in the long wavelength response which indicates nearly the same S_{eff} behavior for all samples. This apparent discrepancy between CV profiles and cell performance can be understood on the basis of the microscopic non-uniformities (etch pits, Al inclusions, etc.) present in even Al-BSFs formed under fast ramp conditions. SEM analysis of the BSF surfaces reveals their existence. The BSF effect is strongly

tempered by these features, and the relatively small V_{oc} variation is attributed to their presence. On the contrary, the CV technique measures across a fairly large sample area ($\approx 7\text{mm}^2$). The profiles are therefore not significantly affected by the microscopic non-uniformities in the p^+ region.

4.2 Assessment of Screen-Printed Thick Al Films for BSF Application

As shown in Fig. 4.5, thick film Al deposition is a critical requirement for effective Al-BSF formation. However, thick Al deposition by evaporation is inappropriate for large scale cell production. Screen-printed (SP) Al has been widely implemented in Si photovoltaics as a low-cost, high-throughput precursor to Al-BSF formation [21,22].

The Al quantity deposited onto a wafer during screen-printing depends on the rheology of the conductor paste as well as the Al content. In this study, a commercially available Al conductor paste (*FX-53-038* from Ferro Corp.) was used. Printing was accomplished using a screen with 325 wires per inch, wire diameter of 0.9 mil, and emulsion thickness of 1 mil. With these conditions, a typical print results in the deposition of 4.10 mg/cm^2 of Al (corresponding to an *effective* Al thickness of $15\text{ }\mu\text{m}$). SEM analysis of samples printed with Al and alloyed at 850°C in an RTP unit (Fig. 4.7) reveals cleanly formed, deep BSF junctions ($\approx 6\text{ }\mu\text{m}$) with a noticeable variation in junction depth. In spite of this junction depth variation, the deep p^+ regions are consistent with the requirement for effective BSF action.

The primary concern associated with screen-printing is possible contamination introduced into the wafer by the Al paste during high temperature alloying. Unlike the high purity Al used for the thermal evaporation studies (99.999%), the conductor paste is formed from lower purity Al (99.7%)

in which the chief contaminant is Fe. At elevated process temperatures, a fast-diffusing impurity like Fe can segregate into the bulk and degrade τ_b throughout the device [23].

The effect of contamination was monitored by measuring the performance of cells with SP Al-BSFs alloyed between 850°C-1000°C. The results (Fig. 4.8) indicate that the cell performance degrades at temperatures above 850°C. V_{oc} reduction is most severe when the alloying temperature is raised to 1000°C. Long wavelength IQE analysis of these cells shows that the degradation is primarily due to a drop in τ_b . However, at 850°C there is no appreciable sign of bulk contamination in these FZ wafers, and the resulting high IQE response in the long wavelength ($\approx 90\%$ at 1000 nm) is indicative of low S_{eff} .

4.3 Incorporating the Screen-Printed/RTP Alloyed Al-BSF into Solar Cell Processes

In order to quantify the effects on solar cell performance, the optimal Al-BSF process conditions discussed above (thick film deposition by screen-printing, RTP fast ramp alloying, and the maximum tolerable alloying temperature) were integrated into two solar cell processes: 1) a high-efficiency laboratory process and 2) a high throughput industry-type process. The results are presented in the following two subsections.

4.3.1 High-Efficiency Laboratory Process

The high-efficiency laboratory process is listed in Ref 7-10. The key features are a light emitter diffusion (90 Ω /sq), thin thermal oxide emitter passivation, front contact formation by vacuum evaporation and lift-off, and double layer AR coating application. Various Al-BSF structures were implemented on the rear surface. The effect of both Al deposition thickness and heating rate were

examined. The trend in performance (Table 4.3) is entirely consistent with the results in Fig. 4.5. Thick film Al deposition and fast ramp alloying are *both* required to achieve the highest cell performance. Moreover, the data shows that the lengthy 10 μm Al evaporation step can be completely replaced by high-throughput screen-printing without any loss in cell performance. Noteworthy efficiencies of 19%-20% are shown for 2.3 $\Omega\text{-cm}$ Si by utilizing the SP/RTP Al-BSF. This represents an efficiency improvement of $\approx 1.5\%$ (absolute) over cells with Al-BSFs formed inappropriately by either slow ramping or thin Al deposition.

4.3.2 High-Throughput Industry-Type Process

The SP/RTP Al-BSF was next incorporated into a high-throughput, industry-type process sequence. The key features of this process are a heavier emitter diffusion (45 Ω/sq), plasma SiN emitter passivation (which also serves as a single layer AR coating), and front contact formation by screen-printing. A step-by-step comparison of this sequence to the high-efficiency laboratory process is given in Ref 10. In addition to RTP alloying, beltline furnace alloying was also applied to BSF formation. Beltline processing is widely used in the commercial PV sector for various solar cell processes (i.e. for emitter diffusion, contact firing, and Al-BSF formation) [24]. In this study, the effects of specific beltline alloying treatments on S_{eff} and cell performance have been analyzed quantitatively.

A schematic of the 3-zone beltline furnace (Radiant Technology Corp.) used in this study is shown in Fig. 4.9. In each zone, the energy source for heating is provided by a bank of tungsten-halogen lamps. Three different beltline thermal cycles (also depicted in Fig. 4.9) were investigated for their ability to form Al-BSFs. These were: 1) a step-up in temperature from 425°C in Zone 1 to

730°C in Zone 3, 2) a step-up in temperature from 550°C in Zone 1 to 850°C in Zone 3, and 3) all zones set to 850°C. The relevance of each cycle is explained below.

Cycle 1 represents a typical front contact sintering recipe. It was included to determine the feasibility of co-firing the Al-BSF with the screen-printed front Ag contact. *Cycle 2* is a variation of Cycle 1 in which the temperature is ramped up to 850°C, a more appropriate setting for Al-BSF alloying. In *Cycle 3*, all three zones were set to 850°C so the sample could be exposed to high temperature immediately upon entering the furnace. As such, Cycle 3 most closely simulates the RTP fast ramp condition. In all experiments, the beltspeed was fixed at 15 inches/minute to maintain a total process time of 2 minutes. The effect of each thermal cycle on cell performance and long-wavelength IQE was measured, and the results are shown in Table 4.4 and Fig. 4.10.

Application of Cycle 1 results in the poorest long-wavelength IQE response corresponding to an S_{eff} of $>10^4$ cm/s and the lowest device efficiency of 15.2%. (As in Section 2.2, S_{eff} extractions were made by fitting the measured IQE response to theoretical spectra calculated using *PC1D-4*. In all cases, the τ_b required to accomplish the simulation was assumed to be very high. This assumption yields conservative or “worst-case” S_{eff} value.) The poor response of Cycle 1, expected due to the slow ramp temperature profile and low peak alloying temperature, indicates that an effective Al-BSF is difficult to form simultaneously during the front contact sintering cycle. This result is significant since many PV manufacturers choose to co-fire the Al-BSF with the front Ag contacts. Similar results are observed for Cycle 2 because of the slow ramp condition. However, application of Cycle 3, which most closely simulates an RTP fast ramp condition, results in a significant performance improvement over the other two treatments. The S_{eff} for this process is reduced to 10^3 cm/s, and the average device efficiency is improved to 16.3%. In spite of this improvement, Fig. 4.10 shows that the RTP process still results in the best long-wavelength IQE corresponding with an

S_{eff} of 200 cm/s and a device efficiency of 17.0%. This result is noteworthy considering the simplicity of the fabrication process (no high temperature oxidation for surface passivation, front and rear metallization by screen-printing, and a single layer AR coating only).

Additional increases in cell efficiency were achieved by incorporating improved light trapping features into the device design. Cell efficiencies of 17.5% ($V_{\text{oc}}=623\text{mV}$, $J_{\text{sc}}=35.4 \text{ mA/cm}^2$, $\text{FF}=0.793$) and 17.6% ($V_{\text{oc}}=616\text{mV}$, $J_{\text{sc}}=37.3 \text{ mA/cm}^2$, $\text{FF}=0.770$) have been officially verified for planar and textured devices, respectively, on 2.3 $\Omega\text{-cm}$ FZ Si with a SiN/MgF₂ double layer AR coating. These efficiency values clearly demonstrate the beneficial effect of optimally formed Al-BSFs on device performance.

4.4 Conclusions

The conditions required to form optimal Al-BSF regions have been established by a combination of theoretical modeling and detailed experimentation. For the first time, treatment of the Al-BSF has been extended to include the effects of junction uniformity on BSF action. Model calculations indicate that the S_{eff} of an Al-BSF is more readily improved by increasing the initial Al deposition thickness (from 1 μm to 10 μm) rather than increasing the alloying temperature (by 50°C between 800-1000°C). Experimental results show that this theoretical prediction is accurate only when RTP fast ramp rates are used to promote BSF uniformity. By combining thick film Al screen-printing and fast ramp RTP alloying at 850°C, Al-BSFs exhibiting S_{eff} as low as 200 cm/s have been achieved on 2.3 $\Omega\text{-cm}$ Si. Integrating this SP/RTP Al-BSF into a high efficiency laboratory fabrication sequence has resulted in Si solar cell efficiencies of 19-20%. The same BSF process applied to a high-throughput, industrial-type sequence has resulted in 17.0% efficient single layer (silicon nitride) AR

coated cells and 17.5% efficient double layer (SiN/MgF₂) AR coated devices. Al-BSF alloying in a beltline furnace, though somewhat less effective than RTP alloying, can still results in reasonable BSF action if: 1) an appropriate alloying temperature ($\approx 850^{\circ}\text{C}$) is used and 2) the fast-ramp condition is properly simulated.

4.5 References

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Table 4.1. Effect of alloying temperature on Al-BSF solar cell V_{oc} . All samples (except the baseline case) were formed by 10 μ m Al evaporation followed by RTP fast ramp alloying. Each data value represents the average of nine 4 cm² cells taken from a wafer.

Alloying Temperature	V_{oc} (mV)
<i>Baseline</i>	606
<i>Process</i>	
850°C	632
900°C	632
950°C	636

Table 4.2. Process sequence comparison: high-efficiency laboratory process and high-throughput industry-type process. *SP* represents screen-printing.

Step	Lab Process	Industrial Process
1	n ⁺ Diffusion (90 Ω/sq)	n ⁺ Diffusion (45 Ω/sq)
2	Thermal Oxide Passivation	PECVD SiN Pass. and SLAR
3	SP or Evap Al/ RTP Alloy	SP Al/ RTP or Beltline Alloy
4	Contacts (Photolithography)	Contacts (Screen Printing)
5	Double Layer AR	

Table 4.3. Al-BSF solar cells formed using a high-efficiency, laboratory fabrication sequence. All results have been officially verified at Sandia National Labs. (Cell area: 4 cm²)

BSF Formation	Res. (Ω-cm)/ Surface	V_{oc} (mV)	Jsc (mA/cm²)	Eff (%)
Baseline	2.3 Planar	606	36.4	17.4
10 μ m Evap Al	2.3 Planar	612	35.9	17.4
Slow Ramp Alloy				
10 μ m Evap Al	2.3 Planar	632	37.6	19.0
RTP Alloy				
Screen Printed Al	2.3 Planar	637	37.4	19.1
RTP Alloy				
Screen Printed Al	1.3 Textured	634	38.5	19.8
RTP Alloy				

Table 4.4. Average performance of Al-BSF solar cells formed using a high throughput, industry-type fabrication sequence. (Cell area: 4 cm²)

Cell Type	Res.	V_{oc}	Jsc	Eff
	(Ω-cm)	(mV)	(mA/cm²)	(%)
Beltline Alloying	2.3 Planar	597	32.7	15.2
Cycle 1				
Beltline Alloying	2.3 Planar	614	34.2	16.3
Cycle 3				
RTP Alloying	2.3 Planar	625	35.1	17.0
Fast Ramp 850°C				

CHAPTER V

ADVANCES IN LOW-COST MULTICRYSTALLINE SILICON SOLAR CELL PROCESSING IN THE LAST DECADE AND A ROAD MAP FOR ACHIEVING 18-19% EFFICIENT MANUFACTURABLE CELLS

5. Advances in Low-Cost Multicrystalline Silicon Solar Cell Processing in the Last Decade and a Road Map for Achieving 18-19% Efficient Manufacturable Cells

The U.S. Photovoltaic Industry Roadmap calls for an increase in low-cost Si PV cell efficiency to 16% by 2003, and 18% by 2010. This paper presents the guidelines for achieving $\geq 18\%$ efficient industrial cells through an assessment of impact of individual cost-effective design features. This paper also reviews recent progress in high-efficiency manufacturable and non-manufacturable mc-Si solar cell technologies with the aim of identifying which technologies are the most promising for the long term goal of silicon photovoltaics.

5.1 Introduction

Worldwide PV shipments are expected to reach 200 MW in the year 2000, with 80-85% modules made from crystalline silicon at a cost of \$3-4/watt. The module cost needs to decrease by about a factor of four to compete with conventional energy sources. Si material, cell processing, and module assembly each contribute about 45%, 25% and 30% of the cost of current PV modules made from ingot materials. Due to the high cost of Si, emphasis is gradually shifting from monocrystalline silicon to multicrystalline cast and ribbon silicon, which now account for about 45% of the market. Development of high efficiency cells on thin, low-cost materials using cost-effective technologies can significantly reduce the cost of Si PV.

Even though laboratory silicon cell efficiencies have reached 24.7%, production cell efficiencies are only in the range of 12-15%. Unfortunately, laboratory cells are too expensive and industrial cells are not efficient enough to meet the target of \$1/watt for PV modules. Detailed examination of the laboratory and industrial cells suggest the efficiency gap between the two can be reduced by cost effective implementation of advanced design features such as a) effective front and back passivation b) effective light trapping by front surface texturing and a good back surface reflector c) reduced shading and contact recombination d) selective emitter formation and e) higher diffusion length to cell thickness ratio. Reasonable efficiency targets for industrial cells are 18-20% for monocrystalline silicon and 16-18% for multicrystalline silicon. This paper shows a roadmap for achieving $\geq 18\%$ efficient industrial cells and highlights recent advances in silicon technologies that can get us there.

5.2 Guidelines for Achieving Manufacturable High-Efficiency Si Cells on Low-Cost Materials

Model calculations were performed using the PC1D program to establish a roadmap for achieving $>18\%$ efficient cells on low-cost materials with a bulk lifetime of only 20 μs . Emphasis is placed on technologies and cell designs that are practical for commercial cells, but may need further development. Figure 5.1 shows that a 300 μm thick 1 Ω -cm materials with a) a bulk lifetime of 10 μs b) poor front and back surface passivation ($S_f = 2 \times 10^5$ cm/s and $S_b = 10^6$ cm/s) c) a poor back surface reflector (BSR) (40%) d) a single layer AR coating with no texturing e) poor screen printed (SP) metallization on a 45 Ω/\square emitter with 8% metal coverage, excess junction shunting ($R_{sh} = 500 \Omega\text{-cm}^2$) and a FF of

0.73-0.74, produces a cell efficiency of 12.9%. This is quite close to the average efficiency of commercial mc-Si cells today. The second bar in Figure 5.1 shows that applying an Al-BSF with an S_b of 500 cm/s can improve this efficiency to 13.1%. If the SP metallization can be improved, more reasonable FF (0.78) with $R_{sh}=10^5\Omega\text{-cm}^2$, $J_{o2}=5$ nA/cm², $R_s=0.6\Omega\text{-cm}^2$, and metal coverage of 6%, a significant improvement in efficiency to 14.6% can be achieved. Improvement of the bulk lifetime from 10 μ s to 20 μ s by appropriate gettering and passivation can improve the efficiency to 15.2%. Improving the front surface passivation from $S_f=10^6$ cm/s to 3.5×10^4 cm/s raises the efficiency to 15.5%. Reducing the cell thickness to 100 μ m has no adverse effect on cell performance if the back surface reflector is 70-80%. Thinning the cell actually improves the efficiency by 0.3% and the addition of a good BSR raises the cell performance to 16.5%. This strongly endorses the use of thinner silicon for cost reduction. The next bar in Figure 5.1 shows that the formation of a selective emitter for SP cells with 85 Ω/\square between the grid line and $\leq 45 \Omega/\square$ underneath the grid, coupled with good front surface passivation, $S_f=7500$ cm/s, can raise the efficiency to 17.1%. Finally, if we can raise the bulk lifetime in 0.6 $\Omega\text{-cm}$, low-cost Si to 20 μ s through an understanding of the dopant defect interaction, then efficiency of 19.0 % can be achieved. Incorporation of a double layer AR coating can raise the efficiency beyond 19%. The following sections show the advances made in Si processing which incorporate the above high efficiency features on mc-Si in manufacturable as well as non-manufacturable fashion.

5.2.1 Advances in Si Technology for Achieving High Efficiency Cells on Low-Cost Materials

Multicrystalline cell efficiencies have increased steadily over the past two decades (Figure 5.2). These gains have been brought about by improved material quality and advanced cell processing. The progress in mc-Si cell efficiencies has been subdivided into three categories: a) small area (1-4 cm²) laboratory cells using non-manufacturable and expensive technology and b) large area cells (≥ 100 cm²) using the combination of manufacturable and non-manufacturable technologies and c) large area cells with technologies that may become manufacturable. In addition, Figure 5.2 shows that large area cells using well established cost-effective technologies, currently are in the 12-14.5% range.

The highest mc-Si cell efficiency (19.8%) on a textured surface has been reported by UNSW using 1.2 Ω -cm, 260 μ m thick, Eurosolare cast mc-Si in conjunction with well documented PERL cell technology [1]. This technology involves multiple high temperature and photomask steps to achieve a phosphorus diffused selective emitter, local boron back surface field, excellent front and back oxide passivation with point contacts on the rear, front and back pl contacts, and a honeycomb textured surface and formed by photolithography.

Georgia Tech reported the highest efficiency (18.6%) planar mc-Si device using a much simpler process without surface texturing, point contacts or a selective emitter [2]. Cell fabrication involved a 900°C/30 minute phosphorus diffusion on the front followed

by a second high temperature step, which provided front oxide passivation, Al-BSF, and hydrogenation of defects via forming gas anneal (FGA). Front contacts were formed by photolithography and a double layer AR coating was applied. It was shown that phosphorus and aluminum gettering and FGA induced hydrogenation were able to raise the starting bulk lifetime of 10 μ s in the HEM mc-Si material to the 35-135 μ s range. LBIC measurements were used to point out that some cells were only 17% due to regions of very high electrically active dislocations and defects, which could not be removed by conventional gettering and passivation. New technologies need to be developed to eliminate such regions in order to achieve large-area high-efficiency cells. The above two cell technologies demonstrate that 18-20% cells are achievable on mc-Si provided advanced cell design features are incorporated and the bulk lifetime in excess of 20 μ s.

5.2.2 Recent Advances in Low-Cost Technologies for High Efficiency Cells on Low-Cost Materials

5.2.2.1 Screen Printed Al Back Surface Field

The second bar in Figure 5.1 shows that replacing an ohmic contact ($S_b=10^6$ cm/s), with a good Al-BSF ($S_b= 500$ cm/s), can raise the efficiency by 0.2% even when the cell thickness is 300 μ m and the bulk lifetime is 10 μ s. Effects are much greater on a thin device. A p-p⁺ high-low junction can be formed by Al alloying or boron diffusion. Boron BSF formation requires a long high temperature ($\geq 950^\circ\text{C}$) diffusion which may occasionally degrade the bulk lifetime in low-cost materials due to the dissolution of

metallic precipitates. An Al-BSF is more desirable because it can be formed at lower temperatures ($\leq 900^\circ\text{C}$) in a very short time (< 5 minutes). Lolgen [3] and Narasimha [4] both measured an S_{eff} value of ~ 200 cm/s from SP Al-BSF formed on 2-3 Ω -cm monocrystalline Si. However, an S_{eff} value for a SP Al-BSF on mc-Si has not yet been established. It could be somewhat higher due to the presence of defects at the p^+ -p interface. Chalfoun [5] and Narasimha [4] also showed that Al-BSF quality is a strong function of the ramp-up rate; faster the rate, more uniform is the BSF. On that basis Narasimha [4] showed (Figure 5.3) that an RTP Al-BSF is superior to a BSF formed in the belt furnace, and co-firing of front and back contacts at 730°C in a belt, which results in a very poor Al-BSF. Many cell manufacturers today use co-firing to eliminate one firing step, but this comes at the expense of BSF quality.

As we move toward thinner cells (~ 100 μm), Al-BSF formation may warp the devices. This will require the development of a bifacial device structure with dielectric passivation on the rear with a punched through Ag or Al grid. Rohatgi et al. [6] reported a SP bifacial device with an efficiency of 17.0% on monocrystalline silicon using an oxide/nitride stack on the rear with a Ag grid. They calculated an S_b of 340 cm/s and a measured rear illuminated efficiency of 11%.

5.2.2.2 Improved Screen Printed Metallization

Most cell manufacturers use screen-printing today because it offers a simple, low-cost, and rapid method for metallization. However, cost and throughput gains are achieved at the expense of FF and cell performance. SP generally introduces more

shadow losses and requires an emitter with high N_s , which introduces heavy doping effects and hurts surface passivation. The latter can be mitigated by selective emitter formation. In addition, some investigators [7] have demonstrated printing of grid fingers with line widths as thin as 50 μm lines using modern screens and reduced emulsion thickness. Rohatgi et al. [6] have shown a methodology for optimized SP firing scheme for a given Ag paste and achieved FF as high as 0.795 on monocrystalline silicon with 0.5 μm deep emitters. However, SP of mc-Si cells with shallow junction emitters ($\leq 0.3 \mu\text{m}$) formed by rapid belt furnace processing still show FF in the range of 0.74-0.77. This is partly due to a paste-defect interaction which leads to junction shunting during firing and increases J_{02} . Firing contacts through the SiN_x AR coating, a scheme developed by IMEC [8], reduces junction shunting and also improves bulk and surface passivation due to the release of hydrogen from the SiN_x film. There is an urgent need for an understanding and optimization of paste purity and composition, frit content, and firing scheme that can give rise to high FF (≥ 0.78) reproducibly on mc-Si cells, because the FF of most production cells are only in the range of 0.70 – 0.75.

5.2.2.3 Simplified Buried Contact Technology

Buried contact solar cell (BCSC) technology was developed at UNSW and is well documented in the literature [9]. Large area cell efficiencies of 17-18% on Cz and 15.8% on mc-Si have been reported using the conventional single sided BCSC technology [10]. A typical process sequence involves texturing and light n^+ diffusion over the entire surface followed by a thick passivating thermal oxide on the front and back. A 40-50 μm

deep mechanical or laser grooving is performed to define grid regions. A heavy n^{++} diffusion is performed into the grooves to form a selective emitter utilizing the thick oxide mask. An Al-BSF is formed, followed by electroless plating of Ni, Cu, and Ag, while the thick oxide between the grid lines serves as a plating mask. Advantages of BCSC technology over SP include high metal conductivity, large cross sectional area and high aspect ratio for the contact grid with minimal shadow losses, and selective emitter. Since the process involves multiple lengthy high temperature steps, groove formation, etching, cleaning, and multi-layer plating, a simplified BC process is being developed which involves mechanical grooving, texturing, a single n^+ diffusion, rear BSF, AR coating and plating. This process reduces the number of high temperature steps but sacrifices V_{oc} . Some initial runs on single crystal silicon have been made, but no results on mc-Si are yet published.

5.2.2.4 Selective Emitter Formation with Good Front Surface Passivation

Figure 5.1 shows that selective emitter for SP devices in conjunction with good front surface passivation ($S_f=7500$ cm/s) can give $\sim 0.6\%$ increase in efficiency. Heavy doping ($\leq 40 \Omega/\square$) reduces the contact resistance and junction shunting, and well passivated lighter field diffusion ($\geq 80 \Omega/\square$) improves the short wavelength response.

Ruby et al. reported on the selective emitter formation by partially etching away the heavily doped layer between the grid lines using plasma RIE followed by SiN_x deposition in the same reactor for surface passivation and AR coating [11]. This process resulted in $\sim 13\%$ efficiency mc-Si cells with some FF reduction.

A second approach involves two separate diffusions followed by alignment of the SP grid to the heavily diffused regions. This resulted in an efficiency of 16 % on 100 cm² mc-Si using oxide passivation [13]. A third technology for selective emitter formation on mc-Si is being developed at IMEC, which involves a single step diffusion from a phosphorus dopant paste which is screen printed in a grid pattern followed by a diffusion in a tube furnace [13]. The areas under the grid are deeply diffused whereas in the areas between the grid, a shallower diffusion is obtained via gas phase transport of the dopant or autodoping. Using this technology, IMEC has recently produced 100 cm² mc-Si cells with efficiencies of 16.3%. The process sequence involved acidic isotropic etching, printing of phosphorus paste followed by burnout of organics in a belt furnace and selective diffusion by autodoping at 850°C in a quartz tube furnace, PECVD SiN_x deposition for surface passivation and AR coating, alignment of the SP grid to the heavily diffused regions, screen printing of Al on the back, and co-firing of both contacts. A double layer AR coating increased the efficiency to 16.9%.

A fourth selective emitter technology involves the use of self-doping Ag paste on a lightly diffused emitter. After firing this specially prepared phosphorus containing paste above the Ag-Si eutectic, a n⁺⁺ doped Si region is formed underneath the grid by liquid phase epitaxy in a process similar to the formation of an Al-BSF. This process forms a self-aligned selective emitter where the Ag grid is self-aligned to the heavily diffused regions. This process has recently produced 13-14% efficient 100 μm thick selective front surface field, n⁺-n-p⁺ Dendritic Web cells and 15-16% selective emitter cells on p-type monocrystalline Si at Georgia Tech.

5.2.2.5 Surface Texturing

Figure 5.1 shows that surface texturing can produce a significant improvement in cell efficiency by reducing reflection, increasing carrier collection, and enhancing light trapping by internal reflection. The best texturing has been achieved by inverted pyramids, but it is not manufacturable because it involves lithography. Random pyramids have been realized on (100) surfaces using anisotropic etching. This process is applicable for single crystal silicon, but not for mc-Si, which exhibits different crystallographic orientations, resulting in not only non-uniform texturing but also small steps between grains of different orientation.

Several promising methods are being explored for texturing mc-Si including RIE texturing, porous Si texturing, acidic isotropic etching, and mechanical V-grooving. Mechanical V-grooving has evolved from a single to multi-blade, high throughput process and has resulted in very low surface reflection and a ~ 1 % enhancement in cell efficiency. A process based on SP of 100 cm² mc-cells and firing through SiN_x was adapted to the processing of mechanically grooved structures and resulted in 16.6% efficiencies [14]. However, additional work is required to assess the reproducibility of SP contacts on such deep V-grooved cells.

RIE texturing involves immersing bare silicon wafers in a direct chlorine plasma [15]. By controlling the gas flow and process conditions, homogeneous microscopic pyramid-like structures are formed independent of the crystallographic orientation of the wafer. However, such surfaces increase surface recombination velocity. A short wet chemical etching improves the surface quality but at the expense of surface reflectance.

Inomata et al. produced a 17.1% efficient 225 cm² mc-Si cell using RIE texturing with Cl₂ gas, emitter diffusion from POCl₃, PECVD SiN_x bulk and surface passivation, and contacts formed by evaporation and lift-off photolithography [16]. This result suggests that RIE surface texturing can be done without causing performance degradation.

Another promising texturing technology involves the formation of a porous Si layer by short acidic etching in a solution of HF and nitric acid. By adjusting the solution composition and processing conditions, one can change the porosity, refractive index, and antireflection properties. Porous Si also shows diffused transmission and thus serves the purpose of light trapping. Porous Si layers with only 5.5% optical loss (reflection and absorption) have been achieved [17], which is superior to single layer SiN_x and TiO₂ coating. Surface passivation seems to be the weak point because of which, the short wavelength response of the PS cells is low. Laboratory cell efficiencies of 14.3% have been achieved on monocrystalline Si with SP contacts [17]. When a PS layer is formed after the front contact, one obtains essentially a selective emitter. However, the high surface recombination velocity negates the beneficial effect of a selective emitter.

Recently another simple, low-cost technique based on isotropic etching using acidic solutions has been developed at IMEC [18]. Large area (12.5 cm x 12.5 cm) SP mc-Si cells fabricated with this surface texturing process produced a 15.7% efficiency. The process sequence involved iso-texturing, POCl₃ emitter, PECVD SiN_x, SP front and back metallization and co-firing. The proprietary acid solution consists of a mixture of HF, HNO₃, and some additives. The removal of saw damage is part of the texture etching which requires only one step to create texture from as-cut wafers.

5.2.2.6 Manufacturable Gettering and Passivation Techniques for Lifetime Enhancement

Model calculations in Figure 5.1 show that lifetime enhancement from 10 to 20 μs can give $\sim 0.9\%$ increase in efficiency for this cell design. Beyond 20 μs , there is only little to be gained from further increases in lifetime especially for a 100 μm thick device. Georgia Tech has shown a rapid, manufacturable process in a belt furnace using a PECVD SiN_x AR coating, can increase the bulk lifetime in most mc-Si beyond 20 μs (Figure 5.4) [19]. This process involves a 925-935°C/6 minute spin-on or SP phosphorus diffusion and gettering in the belt, followed by SiN_x deposition on the front, and SP Al on the back and a short 850°C/2 minute anneal in the belt furnace. The simultaneous anneal in the presence of Al enhances the SiN_x -induced hydrogenation of bulk defects and also achieves Al gettering.

Remote plasma hydrogen passivation (RPHP) has been shown to improve the efficiency of solar cells on low-quality and high-quality mc-Si by 0.4-1.7% (absolute) on average. The advantage of RPHP is that hydrogenation is performed without plasma induced surface damage associated with direct PECVD deposition of silicon nitride. Currently, best results have been achieved in 30-60 minute processes at 400°C [20].

5.3 Summary and Conclusions

This paper reviews the progress in mc-Si cell efficiencies and provides a roadmap for achieving $\geq 18\%$ mc-Si cells using low-cost materials and potentially low-cost cell fabrication technologies. In addition to reviewing some of the highest efficiency mc-Si cells, recent advances in promising and emerging technologies are discussed. Particular

emphasis is placed on efficiency enhancing low-cost technologies such as back surface fields, defect gettering and passivation in a belt furnace, improved screen-printing, surface texturing, and selective emitters. Even though significant progress has been made, considerable research and development is still required to transform current 300-400 μm thick, 12-14% industrial cells to 100 μm thick 18-20% efficient cells in the near future.

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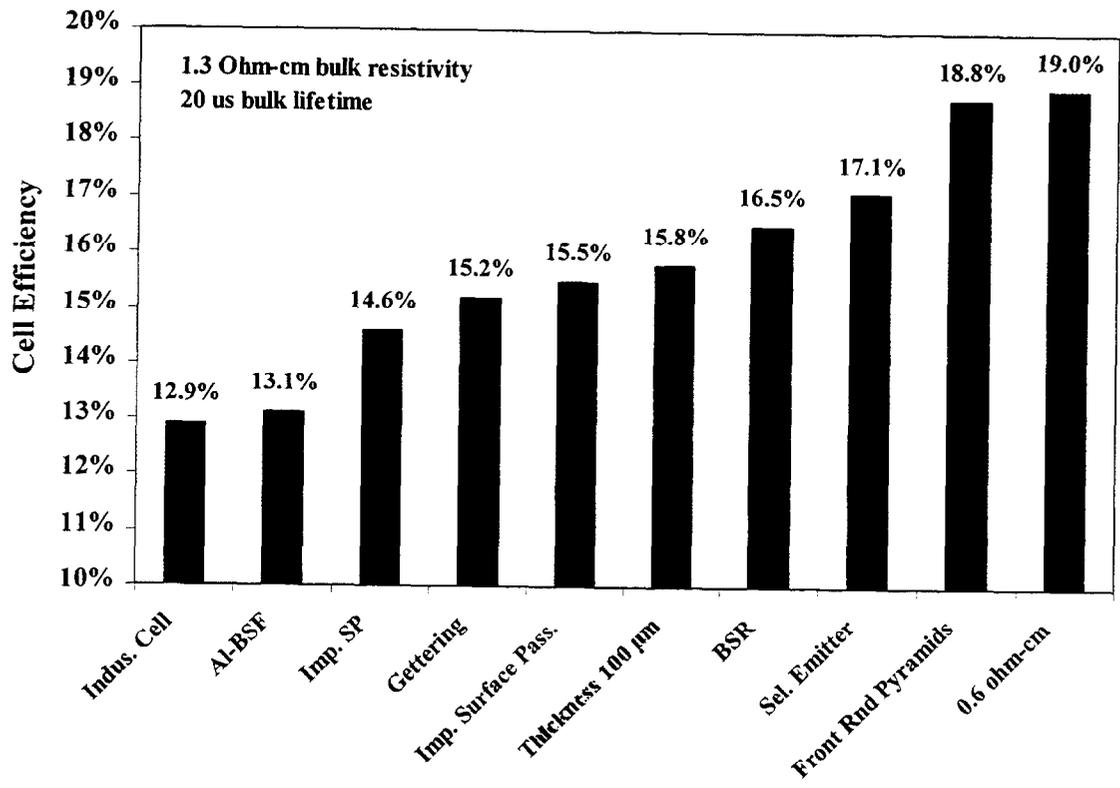


Figure 5.1: Incremental Improvement in Cell Performance with Manufacturable High Efficiency Technologies.

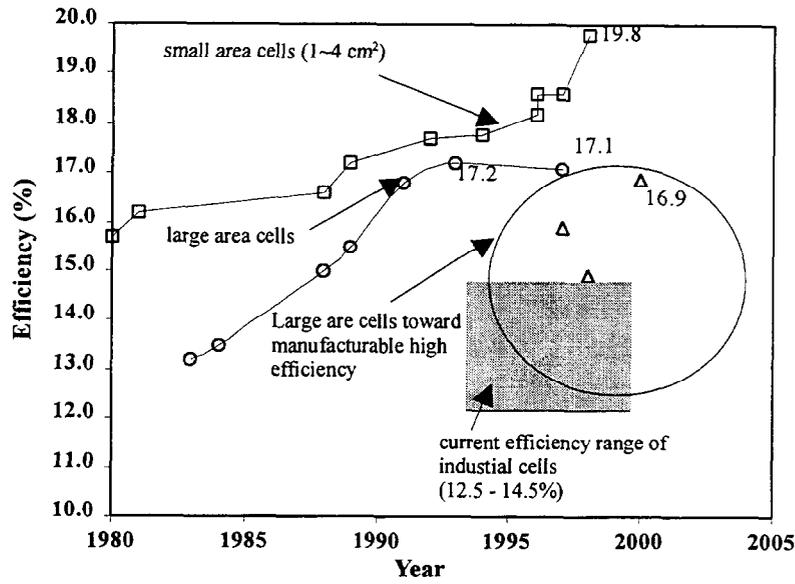


Figure 5.2: Progress in mc-Si cell efficiency over the past two decades.

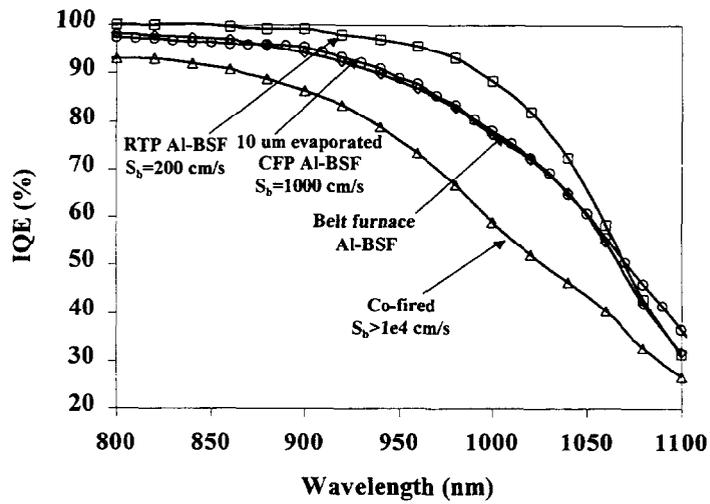


Figure 5.3: Effects of RTP and belt furnace processing on Al-BSF quality

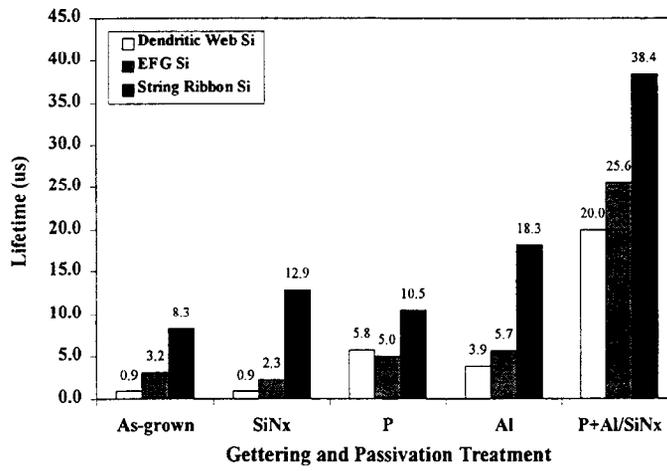


Figure 5.4: Effect of manufacturable gettering and passivation treatments on ribbon Si materials

CHAPTER VI

DEVELOPMENT OF HIGH EFFICIENCY SOLAR CELLS ON LOW-COST PV GRAD SI MATERIALS

6. Development of High Efficiency Solar Cells On Low-Cost PV Grade Si Materials

6.1 Development of High Efficiency Screen-Printed Multi-Crystalline Silicon Solar Cells By Incorporating Bulk Defect Passivation By SiN

6.1.1 Introduction

In the previous chapters research was focused on single crystals. In the following chapters emphasis is placed on multi-crystalline silicon materials. Multi-crystalline silicon has the potential of achieving low cost and high efficiency solar cells. Multi-crystalline silicon substrates, however, contain defects and residual impurities as compared to single crystalline silicon. These impurities degrade the minority carrier lifetime in the bulk, which often lead to lower solar cell efficiency than in the single crystalline silicon. Therefore, in order to improve the bulk lifetime or the diffusion length of the minority carriers to meet the criterion of $L/W > 2$, without adding to the cost of cell fabrication, low cost impurity gettering and defect passivation techniques must be developed.

Hydrogen from the SiN film has been reported to passivate the dislocations as well as grain boundaries [1] in multi-crystalline silicon substrates. In most of the work reported in the literature, the effect of high temperature anneal of the SiN film on multi-crystalline silicon without prior gettering has not been investigated systematically. Therefore, one of the objectives of this study was to investigate the bulk defect passivation due to SiN induced hydrogenation in Eurosolare grown cast multi-crystalline silicon before and after the three high temperature anneals, namely emitter diffusion, BSF formation and contact firing, consistent with screen-printing technology.

In the present investigation, the bulk lifetime and hydrogen concentration measurements were performed before and after various heat treatments of the SiN film deposited on p-type, 0.8

Ω -cm, EuroSolare grown cast multi-crystalline silicon. Finally the screen-printed multi-crystalline silicon solar cells were fabricated and characterized.

6.1.2 Experimental

The process sequence used for the lifetime study and screen-printed solar cell fabrication on multi-crystalline silicon is outlined in Fig. 6.1. This sequence is completely manufacturable and is consistent with low-cost and high throughput.

6.1.2.1 Photo Conductance Decay (PCD) Measurements Of Bulk Lifetime After Each High Temperature Anneal

Laser PCD lifetime measurements were performed on all the samples. To measure the bulk lifetimes in each sample, the SiN film was removed in 20% HF and then the samples were placed in 0.001M of I₂ (placed in sandwich zip lock bag) for the measurements. The results of the bulk lifetime measurements are summarized in Figure 6.2.

6.1.2.2 Hydrogen content measurements

The hydrogen content of all the samples was measured by FTIR. The concentration of hydrogen for each sample was estimated using the Gaussian fit to the peak to determine the area under the absorption peaks.

6.1.2.3 Screen-printed solar cell characterization

The process sequence adopted for the fabrication of the screen-printed solar cells using the lamp heated belt line furnace is shown in Fig. 6.1. Selected solar cell results are given in Table 6.1. Figures 6.3 and 6.4 show the I-V characteristics of one of the cells and the corresponding internal quantum efficiency. Figure 6.5 shows the dark I-V analysis of this cell.

Table 6.1: Electrical characteristics of selected belt line screen-printed multi-crystalline silicon solar cells. Cell area is 4 cm² and the measurement is performed under AM1.5G, 100 mW/cm², 25°C.

Cell ID	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF	Eff (%)	n _{eff}	Jo _{eff} (A/cm ²)	Rs (□- cm ²)	Rsh@-1 (□-cm ²)	Rsh@0 (□-cm ²)
euo6-1	605	31.43	0.746	14.2	3.26	2.0E-12	0.59	680	1,590
euo6-2	592	30.60	0.693	12.6	5.16	3.0E-12	0.54	82	318
euo6-3	594	31.02	0.674	12.4	6.61	2.9E-12	0.56	67	190
euo6-4	605	31.28	0.743	14.1	2.74	1.9E-12	0.59	5,648	25,456
euo6-5	596	30.55	0.744	13.6	3.15	2.7E-12	0.50	1,183	2,320
euo6-6	601	31.40	0.725	13.7	4.05	2.3E-12	0.77	381	790
euo6-7	605	31.57	0.750	14.3	2.74	1.9E-12	0.49	20,122	46,465
euo6-8	597	30.51	0.748	13.6	3.11	2.6E-12	0.53	1,510	3,437
euo6-9	598	30.66	0.752	13.8	2.91	2.5E-12	0.61	1,835	2,545
Average	599	31.0	0.731	13.6				3501	9235
EUO4-1	612	32.37	0.757	15.0	2.34	1.4E-12	0.67	8,077	27,736
EUO4-2	603	31.11	0.756	14.2	2.59	2.0E-12	0.55	8,828	21,582
EUO4-3	602	31.25	0.765	14.4	2.43	2.0E-12	0.60	4,621	15,740
EUO4-4	594	31.14	0.737	13.6	2.92	2.8E-12	0.69	3,842	8,153
EUO4-5	605	31.61	0.745	14.2	2.96	1.9E-12	0.69	3,555	3,471
EUO4-6	608	32.00	0.761	14.8	2.46	1.7E-12	0.63	25,261	30,488
EUO4-7	599	31.68	0.713	13.5	4.77	2.4E-12	0.78	421	426
EUO4-8	609	32.19	0.754	14.8	3.55	1.7E-12	0.56	1,324	1,441
EUO4-9	602	31.64	0.750	14.3	3.04	2.1E-12	0.67	2,437	2,442
Average	610	32.18	0.757	14.9			0.62	11554	19888
EUO1-1	597	32.10	0.680	13.0	6.54	2.7E-12	0.56	211	215
EUO1-2	595	31.31	0.671	12.5	6.55	2.9E-12	1.22	163	172
EUO1-3	592	31.58	0.650	12.2	9.17	3.2E-12	0.59	108	114
EUO1-4	589	31.75	0.685	12.8	5.27	3.6E-12	0.66	312	331
EUO1-5	591	31.77	0.690	12.9	5.77	3.3E-12	0.67	235	258
EUO1-6	603	32.37	0.683	13.3	6.85	2.1E-12	0.85	154	184
EUO1-7	584	33.22	0.638	12.4	7.15	4.6E-12	0.51	125	131
EUO1-8	594	32.01	0.673	12.8	7.25	3.0E-12	0.66	168	164
EUO1-9	598	31.91	0.711	13.6	5.49	2.6E-12	0.64	287	308
Average	595	31.93	0.694	13.2			0.63	244	260

6.1.3 Results and Discussion

6.1.3.1 Bulk defect passivation and hydrogen concentration measurements in SiN film.

6.1.3.1.1 Bulk defect passivation by SiN induced hydrogenation

As shown in Figure 6.2, the bulk lifetime improved remarkably, immediately after the SiN deposition. Since silicon nitride film was deposited at 300°C, increased bulk lifetime suggests that some of the defects responsible for the low as-grown lifetime in Eurosolare material have been passivated by hydrogen incorporated during the SiN deposition. In another study we found that certain multi-crystalline silicon material like EFG do not respond to SiN hydrogenation alone without prior or post heat treatment [2]. The bulk lifetime in Eurosolare silicon showed additional improvement after SiN anneal at 730°C. However, post deposition anneal at 850°C showed some reduction in lifetime. The maximum improvement in the bulk lifetime was observed after a 400°C forming gas anneal treatment. Notice that no phosphorus or Al gettering was performed in this experiment. This suggests that either SiN is ineffective or lifetime is being dictated by impurities when no gettering treatment is performed.

6.1.3.1.2 Hydrogen content of SiN by FTIR Measurements

Figure 6.6 shows the FTIR spectra of SiN film after each heat treatment. Fig. 6.6 shows the two absorption bands, N-H and Si-H, which indicate that the films contain large amount of hydrogen to passivate the bulk defects. It was observed that both the N-H bands shrink rapidly due to the evolution of the hydrogen after the 730°C anneal and N-H band is completely eliminated after the 850°C anneal. This indicates that large amount of atomic hydrogen is released from SiN during the annealing process.

6.1.3.2 Belt line screen-printed multi-crystalline silicon solar cells

Table 6.1 shows the electrical characteristics of 4 cm² multi-crystalline silicon solar cells. The data represents the average efficiency on three wafers, which varied from 13.2 to 14.8%

indicating a wide spread in the bulk lifetime of the substrate. Sandia National Laboratories confirmed the cell EUO4-1 to be 14.8% with a 76.8% fill factor and a short circuit current density of 31.58 mA/cm^2 which suggest a bulk lifetime of over $20 \mu\text{s}$ based on PC-1D device modeling. This indicates that phosphorus and Al gettering, along with SiN hydrogenation, are playing a significant role in enhancing the as-grown bulk lifetime. Dark I-V measurements and analysis gave J_{o_2} value of 255 nA/cm^2 , R_{sh} of $49894 \Omega\text{-cm}^2$ and series resistance of $0.44 \Omega\text{-cm}^2$ (Fig. 6.5). These numbers are quite respectable for a screen printed cell except for the J_{o_2} value which was on the high side of the limit for achieving fill factors in excess of 78% on multi-crystalline silicon.

6.1.4 Conclusion

The bulk lifetime of the Eurosolare multi-crystalline has been measured before and after SiN deposition and various high temperature anneals. It was found that the bulk defect in Eurosolare material could be passivated effectively with hydrogen from SiN and/or forming gas anneal without any prior gettering.

The hydrogen contents of the SiN films on all the samples showed the same trend as observed in the FZ material [2]. The as-grown film had enough hydrogen for the bulk defect passivation of the material, yet the effects were quite different. Thus the impurities in the bulk may need to be gettered first before realizing the full potential of the bulk defect passivation by hydrogen.

The lamp heated belt line screen-printed multi-crystalline silicon solar cells fabricated showed promising results. The fill factors averaging 69.4-75.7% for the three cells indicate some difference in these substrates. The short circuit current density of 31.58 mA/cm^2 and open circuit voltage of 610 mV indicated a lifetime value of about $20 \mu\text{s}$. The initial efficiency of 14.8% with a fill of 77% looks quite promising for a screen-printed manufacturable process on multi-crystalline silicon.

6.1.5 References

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6.1.6 Fabrication of Photolithography Solar Cells on EurosolareMc-Si material

This section summarizes cell fabrication done using our standard baseline (SBLC) process involving all conventional furnace processing (CFP). The Eurosolar solar cells were made by photolithography contacts on two different resistivity materials, 1 Ω -cm and 0.3 ohm-cm, with a thickness of ~14 mills.

In the SBLC CFP-CFO PL process the Eurosolare wafers were subjected to POCl_3 diffusion at 845 $^\circ$ C. The wafers were placed in the furnace at 800 $^\circ$ C then ramped up to 845 $^\circ$ C temperature and finally ramped back down to 800 $^\circ$ C before being pulled. After the removal of phosphorus glass in HF, a sheet resistance of $\sim 90 \Omega/\square$ was measured. Remainder of the SBLC process involved Al BSF formation by Evaporation of 2 μm thick Al on the back of the wafer followed by a furnace annealing at 850 $^\circ$ C for 10 min in Oxygen and 25 min drive in Nitrogen. Then all the wafers were ramped down to 400 $^\circ$ C and subjected to a 2 hr min Forming Gas Anneal (FGA) in an attempt to improve surface and bulk defect passivation via hydrogen. This results in $\sim 1 \mu\text{m}$ deep lower quality BSF with a back surface recombination velocity in excess of 10^4cm/s . The back contact was formed by evaporation of Al-Ti-Pd-Ag and the front metal grid was formed by photolithography and thin lift-off of Ti-Pd-Ag. These cells were then plated to $\sim 8 \mu\text{m}$ thick Silver by Silver Plating. The cells were isolated by mesa etching followed by an anneal in FGA at 400 $^\circ$ C. Finally MgF_2 -ZnS double layer antireflection coating was applied by evaporation. Cells were analyzed by light and dark I-V and spectral response measurements.

Table 6.2 shows the Efficiency Distribution of cells fabricated on 1 Ω -cm and 0.3 ohm-cm wafers. Both 1cm x 1cm and 2 cm x 2 cm cells were fabricated on large area (10 cm x 10 cm) wafer which gave cell efficiencies in the range of 17.1 to 15.7% with an average efficiency of 16.4% on 1 ohm-cm material. Cells made on low resistivity material had cell efficiencies in range 14.8 to 16.8% with an average efficiency of 15.9%. It is noteworthy that a very high V_{oc} of 645 mV was achieved on the low resistivity material. Resistivity was measured to be quite non-uniform in different regions of this material and varied from 0.2 to 2 Ω -cm.

Detailed analysis shows that further optimization and development of quality enhancement techniques such as gettering defect passivation, and thicker Screen printed BSF by RTP or BLP can produce greater than 18% efficiency on Eurosolare material without any surface texturing and point contacts.

Table 6.2: Efficiency Distribution of cells fabricated on 1 ohm-cm and 0.3 Ω -cm wafers

Cell ID	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF	Eff (%)	n _{eff}	Jo _{eff} (A/cm ²)	Rs (\square -cm ²)	Rsh@-1 (\square -cm ²)	Rsh@0 (\square -cm ²)
1 Ω -cm resistivity									
E1-1	608	34.02	0.792	16.4	2.10	1.9E-12	0.65	86,524	87,892
E1-2	608	34.49	0.788	16.5	2.17	1.9E-12	0.65	86,524	87,892
E1-3	621	34.74	0.791	17.1	1.49	1.2E-12	0.47	88,074	88,230
E1-4	603	33.91	0.788	16.1	2.01	2.3E-12	0.46	87,520	88,006
E1-5	605	34.02	0.787	16.2	1.83	2.1E-12	0.56	86,406	87,759
E1-6	612	34.45	0.789	16.6	2.10	1.6E-12	0.57	88,160	87,796
E1-7	602	33.56	0.786	15.9	2.02	2.4E-12	0.39	88,444	88,128
E1-9	598	33.53	0.783	15.7	2.14	2.8E-12	0.51	86,371	87,703
<i>Ave</i>	608	34.17	0.789	16.4	1.96	1.9E-12	0.54	87379	87958
0.3 Ω -cm resistivity									
E3-1	620	31.82	0.750	14.8	2.22	1.10E-12	0.82	81,625	52,233
E3-2	641	32.58	0.800	16.7	2.19	5.00E-13	0.44	87,042	51,799
E3-3	635	31.72	0.798	16.1	2.24	6.20E-13	0.36	112,239	80,826
E3-6	632	32.06	0.779	15.8	1.95	7.10E-13	0.40	113,190	211,527
E3-7	633	31.70	0.760	15.3	2.49	6.80E-13	0.64	60,960	18,116
E3-9	645	32.61	0.799	16.8	1.87	4.20E-13	0.40	76,748	112,619
<i>Ave</i>	634	32.08	0.781	15.9	2.16	6.7E-13	0.51	88634	87853

6.2 Development of Front Surface Field Al Back Junction $n^+ - n - p^+$ Screen-Printed Cells On Dendritic Web Silicon.

A new silicon solar cell structure is presented in which the p-n junction is formed by alloying aluminum with n-type silicon, and where this p-n junction is located at the back (non-illuminated) surface of the cell. With a phosphorus front diffusion, the resultant n^+np^+ structure has been implemented using dendritic web Si substrates which are 100 μm thick and doped with antimony to 20 $\Omega\text{-cm}$. Such a structure eliminates shunting of the p-n junction, provides an effective front surface field, enables a high minority carrier lifetime in the base, and is immune to light-induced degradation. Using only production-worthy, high-throughput processes, aluminum alloy back junction dendritic web cells have been fabricated with efficiencies up to 14.2% and corresponding minority carrier (hole) lifetime in the base of 115 μs (diffusion length of 370 μm).

6.2.1. Introduction

Silicon substrates of a sufficiently high quality that minority carrier diffusion length exceeds the substrate thickness lend themselves to non-conventional solar cell structures. Dendritic web silicon ribbon, which can be grown quite naturally at a thickness of 100 μm , is such a substrate. A solar cell structure designed to exploit this property is illustrated in Fig 6.7. The most striking feature of this cell is the aluminum alloy p-n junction on the back (non-illuminated) side. The substrate is doped lightly with antimony in order to ensure a high minority carrier (hole) diffusion length. A phosphorus-doped layer, which gives rise to a strong electric field for effectively passivating the front surface, leads to an n^+np^+ structure. With a silicon nitride anti-reflective (AR) coating and solderable silver contacts as a grid on the front and as two stripes over the aluminum-silicon eutectic metal on the back, the cell is complete. This cell has been named “PhosTop” because the top surface is doped with phosphorus rather than boron, as is usually the case for an n-base cell.

A comparison of a conventional silicon cell with the dendritic web silicon PhosTop cell is given in Table 6.3. There are several potential advantages of the PhosTop cell over the conventional cell. First, shunting of the p-n junction is eliminated. The junction is formed by alloying aluminum with n-type silicon to form a p⁺n structure. The aluminum-silicon eutectic remains as a self-aligned metal to contact the p⁺ surface. Aluminum cannot shunt the p-n junction because the aluminum creates a junction everywhere it contacts silicon. Moving the p-n junction from the front of the cell to the back opens the possibility of making the front diffused layer thinner without fear of shunting. The prospect of enhancing the blue response of the cell in this way was recognized previously in fabricating cells with a p⁺pn⁺ structure using 100 μm thick wafers sawn from a three-grain ingot [1].

A second advantage of the PhosTop cell is the existence of a strong front surface field. This arises from the phosphorus-diffused layer on the lightly doped n-type substrate, which creates a strong electric field. The recombination velocity of minority carrier holes at the front n⁺n junction is therefore, quite low. A previous study of such an n⁺n junction in a dendritic web silicon cell concluded that the effective recombination velocity must be <100 cm/s at the n⁺n junction, with a value of 25 cm/s at the maximum power point deduced [2].

Table 6.3: Conventional silicon solar cells versus dendritic web n⁺np cell

Cell Feature	Conventional Cell	Dendritic web n ⁺ np cell
Substrate thickness	300 μm	100 μm
Substrate type (dopant)	p-type (B)	n-type (Sb)
Substrate resistivity	1 Ω-cm	20 Ω-cm
Junction (dopants)	n ⁺ p (P,B)	p ⁺ n (Al,Sb)
Junction location	Front (n ⁺ pp ⁺)	Back (n ⁺ np ⁺)

The dendritic web silicon PhosTop cell holds a third potential advantage over the conventional cell in its high lifetime for minority carriers in the base. Light substrate doping ($20 \Omega\text{-cm}$) reduces the recombination activity associated with electrically active defects in the material by virtue of the location of the Fermi level near the center of the bandgap [3]. The choice of n-type is also important because minority carrier holes carry a positive charge. The principal defect in dendritic web silicon is an oxide precipitate decorating a dislocation core. The surface of such an oxide precipitate is expected to have a positive charge, which would repel holes from the defect but attract electrons. Lifetime degradation associated with oxygen precipitates has been observed to be much more severe in p-type silicon than in n-type [4]. Thus, the choice of n-type dopant having low concentration ensures a large minority carrier diffusion length for typical dendritic web silicon crystals.

A final advantage of the PhosTop cell is that there is no light-induced degradation since it has an n-type base. Conventional cells using Czochralski grown wafers doped with boron to $1 \Omega\text{-cm}$ exhibit a stabilized 4% drop in V_{oc} after exposure to one-sun illumination for only six hours [5]. This degradation has been traced to the existence of boron-oxygen pair [6]. Since PhosTop substrates have no boron they are free from light-induced degradation.

6.2.2 Experimental Results

The PhosTop cell of Fig. 6.7 was fabricated from dendritic web silicon substrates nominally $100 \mu\text{m}$ thick and doped with antimony to $20 \Omega\text{-cm}$. Only simple, high-throughput processes, thought to be compatible with a production environment, were used. The front surface field (n^+n) was created by applying a phosphorus liquid dopant with diffusion in a radiantly-heated belt furnace to approximately $42 \Omega/\square$. Silicon nitride was deposited on the front by plasma-enhanced chemical vapor deposition (PECVD) as an anti-reflective coating. The back junction (p^+n) was formed by screen-printing aluminum, then alloying with silicon in a belt furnace. Finally the front metal contact was formed by screen-printing silver, baked and fired in a belt furnace.

The lighted I-V curve, as measured at Sandia National Laboratories, for a dendritic web silicon PhosTop cell 2 cm x 2. cm in size is given in Fig. 6.8. In this case, cell efficiencies up to 14.2% were realized, with J_{sc} of 31.0 mA/cm², V_{oc} of 0.606 V, and FF of 0.756. Spectral data taken with a one-sun light bias for the same cell are given in Fig.6.9. The location of the p-n junction at the back of the cell is clearly indicated by the positive slope of the internal quantum efficiency (IQE) curve over its central portion. The reflectivity from the front surface is fairly high with a weighted value of 13.0% for the global spectrum. This represents a loss of 2.0% (absolute) in efficiency. An estimate of the minority carrier (hole) lifetime in the base was obtained by fitting the IQE curve using PC-1D. This gave a value of 115 μ s, equivalent to a hole diffusion length of 370 μ m which significantly exceeds the 100 μ m substrate thickness.

6.2.2. Discussion

It is desirable to boost the efficiency beyond the 14% demonstrated for dendritic web PhosTop cells to date. Values of V_{oc} and FF are usually quite acceptable, but J_{sc} is lower than desired. This is largely because significant amount of light is lost to reflection and because the blue response of the cell is relatively poor. Methods of texturing the (111) surface of dendritic web silicon are currently being explored to reduce reflection losses. Efforts to improve blue response are aimed at reducing phosphorus doping concentration near the front surface. This may require a more sophisticated surface passivation scheme and a modification of the front metallization process to retain low resistance ohmic contacts.

It may also be desirable to segment the back aluminum in some fashion. This would reduce the consumption of aluminum paste and also alleviate the bowing that sometimes occurs because of the mismatch in thermal expansion coefficient between aluminum and silicon. Preliminary attempts to reduce the back aluminum coverage have shown that even a modest opening in the aluminum cause a severe reduction in cell performance. It is clear that the exposed silicon must be passivated in some way. Promising approaches include thermal oxide, deposited dielectric layers, and a light diffusion with boron or phosphorus. If an effective

method for passivating exposed back silicon is found, the front metal contact could be moved to the back in an interdigitated back contact configuration. Such an approach not only eliminates grid shadowing, but also enables simpler methods to interconnect cells.

6.2.4. Conclusions

From this work the following conclusion can be drawn:

1. The quality, uniformity, and reproducibility of aluminum alloy p-n junctions are satisfactory for silicon solar cells;
2. A high-throughput, low-cost process utilizing screen-printing and belt furnace diffusion, alloying, and firing can be applied to 100 μm thick dendritic web silicon substrates with acceptable yield;
3. Cell efficiency in excess of 14% and minority carrier lifetime in excess of 100 μs can be achieved with the PhosTop cell structure using 100 μm thick dendritic web silicon substrates and high-throughput processes.

6.2.5 References

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6.3 Fabrication of Record High 16.2% Efficient Solar Cells on Evergreen String Ribbon material by Photolithography

This section summarizes recent cell fabrication done using our standard baseline (SBLC) process involving all conventional furnace processing (CFP). The solar cells were made by Photolithography contacts on different resistivity of Evergreen materials to study the effect of dependent-defect interaction and doping dependence on the final cell performance.

In this SBLC CFP-CFO PL process the Evergreen materials were subjected to a POCl_3 diffusion at 845°C . The wafers were placed in the furnace at 800°C then ramped up to 845°C temperature and finally ramped back down to 800°C before being pulled. After the removal of phosphorus glass in HF, a sheet resistance of $\sim 80 \Omega/\square$ was achieved. No emitter etch back was used in this SBLC process. Remainder of the SBLC process involved Al BSF formation by Evaporating of $2 \mu\text{m}$ of Al on the back of the wafer followed by annealing at 850°C for 10 min in Oxygen and 25 min drive in nitrogen. Then the Evergreen samples were ramped down to 400°C in Nitrogen and subjected to 2 hours of forming gas anneal to provide defect passivation by hydrogenation.

The back contact consisted of evaporated Al-Ti-Pd-Ag and the front metal grid was formed by photolithography and thin lift-off of Ti-Pd-Ag. These cells were then plated to $\sim 8 \mu\text{m}$ by silver plating. The cells were then mesa etched and annealed in forming gas at 400°C for 10 min. Finally ZnS-MgF₂ double layer antireflection coatings was applied by evaporation. Dark and Light IV and spectral response were performed for the analysis of these devices.

Figure 6.10 shows the doping dependence of string ribbon cell efficiency. In this experiment, optimum resistivity was found to be 1.5 Ω -cm, which also gave the highest V_{oc} and J_{sc} . This is indicative of best combination of bulk lifetime and surface recombination velocity. IQE measurements in Fig 6.11 clearly demonstrate that the 1.5 Ω -cm cell had the best long wavelength response. This is due to the fact that lower resistivity material has lower bulk lifetime and higher resistivity (3 Ω -cm) has higher J_{ob} due to higher base doping. This is especially true in these SBLC cells where thin evaporated Al BSF results in high back surface recombination velocity.

Table 6.4: Effect of doping concentration on the efficiency of string ribbon silicon solar cells.

Cell ID	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF	Eff (%)	V_{oc} (mV)	Eff25 (%)	n_{eff}	$J_{o_{eff}}$ (A/cm ²)	R_s (\square -cm ²)	$R_{sh@-1}$ (\square -cm ²)	$R_{sh@0}$ (\square -cm ²)
$R_s = 0.3 \text{ ohm-cm}$											
EK01-1	591	28.60	0.752	12.7	591	12.7	1.68	3.0E-12	0.33	60,594	53,734
EK01-2	584	28.63	0.762	12.7	584	12.7	2.43	4.1E-12	0.65	68,187	59,779
<i>Ave</i>	587	28.61	0.757	12.7	587	12.7	2.06	3.6E-12	0.49	64391	56756
$R_s = 0.7 \text{ ohm-cm}$											
EK71-1	602	31.24	0.778	14.6	602	14.6	2.08	2.2E-12	0.32	108,899	56,003
EK71-2	600	30.86	0.776	14.4	600	14.4	2.35	2.3E-12	0.38	99,578	55,418
<i>Ave</i>	601	31.05	0.777	14.5	601	14.5	2.22	2.2E-12	0.35	104238	55711
$R_s = 1.5 \text{ ohm-cm}$											
EK11-1	602	35.42	0.769	16.4	602	16.4	2.21	2.5E-12	0.47	85,579	82,999
EK11-2	600	34.87	0.760	15.9	600	15.9	2.54	2.7E-12	0.46	46,141	46,758
<i>Ave</i>	601	35.14	0.765	16.1	601	16.1	2.38	2.6E-12	0.47	65860	64879
$R_s = 3.0 \text{ ohm-cm}$											
EK31-1	562	34.65	0.756	14.7	562	14.7	2.21	1.2E-11	0.65	79,445	84,772
EK31-2	549	33.40	0.754	13.8	549	13.8	2.02	1.9E-11	0.61	91,234	87,729
<i>Ave</i>	555	34.02	0.755	14.3	555	14.3	2.12	1.5E-11	0.63	85339	86251

Table 6.4 shows the data for several 2cm x 2cm cells made from each material. The best cell efficiency achieved in this study was 16.2%. This was confirmed by SNL, as shown in Figs 6.12 & 6.13. This also happens to be the record high cell efficiency on String ribbon to date.

6.3.2 Fabrication of High Efficiency Cells on EFG Material using Photolithography Contacts

In this section we summarize the results of applying various technologies on EFG sheet silicon. In an effort to achieve high efficiency, EFG cells were fabricated by different technologies or process sequences. The objectives of this study were to:

- a) Evaluate the effect of ramp-up rate on Al BSF and cell efficiency.
- b) Evaluate the effect of Al BSF thickness on EFG cell efficiency.
- c) Compare the effect of furnace oxide and rapid thermal oxide passivation on cell efficiency.
- d) Compare the full CFP and RTP cells on EFG
- e) Evaluate the impact of PECVD AR coating hydrogenation.

In order to accomplish the above objectives, six different runs were made. Run A involved standard SBLC process with furnace diffusion and oxidation, 1 - 2 microns evaporated Al BSF, photolithography contacts and double layer ZnS/MgF₂ AR coating. In this run a slow ramp-up of 10°C / min was used during the Al BSF formation. Run B, was similar to Run A except 5 microns Al BSF was used to see the effect of deeper BSF. In Run C a thin 1 - 2 microns Al BSF was used but a fast ramp-up of 25°C / min was employed during the Al alloying process. In Run D, emitter was formed in a furnace but the 1 - 2 microns evaporated Al BSF and 100 Å RTO was formed simultaneously in the RTP system. The ramp rate in RTP was much higher 20°C / seconds. Run E involved a full RTP process in which emitter diffusion, 1 - 2 microns Al BSF formation and front surface passivation were done in the RTP system. Runs A to E were coated with two layer ZnS/MgF₂ AR coating. Finally, Run F involved a full RTP/RTO process, similar to Run E, with the exception of a PECVD SiN/MgF₂ AR coating which was annealed at 720°C in Air for 1.5 min for hydrogenation of bulk defects in EFG.

Tables 6.5 and 6.6 summarize the cell data from the above six runs. In all six runs cell efficiencies in excess of 14% were achieved (Table 6.5). Table 6.6 shows that there was only a slight improvement in going from 1 to 5 micron Al BSF using the slow ramp condition (Runs A and B). Switching from the slow ramp-up to fast ramp-up condition in the CFP process (Runs A and C) again did not show much improvement. This may be the result of smaller diffusion length in EFG ($L < W$), therefore changes in BSF quality due to increased thickness and fast ramp-up rate do not show a strong influence in cell performance which remained about 15.5%. Therefore, the EFG material used in this study needs to be thinned down to take advantage of the beneficial effect of thickness and fast ramp rate for higher efficiency EFG cells.

Runs D, E, and F involved RTP processing. Run E shows that RTP Al BSF and RTO formation reduced the EFG cell efficiency by about 1%. This is reflected in lower V_{oc} and J_{sc} , which also indicates low bulk lifetime. This could be the result of ineffective Al gettering during the short 2 min RTP process. Run E, which is a full RTP process gave an efficiency of 14.9% (Table 6.6), which is about 0.5% lower than the counterpart full CFP cell.

Run F, which involved a combination of full RTP and PECVD SiN, hydrogenation gave the best result with cell efficiencies exceeding 16%. High V_{oc} (582 mV) and J_{sc} (35.9 mA/cm²) values in this run relative to the above five runs indicate higher bulk lifetime due to PECVD SiN induced hydrogenation of defects in EFG Si. Thinning the EFG Si and applying a thicker Screen Printed BSF should be able to give even higher EFG cell efficiency.

Table 6.5: High Efficiency Solar Cells Fabricated on EFG ribbon material with Various Technologies. (Thickness=11 mills, $R_s=2-3$ ohm-cm, Area = 1 sq cm)

Cell ID #	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)
Run A - CFP/CFO (Slow Ramp, 1 - 2 micron Al BSF)				
N3-1	570	33.3	78.3	14.9
N3-2	566	32.9	77.9	14.5
N3-3	565	32.7	77.7	14.4
N3-4	563	32.4	77.7	14.1
ET2-2	564	32.6	78.5	14.4
N5-5	577	33.7	78.5	15.3
N5-6	558	32.3	77.7	14.0
N5-9	560	32.4	77.7	14.1
Run B - CFP/CFO (Slow Ramp, 5 micron Al BSF)				
N21a1-1	578	34.6	77.1	15.4
N21a1-2	577	34.9	77.1	15.5
N21a1-3	574	34.7	77.3	15.4
N21a1-9	562	32.4	77.3	14.1
N21a1-10	560	32.5	77.4	14.1
N21a1-11	560	31.4	77.1	14.0
N4-2	570	33.6	77.0	14.8*
Run C - CFP/CFO (Fast Ramp, 1 - 2 micron Al BSF)				
N1-1	567	33.3	78.1	14.7
N1-2	565	33.1	78.1	14.6
N1-3	560	32.8	77.7	14.3
N1-4	565	33.3	77.8	14.6
N1-8	559	32.6	77.5	14.1
N1-10	569	33.6	78.4	15.0
N1-11	573	33.9	77.5	15.0

N1-12	575	34.3	78.0	15.4
Run D - CFP/RTO (Fast Ramp, 1 - 2 micron Al BSF)				
N3-10	550	33.9	76.0	14.1
N3-11	556	33.3	75.9	14.1
Run E - Full RTP /RTO (1 - 2 micron Al BSF)				
N1-3	569	34.1	77.0	14.9
N1-11	554	33.5	76.5	14.2
Run F - Full RTP /RTO (1 - 2 micron Al BSF, PECVD SiN anneal @720C in air, etch thru , SiN/MgF2 ARC)				
E1-10	578	36.1	77.0	16.0
E1-13	554	34.0	75.1	14.1
E1-14	582	36.0	76.7	16.1

*Area 4 sq cm

Table 6.6: Effect of Various Processes on the Cell Performance on EFG Ribbon Material

Run #	Voc (mV)	Jsc (mA/cm ²)	FF (%)	Eff (%)	Process
Run A	577	33.7	78.5	15.3	CFP/1 – 2um-Al BSF,slow ramp/CFO/DLAR/PL
Run B	577	34.9	77.1	15.5	CFP/5um-Al BSF,slow ramp/CFO/DLAR/PL
Run C	575	34.3	78.0	15.4	CFP/1 – 2um-Al BSF,fast ramp/CFO/DLAR/PL
Run D	553	33.7	76.1	14.2	CFP/1 - 2um-Al BSF/RTO/DLAR/PL
Run E	569	34.1	77.0	14.9	Full RTP/1 - 2um-Al BSF/RTO/DLAR/PL
Run F	582	35.9	76.7	16.1	Full RTP/1 – 2um-Al BSF/RTO/ etch thru. SiN/MgF2/PL Anneal Air @ 720 ^o C for 90 sec

6.3.3 Fabrication of High Efficiency SBLC cells on p-type Dendritic Web Silicon Ribbon

This section summarizes cell fabrication done on P Web material from Ebara Solar Inc. using our standard base line (SBLC) process. This process involves conventional furnace processing (CFP) and photolithography contacts. Two different resistivity of P-Web material (0.3 and 7 ohm-cm) were used to study the effect of dopant-defect interaction and doping dependence on the final cell performance. In the standard SBLC process only 2 microns of evaporated Al BSF is used which results in high surface recombination velocity of $> 10^4$ cm/s. The cells were analyzed by light and dark J-V measurements and the results are summarized in Tables 6.6 and 6.7.

Table 6.6: LIGHT IV

P-Web Resist.	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)	n_{eff}	J_{off}	R_s	R_{sh-l}
0.2	632	33.0	80.9	16.8	1.89	7.2e-13	0.22	23,098
	630	32.9	80.4	16.7	2.02	7.7e-13	0.21	23,149
7.0	575	34.6	79.5	15.8	1.53	7.0e-12	0.18	23,067
	570	34.7	78.6	15.6	1.60	8.3e-12	0.17	23,016

Table 6.7: DARK J-V ANALYSIS OF BEST CELL

P-WEB Resistivity (Ω -cm)	J_{o1} (pA/cm ²)	J_{o2} (nA/cm ²)	R_{sh} (Ω -cm ²)	R_s (Ω -cm ²)	n_2
0.2	0.64	58.82	27879	0.19	2.41
7.0	2.28	5.33	24719	0.10	1.46

In this experiment low resistivity material gave an impressive cell efficiency of 16.8% while the high resistivity material gave an efficiency of 15.8%. The data shows that 0.2 ohm-cm silicon gave very high V_{oc} of 630 mV and fill factors in excess of 0.8 while the 7 ohm-cm cell gave high J_{sc} (34 – 35 mA/cm²) but lower V_{oc} (570 mV) and Fill Factor (<0.8). Higher resistivity cell gave lower cell efficiency (15.8%) because of higher J_{o1} value; inspite of higher bulk

lifetime. This is partly because of the 2 microns deep poor Al BSF which gives a recombination velocity of $> 10^4$ cm/s. Detailed analysis and model calculations show that the high resistivity material with a good BSF (BSRV < 500 cm/s) and high lifetime should outperform low resistivity cells with low lifetime. Therefore a screen-printed deeper BSF is expected to give higher efficiency on high resistivity web material. Experiments are in progress to make screen-printed RTP BSF cells to achieve $> 17\%$ efficient p-web cells.

6.3.4 Development of 14+% EFG solar cells using Rapid thermal processing

Rapid thermal anneal process has been optimized and applied to achieve 14+% efficiency in large area ($10 \times 10 \text{ cm}^2$) screen-printed EFG silicon solar cells. Large area EFG silicon cells were fabricated in collaboration with ASE Americas. The n^+ emitter, PECVD SiN single layer AR coating, and printing of silver contacts on the front and Al on the back were done at ASE Americas. The co-firing was done using a rapid thermal processor at Georgia Tech. During the RTP co-firing, PECVD silicon nitride on the front, aluminum paste on the back, and silver front contact metals were annealed simultaneously to achieve silicon nitride induced hydrogenation, aluminum back-surface-field, and ohmic contact of silver grids through the silicon nitride film. The objective was to optimize the rapid thermal processing to enhance hydrogenation, obtain a uniform deep Al-BSF, and Ag ohmic contacts on the front with good fill factor.

Figure 6.14 shows the temperature profile used during the rapid thermal processing that produced 14+% efficient large area EFG silicon solar cells. The profile includes a 60 sec anneal at $350 \text{ }^\circ\text{C}$ to burn off the organics in the Al and Ag pastes. The ramp-up rate from the burn-off step to the peak temperature found to be critical for achieving high fill factor. An optimum ramp-up rate was found to be $50 \text{ }^\circ\text{C}/\text{sec}$. At the peak temperature, the wafers were heated for 5 sec. Finally, samples were cooled down to room temperature with a rate of $33 \text{ }^\circ\text{C}/\text{sec}$. Total processing time was less than 110 sec.

Table 6.8 summarizes the cell data as a function of peak temperature. The co-firing peak temperature of $680 \text{ }^\circ\text{C}$ produced the best cell efficiency of 14.12 %. Fig. 6.15 shows the lighted I-V curve for the 14.12 % large area EFG cell. Detailed analysis is in progress to understand the competition between SiN-induced hydrogenation and Al-BSF formation during the co-firing. Higher temperature is expected to give better Al-BSF but it may hurt the hydrogenation because of the lower retention probability of hydrogen at defects. Figure 6.16 shows that co-firing of Al and SiN is much more effective for hydrogenation compared to sequential firing of Al and SiN. More work is in progress to optimize the final firing cycle to achieve superior Al-BSF, higher bulk lifetime, better FF, and greater than 15 % efficient large area RTP fired EFG solar cells.

6.4. Optimization of Paste and Front Metal Contact Firing Scheme To Achieve High Fill Factors On Screen Printed Silicon Solar Cells

For widespread implementation of silicon PV, the module cost must be reduced by a factor of 2 to 4. This can be accomplished by lowering the cost of solar cell materials and processing without sacrificing cell efficiency. A combination of high throughput belt line processing, SP contacts and mc-Si material offers an opportunity for significant cost reduction. However, most cell manufacturers who use the above combination are only able to achieve fill factors in the range of 0.68-0.75 with cell efficiencies in the range of 10-14%. Thus throughput gains are attained at the expense of device performance. In addition, there is considerable scatter in the fill factor of the SP cells in the literature with no clear guidelines for achieving high fill factors. This study shows that proper understanding of loss mechanisms and optimization of SP paste and firing cycle, can lead to fill factors approaching 0.77 and 0.79 on mc-Si and single crystal silicon, respectively, on a $45 \Omega/\square$ rapidly formed belt line emitter with a shallow junction depth of $\sim 0.27 \mu\text{m}$. It was observed that, deep and shallow emitters on mc-Si could lead to the same values of fill factors ~ 0.77 when the proper combination of paste and firing cycle is applied. The peak firing temperature for deep emitter is higher than the shallow ones with superior value of junction leakage current.

6.4.1 . Introduction

One of the most difficult aspects of large-scale solar cell production is the formation of high quality front contacts. The photolithography and buried contact metallization techniques are somewhat expensive and time consuming for large-scale application. In contrast, the screen-printing (SP) is a simple, cost effective contact formation technique that is consistent with the requirements for high volume manufacturing. However, the throughput gains achieved with SP usually come at the expense of device performance. The losses associated with SP metallization include: a) increased minority carrier recombination in the required heavily doped n^+ regions, b) increased shading due to wider grids ($> 100 \mu\text{m}$), and c) lower fill factor (FF) due to poor contact quality. The purpose of this research is to investigate the combination of firing cycle and Ag paste composition to improve the contact quality of screen-printed solar cells to achieve high FF on both mono and multi-crystalline substrates.

Model calculations, Fig. 6.17, show that high fill factors (FF), ≥ 0.78 , can be achieved on screen-printed mono-crystalline silicon solar cells if the following requirements are met; junction depth $\approx 0.5 \mu\text{m}$ on $40 \Omega/\square$ emitter, $J_{02} \approx 10^{-8} \text{ A/cm}^2$, $R_s \leq 0.5 \Omega\text{-cm}^2$ and $R_{sh} \geq 1 \text{ k}\Omega\text{-cm}^2$ [1]. However, for low-cost solar cells, multi-crystalline Si materials are used and the emitter is formed in a belt furnace, resulting in a junction depth of $\sim 0.25\text{-}0.35 \mu\text{m}$. In addition, low quality materials prefer shorter time at high temperature in order to preserve the bulk lifetime. Therefore, a junction depth of $0.5 \mu\text{m}$ as a criterion for achieving high fill factor, as in the case of mono-crystalline silicon, may not be as applicable and cost effective for multi-crystalline silicon cells. Also, defect density, defect non-uniformity, and paste/defect interaction in multi-crystalline

silicon material could further complicate the process, so that even if the 0.5 μm junction depth criterion is met, the FF may still be lower than 0.78. To investigate these issues, a study was conducted on multi-crystalline, CZ and FZ silicon materials using both rapid belt line and conventional furnace processing of the emitter in conjunction with screen-printed contacts. A 40-50 Ω/\square emitter was formed by a 925°C/6 min and 890°C/30 min diffusion, in a lamp heated belt line system and conventional furnace, respectively. The belt line process gave a junction depth of 0.25 μm while the conventional furnace diffusion resulted in a junction depth of 0.5 μm . It should be noted that even though 45 Ω/\square emitter with a junction depth of only 0.25 μm (lamp heated furnace emitter) minimizes the heavy doping effects, it makes the emitter more vulnerable to junction shunting and leakage. That is why it is necessary to use the appropriate paste and the compatible firing cycle in order to achieve high FF on defective materials. On the other hand, for the conventional furnace emitter with junction depth of $\geq 0.5 \mu\text{m}$, the fill factor is expected to be higher due to reduced junction leakage and shunting.

We investigated the effects of two different Ag pastes and two firing cycles on the FF of screen-printed shallow junction solar cells on both multi and mono crystalline silicon. These pastes, (A and B, obtained from Ferro Corporation), had the same frit content but different frit composition. The effect of slow and fast firing cycles was examined on FF using both pastes.

6.4.2. Cell fabrication

A rapid cell fabrication sequence was used which involved emitter formation by spin-on, bake, and 6-min belt line diffusion at 925°C. This resulted in a 40-45 Ω/\square emitter with a junction depth of $\sim 0.25 \mu\text{m}$ and peak (near surface) concentration of 6.4×10^{19} (Fig. 6.18). It

should be noted that a 45 Ω/\square diffusion in the conventional diffusion furnace could take up to 60 minutes from start to finish. After the phosphorus glass removal and DI water rinse, a single layer PECVD SiN antireflection coating was deposited on the front at 300°C. This was followed by screen-printing of Al on the back and a 2 min drive-in at 860°C in the belt furnace to form a very effective Al back surface field. A Ag grid was screen printed on top of the SiN and then fired through the SiN for various times and temperatures to optimize the firing cycle for each paste. Even though 45 Ω/\square emitter with a junction depth of only 0.27 μm minimizes the heavy doping effects, it makes the emitter more vulnerable to junction shunting and leakage. Frit composition or impurity content in the paste can also degrade junction quality if the impurity can migrate to the junction. That is why a compatible firing cycle needs to be established for each paste. Firing cycles involving belt speeds of 15-30 inch/min in conjunction with low firing temperatures (700-800°C) are referred to as slow firing cycles and belt speeds of 60-75 inch/min with firing temperatures of 750-900°C are referred to as spike firing cycles in this study.

6.4.3. Results and Discussion

6.4.3.1. The effect of slow and spike firing cycles on FF for shallow junction cells

Since the primary fill factor loss mechanism associated with SP metallization are contact/series resistance, shunt resistance, and junction leakage (J_{o2} and n), detailed dark I-V measurements were performed to decouple R_s , R_{sh} , J_{o2} and n values by the measured I-V fit to the double exponential model

$$I = I_{o1} \left(e^{\frac{q(V-IR_s)}{kT}} - 1 \right) + I_{o2} \left(e^{\frac{q(V-IR_s)}{nkT}} - 1 \right) + \frac{V - IR_s}{R_{sh}} \quad (1)$$

Change in fill factor was assessed and explained on the basis of above parameters for various pastes, firing cycles and silicon materials used in this study. Figure 6.19 shows fill factors and the corresponding values of R_s , R_{sh} , J_{o2} and n for the two pastes fired under slow and spike firing conditions. These cells were fabricated on 1 Ω -cm mc-Si from Eurosolare. There are several noteworthy features; slow firing condition (730°C with a belt speed of 15 inch/min) gave a very low fill factor (0.689) for paste A primarily due to junction shunting ($R_{sh} \approx 329 \Omega\text{-cm}^2$) and high junction leakage ($J_{o2} \approx 4700 \text{ nA/cm}^2$). This suggests that metal or impurities from this paste are able to get to the depletion region and give rise to generation/recombination centers. On the other hand, the contaminant resistant paste B gave decent fill factor of 0.765 with reasonable series and shunt resistances ($R_s \approx 0.44$ and $R_{sh} \approx 48,000 \Omega\text{-cm}^2$) but slightly higher junction leakage current of 45 nA/cm^2 with an n factor of 2.3. Model calculations were performed to show that $R_s \leq 0.5 \Omega\text{-cm}^2$, $R_{sh} > 1\text{K}\Omega\text{-cm}^2$ and $J_{o2} \leq 10^{-8} \text{ A/cm}^2$ are generally required for very high fill factor in excess of 0.78.

Figure 6.19 shows that a fill factor of ~ 0.76 was also achieved on Euroslare mc-Si cells using paste A when spike firing (850°C with a belt speed of 75 inch/min) is used. However spike firing gives higher series resistance, $1.23 \Omega\text{-cm}^2$ for paste B and $0.65 \Omega\text{-cm}^2$ for paste A. Thus slow firing works well for paste B while spike firing gives better result with paste A.

6.4.3.2. Effect of contact firing temperature on FF of shallow junction cells.

In an effort to achieve even higher fill factor we decided to raise the slow firing temperature gradually from 730 to 770°C using paste B. In this experiment cells were fabricated on Solarex mc-Si, CZ Si from Siemens Solar and a FZ silicon. Figure 6.20 and table 6.8 show

the result of this study. We observed a slight increase in the fill factor for all materials, with the exception of FZ, which remained same, when the firing temperature was raised from 730 to 750°C. This is because series resistance decreased below $0.7 \Omega\text{-cm}^2$ and junction leakage improved slightly. It was found that for single crystals, fill factor value peaked at a firing temperature of 760°C while the peak temperature for mc-Si was 750°C. Dark I-V analysis showed that, beyond the peak temperature, fill factor begins to degrade due to high junction leakage current. This suggests that mc-Si are somewhat more vulnerable to junction leakage due to the defect/paste interaction. Therefore firing cycle should be optimized for each mc-Si due to the difference in the defect structure.

Figure 6.20 and table 6.8 show that in this study a best fill factor value of 0.77 was achieved on mc-Si cells with efficiency of $\sim 15\%$, while single crystal cells gave a fill factor of 0.79 with an efficiency of 16.5%. These fill factors are much higher than what is currently achieved on industrial cells. In addition, the combination of belt line diffusions and screen-printed contact offers a low-cost, high throughput, manufacturable technology. Further understanding and optimization can lead to even higher fill factor and efficiencies, reducing the gap between the screen-printed and buried or photolithography contact technologies.

Table 6.20: The Electrical output parameters for the screen-printed solar cells on different materials.

Material	Slx1	SCZ1	FZ1	Slx2	SCZ2	FZ2
Fill Factor	0.733	0.705	0.771	0.76	0.767	0.771
R_s (ohm-cm ²)	0.83	0.76	0.48	0.66	0.5	0.43
R_{sh} (ohm-cm ²)	6292	4590	44391	14985	59643	67557
J_{o2} (nA/cm ²)	612	1268	123	154	117	160
n	2.3	2.5	2.2	2.2	2.2	2.3
Material	Slx3	SCZ3	FZ3	Slx4	SCZ4	FZ4
Fill Factor	0.752	0.787	0.786	0.717	0.768	0.773
R_s (ohm-cm ²)	0.44	0.37	0.37	0.55	0.49	0.42
R_{sh} (ohm-cm ²)	2843	4668	1616	1160	60000	68789
J_{o2} (nA/cm ²)	832	43	8.2	4956	89	86
n	2.6	2.2	1.8	3.0	2.1	2.1

6.4.3.3 Effect of contact firing temperature on the FF of deep junction cells

In order to assess the impact of paste/defect interaction on FF in multi-crystalline silicon, the conventional furnace was used to form the emitter at 890°C for 30 minutes. This resulted in 45 Ω/\square emitter with a junction depth of $\sim 0.5 \mu\text{m}$ and peak (near surface) concentration of 4×10^{19} . After the diffusion, the cells were fabricated by the same process sequence outlined in section 2. Paste B was used and the slow firing temperature was gradually raised from 730°C to 770°C. The idea was that deeper junction may permit higher firing temperature, according to Mertens et al [2], without excessive junction leakage which may be caused by paste/defect interaction at the junction.

Figure 6.21 shows the results of this study. We observed a slight increase in the fill factor of mc-Si cell when the firing temperature is raised from 730°C to 770°C. Firing time was maintained at 30 seconds. It was interesting to note that the fill factor value peaked at a firing temperature of 770°C for the deep junction while 750°C was the peak for the shallow junction

devices. The dark I-V analysis showed that before the peak temperature fill factor is poor due to high junction leakage current (J_{02}). This suggests that for mc-Si, even though the junction is deep, the low fill factor can result from increased junction leakage due to paste/defect interaction.

6.4.4. Conclusion

The understanding and optimization of SP paste, firing cycle, and loss mechanisms has led to the achievement of fill factors approaching 0.77 and 0.79 on mc-Si and single crystal silicon, respectively, on a $45 \Omega/\square$ rapidly formed belt line emitter. It was found that, for mc-Si, even the deep emitter of $\sim 0.5 \mu\text{m}$ does not guarantee high fill factor because of the paste/defect interaction which tend to increase the junction leakage current. However, it was observed that the deep junction could stand higher temperature firing cycle than the shallow junction. The shallow junction FF peaked at 750°C firing temperature, while the FF peaked at 770°C for deep junction devices for a firing time of 30 seconds. Even though we have demonstrated high FF for SP cells, further research on paste composition and firing cycles is necessary to achieve FF in excess of 0.78 repeatedly on mc-Si.

6.4.5 Reference

1. A. Rohatgi, S. Narasimha, A. Ebong and P. Doshi, "Understanding and implementation of rapid thermal technologies for high efficiency silicon solar cells" IEEE Transaction on Electron Devices 46 (10) 1970-1977 (1999).
2. R. Metens, M. Eyckmans, G. Cheek, M. Honore, R. Van Overstraeten and L. Frisson, in Conf. Proc., IEEE PVSC, 1347, (1984).

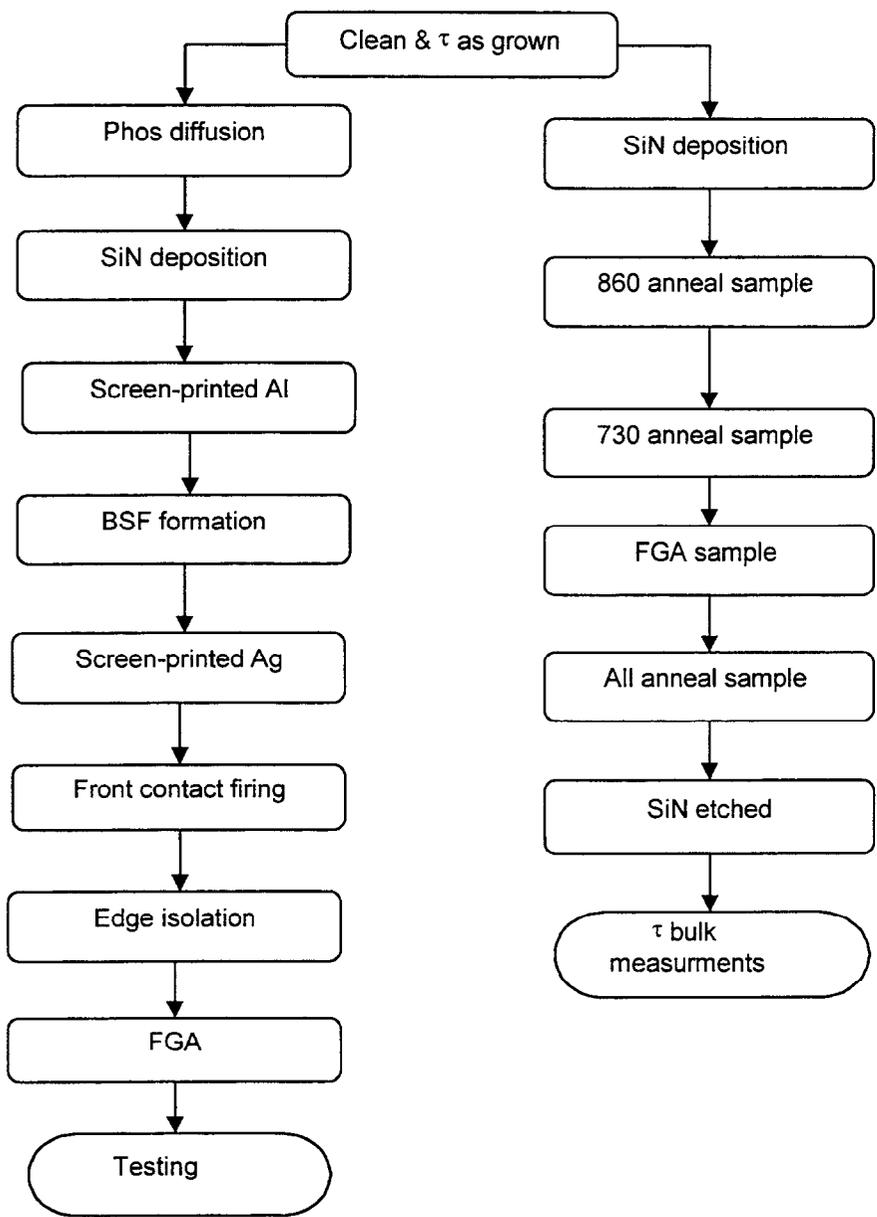


Fig. 6.1: Process sequence for belt line screen-printed silicon solar cell fabrication and lifetime studies.

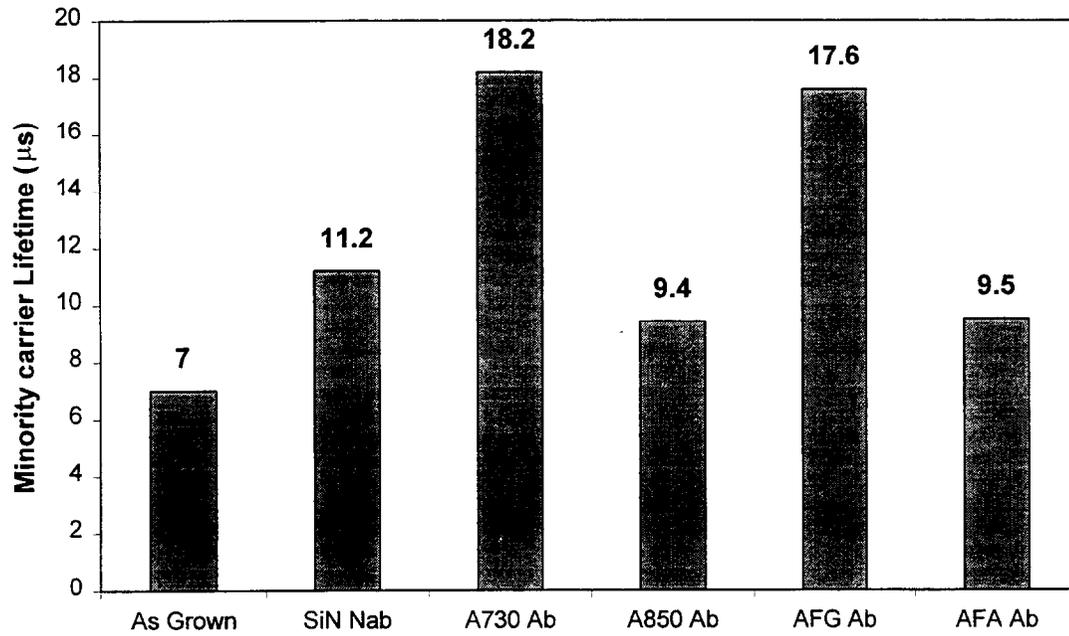
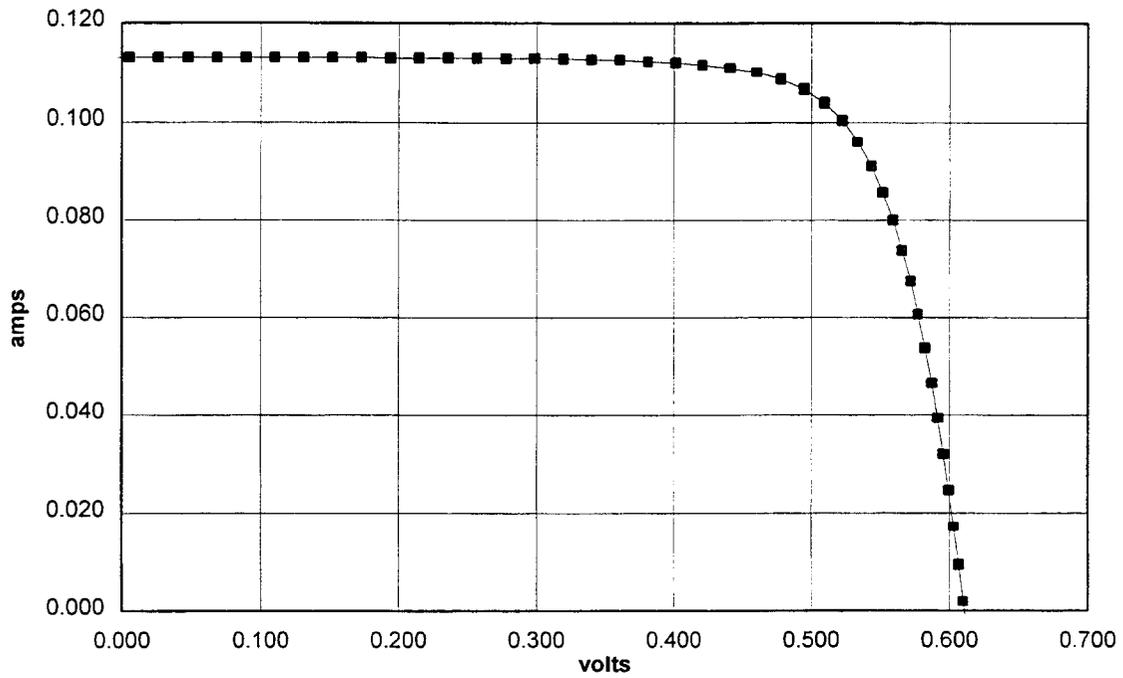


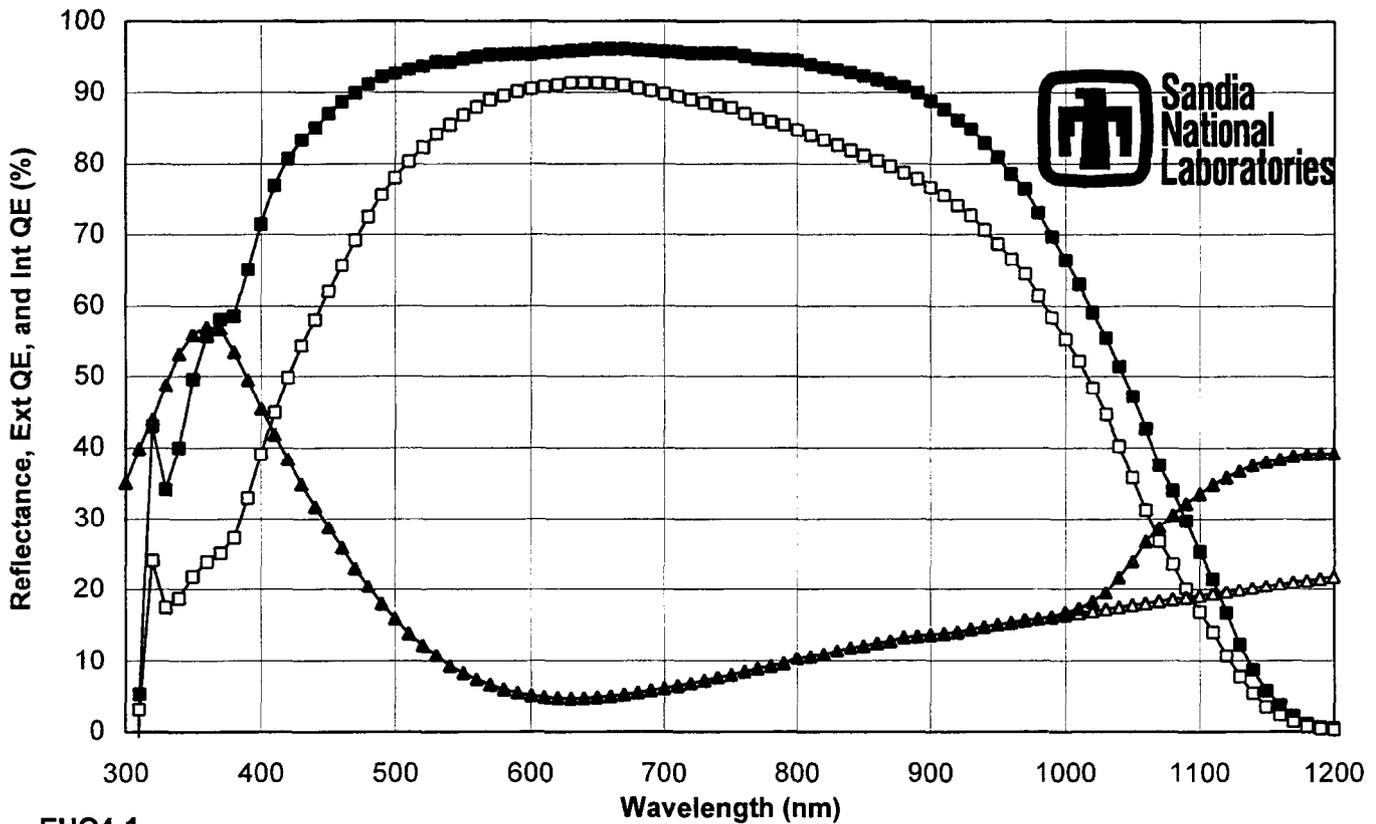
Figure 6.2: SiN-induced hydrogenation of cast (Euroslare) mc-Si (Note N_{ab} – no anneal bulk lifetime; A_b – bulk lifetime after the prescribed heat treatment).



03/03/99 12:50 PM 25.0 °C 3.58 cm² 31.58 J_{sc}(mA/cm²) 0.768 FF AM1.5G
EUO4-1 0.9951 M* 610.4 V_{oc}(mV) 0.113 I_{sc}(A) 14.80 % Eff ONE SUN
1.0000 S* 503.5 V_{mp}(mV) 0.105 I_{mp}(A)

Used mask #007

Figure 6.3: Lighted I-V curve for lamp heated belt line screen-printed multi-crystalline (EUO4-1) solar cell.



EUO4-1

Spectral Response: x:\ruby\asr\99028-07.s01 Reflectance: x:\ruby\rfi\99028-07.csv

Current Density at 1 kW/m2 (mA/cm2): 31.9 (Global), 31.7 (Direct), 27.9 (Space)

Weighted Front Reflectance (%): 12.8 (Global), 12.2 (Direct), 13.4 (Space)

Figure 6.4: Spectral response of the lamp heated belt line screen-printed multi-crystalline (EUO4-1) silicon solar cell.

Dark JV Analysis: Measured and Simulated JV Responses

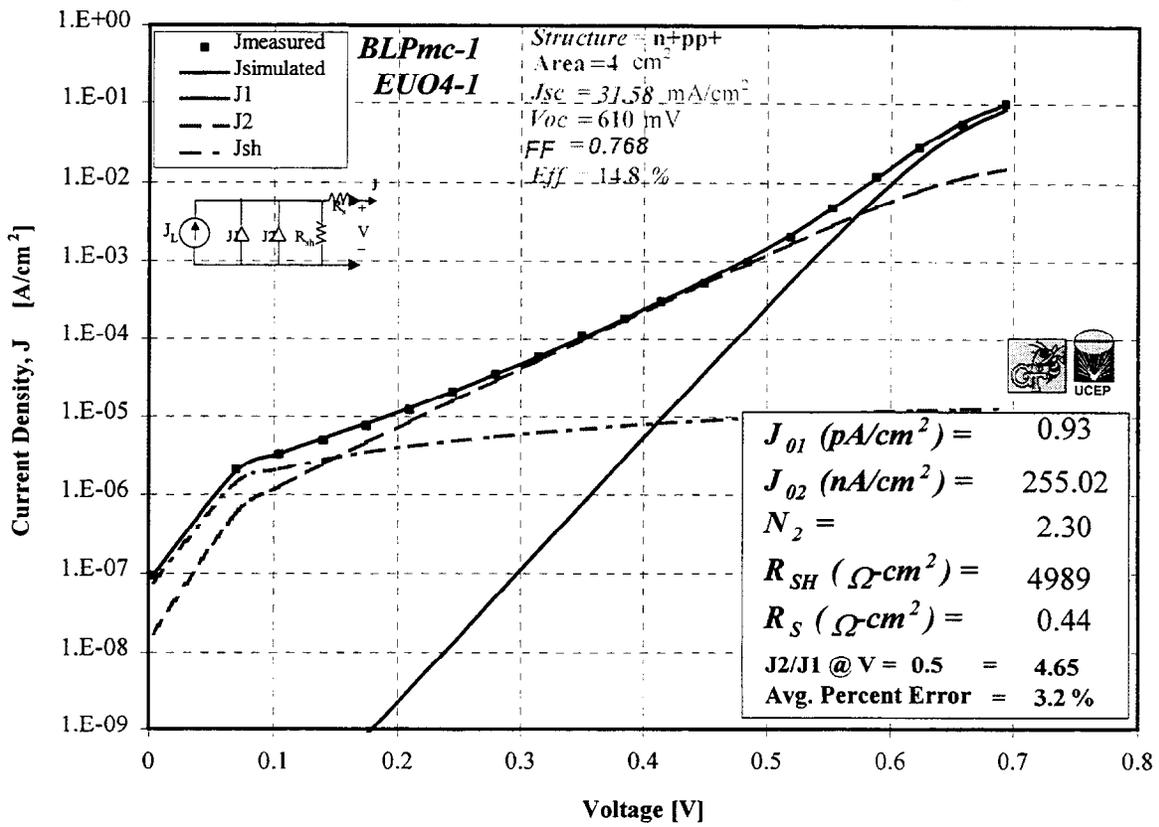


Figure 6.5: Measured and simulated J-V response for belt line screen-printed multi-crystalline (EUO4-1) silicon solar cell.

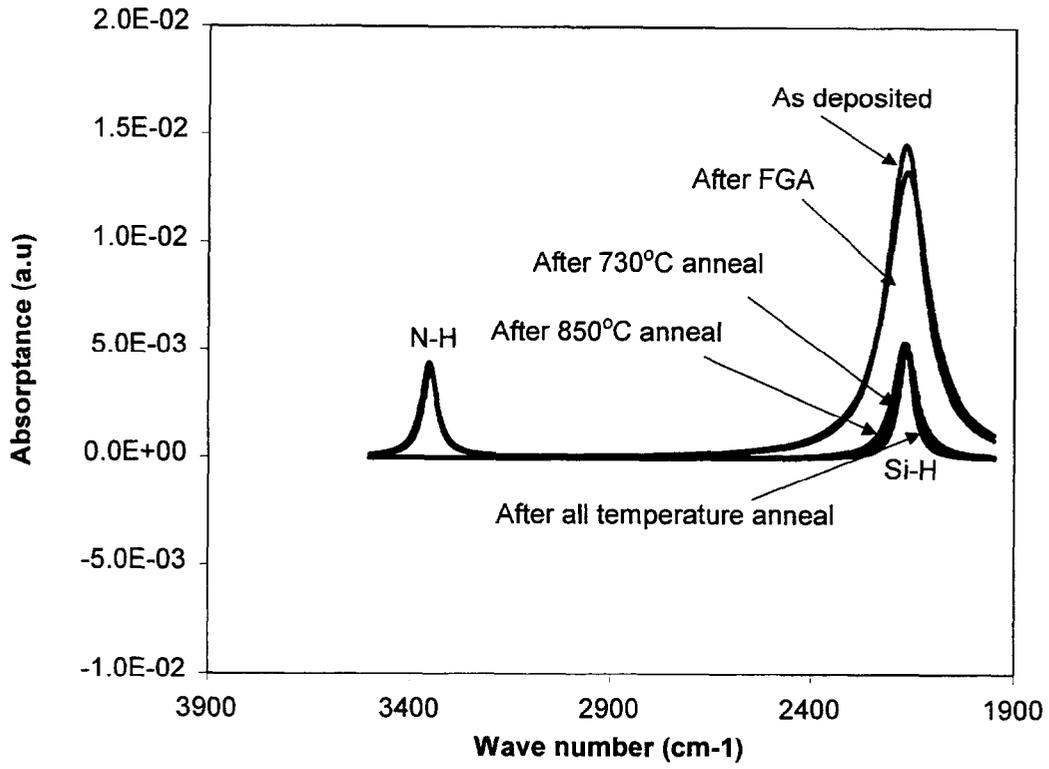


Fig. 6.6: Hydrogen concentration in SiN film deposited on multi-crystalline silicon after each high temperature anneal.

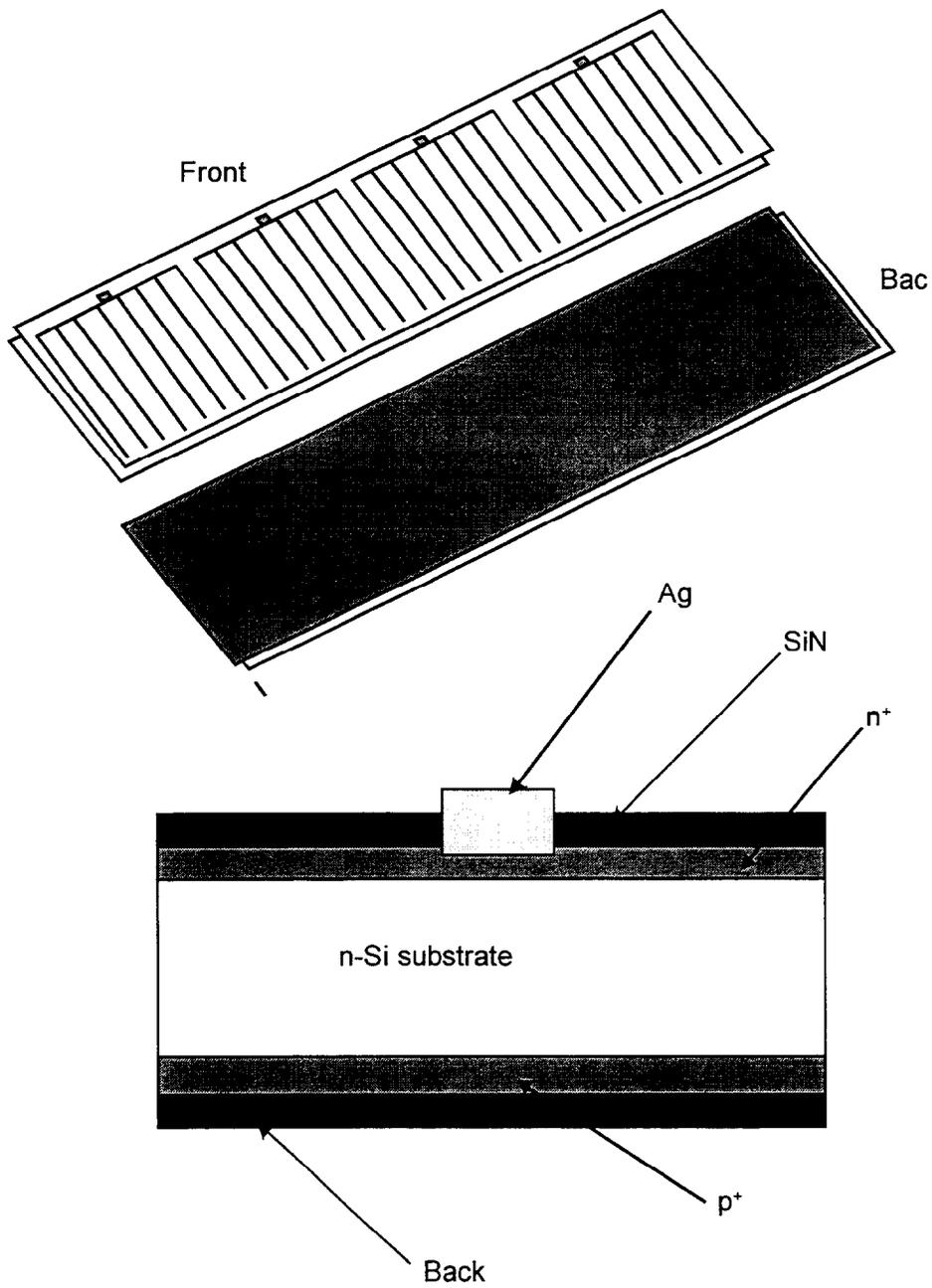


Fig. 6.7: Structure of aluminum alloy back junction silicon solar cell

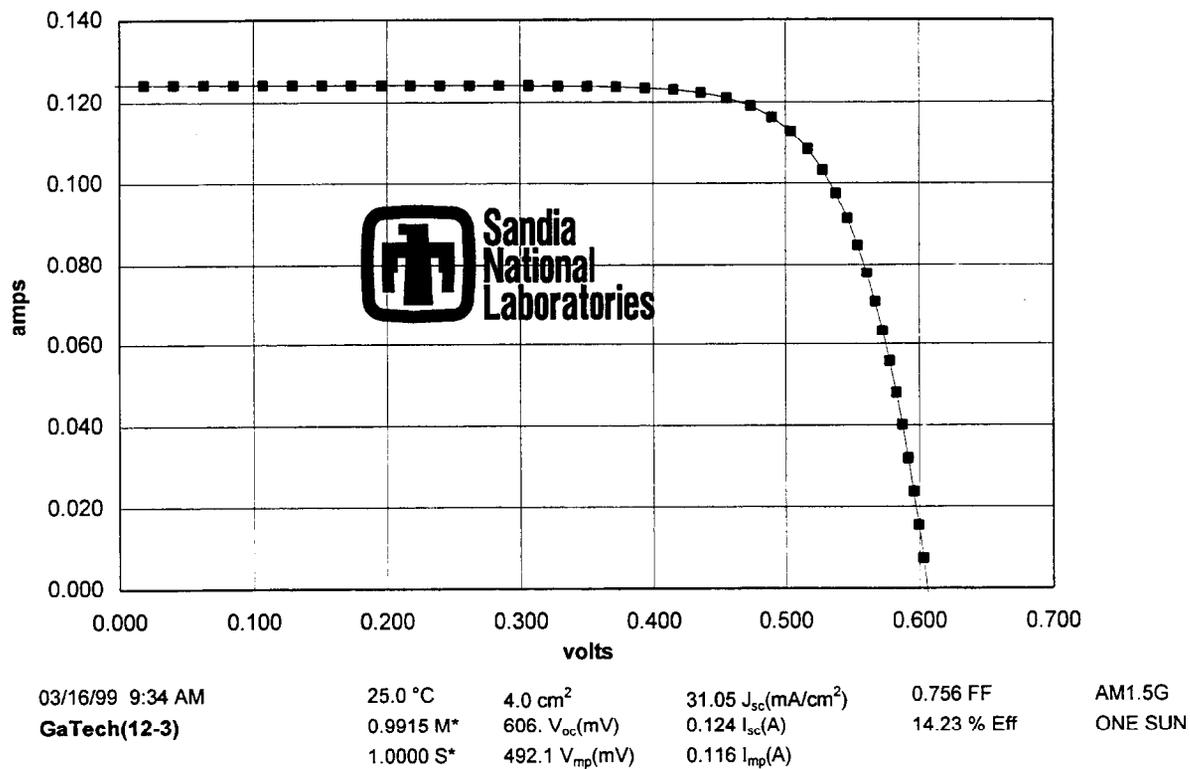


Fig. 6.8: Lighted I-V data for n⁺np⁺ aluminum alloy back junction solar cell, 4 cm² in area. Cell fabricated from a dendritic web silicon substrate (100 μm thick, antimony-doped to 20 Ω-cm).

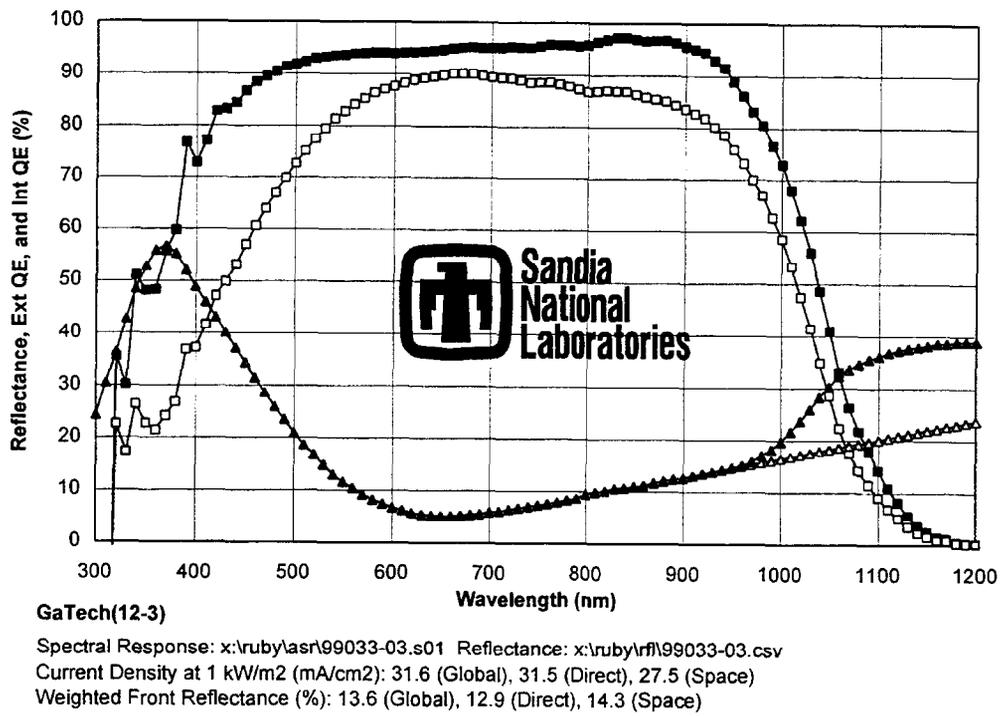


Fig. 6.9: Measured spectral data for 14.2% aluminum alloy back junction solar cell fabricated from 100 μm thick dendritic web silicon.

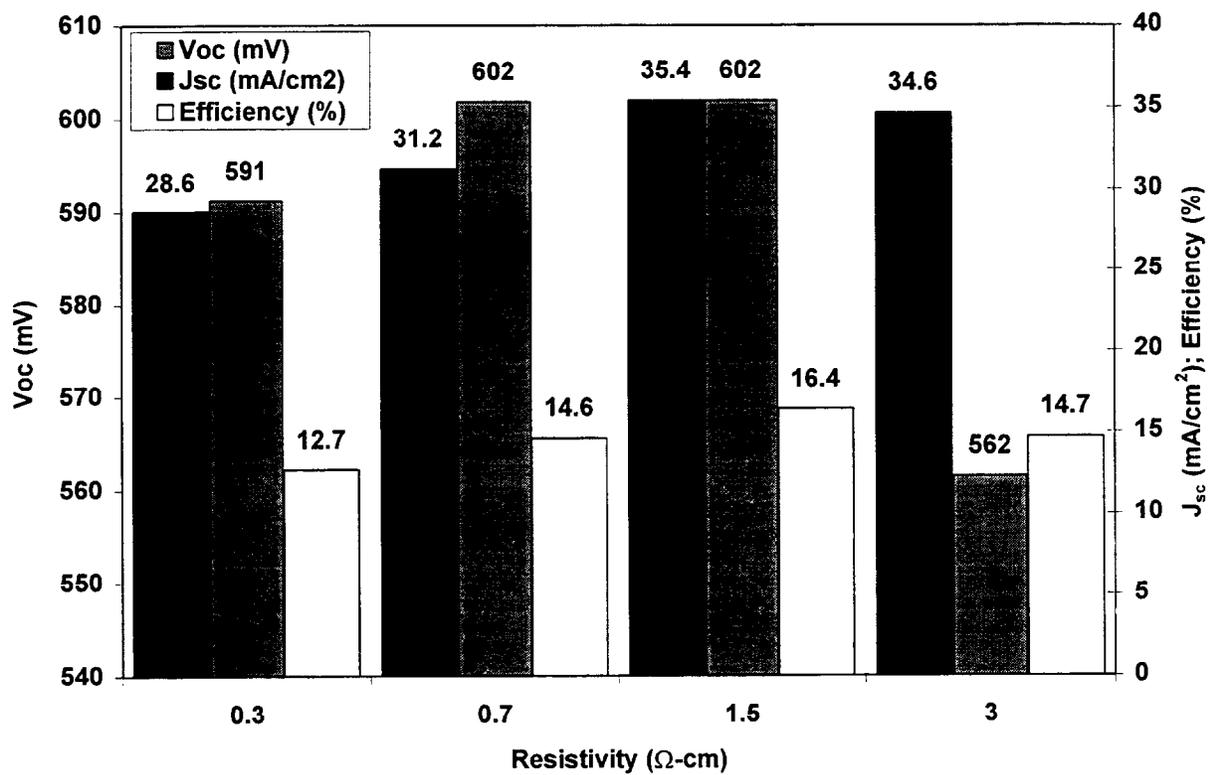


Fig. 6.10: Doping dependence of string ribbon cell efficiency.

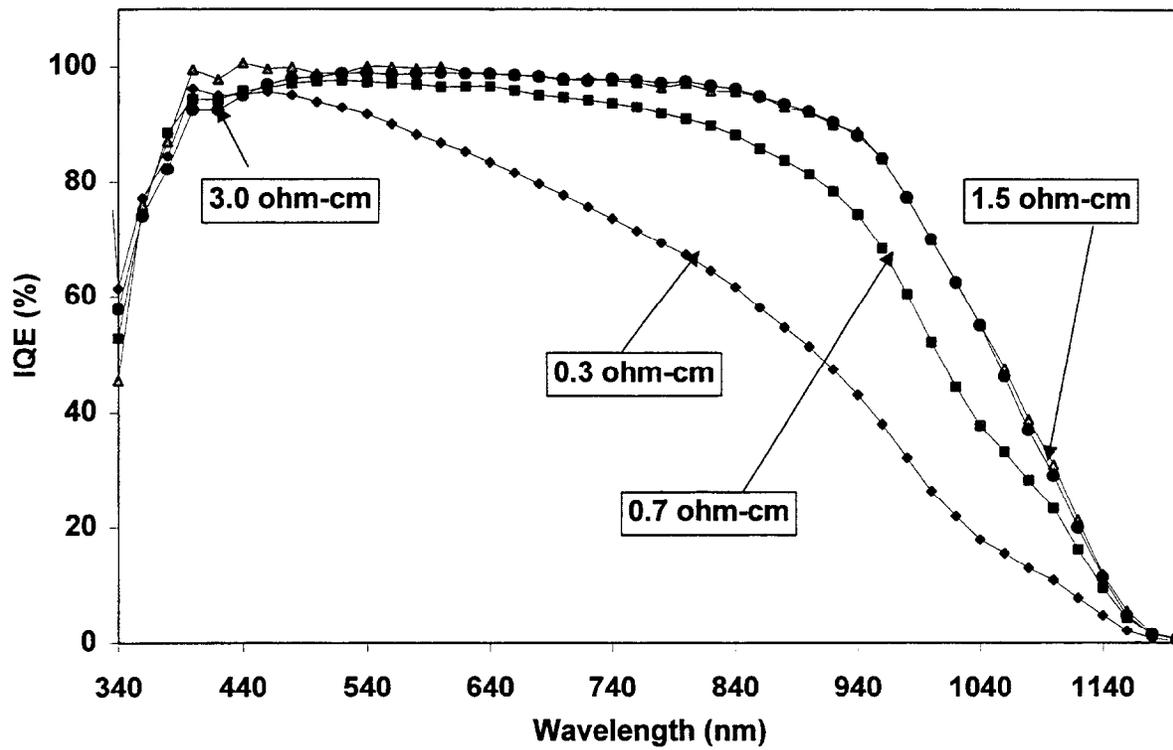
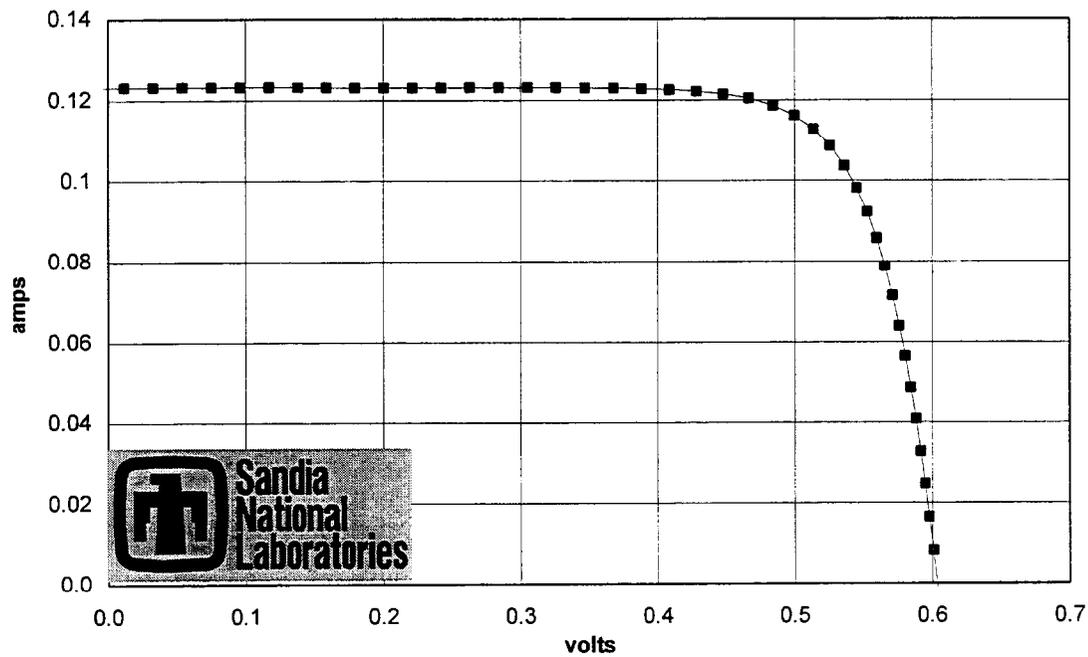


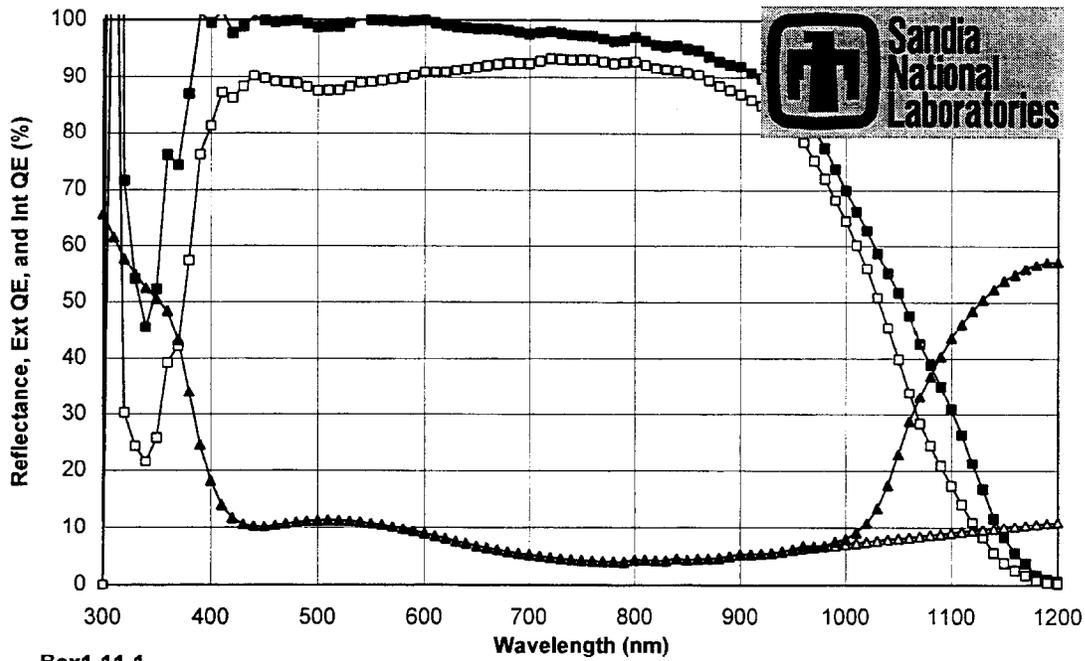
Fig. 6.11: Resistivity effect on string ribbon IQE.



07/06/99 9:16 AM 24.9 °C 3.58 cm² 34.41 J_{sc}(mA/cm²) 0.781 FF AM1.5G
Box1-11-1 1.0002 M* 603.5 V_{oc}(mV) 0.123 I_{sc}(A) 16.22 % Eff ONE SUN
 1.0000 S* 502. V_{mp}(mV) 0.116 I_{mp}(A)

masked.

Fig. 6.12: Light I-V measurements for the 16.2% cell



Box1-11-1

Spectral Response: c:\iqe-win\99075-03.s01 Reflectance: c:\iqe-win\99075-03.csv

Current Density at 1 kW/m2 (mA/cm2): 35.4 (Global), 35.0 (Direct), 31.4 (Space)

Weighted Front Reflectance (%): 8.1 (Global), 7.6 (Direct), 9.2 (Space)

Fig. 6.13: Spectral response data for the 16.2% string ribbon silicon solar cell.

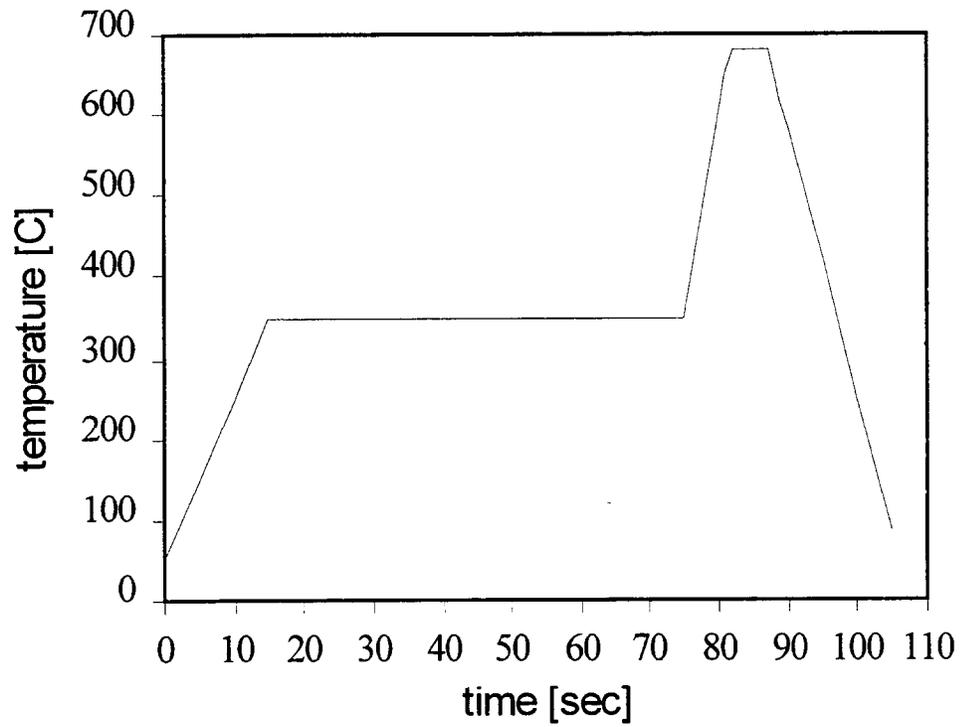


Figure 6.14. The temperature profile of RTP co-firing that produced 14.12 % efficiency on large area EFG silicon solar cell.

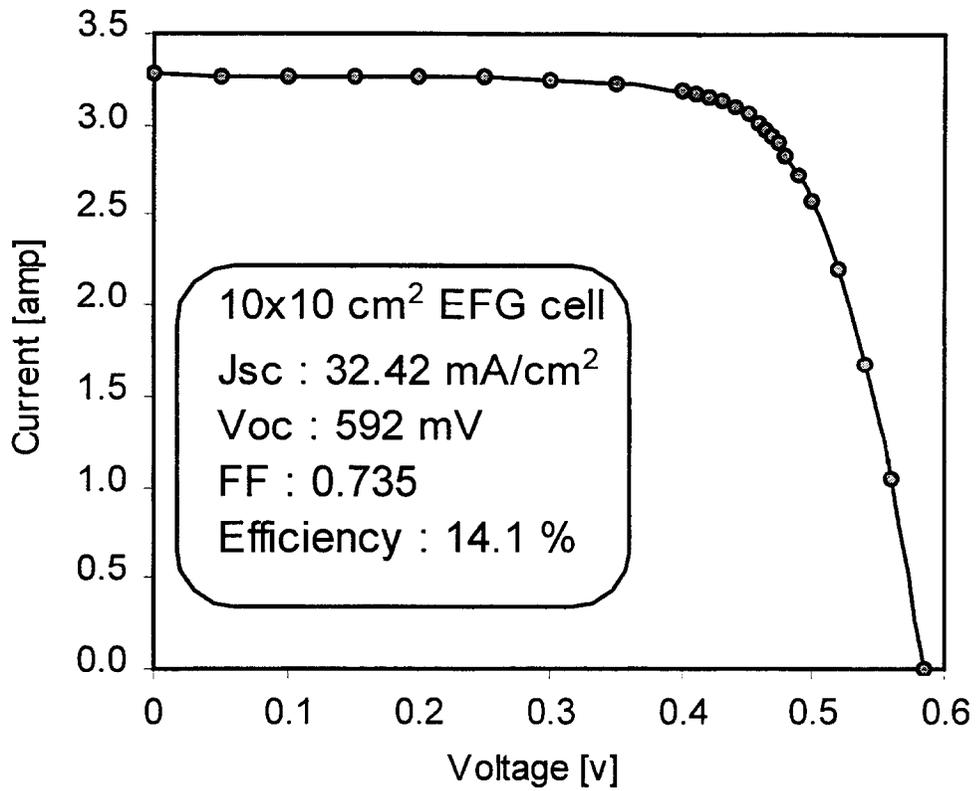


Figure 6.15. Lighted I-V curve for the 14.12 % cell.

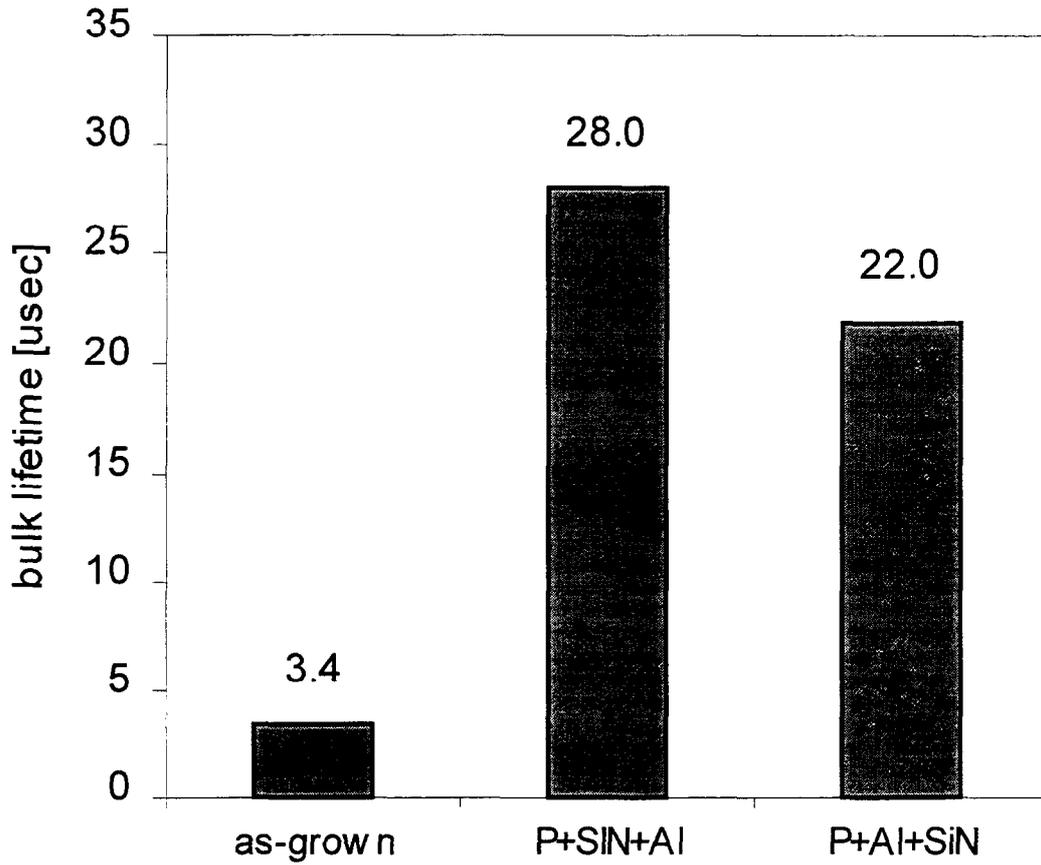


Figure 6.16. Measured minority carrier bulk lifetimes for co-firing (P+SiN+Al) and sequential (P+Al+SiN) firing in a conveyor lamp heated belt furnace.

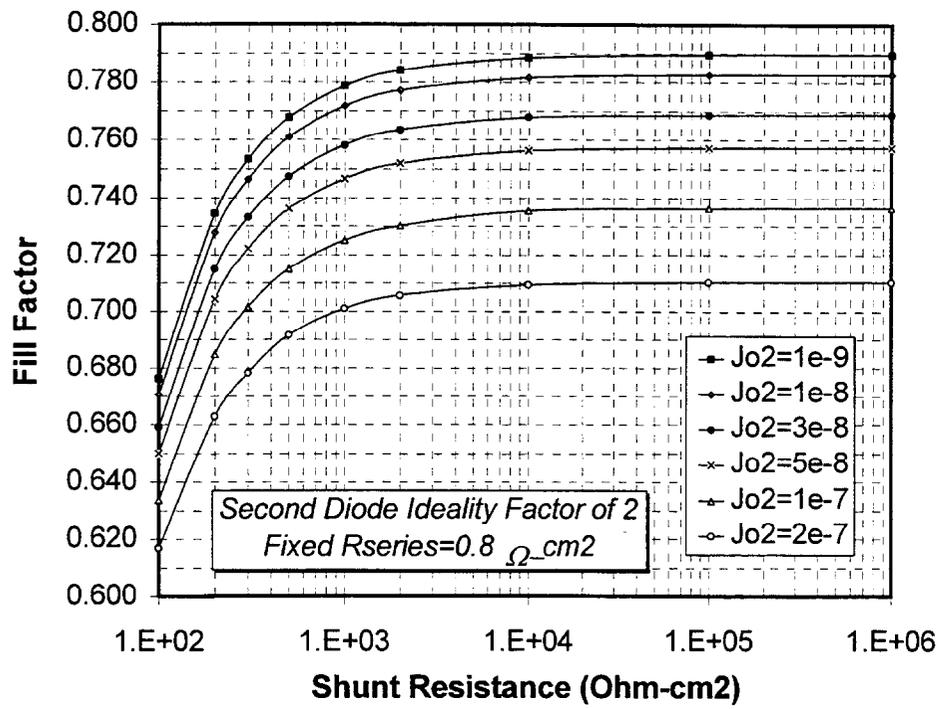


Fig. 6.17: The effect of R_{sh} and J_{o2} on FF for 4 cm^2 cells

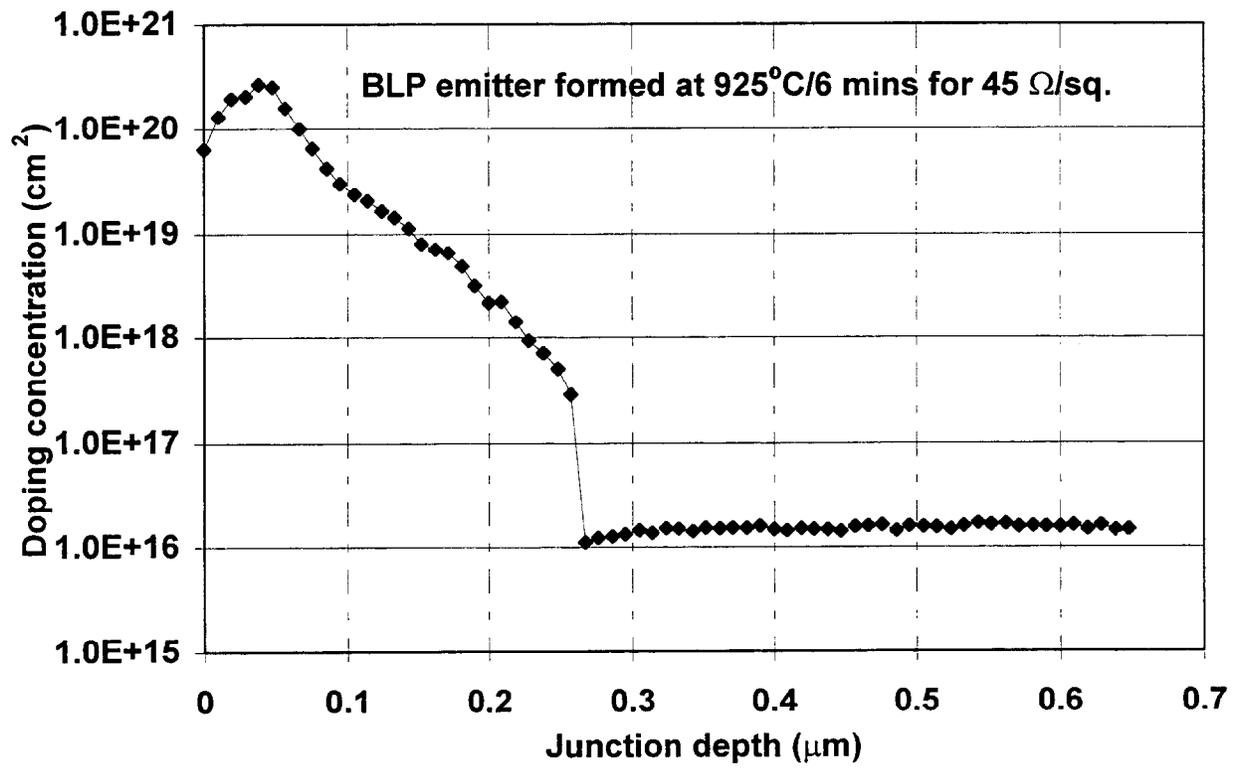


Fig. 6.18: BLP emitter profile deposited at 925°C for 6 minutes.

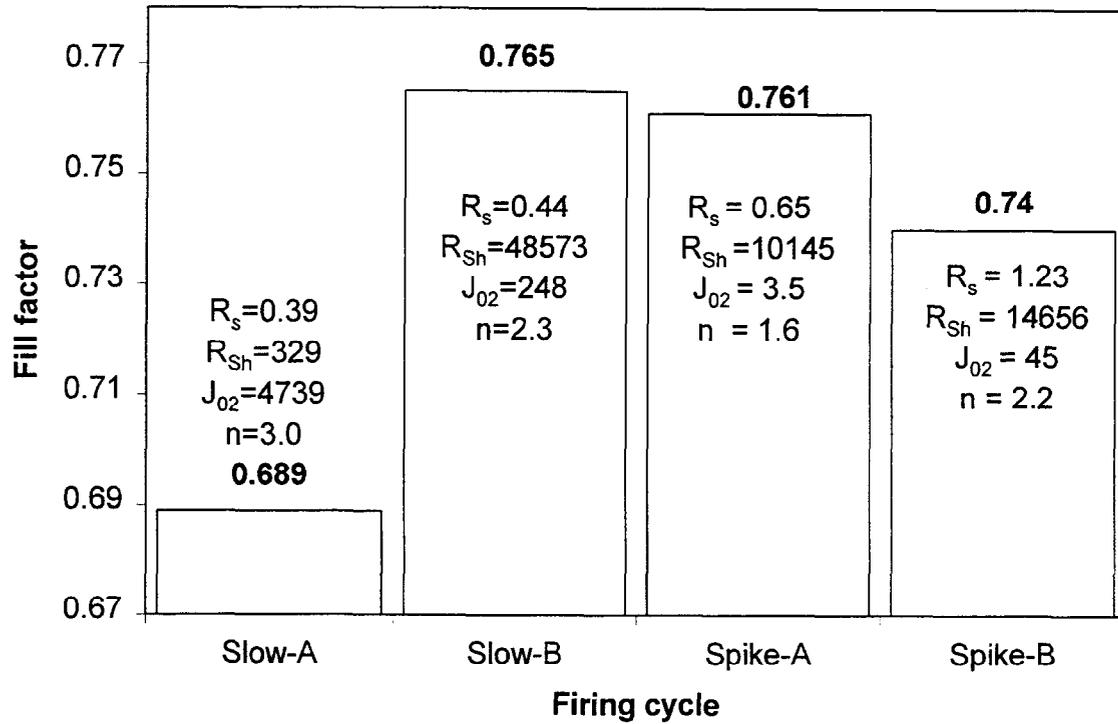
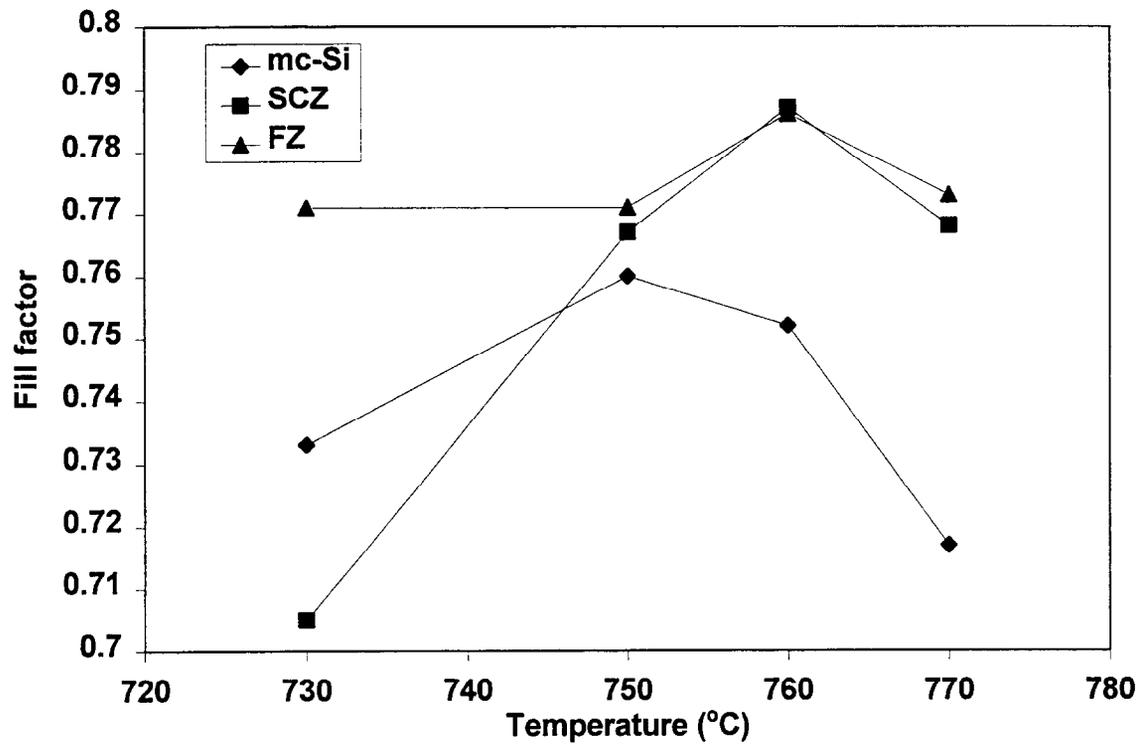


Fig. 6.19: Effect of paste and firing cycle on fill factor of screen-printed solar cells on mc-Si with 0.25 μm deep emitter



6.20: Effect of temperature cycle and paste B on fill factor.

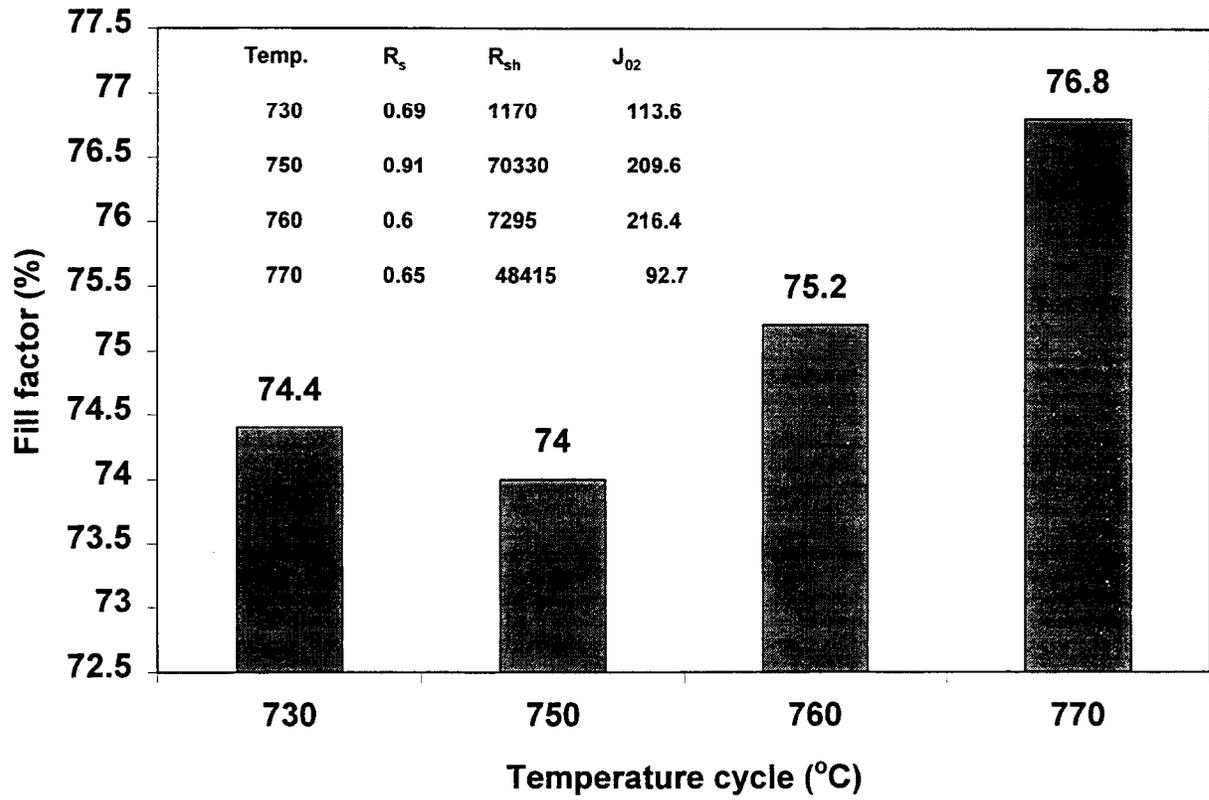


Fig. 6.21: Effect of contact firing temperature on fill factor of 0.5 μm deep emitters formed by CFP.

CHAPTER VII

A NOVEL PROCESSING TECHNOLOGY “STAR” FOR HIGH- EFFICIENCY SILICON SOLAR CELLS

7.0 A Novel Processing Technology “*STAR*” for High-Efficiency Silicon Solar Cells

7.1 Introduction.

For widespread implementation of silicon photovoltaics, the cost as measured in dollars/watt must be reduced from the current level of \$4/Watt to about \$1/Watt to be competitive with fossil fuels [1]. Of the many components contained in a silicon solar cell module, the processed solar cells account for nearly 70% of the total cost. Thus it is imperative to reduce solar cell material and processing costs, while improving device performance to achieve a cost/Watt competitive with conventional energy sources. A typical n^+pp^+ silicon solar cell fabrication process incorporating a phosphorus emitter, boron (or aluminum) Back Surface Field (BSF), and thermal oxide surface passivation, requires anywhere from 2-5 high temperature furnace steps for the growth of masking and passivating oxides and dopant diffusions. Each high temperature step adds cost in terms of processing time and resources. In this paper we present a novel simultaneous boron and phosphorus diffusion technique capable of producing simple high-efficiency n^+pp^+ silicon solar cells in one furnace step. This process incorporates many significant efficiency -enhancing features, and is completely compatible with the current PV manufacturing technology base.

Historically, the simultaneous diffusion of boron and phosphorus in silicon has been implemented in several ways. For example, using boron and phosphorus Spin-On Dopants (SOD) films, boron and phosphorus can be simultaneously diffused in a rapid thermal processor [2] or in a conventional diffusion furnace [3], without significant cross doping. The drawbacks of this approach are that the wafers are left with a thick diffusion glass which in most cases must be removed in order to apply an effective antireflection coating, thus eliminating any potential

for *in-situ* oxide surface passivation. In addition, our experience has been that it is often difficult to obtain high minority carrier lifetimes in processed wafers using commercially available boron spin-on dopants, due to residual impurities in the films. An alternative approach towards simultaneous boron and phosphorus diffusion is to deposit B and P-doped oxides on opposite sides of a silicon wafer using Chemical Vapor Deposition (CVD) techniques [4], prior to a high temperature diffusion. A major drawback of using CVD-doped oxides in a solar cell fabrication line is the costs associated operating and maintaining a CVD system, which typically uses the highly toxic gasses PH_3 , B_2H_6 and SiH_4 . While this process has been used to produce high performance solar cells [4], again one is still left with a thick diffusion glass which needs to be removed and a passivating oxide re-grown, requiring an additional high temperature cycle.

The approach used in our work is to simultaneously diffuse phosphorus and boron in a conventional diffusion furnace using solid doping sources containing extremely low concentrations of boron and phosphorus oxides. The solid doping sources are fabricated from dummy silicon wafers coated with phosphorus and boron spin-on dopants, containing controlled amounts of the volatile dopant species. It is shown in this paper that by using *limited* solid doping sources fabricated in this way, in one furnace step one can independently tailor the phosphorus and boron diffusion profiles to be compatible with high efficiency solar cell designs. It is also shown that by using this approach the resulting diffusion glass is extremely thin (~ 60 Å), allowing for the growth of a high quality *in-situ* thermal oxide for surface passivation, without appreciably increasing the device reflectance. A model is presented to describe the dependence of sheet resistance on the dopant source concentration, and is used to explain the observed sheet resistance dependence on surface morphology. In addition to demonstrating flexibility in process design as well as *in-situ* oxide surface passivation, a powerful

contamination filtering action is observed in the case of boron diffusions. This filtering action is used to obtain extremely high bulk minority carrier lifetimes in excess of 1 ms for wafers facing a boron SOD-coated source wafer, which in itself had a processed lifetime as low as 6 μ s after a typical diffusion/oxidation cycle. Finally, we present typical results for devices fabricated from the described simultaneous diffusion and *in-situ* oxidation process, where 19-20% efficient solar cells are produced in one furnace step.

This paper is organized as follows: In the following section we present the experimental procedure for the simultaneous boron and phosphorus diffusion technique. Next, a model is presented which describes the reaction pathways for the limited diffusion sources developed in this work. This model is used to explain two unique attributes of this process dealing with *in-situ* oxide surface passivation and the dependence of sheet resistance on surface morphology. Next, we demonstrate a powerful impurity filtering action obtained through implementing a separate source/sample arrangement, resulting in high minority carrier lifetimes from a relatively impure boron spin-on dopant source. Finally we apply this knowledge to the fabrication of silicon solar cells with resulting conversion efficiencies in the 19-20% range, demonstrating the potential of this novel processing technique to produce simple, high efficiency n^+pp^+ silicon solar cells in one high-temperature step.

7.2 Experimental

Figure 7.1 shows the furnace stacking arrangement for the described boron and phosphorus simultaneous diffusion technique. The boron and phosphorus solid doping sources, B and P respectively, are interleaved with the solar cell sample wafers, S, with the back side of the solar cell wafers facing the boron sources and the front side facing the phosphorus sources.

The boron and phosphorus sources are fabricated from 100 mm diameter dummy silicon wafers, coated with 1-2 ml of phosphorus or boron spin-on dopant film containing a controlled concentration of the volatile dopant compound. The phosphorus and boron SOD's used in this work were supplied by Filmtronics Incorporated and were found to be of consistently high quality. After applying the SOD to the sources, the wafers were spun on a clean delrin plastic chuck and baked on a clean quartz sheet on top of a 150 °C hotplate for 3 min (boron) or for 10 min (phosphorus), and loaded directly into the furnace. A typical simultaneous diffusion cycle is to load the wafers at 800 °C in N₂, ramp up to 900-1000 °C and diffuse in N₂ or Ar₂ for 60 minutes. If an *in-situ* oxide is required, a low O₂ flow is added to the N₂ ambient for 5-60 min depending on the desired oxide thickness, and the furnace ramped down to 700 °C at a rate of 4 °C /min, and the wafers pulled in a high N₂ flow. The source wafers are recycled (as sources) after each diffusion cycle, following a brief dip in 10% HF and re-application the phosphorus or boron SOD. It should be noted that the source wafers are depleted of the dopant compounds after one diffusion cycle, and need to be re-fabricated as doping sources prior to each diffusion step. This is not a significant drawback of this technique since the source wafers can be fabricated by high throughput techniques such as spray coating or dip-coating full wafer cassettes. As shown below, the limited nature of the solid doping sources enables several high efficiency features to be realized in one furnace step using this simultaneous diffusion technique. It is noted that this process is similar to a previous approach [5] in which we had fabricated the boron and phosphorus sources by growing a doped oxide on the source wafers using POCl₃ and BBr₃.

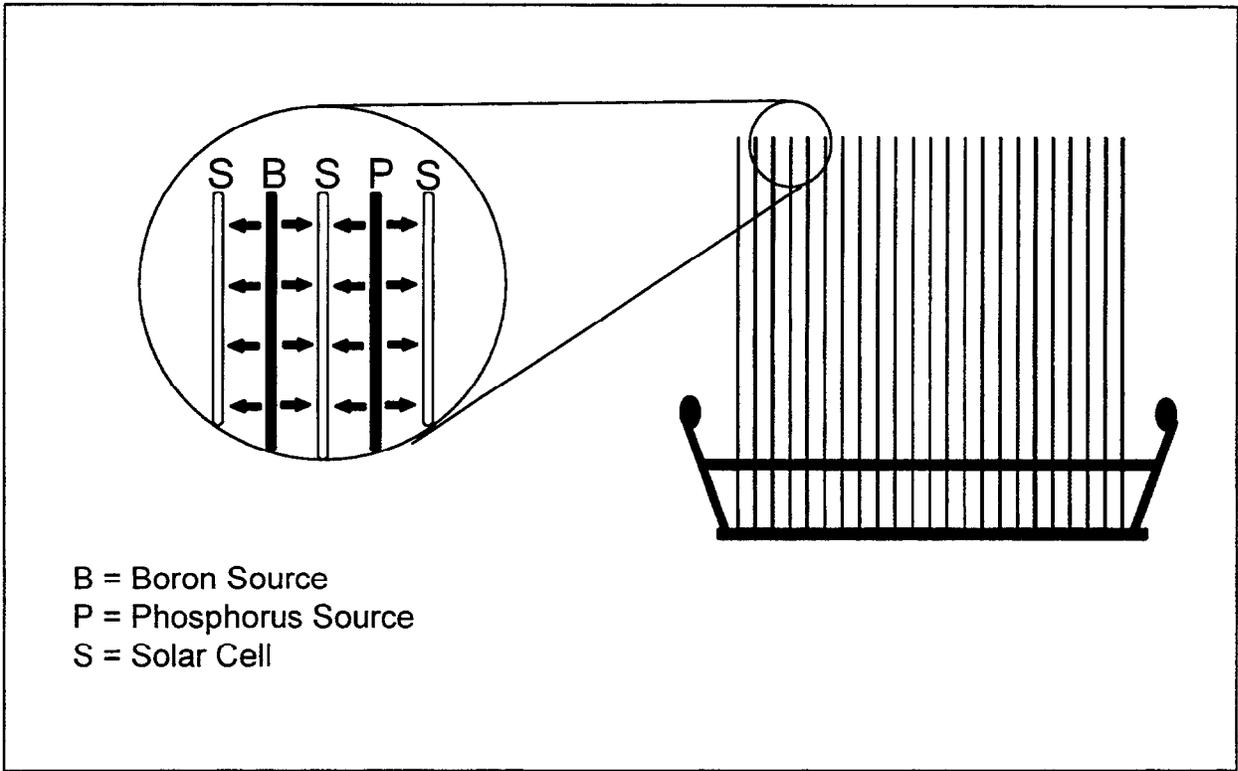


Figure 7.1. Furnace stacking arrangement, with the solar cell wafers (S) interleaved with the Boron (B) and Phosphorus (P) solid sources developed in this work.

From a practical point of view the implementation of this process using SOD's has several advantages over POCl_3 and BBr_3 , such as the elimination of separate POCl_3 and BBr_3 diffusion furnaces and the precautions associated with handling these pyrophoric chemicals, and the ability to reproducibly obtain high minority carrier lifetimes using a boron SOD in place of BBr_3 to fabricate the boron sources.

7.3 Results and Discussion

7.3.1 Process Flexibility

To simultaneously form the emitter and BSF diffusions for a high efficiency cell design, it is important to have the flexibility of independently tailoring the resulting boron and phosphorus diffusion profiles for a given thermal budget. Figure 7.2 shows the flexibility in diffused sheet resistance (ρ_s) as a result of tailoring the concentration of dopant compounds in the SOD films applied to the source wafers. Measurements were made on 100 mm diameter, 500-1000 $\Omega\text{-cm}$ n-type, (100) float zone silicon wafers, with the error bars representing 1 standard deviation for 16 measurements across a 49 cm^2 area. It is noted that all the samples in figure 7.2 were diffused using the same 1000 $^\circ\text{C}/60$ min diffusion cycle, with the only variable being the concentration of dopant compounds in the SOD's applied to the source wafers. The dopant compound in the phosphorus SOD is P_2O_5 , which was varied to obtain a wide range of diffusion profiles ranging from 17 to 378 Ω/\square . The boron SOD, sold under the product name Boron-A, is made from a proprietary boron polymer dissolved in cyclohexane, and was diluted by the manufacturer using semiconductor grade toluene. The % listed on the top x-axis is the % by volume of the Boron-A SOD sold by Filmtronics.

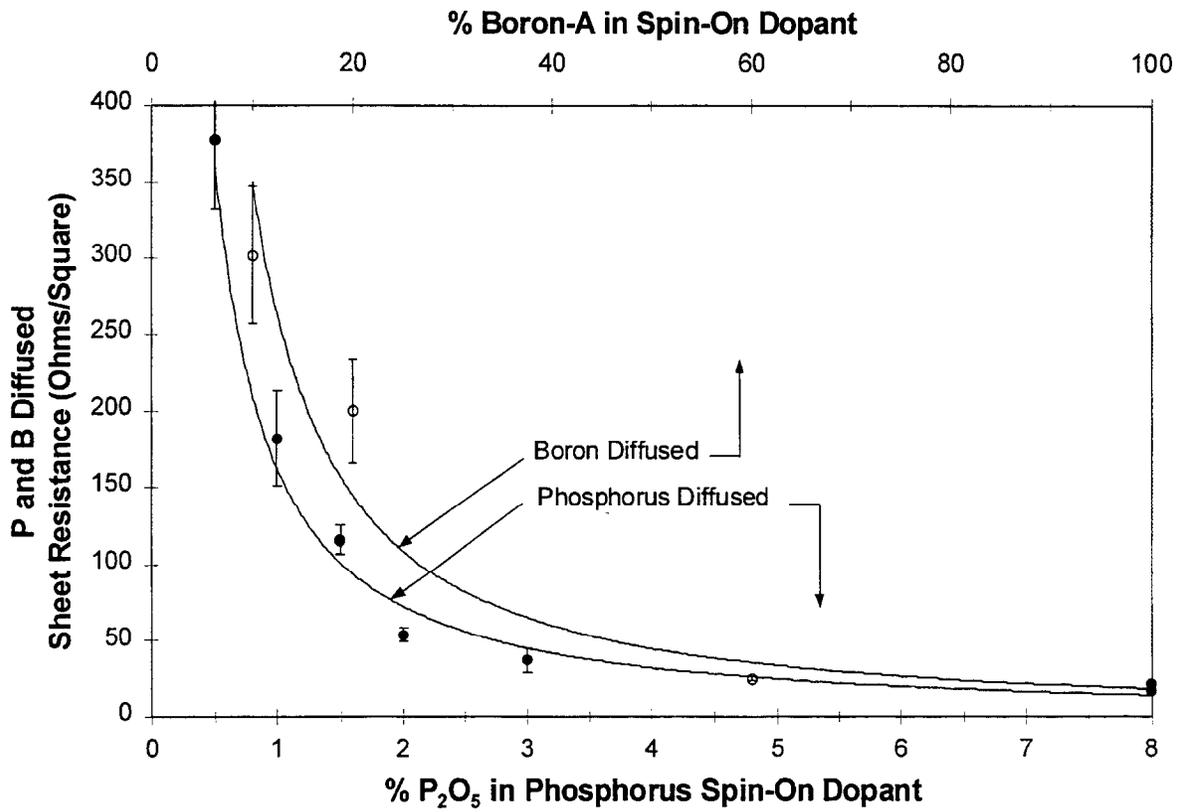


Figure 7.2. Dependence of phosphorus and boron-diffused sheet resistance on source fabrication conditions for a 1000 °C/60 min process. The phosphorus sources were tailored by adjusting the concentration of P₂O₅ in the SOD film, while the boron sources were tailored by diluting the 100% Boron-A SOD film with toluene.

As was the case with phosphorus, a wide range of boron diffusions, ranging from 22 to 302 Ω/\square can be obtained by diluting the boron SOD applied to the source wafers. Thus based on the data in figure 7.2, one can easily obtain a boron BSF having a low sheet resistance in the 20 Ω/\square range, and a phosphorus emitter compatible with either screen printing metallization requiring $\sim 50 \Omega/\square$ or photolithography-based metallization where $\sim 85 \Omega/\square$ is optimal, using a 1000 °C 60 min diffusion cycle.

The dependence of sample sheet resistance on the concentration of dopants on the source wafers observed in figure 7.2 is quite different than what is observed with conventional solid doping sources. Commercially available solid sources, such as silicon pyrophosphate (SiP_2O_7)-based solid sources [6,7] and boron nitride solid sources [8] are designed to be used for hundreds of hours, and essentially deposit infinite amounts of P_2O_5 and B_2O_3 respectively, so that the surface concentrations approach the dopant solid solubility at a given diffusion temperature. Using data from reference [7], if conventional phosphorus solid sources were used under conditions required for a deep boron BSF ($\sim 1000^\circ\text{C}/30 \text{ min}$), the sheet resistance would be approximately 4 Ω/\square . If solar cells were made using this emitter profile, heavy doping effects would result in low quantum efficiencies for UV and visible radiation absorbed near the surface, thus lowering the cell efficiency. In addition, the residual oxide thickness deposited from the SiP_2O_7 solid sources would be on the order of 750 Å for a 30 minute diffusion at 1000 °C [7], which would result in a high optical reflectance if incorporated into a module. For this reason, most manufacturers remove the phosphorus diffusion glass and deposit an appropriate anti-reflection coating prior to encapsulating the solar cells, thereby eliminating any passivating effects of the diffusion glass.

7.3.2 Residual Oxide Thickness

Figure 6.3 shows the residual oxide thickness for boron and phosphorus diffused samples resulting from the limited solid doping sources developed in this work. The three sets of data are for boron and phosphorus diffusions at 1000 °C for 60 min in N₂, at which point the wafers were cooled to either 700 °C (open and closed circles for B and P respectively), or to 100 °C for a second set of phosphorus diffusions, and pulled into a cleanroom ambient. In comparing the B and P diffused samples pulled at 700 °C, it appears that the residual glass thickness is approximately the same value for both dopants, for sheet resistance (ρ_s) values greater than about 30 Ω/\square . For ρ_s values below about 30 Ω/\square , the glass thickness rises sharply with decreasing ρ_s , and the differences in glass thickness between boron and phosphorus diffused samples becomes more pronounced. One plausible explanation for the same glass thickness being measured on B and P diffused samples pulled at 700 °C is that a native silicon oxide is growing while the wafers are pulled into the cleanroom ambient. To investigate this idea, selected phosphorus diffusions were repeated, with the wafers cooled in N₂ and pulled at 100 °C so that any native oxide grown would be much thinner than if pulled at 700 °C. Figure 7.3 shows that the residual glass thickness for wafers pulled at 100 °C is essentially the same value than if pulled at 700 °C, and therefore that the 50-60Å of residual glass is a by-product of the (limited) diffusion sources.

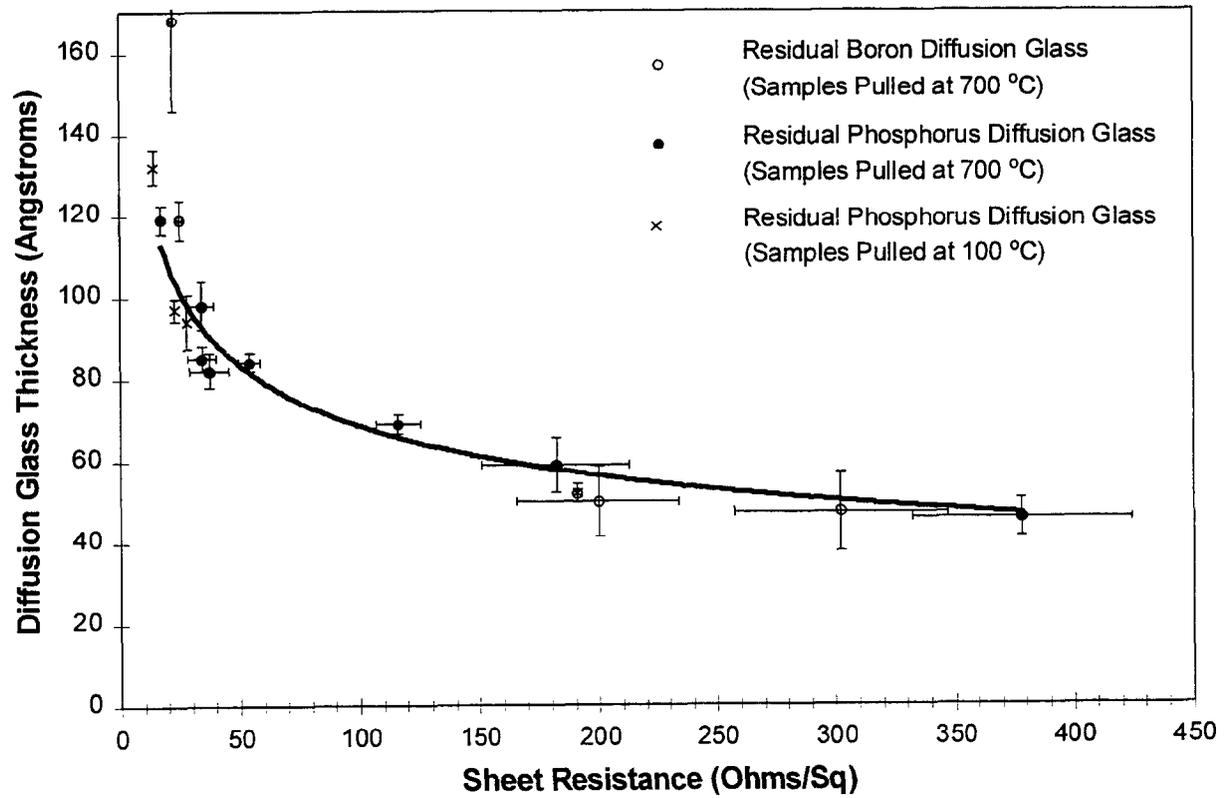
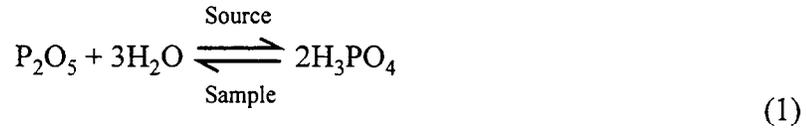


Figure 7.3. Residual diffusion glass thickness vs. sheet resistance for a 1000 °C/60 min process in N₂ for phosphorus and boron diffusions, with no *in-situ* oxidation.

7.3.3 *Proposed Model*

The results of the above experiments could be interpreted in several ways. One explanation is that below 700 °C, the partial pressure of the phosphorus species liberated from the source wafer is negligible, therefore no additional dopant is deposited below 700 °C to increase the residual glass thickness (fig 7.3). If that were true, then the phosphorus sources would be re-useable for additional diffusion cycles, which we have found not to be the case. A more likely situation is that the dopant sources used for lower surface concentrations (i.e. $\rho_s > 30 \Omega/\square$) deposit a limited dose of volatile dopant species which is *consumed* by the intended sample instead of piling up on the silicon surface, which would lead to the formation of a thick glass layer.

The phosphorus SOD used in this work is an industry-standard solution of P₂O₅, H₂O, tetraethylorthosilane (TEOS), and ethanol. The hotplate bake prior to diffusion serves to drive off the ethanol solvent leaving a glassy phosphosilicate film (PSG). As temperatures are increased toward the target diffusion temperature (900-1000 °C), the PSG film polymerizes to form SiO₂, H₂O and C₂H₄ [9,10]. It is well known that P₂O₅ is extremely hygroscopic, and will react with H₂O in the SOD film, as well as with trace amounts of moisture in the process gasses, to form the volatile species H₃PO₄ (phosphoric acid), which is weakly bonded to the PSG structure. It is assumed that this is the phosphorus containing species transported from the source to the sample wafer. On the sample surface, the reverse reaction takes place whereby H₃PO₄ reacts to form P₂O₅, with H₂O as a byproduct; a process which was shown to occur during the direct vaporization of H₃PO₄ at elevated temperatures [12].



The pentoxide of phosphorus, P_2O_5 , deposited on the sample surface proceeds to react with silicon to form SiO_2 and P, which preferentially diffuses into silicon:



For the case of limited doping sources, we propose that the starting thickness of P_2O_5 formed on the sample surface is extremely thin, and is limited by the dose of H_3PO_4 from the source. During the diffusion cycle reaction (2) is essentially driven to completion, resulting in a thin layer of SiO_2 rich glass on the sample surface, and the surface concentration of P below the solid solubility. Thus by controlling the concentration of P_2O_5 in the SOD film, we can limit the dose of H_3PO_4 , and thus the thickness of P_2O_5 on the sample, allowing the underlying silicon to consume virtually all of the available phosphorus for surface concentrations below the solid solubility. As the P_2O_5 content in the SOD is increased, resulting in a greater dose of H_3PO_4 , the residual P_2O_5 layer on the sample exceeds what can be consumed during the diffusion cycle. At this point, the sources used in our process behave like conventional phosphorus solid sources in which the P_2O_5 supply exceeds what the sample can consume, resulting in a fixed surface concentration which is limited by the diffusion temperature (i.e. solid solubility). This concept is shown schematically in figure 7.4, in which the surface concentration increases with P_2O_5 thickness on the sample until the supply of phosphorus exceeds the solid solubility, at which

point the surface concentration is fixed by the phosphorus solid solubility for increasing P_2O_5 thickness.

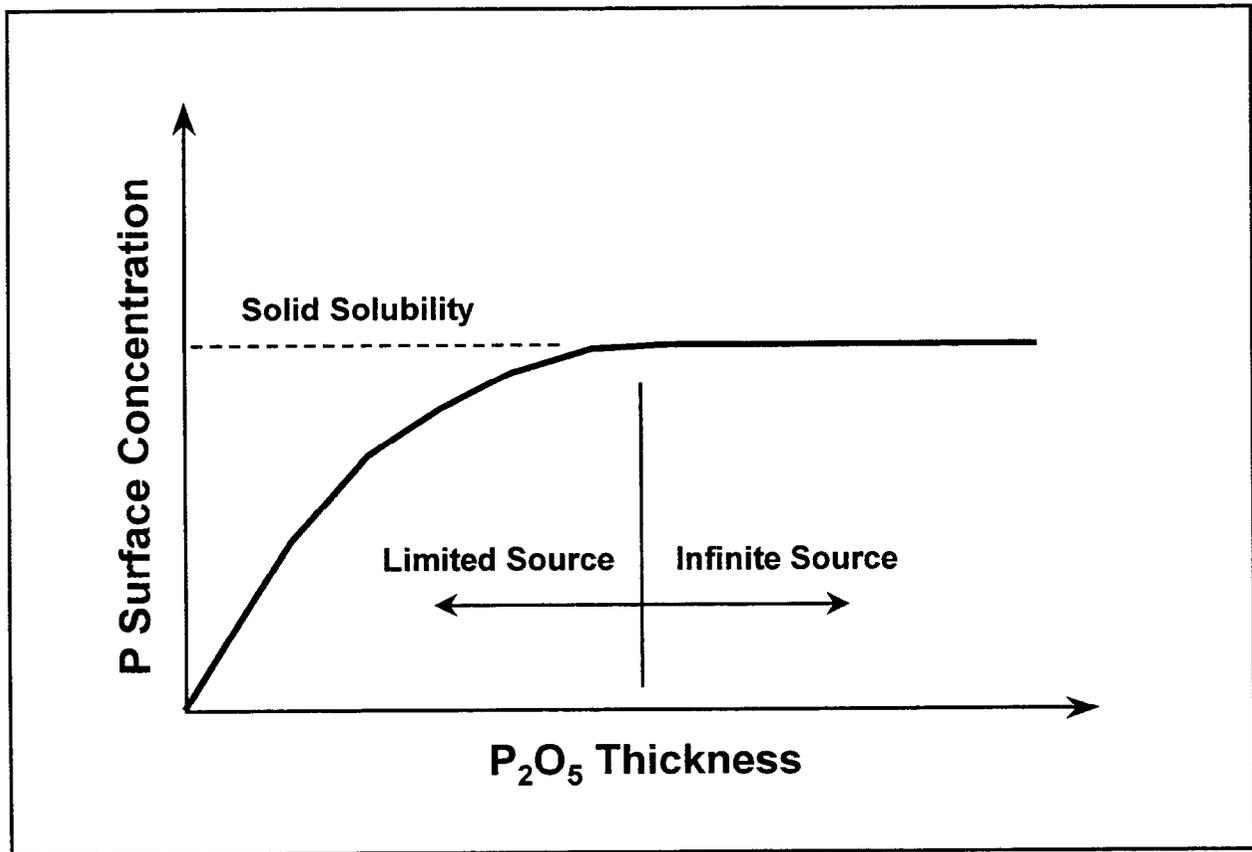


Figure 7.4. Proposed reaction pathway for phosphorus diffusions using solid sources fabricated from a spin-on dopant film.

This result is notably different than conventional SiP₂O₇-based solid sources which are designed to be reused for hundreds of hours. These conventional solid sources continually deposit a stream of P₂O₅ on the sample wafers, which results in a thick layer of diffusion glass on the surface [7], and thus provides a supply of phosphorus which exceeds the solid solubility. In this case the surface concentration is ultimately limited by the solid solubility of P in Si, and thus the only degrees of control is the diffusion temperature and time. But by fabricating solid doping sources in the limited source regime we can now control the (diffused) surface concentration by controlling the SOD source concentration.

The situation for boron diffusions is analogous to phosphorus. The Boron-A film used in these experiments is a proprietary boron-based polymer dissolved in cyclohexane and diluted with toluene, which converts directly to B₂O₃ at about 450 °C. It is likely that B₂O₃ is directly transported from the source to sample wafer, although HBO₂ which has a much higher vapor pressure than B₂O₃ is known to form in the presence of even trace amounts of moisture [13, 14]. For the case of limited boron diffusions, the reactions on the sample surface proceed as in the case of phosphorus:



resulting in a thin SiO₂-rich glass layer and a boron concentration below the solid solubility and a thick borosilicate glass layer for surface concentrations above the solid solubility. As explained below, an important advantage to using separate boron sources as fabricated in our process is the ability to filter out impurities contained in the boron SOD film, resulting in very high processed bulk minority-carrier lifetimes.

The assertion that the doping sources fabricated in our simultaneous diffusion process results in a limited thickness of P_2O_5 or B_2O_3 onto the intended sample was tested by examining the dependence of sheet resistance, ρ_s , on surface morphology. Figure 7.5 shows the resulting sheet resistance for the case of textured and planer sample wafers each facing the same phosphorus source, for a range of P_2O_5 concentrations in the SOD films. Surface texturing was achieved by etching upright pyramids with [111] oriented facets in the (100) silicon surface, using a weak alkaline solution at 80 °C for 30 min. Sheet resistance measurements were made by the four point probe technique, in which the sheet resistance is independent of the absolute probe spacing and is therefore assumed to be independent of the surface morphology [15]. All the planer and textured samples in figure 7.5 were diffused at the same time using a 925 °C diffusion cycle in N_2 for 60 min, followed by a 15 min *in-situ* oxidation. As the data in figure 6.5 shows, for low concentrations of P_2O_5 in the SOD films used to fabricate the sources, the textured wafers have a higher sheet resistance than the planer wafers by a factor of about 2 when facing the same sources. As the % P_2O_5 in the SOD film is increased, the difference in ρ_s is reduced until the ρ_s 's for the textured and planer wafers approach the same value for the “infinite” P_2O_5 case, which corresponds to that of conventional solid sources. For comparison, diffusions were carried out using $POCl_3$ and conventional SiP_2O_7 - based solid sources, with textured and planer wafers diffused simultaneously. As shown in Table 7.1, the values of ρ_s for textured and planer wafers is nearly identical when using $POCl_3$ and conventional solid sources. However, in the case of *limited* solid sources used in this technique, the same source can produce an 86 Ω/\square textured emitter and a 46 Ω/\square planer emitter. This is because a fixed dose of H_3PO_4 impinging on a textured surface (with a larger surface area), results in a thinner P_2O_5 layer, which in turn results in a lower surface concentration and higher sheet resistance.

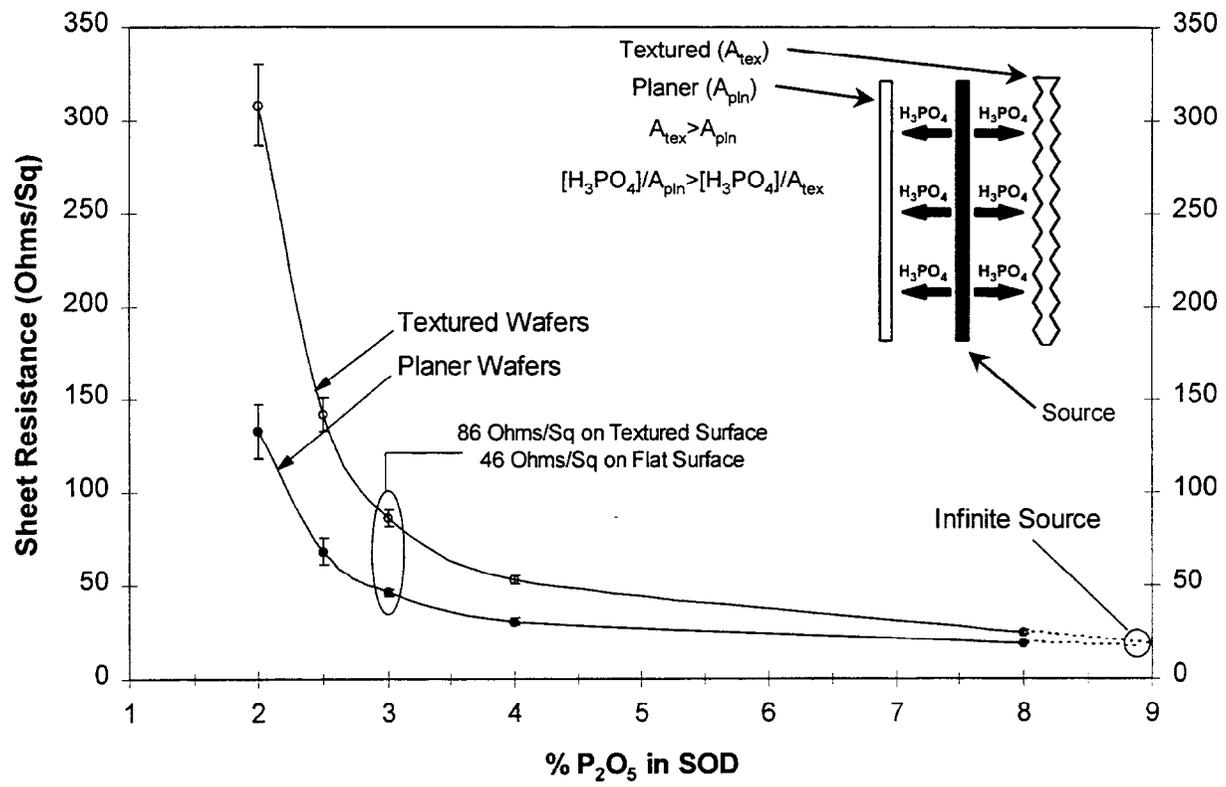


Figure 7.5. Dependence of sheet resistance on % P₂O₅ in phosphorus SOD film for a 925 °C/60 min process, for planer and pyramid-textured surfaces.

	Conventional Solid Sources	POCl₃	<i>Limited Solid Sources</i>
Textured Wafer Sheet Resistance	101 Ω/□	82 Ω/□	<i>86 Ω/□</i>
Planer Wafer Sheet Resistance	98 Ω/□	88 Ω/□	<i>46 Ω/□</i>

Table 7.1. Comparison of conventional SiP₂O₇-based solid sources, POCl₃ and the limited solid sources developed in this work, to form light phosphorus diffusions on planer and textured silicon wafers.

Thus it appears that the limited solid sources used in this work are unique in their ability to deposit a fixed, relatively thin dose of dopant oxide, resulting in a clear dependence of sheet resistance on surface texturing.

The dependence of sheet resistance on surface morphology displayed in fig. 7.5 using limited solid sources is a significant result because it offers a way of obtaining a selective emitter for screen-printed based metallization, which requires heavy diffusions under the metal grid contact, while maintaining a light diffusion in the textured field region with a well passivated surface. This could be achieved by patterning a suitable texture mask, such as PECVD SiN, to obtain a flat grid region and a textured field. For example, the data set in figure 7.5 shows that using a phosphorus SOD film containing 3% P₂O₅ to fabricate the sources, one can obtain 86 Ω/□ on a textured surface, which is ideal for high efficiency cell designs, and 46 Ω/□ on a flat region which is suitable for screen printing.

7.3.4. *In-Situ Oxide Surface Passivation*

Since the residual diffusion glass is thin for light phosphorus and boron diffusions formed using limited doping sources, a passivating thermal oxide can be grown *in-situ* thus eliminating the need for a diffusion glass removal step and additional high temperature oxidation cycle. To examine the passivating qualities of this thin *in-situ* thermal oxide, measurements were made of the emitter saturation current density (J_0) using the Photo-Conductance Decay (PCD) technique [16] for both phosphorus and boron diffusions. By plotting the inverse effective lifetime $1/\tau_{eff}$, as a function of injection level n , for a sample with identical diffusions and passivation on each side, the slope is proportional to the saturation current density, J_0 according to the relation:

$$\frac{1}{\tau_{eff}} - C_n n^2 = \frac{1}{\tau_{bulk}} + \frac{2J_0}{qn_i^2 W_{bulk}} n \quad (4)$$

where C_n is the Auger coefficient, τ_{bulk} the bulk minority carrier lifetime, W_{bulk} the bulk wafer thickness and n_i the intrinsic carrier concentration (at 25 °C). Table 2 shows the results of J_0 measurements for 80-90 Ω/\square boron and phosphorus diffusions on un-textured 500-1000 $\Omega\text{-cm}$ n-type float zone wafers. The resulting J_0 values for light boron and phosphorus diffusions are quite low, giving a value of 118 fA/cm^2 and 67 fA/cm^2 respectively for the case of *in-situ* oxide surface passivation. After removing the *in-situ* oxide in dilute HF and allowing a native oxide to form, the J_0 's increased substantially to 404 fA/cm^2 in the case of boron and 809 fA/cm^2 for the case of phosphorus, thus demonstrating the superb passivating qualities of the *in-situ* oxide provided by this simultaneous diffusion technique.

7.3.5. Impurity Filtering

Boron diffusions are not widely used in the photovoltaic industry, which is due in large part to the difficulty in obtaining high minority carrier lifetimes, and forming the boron diffusions in a straight-forward, cost-effective way. Several groups have been successful [17, 18] at producing record high efficiency solar cells using BBr_3 as a boron source, but in our experience with BBr_3 it has proven to be difficult to reproducibly obtain high bulk lifetimes without extensive furnace gettering cycles prior to diffusion. In addition, the use of BBr_3 requires a masking oxide be grown prior to diffusion thus requiring an additional high temperature step which increases processing costs and complexity. Several groups have reported similar lifetime problems using boron nitride solid sources [19, 20]. In this work it was discovered that by fabricating boron solid sources out of silicon wafers, one could reproducibly

obtain high bulk minority carrier lifetimes from a relatively impure boron SOD film. Figure 6.6 shows the results of PCD bulk lifetime measurements for boron diffused samples, in which the diffusions were etched and the surfaces passivated in 20% HF [21] during the measurement. High quality p-type (2.3 Ω -cm) float zone silicon was used in these experiments, and special care was taken at all stages to insure cleanliness of the diffusion process. In the first case, a 100% Boron-A film was applied to a float zone wafer, which was subsequently boron diffused directly from the SOD film in a 60 min, 1000 °C thermal cycle in N₂. A second float zone wafer adjacent to the first was doped indirectly by the transport of B₂O₃ from *this* SOD film. From the inset of figure 6.6, at an injection level of $5(10)^{14}$ cm⁻³, the minority carrier lifetime was 227 μ s for the wafer on which the boron SOD was directly applied (i.e. the source wafer), while the *adjacent* sample wafer had a much higher bulk lifetime of 1306 μ s. A more dramatic difference in bulk minority carrier lifetime is seen from the second set of samples in which a thick *in-situ* oxide was grown for 66 min at 1000 °C after the 60 min diffusion process in N₂ at 1000 °C. It is noted that the same lot of boron SOD film was used for the source wafers in figure 6.6. For the thick oxide case, the wafer which had the boron SOD directly applied had a low bulk lifetime of only 5.91 μ s, while the adjacent sample wafer had a bulk lifetime of 1010 μ s, corresponding to a factor of 171 higher. We have observed this behavior numerous times using 5 different lots of boron SOD film manufactured over the course of three years. The mechanism responsible for impurity filtering can be understood conceptually from figure 7.7. The impurity level in the Boron-A SOD used in this work is relatively high for achieving very high minority carrier lifetimes, containing levels of Fe, Cu, Ni, Cr, Mn in the 10 ppb range [22].

Dopant	Sheet Resistance	Surface Passivation	J_0
Boron	83 Ohms/Sq	In-Situ Oxide	118 fA/cm ²
Boron	83 Ohms/Sq	Un-Passivated	404 fA/cm ²
Phosphorus	90 Ohms/Sq	In-Situ Oxide	67 fA/cm ²
Phosphorus	90 Ohms/Sq	Un-Passivated	809 fA/cm ²

Table 7.2. Saturation current density (J_0) measurements for in-situ oxide passivated and un-passivated 80-90 Ω/\square boron and phosphorus diffusions.

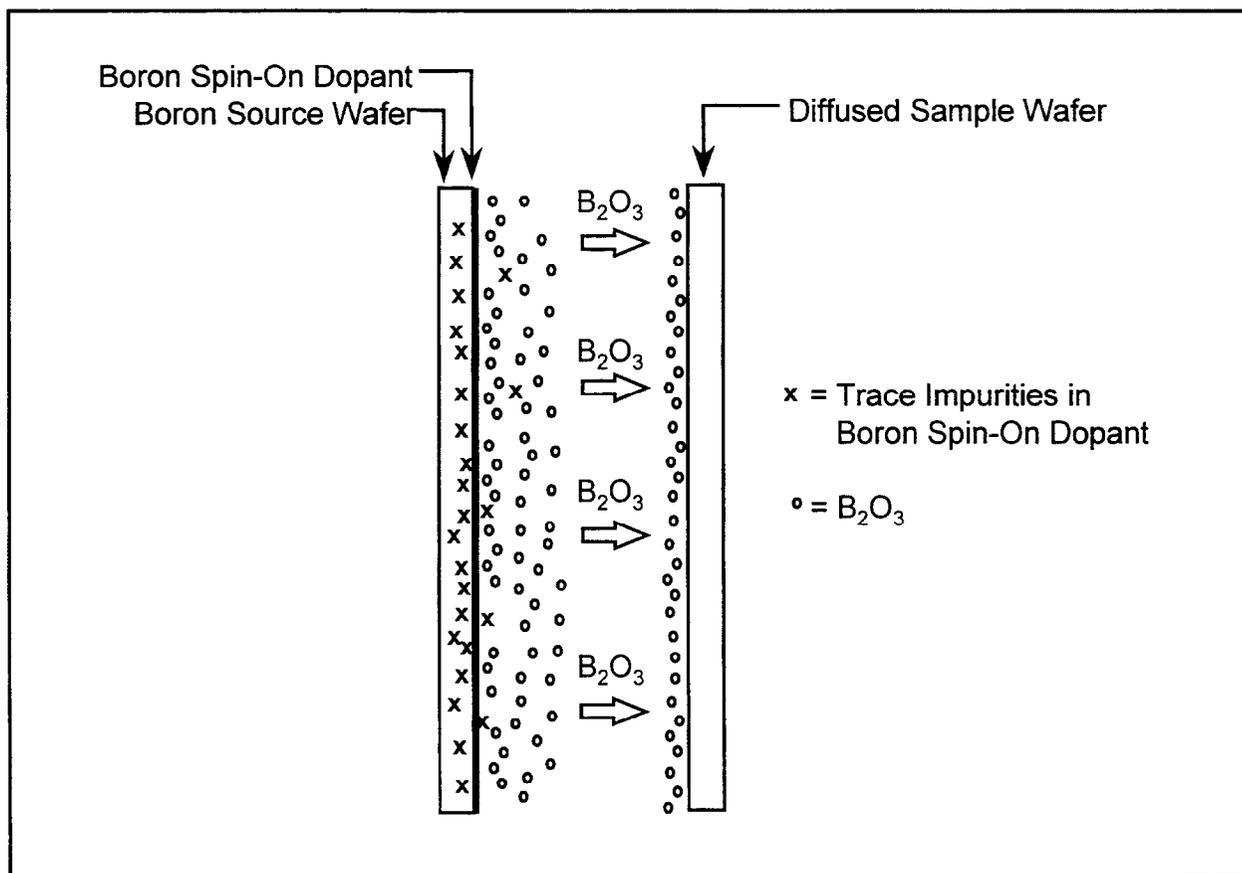


Figure 7.6. Demonstration of high minority carrier lifetimes due to impurity filtering from

SOD-coated solid sources. Source 1 wafer on which the boron SOD was applied was facing Sample 1 in a 1000 °C/60 min process with no *in-situ* oxidation, while the Source 2 wafer was facing Sample 2 in a 1000 °C/60 min process with an additional 66 min *in-situ* oxidation at 1000 °C.

This is why it is generally difficult to obtain high lifetimes in excess of 1 ms using boron SOD sources. At diffusion temperatures of 1000 °C, the partial pressure of these trace metals is extremely low [23], so that in our diffusion scheme only the volatile B₂O₃ is transported from the source to sample wafer, leaving the impurities in the source wafer. Thus by simply fabricating boron sources out of silicon wafers using a commercially available boron SOD film, one can obtain clean boron diffusions and in the process benefit from the *in-situ* passivating oxide which from Table 7.2 resulted in J₀ values in the 100 fA/cm² range.

7.3.6. Boron Gettering

Transition metals such as Fe, Cr, Cu and Ni are fast diffusing elements in silicon, and if present in the boron SOD film in 10 ppb levels will certainly degrade the lifetime of the p-type silicon float zone silicon wafers used in this work [24]. Thus it is interesting to note that the sample which was oxidized for an additional 66 min at 1000 °C had a substantially lower bulk lifetime than the sample diffused in a N₂ ambient for 60 minutes at 1000 °C. For fast diffusing metallic impurities such as Fe, Cu and Mn it is assumed that the diffusion lengths, $\sqrt{D_{metal}t}$, during a 60 min 1000 °C thermal cycle, is greater than the 300 μm wafer thickness [25]. This type of lifetime dependence on oxidation was recently reported for p⁺ diffusions formed using boron nitride solid doping sources [19], and was attributed to the re-injection of impurities from the p⁺ region into the wafer bulk during a subsequent oxidation step. By growing an oxide on the p⁺ diffused surface, the boron is preferentially segregated into the oxide [13], thus lowering the diffused boron surface concentration. Recently, workers at Bell Laboratories [25] and elsewhere

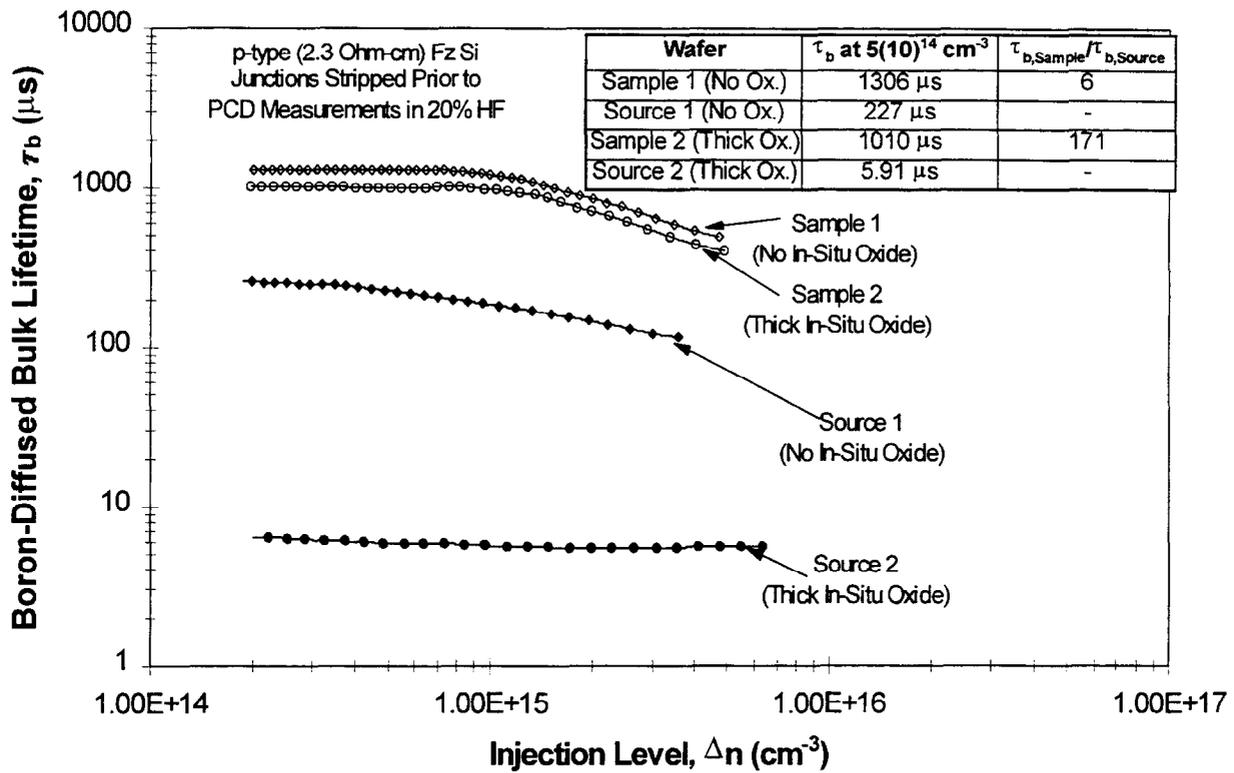


Figure 7.7. Schematic of impurity filtering action commensurate with boron SOD-coated source wafers: The impurities (X) in the SOD film are diffused into the source wafers while the volatile dopant species, B_2O_3 , (O) is transported to the sample wafer, resulting in a high-purity boron diffusion.

[26] have shown that boron is effective at getting transition metals such as Fe, Cr and Mn through the formation of metal acceptor pairs, and in the case of iron have shown a clear dependence of the getting efficiency on the boron concentration in the getting region [25]. Figure 7.8 shows the spreading resistance profiles for two boron diffused samples, in which one was diffused for 60 min at 1000 °C in N₂, and the other diffused for 60 min at 1000 °C in N₂, and *in-situ* oxidized for an additional 66 min at 1000 °C. A possible explanation for the lower bulk lifetime for the oxidized source wafer (fig 7.6) is the reduction in the *getting efficiency* of impurities introduced by the boron SOD film, as a result of lowering the boron surface concentration (shown by the hatched area in figure 6.8) during the *in-situ* oxidation. It is noted that although no attempt has been made in this work to identify the lifetime limiting impurities or quantify the getting effectiveness of boron, our results are consistent with those reported in the literature for boron getting of the metallic impurities present in the Boron-A SOD film [25, 26]. This work demonstrates that one can obtain clean boron diffusions in a simple way (via impurity filtering), which makes this an ideal materials system for studying the getting effectiveness of boron, and possibly boron and phosphorus co-getting phenomena [27], in a process which is compatible with commercial solar cell manufacturing technology.

7.3.7. High Efficiency Silicon Solar Cells

Textured n⁺pp⁺ solar cells have been fabricated by this simultaneous boron and phosphorus diffusion process, and has reproducibly given over 19% efficiencies on float zone silicon for a variety of bulk resistivities. Figure 7.9 shows the results of light IV, internal quantum efficiency and reflectance measurements provided by Sandia National Laboratories.

The 4 cm² devices were fabricated from textured 2.3 Ω-cm (p-type) float zone silicon by simultaneously

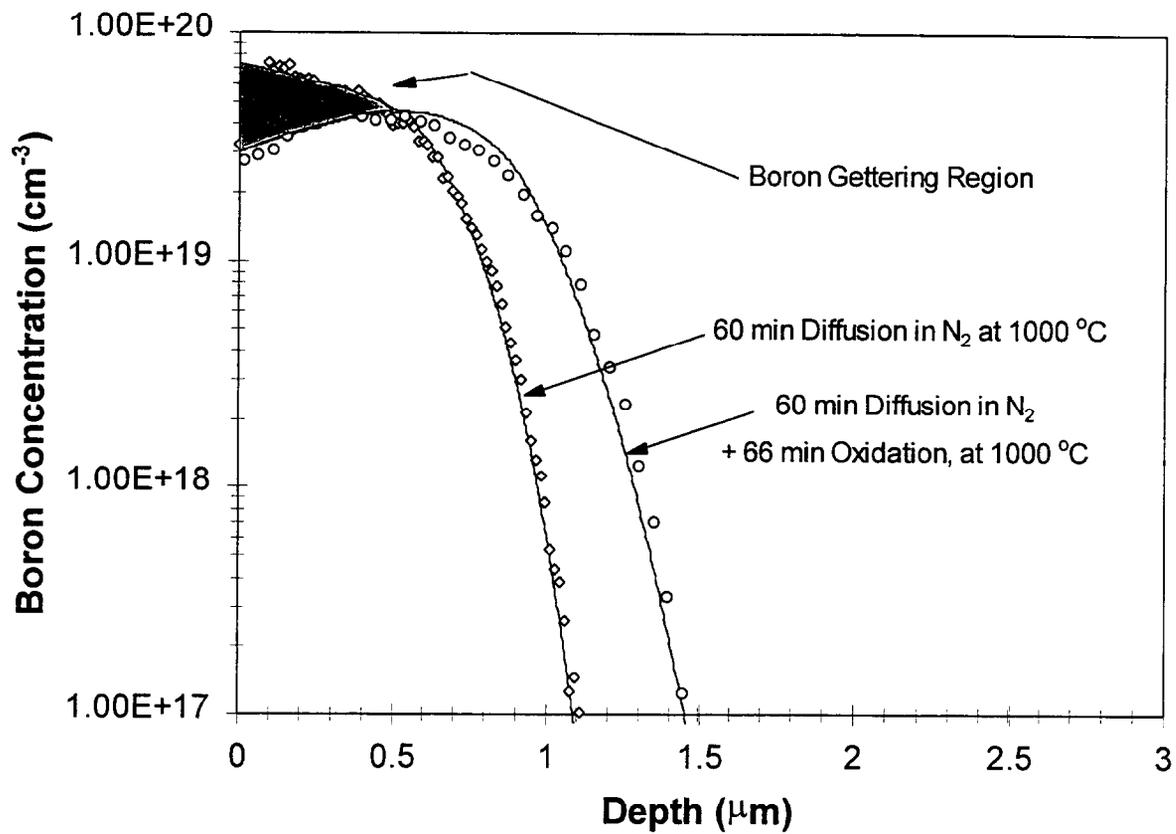


Figure 7.8. Spreading resistance measurements for boron diffusions formed in a 1000 °C/60 min process, with and without *in-situ* oxidations. The reduction in boron surface concentration for the oxidized case is believed to reduce the gettering effectiveness of the diffused region relative to the non-oxidized case.

diffusing a $100 \Omega/\square$ phosphorus emitter, $35 \Omega/\square$ boron BSF, and growing a thick ($\sim 1070 \text{ \AA}$) *in-situ* thermal oxide for surface passivation and as a rudimentary anti-reflection coating. In addition to providing excellent surface passivation and anti-reflection properties, the *in-situ* oxide on the back was used as a dielectric for a Si/SiO₂/Al Back Side Reflector (BSR), to improve the light trapping capabilities of the devices. This device structure, referred to as a Simultaneously diffused, Textured, *in-situ* passivating oxide AR-coated solar cell (**STAR** cell), has produced efficiencies as high as 20.1% [28] in a single thermal cycle, using photolithography-based metallization. Figure 6.9 shows the results for two STAR cells, in which the first had a boron SOD film directly applied to the backside, which was used as a boron source for the second cell in figure 6.9. The benefits of impurity filtering are clearly shown in figure 7.9, in that the cell which had the boron SOD directly applied has a low efficiency of only 15.2%, whereas the cell doped indirectly from the boron film on the 15.2% cell had a much higher efficiency of 19.4%. These results demonstrate the ability of this novel simultaneous boron and phosphorus diffusion technology to provide several efficiency-enhancing features, (optimal profiles, *in-situ* oxide surface passivation, *in-situ* SiO₂ AR-coating, BSR), in a single thermal cycle.

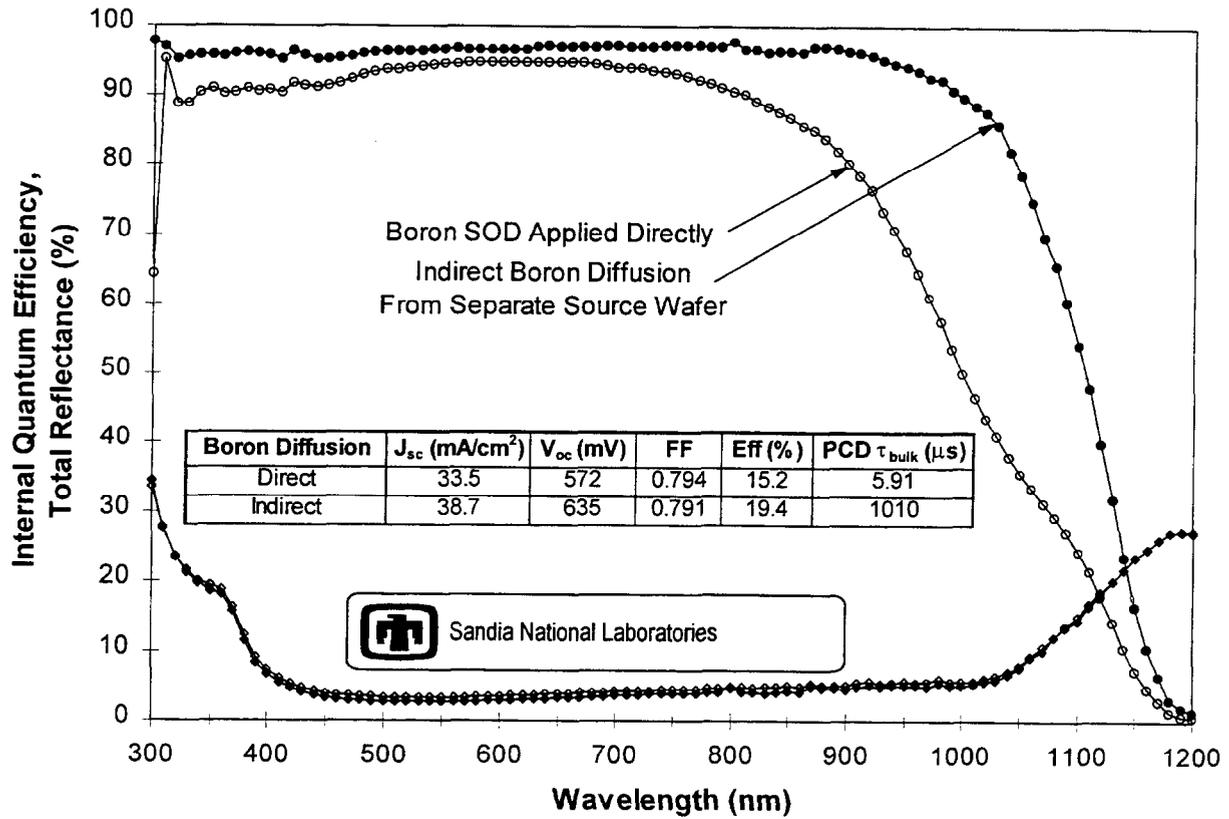


Figure 7.9. Internal Quantum Efficiency and Reflectance vs. Wavelength measurements for a solar cell wafer on which the boron SOD was directly applied (source wafer) and the adjacent solar cell (sample wafer) that was facing this source in the diffusion furnace. The 4.2% increase in absolute efficiency for the sample wafer is attributed to impurity filtering, resulting from the separate source/sample arrangement in the diffusion furnace.

7.4 Conclusion

In conclusion, we have presented a novel simultaneous boron and phosphorus diffusion technology that is well suited for the production of simple, but high efficiency silicon solar cells. In addition to providing the flexibility to simultaneously obtain a wide range of emitter and BSF profiles, this process also allows for the *in-situ* growth of a thin passivating thermal oxide. Measurements of the emitter saturation current density, J_0 , have shown that the passivating qualities of the *in-situ* oxide is excellent, producing J_0 values in the 100 fA/cm^2 range for light phosphorus and boron diffusions. A physical model is presented to explain the behavior of the limited solid doping sources developed in this work. It is proposed that by fabricating solid sources out of silicon wafers using spin-on dopant films, the resulting sources deposit a *limited* dose of dopant oxide which is consumed by the intended sample. Thus for surface concentrations below the solid solubility, the surface concentration is controlled by the thickness of P_2O_5 or B_2O_3 deposited from the sources and absorbed by the sample wafers. This model was used to explain two unique attributes of this process, namely the ability to obtain an extremely thin layer of residual oxide on the diffused surface, and the dependence of sheet resistance on surface texturing, where it was shown that one could obtain $86\Omega/\square$ on a random textured surface, and $46\Omega/\square$ on a flat surface, using the same phosphorus source.

During the course of this work it was shown that by fabricating separate boron solid sources using a boron SOD film, that one could filter-out trace impurities present in the SOD film and obtain high minority carrier lifetimes in the adjacent sample wafers. Bulk minority carrier lifetimes in excess of 1 ms were obtained on boron-diffused $2.3 \Omega\text{-cm}$ float zone wafers doped indirectly by separate source wafers. The $2.3 \Omega\text{-cm}$ float zone source wafers to which the boron SOD was directly applied had lifetimes as low as $5.91 \mu\text{s}$ after a prolonged *in-situ*

oxidation step. The impurity filtering action commensurate with separate boron sources was used to fabricate high-efficiency n^+pp^+ solar cells. It was shown that the cell which the boron SOD film directly applied had a low efficiency of 15.2%, while the adjacent cell doped from the same SOD film had a much higher conversion efficiency of 19.4%.

7.5 References

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CHAPTER VIII

NOVEL PROCESSING OF SOLAR CELLS WITH POROUS SILICON TEXTURING

8.0 Novel Processing Of Solar Cells With Porous Silicon Texturing

A simple porous silicon texturing technique that is applicable to various kinds of silicon material, including multicrystalline and ribbon Si, of any doping type and level is used to fabricate solar cells. Acidic etching of Si leads to a homogeneous porous silicon (PS) surface layer with reflectance as low as 9%. Phosphorus diffusion and thermal oxidation are shown to produce very low emitter saturation current density, 128 fA/cm^2 , which is only slightly higher than values obtained on planar surfaces, but still capable of giving open-circuit voltages in excess of 650 mV. The dopant oxide solid source (DOSS) solar cell process with its simultaneous formation of phosphorus emitter and *in-situ* surface oxide leads to an excellent surface passivation, while maintaining low reflectance on PS-textured wafers. The fabricated solar cells show efficiencies of up to 14.9% using the PS layer as an anti-reflection coating (ARC) and surface passivation. This is the highest reported value with this kind of texturing and without any additional ARC. The simplicity of the process makes it a very promising technology and easily transferable into industrial production.

8.1 Introduction

Surface texturing is an important tool to improve the conversion efficiency of silicon solar cells. In addition to reduced reflection of the incoming light, light-trapping of long wavelength light is also desirable, which becomes even more important for thinner wafers or ribbon materials. While monocrystalline silicon can easily be textured by alkaline solutions etching preferably in $\langle 111 \rangle$ direction, texturing of multicrystalline (mc) Si consisting of grains with different orientation is still a challenge. A promising technique is the formation of porous silicon (PS): Etching of silicon wafers in

diluted nitric and hydrofluoric acid at room temperature leads to an appropriate porous surface layer, which gives the wafer a blue-to-purple look in order to minimize reflection.

Several groups are working on the application of PS layers to silicon solar cells (a review is given in [1]). The common objective is to form an antireflective (AR) "coating" and simultaneously etch back the emitter by forming PS on finished cells. Since the metallization acts as an etch mask, a selective emitter is formed. However, this method has several draw-backs: The metallization is attacked by the etching, leading to in homogeneity and, most important, to a degradation in fill factor [2]. In addition, the etch solution is contaminated with metal, which limits its usability and re-usability and demands expensive waste management. Moreover, another wet-chemical step does not fit well into an industrial fabrication sequence and holds the risk of carrying off chemicals (especially since porous surfaces tend to soak liquids). Therefore, we focus on the formation of PS during the normal cleaning sequence at the beginning of the solar cell process.

8.2 ACIDIC SURFACE TEXTURING

8.2.1 Porous Silicon Formation

Porous silicon is typically formed using the electrochemical process for uniformity reasons and controllability [3]. A more simple, pure chemical technique is the so-called stain etching in a HNO_3/HF . This etching strongly depends on the type and doping level of the silicon material, since the reaction is actually a localized electro-chemical etching [4]. Therefore, lower resistivity wafers etch faster. However, we have succeeded in forming PS on different float zone (FZ), Czochralski (Cz), multicrystalline (mc) silicon, and even ribbon material like EFG and String Ribbon of different

resistivities using the acidic etch or stain etching process. Even high resistivity n-type FZ can be etched.

The stability of the porous silicon texture against subsequent processing, particularly other chemical etching steps, is one of the most challenging technological problems of this technique [5]. The PS layer formed by our process, though, is the final step in the cleaning process and is subsequently dried and loaded into the furnace. A thin PS layer was found to maintain anti-reflection qualities over a 60 min. diffusion followed by a 15 min. oxidation at 925°C. If the PS layer is too thick, the optical qualities are not maintained during the diffusion cycle. However, removal of the phosphorsilicate glass (PSG) removes the PS texturing at least partly.

8.2.2 *Optical Properties of Porous Silicon*

The diffuse reflectance (Fig. 8.1) of PS-textured silicon shows a minimum at about 600 nm, reflecting its color after etching. The weighted reflectance (R_w), that is the integral reflectance between 400 and 1100 nm weighted with the AM 1.5 global spectrum, is as low as 9 % for low-resistivity p-type FZ and mc-Si and 15 % for high-resistivity n-type FZ-Si, respectively, compared to 35 % of a planar surface. The higher reflectance of high-resistivity silicon is due to the slower etching resulting in a thinner PS layer that does not minimize the reflectance.

It is interesting to note, that above 500 nm the reflectance characteristic of PS texturing is similar to that of a SiN_x antireflective (AR) coating. This might indicate, that the porosity of the PS layer is low, so that above 500 nm it acts like a virtual dielectric layer resembling SiN_x with $n=2$ and 780 nm thick layer. The weighted reflectance, though, is still more than 0.5 % absolute lower than that of an SiN_x AR coating.

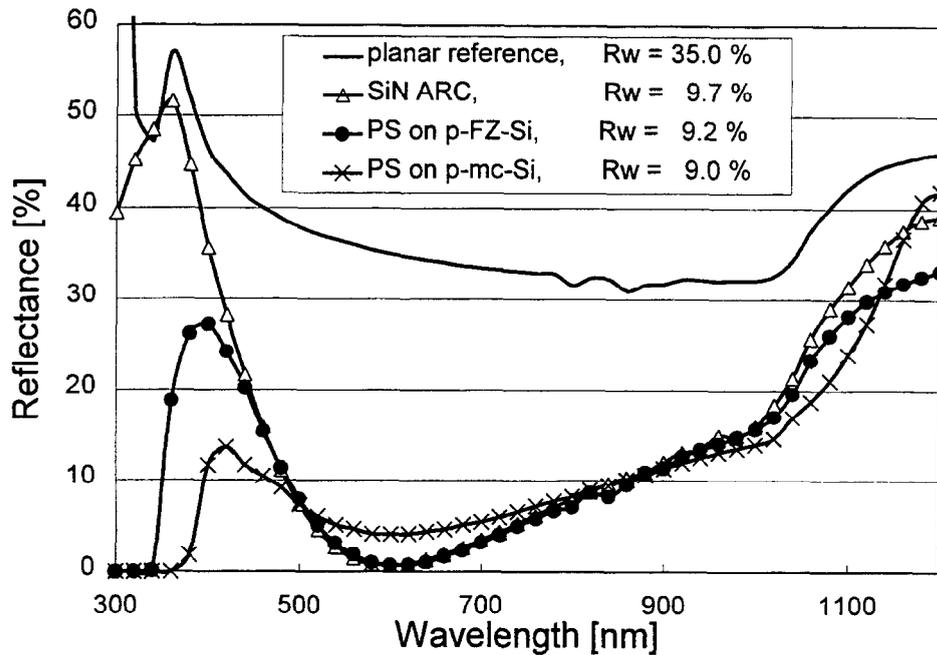


Fig. 8.1. Reflectance of planar silicon, silicon with SiN AR coating, and with porous silicon texturing, respectively.

8.2.3 Electrical properties of porous silicon emitter

The good reflectance comes with a rough surface that leads to high surface recombination velocities (SRV), on the order of 10^5 cm/s if not passivated. In addition to the above mentioned problem, the porous silicon texture could be removed by the PSG etching after diffusion. This calls for a special emitter formation process, that includes surface passivation but no PSG removal. We have therefore applied the dopant oxide solid source (DOSS) diffusion method [6] described in more detail below. This process simultaneously forms a phosphorus emitter and an *in-situ* surface oxide leading to excellent surface passivation, while maintaining low reflectance on PS-textured wafers.

The phosphorus source used for diffusion in this process yields a sheet resistivity range of 6-600 \square /sq. at 925°C, and can be tailored to the desired sheet resistivity by selecting the proper concentra-

tion of P_2O_5 . For a diffusion cycle that gave a $40 \Omega/\text{sq.}$ emitter on a planar surface, an emitter saturation current J_{oe} of $500 \text{ fA}/\text{cm}^2$ is obtained. A PS textured sample diffused during the same furnace process gave a J_{oe} of $128 \text{ fA}/\text{cm}^2$, which could give open-circuit voltage V_{oc} values in excess of 650 mV.

Due to the porous structure the sheet resistivity on textured samples is not measurable by the four-point probe method directly. After removing the PS layer by a 4 min. oxide etch (BOE) to expose a bare silicon surface, a sheet resistivity of approx. $250 \Omega/\text{sq.}$ is measured. However, the doped porous silicon surface layer might contribute to the lateral current transport, so the actual sheet resistance could be lower than $250 \Omega/\text{sq.}$. An alternate way of extracting a realistic value can be done from using the J_{oe} dependency on the sheet resistance: Fig.8.2 shows a graph of values obtained on planar samples using the DOSS diffusion method. The corresponding emitter sheet resistivity to a J_{oe} value of $128 \text{ fA}/\text{cm}^2$ as measured for a PS textured sample is around $100 \Omega/\text{sq.}$. In contrast, a $250 \Omega/\text{sq.}$ planar sample has an emitter saturation current as low as $\sim 75 \text{ fA}/\text{cm}^2$.

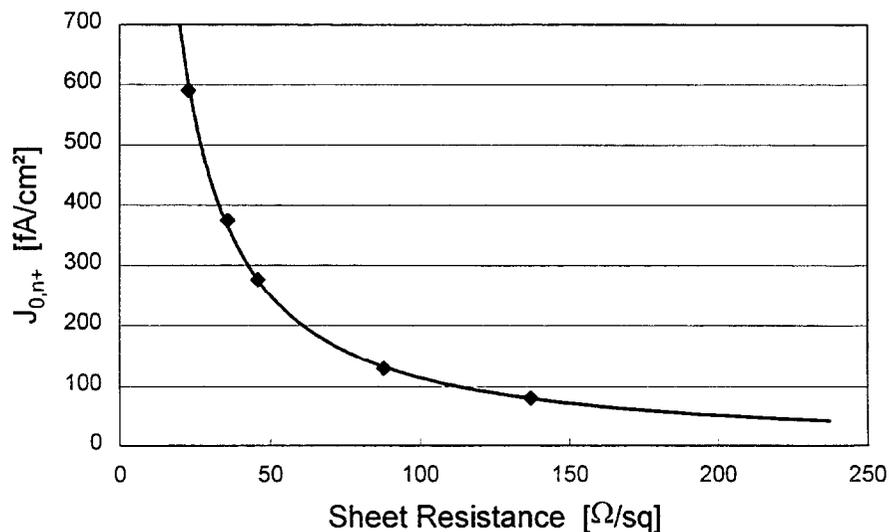


Figure 8.2: Emitter saturation currents as function of sheet resistance for planar samples diffused with the STAR process. PS had a $128 \text{ fA}/\text{cm}^2$ J_{oe} for an approximate $250 \Omega/\text{sq.}$ diffusion under the PS layer.

So, by forming the PS layer before furnace diffusion and in-situ oxidation, the emitter saturation current density, J_{oe} , that results from a DOSS diffusion is comparable to planar values which now enables us to implement this texturing scheme in a high-efficiency solar cell process.

8.3 POROUS SILICON TEXTURED SOLAR CELLS

8.3.1 DOSS solar cell processing

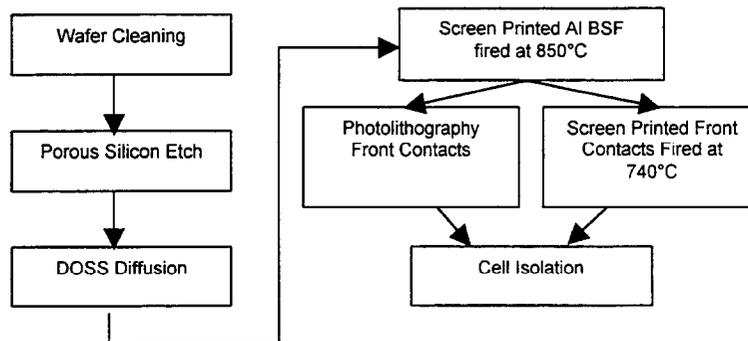


Fig. 8. 3. Process Flow Chart

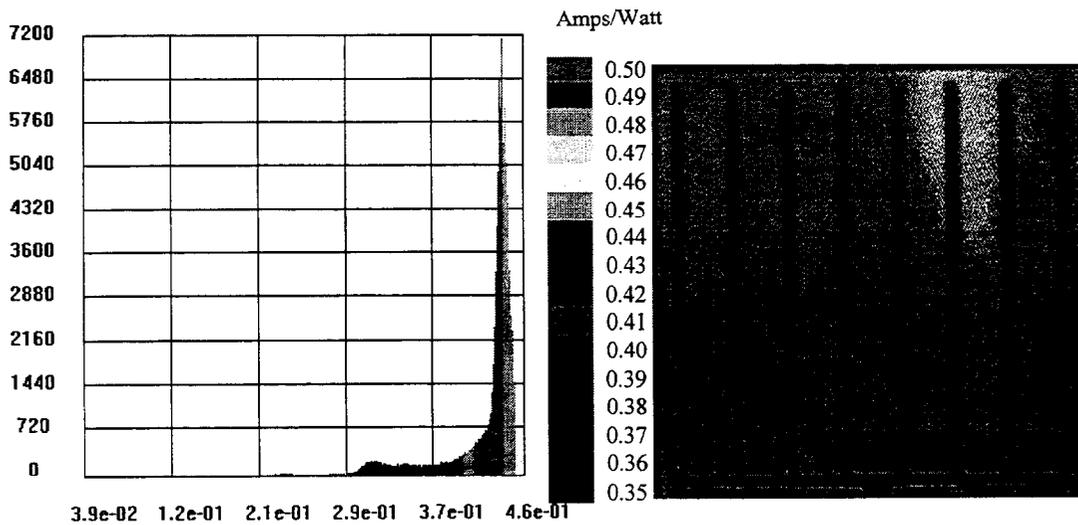


Figure 8.4: LBIC map of 0.6 Ω -cm FZ 4 cm² sample with a Porous Silicon anti-reflection coating

Using the dopant oxide solid source (DOSS) diffusion method [6], porous silicon textured solar cells with a screen printed Al BSF have been fabricated from 0.6 $\Omega\cdot\text{cm}$ FZ-Si (Shin Etsu), 0.7-1.3 $\Omega\cdot\text{cm}$ Cz-silicon (Bayer) and 0.2 $\Omega\cdot\text{cm}$ mc-Si (Eurosolare). The process sequence is shown in Fig. 3. The diffusion of phosphorus has been performed by using source wafers with spin-on dopant applied to both sides, which have been introduced to the furnace together with the samples so that every sample is stacked in front of one source wafer for emitter formation. Phosphorus is released from the source wafers at 925 °C, diffuses into the samples to form the emitter. By offering oxygen, an in-situ oxidation is achieved. The actual diffusion time has been one hour, followed by an oxidation step for 15 min to obtain the *in-situ* oxide. This one step furnace process leads to diffused, textured, *in-situ* oxide passivated, and AR-coated solar cells using a porous silicon layer. It has to be noted, that no PSG removal is included in this process. Thus, the DOSS method is a perfect match for PS texturing.

By stacking high resistivity (>100 $\Omega\cdot\text{cm}$) n-type float zone silicon wafers between two phosphorus source wafers, samples to measure the lifetime and dark saturation current density with n^+in^+ structure have also been fabricated.

The phosphorus dopant is a limited diffusion source and can be tailored to obtain any desired sheet resistivity for a given process by changing the concentration of P_2O_5 contained in the spin-on glass. This is an important consideration for porous silicon textured samples. The porous silicon layer acts somewhat as a diffusion barrier by limiting the phosphorus dopant implanted into the bulk silicon region for junction formation. Thus a much heavier concentration of P_2O_5 is required to obtain the desired sheet resistivity as would be necessary for a planar sample or even a random pyramid textured sample. The overall thickness of the PS layer contributes to whether or not the PS layer is completely oxidized during the furnace step.

8.4 DOSS solar cell results

Table 8.1. Best porous silicon solar cell results for photolithography (PL) and screen printed porous silicon solar cells. **Confirmed at Sandia National Labs.

Material	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF	Eff(%)
**0.6 \square cm FZ	629	29.32	0.807	14.9 (PL)
1.0 \square cm Cz	618	27.61	0.785	13.4 (PL)
0.2 \square cm mc	615	27.07	0.762	12.7 (PL)
0.6 \square cm FZ	627	28.91	0.759	13.8 (SP)
1.0 \square cm Cz	613	27.05	0.768	12.7 (SP)
0.2 \square cm mc	602	26.70	0.741	11.9 (SP)

The PS layer has been formed prior to emitter diffusion and metal contact formation. The solar cells have been fabricated using a diffusion process that yields 20 \square /sq. on a planar surface. This ensures a sufficiently heavy diffusion on the PS textured samples. Table 8.1 shows results obtained for both photolithography front contacts and screen printed front contacts. For the photolithography process metal contact has been made by removing the in-situ oxide and PS layer below the area to be covered by metal. Screen printed front contacts were simply added directly to the PS surface. Initial results show excellent potential for further development including the highest confirmed efficiency reported to date at 14.9 %. Excellent open circuit voltages and fill factors in excess of 80 % are demonstrated for photolithography cells. A 29.3 mA/cm² short circuit current is obtained for a AM1.5 global weighted reflectance of 17 %. Since PS layers with a 9% AM1.5 global weighted reflectance are already demonstrated (see Fig. 8.1), there is potential for even higher current collec-

tion. Further optimization of the starting sheet resistance and lower reflectance can result in much higher cell efficiency.

As is apparent from the open circuit voltage the surface passivation is sufficient to maintain good V_{oc} values. The reduced efficiency results from the decreased current collection due to the non-optimal PS layer.

The potential for increase performance is supported by the following two graphs. Fig. 8.4 and Fig. 8.5 show the uniformity of the PS as a anti-reflection coating as well as a good internal quantum efficiency, IQE. The uniformity of the PS layer as an anti-reflection coating is shown in the LBIC map in Fig. 8.4. This demonstrates that the reflectivity of the solar cells can be tightly controlled allowing for maximum current collection when coupled with the good IQE shown in Fig. 8.5. The non-uniformity of PS can be avoided through a more thorough understanding of PS formation via a stain etching method. A $0.6 \text{ } \Omega/\text{cm}$ FZ sample is used to focus on any artifacts that may arise in the use of a PS layer for the IQE measurement.

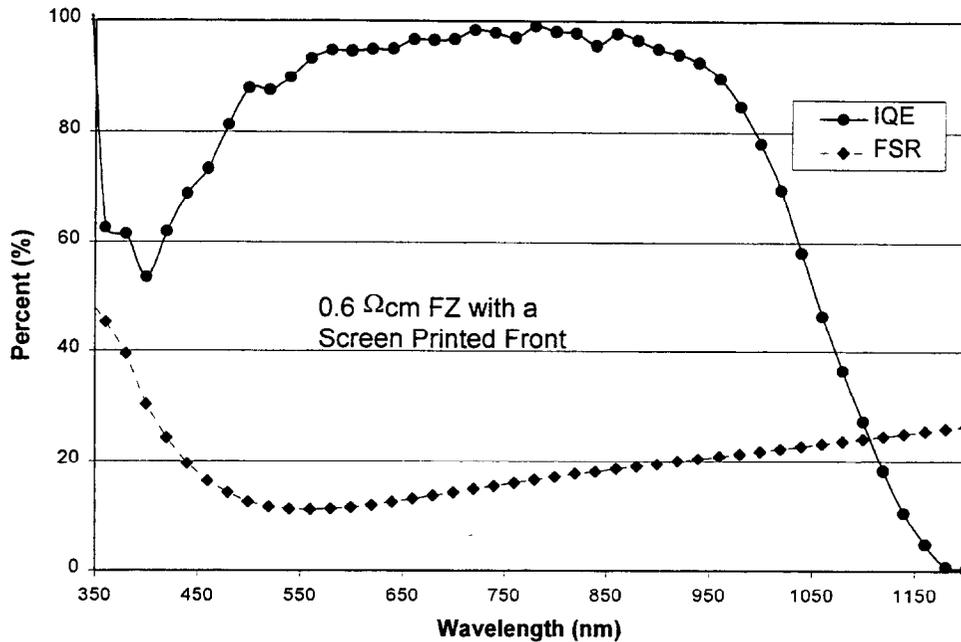


Figure 8.5: Internal Quantum Efficiency and Front Surface Reflectance for Porous Silicon textured FZ

8.5 CONCLUSIONS

Porous silicon etching is a very simple technique to texture multicrystalline silicon. Low reflectance and very good surface passivation is possible. The DOSS solar cell process is able to take full advantage of this kind of surface texturing. The diffusion from a limited source can be tailored to obtain the desired sheet resistivity underneath the PS layer that will maximize the solar cell performance and has demonstrated excellent fill factors. Poor fill factors have been a problem in the past for further development of PS textured solar cells. This problem is completely overcome in this study which resulted in a 0.807 fill factor. The *in-situ* oxidation appears to completely oxidize the PS layer to obtain excellent surface passivation, and because the process does not require the removal of the phosphorus silicate glass after diffusion, which would remove the texturing, low reflection can be

maintained. The simplicity of the whole process can make the transfer into production easy and fast, leading to commercially available high efficiency multicrystalline silicon solar cells. Cell fabrication needs to be optimized, though, in order to realize the full potential of PS texturing.

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CHAPTER IX

LIGHT INDUCED DEGRADATION IN CZ, MCZ AND FZ SILICON CELLS FABRICATED BY FURNACE AND BELT LINE PROCESSING

9. Light Induced Degradation In Cz, Mcz and Fz Silicon Cells Fabricated By Furnace and Belt Line Processing

9.1 Introduction

Although Si grown by the Float Zone process is the highest quality silicon, Czochralski (Cz) grown silicon offers many advantages for cost effective solar cell fabrication because of lower cost and larger wafer size and a reasonably high quality single crystal substrate. In 1972, R.L. Crabb first observed a degradation in the minority carrier lifetime in 10 Ω cm Fz cell via a decrease in the long wavelength spectral response after photon illumination between 200-1000 nm over a period of 200 hours at 10 suns irradiation [1]. Then in 1973, Fischer and Pschunder observed a decrease in solar cell performance during the first few hours of illumination of 1 Ω -cm boron doped Cz Si. Light induced degradation (LID) of Cz material presents a problem for the overall performance of the finished solar cell [2]. Formation of interstitial oxygen (O_i) and boron (B_i) pairs after dissociation from a substitutional carbon (B_i-C_s) complex has been recently modeled as the source of LID [8]. Therefore, all boron doped silicon materials that have a high oxygen concentration should also suffer from LID. Multicrystalline Si was shown to degrade by Schmidt et. al. after a phosphorous gettering step, which raised the lifetime to a level that LID could be detected. Metallic impurities are generally not found in Cz materials and thus LID is readily observed. It has been shown that lifetime recovery of the light degraded samples is completely reversible by annealing the samples above $\sim 175^\circ\text{C}$ [5]. In addition, the degradation has been shown to be a strong function of B_i and O_i concentrations [8,9]. The degradation is found to decrease when higher temperature steps are used during cell fabrication, possibly pointing to oxygen precipitation, which reduces the O_i by forming clusters of oxygen [7].

Degradation is observed under forward bias and thermal treatments $\geq 100^\circ\text{C}$ as well as under light bias indicating that the effect is not a photon-activated event but results from excess carrier injection [6]. The degradation decreases the long wavelength response and results in lower V_{oc} , J_{sc} and cell efficiency due to the lower lifetime [2].

9.2 Objective

The objective of this chapter is to improve the fundamental understanding of LID and observe its impact on low-cost screen printed devices fabricated with furnace as well as belt line diffusion. Ten different crystals were used with various amounts of B and O. Fz and MCz crystals were used to reduce O_i content while Ga was used to replace B as the base dopant in some crystals.

9.3 Approach

Screen Printed (SP) devices reduce the production cost and shorten fabrication time, however, a 2% (absolute) loss in efficiency is incurred in the current SP cells as compared to photolithography (PL) cells. Single step furnace processing using the DOSS technique [14] and belt line processing (BLP) offer two viable solutions for high efficiency low cost solar cells. By using conventional furnace processing (CFP) methods, similar to the DOSS technique an in-situ oxide can be grown for passivation, along with the front and back diffusion. This STAR process reduces the number of high temperature steps. On the other hand BLP offers shorter fabrication time. The losses due to BLP compared with CFP are analyzed in this paper with special attention paid to light induced degradation in CZ, MCZ and FZ Si cells fabricated by both techniques.

9.4 Experimental

9.4.1 Cell Fabrication Techniques

Conventional Furnace Processing (CFP) Using DOSS Technique

- 1.1. RCA clean
- 1.2. Solid source preparation (spin-on phosphorous application 200°C)
- 1.3. Sample diffusion and oxidation 60 minutes and 7.5 minutes at 925°C respectively
- 1.4. SiN_x single layer AR coating by direct HF PECVD 300°C
- 1.5. Screen Printed Al BSF 860°C belt fired
- 1.6. Screen Printed Front metallization 760°C

Belt Line Processing (BLP)

- 1.7. RCA clean
- 1.8. Spin-on phosphorous applied to sample 150°C hot plate bake
- 1.9. Belt Line furnace diffusion 925°C 6 minutes
- 1.10 Spin-on glass removal, HF dip
- 1.11 SiN_x single layer AR coating by direct HF PECVD 300°C
- 1.12 Screen Printed Al BSF 860°C belt fired
- 1.13 Screen Printed Front metallization 760°C

9.5 Results and Discussion

9.5.1 FTIR Measurements

Table 9.1 shows the C and O content for all ten crystals used in this investigation. FTIR measurements showed no appreciable substitutional carbon (C_s) content in the boron-doped

samples. According to a recently proposed model by Schmidt and Aberle [3], B_iC_s pairs dissociate to form the more detrimental B_iO_i defect. Trap concentrations are estimated to be around $1 \times 10^{12} \text{ cm}^{-3}$, which is below the detection limit of the FTIR measurement at room temperature. Therefore bulk lifetime and cell efficiency degradation with light exposure time were used to detect and understand evolution of defect.

Table 9.1: Material specifications

<i>Measured at GT</i>					
Material	Thickness	$\rho(\Omega\text{cm})$	NA (cm^{-3})	O_i (ppma / atoms per cm^3)	C_s (ppma / atoms per cm^{-3})
1 Cz Boron	15.5 mils	0.72	2.20E+16	9.654 ppma / 4.827e17	0 ppma
2 Cz Boron	15.5 mils	0.70	2.23E+16	13.629ppma / 6.814e17	0 ppma
3 MCz Boron	15.5 mils	5.25	2.65E+15	9.618 ppma / 4.809e17	0 ppma
4 MCz Boron	15.5 mils	1.20	1.24E+16	1.258 ppma / 6.289e16	0 ppma
5 MCz Boron	15.5 mils	4.75	2.90E+15	1.829 ppma / 9.143e16	0 ppma
6 Fz Boron	15.5 mils	0.63	2.47E+16	0 ppma	0.07 ppma / 3.64e15
7 Fz Boron	15.5 mils	4.10	3.41E+15	0 ppma	0.07 ppma / 3.6e15
8 Cz Galium	10 mils	2.55	5.71E+15	12.01 ppma / 6.005e17	0 ppma
9 Cz Galium	10 mils	4.15	3.37E+15	14.772ppma / 7.386e17	0 ppma
10 Cz Galium	10 mils	33.30	4.04E+14	14.306 ppma / 7.135e17	0.04 ppma / 2.0e15

9.5.2 Effective Lifetime Measurements

As grown materials were first passivated by a 70nm SiN_x layer deposited in a direct plasma PECVD at 300°C. The samples were analyzed by PCD lifetime measurements after a FGA at 400°C for 15 minutes. Effective lifetime, τ_{eff} , values were plotted as a function of injection level. Then all the samples in Table 9.1 were degraded under light bias of

approximately 1 sun for more than 24 hours and re-measured. Figure 9.1 shows how the Boron doped Cz sample #1 with 10 ppma O_i degrades under light bias as a function of exposure time. Lifetime measurements were made every twenty minutes for the first hour then a final measurement was made for the stabilized degraded τ_{eff} after more than 24 hours of illumination. The number of traps is clearly seen to increase with the exposure time because of the τ_{eff} continually decreases until the saturation value is achieved for complete degradation. Sample degradation as a function of time occurs in both finished solar cells as well as un processed substrates.

9.5.3 Light Induced Efficiency Degradation Due to B_i and O_i

Table 9.1 shows the thickness, resistivity, C and O content, and the growth technique for the ten Si crystals used in this investigation. All ten samples were subjected to approximately 1 sun bias light at 25-27°C over various periods of time. Figures 9.1 and 9.2 show a graph of efficiency versus time for light degraded CFP and BLP solar cells. Boron doped Cz showed the most degradation in efficiency, dropping over 0.5% in absolute efficiency in less than three hours, regardless of cell processing technique. The Boron doped MCz (crystal #3) with the high O_i concentration also showed a slight degradation for both processes. Gallium doped Cz showed no degradation in spite of high O_i concentrations (Fig. 9.2). This indicates that Boron plays an important role in LID. The other two Boron doped MCz samples (#4 and 5) with low O_i concentration showed no degradation. Thus, by limiting the O_i concentration in a crucible grown sample, using the MCz growth technique no degradation is observed. This indicates that O_i also plays a key role in causing LID [13]. This is further supported by the fact that B doped FZ Si does not degrade because of the very low (undetectable) O_i concentration.

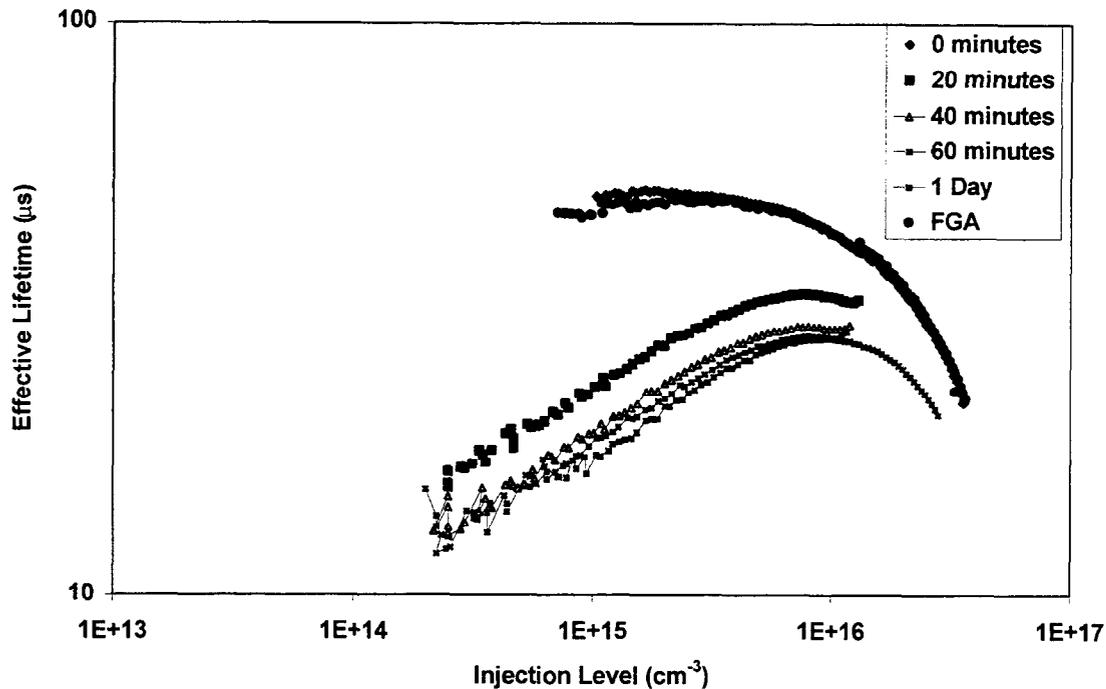


Fig. 9.1: Effective lifetime measured using Ron Sinton's lifetime tester. High O_i and B_i concentration cause up to 80% decrease in lifetime.

Figures 9.2 and 9.3 show that the overall degradation is similar for both cell technologies, CFP/SP and BLP/SP. The low resistivity samples Cz1 and Cz2 ($0.6 \Omega\text{-cm}$) degrade 1% absolute in efficiency for both processes. The reduced B_i in the MCz 3 sample ($5 \Omega\text{-cm}$, $9.6 \text{ ppma } O_i$) sample due to the higher resistivity, resulted in a less severe efficiency decline of around 0.3% absolute. This indicates that LID trap concentration, N_t , is related to B_i . The direct correlation between O_i concentration N_t can also be seen in MCz samples. MCz3 and MCz5 samples have approximately equal B_i concentrations but MCz5 has an order of magnitude lower O_i concentration and as a result MCz5 sample shows no degradation.

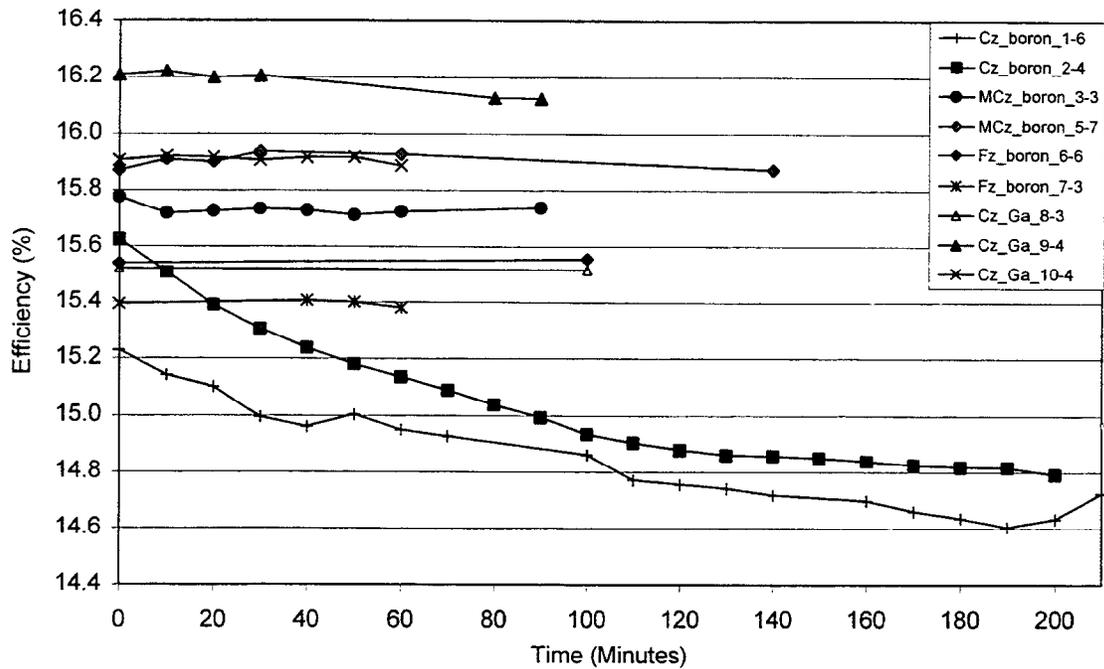


Fig. 9.2: Efficiency degradation of screen-printed BLP solar cells. Samples 1-7 are boron doped and 8-10 Ga doped according to table 9.1.

9.5.4 Role of Ga Doping and MCz Growth in Eliminating Light Induced Degradation

Many of the samples analyzed in this study showed no degradation (Fig. 9.1). Fz samples and Ga doped Cz material showed no decrease in either cell performance or initial lifetime values]. Boron doped magnetically grown Czochralski, MCz, showed degradation only when the O_i concentration reached 10ppma. Figure 9.4 shows the annealed and degraded τ_{eff} for 4 different samples of similar base resistivity, 4-5 Ωcm , Ga or B doped, but varying O_i concentrations. Only the Cz sample containing both B_i and O_i showed any degradation after 24

hours of 1 sun illumination. However, the Ga doped Cz sample with high O_i concentration showed no degradation. Therefore the degradation is not inherent to the Cz process which traditionally contains high O_i concentrations. It is also apparent from the B doped MCz sample with the low oxygen concentration that B alone does not cause the degradation. However, the MCz sample with high O_i not shown in Fig. 9.4, does show same degradation, re-affirming that both B_i and O_i need to be present for degradation. This can be seen in Figs. 9.2 and 9.3. The increase in τ_{eff} for samples that do not show any degradation in Fig. 9.4, is currently being investigated and is believed to be the result of enhanced surface passivation due to the light exposure. The SiN_x layer used for passivation achieved as low as 4 cm/s surface recombination velocity on the Ga doped 33 Ω -cm Cz sample at low 1×10^{14} injection level.

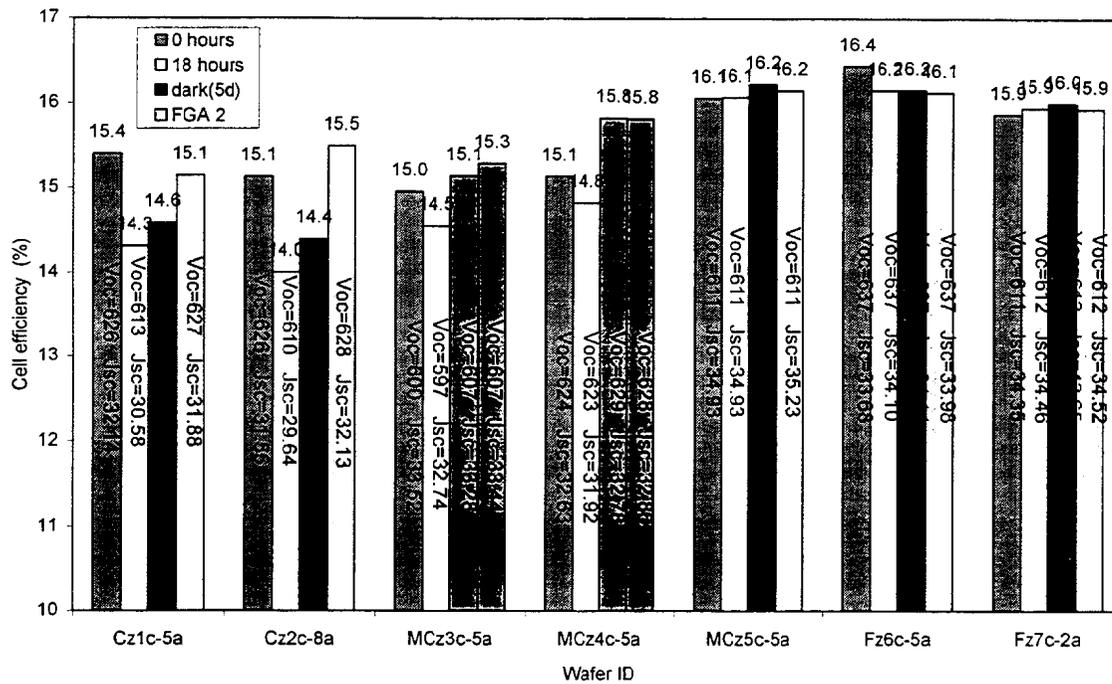


Fig. 9.3: Efficiency map of samples over a period of time initially after a FGA followed by light induced degradation then room temperature anneal in the dark for 5 days and finally another FGA at 450°C of the CFP cells.

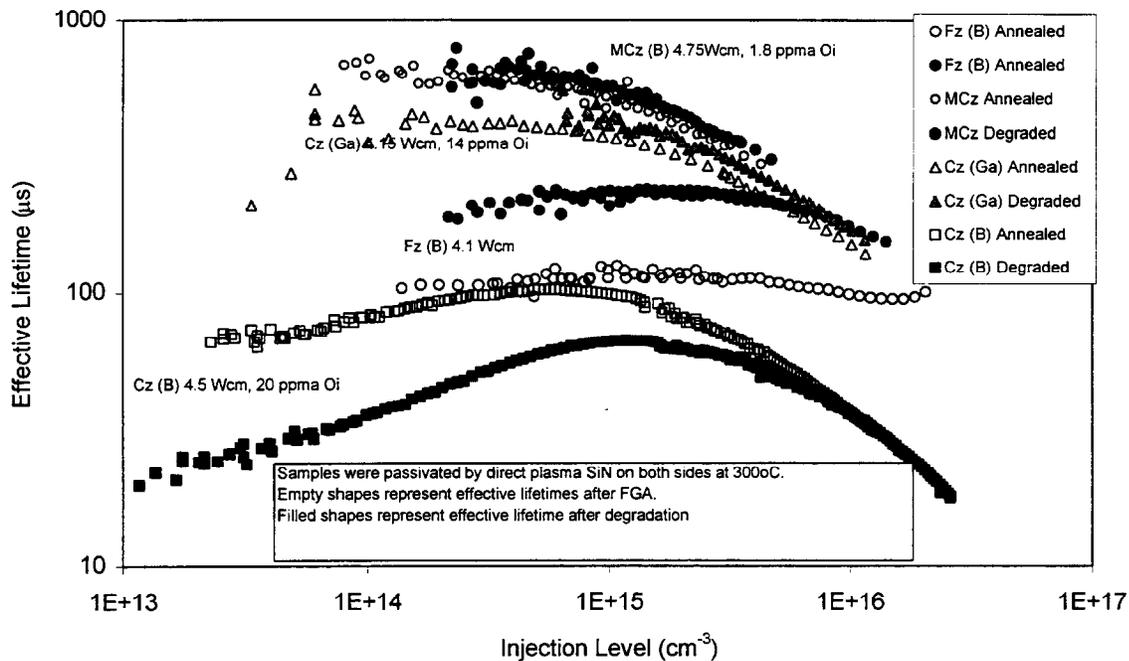


Fig. 9.4: Effective lifetime for 4-5 Ω -cm samples before and after degradation. Only samples with both high Oi and Bi content showed any degradation.

Figure 9.3 shows that the overall degradation of the finished solar cells was 8-10% of the initial values. This is similar to the degradation observed in the much higher efficiency cells (+20%) fabricated at Fraunhofer. Therefore the same amount of light exposure results in higher final efficiency of Fraunhofer cells. This suggests that the higher efficiency cells made at Fraunhofer perform better after LID either due to advanced cell features or due to lower light induced trap concentration because of the higher temperature processing. Oxide precipitation during high temperature processing has been suggested to reduce degradation [5].

The two technologies (CFP and BLP) used to fabricate cells in this study gave similar starting efficiencies and showed similar amount of LID. This may be the result of a lower

thermal budget and lower temperature processing used for both technologies which may not alter the basic material characteristics, such as O_i concentration.

9.6 Conclusion

This study shows that light-induced degradation occurs only when both B_i and O_i are present in sufficient quantity. Boron doped FZ and low O_i MCz, Boron doped Cz, and Gallium high oxygen Cz samples analyzed in this paper clearly support the above observation. Samples with same oxygen concentration but higher resistivity showed lower degradation, due to a limited supply of B_i available to form the trap level that causes the efficiency degradation. Gallium (Ga) doped samples showed no degradation regardless of the C_s and O_i content. MCz growth was able to limit the degradation by allowing lower O_i content. This provides a means to achieve a more stable performance while still taking advantage of the Crucible growth method. Cz cells efficiencies were lower than FZ and MCz. However, low oxygen MCz cell efficiency was comparable to FZ cells Thus Ga doped MCz offers a great opportunity of low-cost high efficiency cells with no light induced degradation.

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CHAPTER X

***INTEGRATION OF RAPID
PROCESS TECHNOLOGIES FOR
HIGH EFFICIENCY SILICON
SOLAR CELLS***

10. Integration of Rapid Process Technologies for High Efficiency Silicon Solar Cells

10.1 Introduction

In the previous chapters we demonstrated a methodology for achieving high fill factors for screen-printed solar cells, rapid and improved formation of emitter and back surface field, and development of a novel and very effective RTO/SiN stack passivation for front and back surfaces which can also withstand screen-printed firing. In this chapter we show the integration of these rapid technologies for achieving high efficiency cells on mono-crystalline silicon.

Figure 10.1 shows the fabrication sequence of a baseline cell using conventional furnace processing (CFP) and photolithography contacts. In this process phosphorous diffusion, Al back surface field formation, and front oxide passivation was done in conventional furnace, resulting in about 5½ hours of high temperature processing. Metal evaporations and photolithography took another 7½ hours, resulting in a total cell processing time of about 16 hours with mono-crystalline cell efficiencies of about 18% (Fig.10.1) without any surface texturing.

The above process was modified by replacing furnace processing by rapid thermal processing (RTP) in which phosphorous diffusion, screen printed Al BSF formation, and oxide passivation was done in a single wafer RTP system from AG Associates. Front and back contacts were formed by evaporation and photolithography. Figure 10.2 shows the detailed process sequence and the corresponding cell performance. Phosphorous diffusion was performed in about 3 minutes by heating the silicon wafers, coated with appropriate spin-on film, under the tungsten halogen lamps. Al back surface field was formed by screen printed Al on the back followed by RTP in an oxygen ambient. Besides forming a very effective and deep BSF, this step also produced a high quality rapid thermal oxide on the front simultaneously. Thus, this RTP

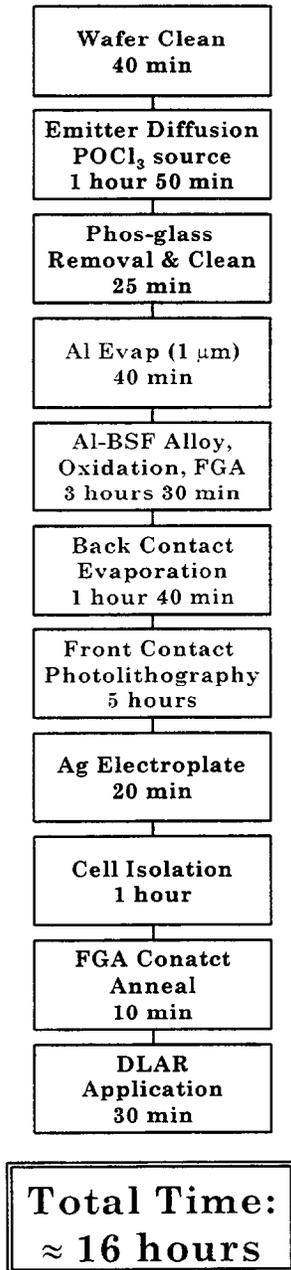
process sequence reduces the total high temperature processing time from 5½ hours (furnace processing in Fig.10. 1) to less than 10 minutes (Fig. 10.2). In addition to reducing the total processing time from 16 hours to 8½ hours, this RTP process produced higher efficiency cells compared to conventional furnace processing. The RTP cell efficiencies of 19.1% were achieved compared to 18% for the CFP cells. This is primarily due to the superior and more uniform RTP SP Al back surface field. As shown in chapter 4, 1 µm evaporated Al BSF formed in conventional furnace, using typical slow ramp up rate, is not uniform and effective.

The above process was modified again by replacing evaporation and photolithography contacts by screen-printed contacts. As indicated in chapter one, we had to reduce the sheet resistance from 80 Ω/□ to 40 Ω/□ to achieve good contacts and high fill factors. Figure 10.3 shows the modified process sequence along with the cell performance. This RTP/SP process reduced the cell processing time from 8.5 hours to less than 2 hours and produced a cell efficiency of 17% without any texturing on mono-crystalline silicon. Notice that we were able to achieve a fill factor of 0.798 on this screen-printed cell. The 2% reduction in absolute efficiency (19% to 17%) is largely attributed to heavy doping effects in the emitter, increased shading and reflectance, and somewhat inferior front surface passivation due to higher surface doping concentration. We are investigating the formation of selective emitter ($\leq 40 \Omega/\square$ underneath the grid and $\geq 80 \Omega/\square$ between the grid lines) for SP cells which should be able to recover majority of the 2% loss in efficiency.

Above cells were fabricated in a single wafer RTP system. Since there is no continuous RTP system available today, we have started modifying continuous belt line processing (BLP) to bridge the gap between RTP and BLP cells. Our initial results look quite encouraging. Figure 10.4 shows that phosphorous diffusion in belt line furnace is slower than in RTP. This is

probably because of the reduced number of high-energy photons in the BLP. A 965°C/12-min phosphorous diffusion in belt furnace gave a junction depth of 0.4 μm as opposed to 0.9 μm in the single wafer RTP system. Therefore, an attempt to keep the phosphorous diffusion time to about 6 min, we had to raise the diffusion temperature from 890°C to 925°C to achieve 45 Ω/\square emitter in BLP. We also gave up RTO for emitter passivation and decided to use direct PECVD SiN on top of the emitter for passivation as well as AR coating. Screen-printed Al BSF was formed in 2 min in the belt furnace at 860°C. Finally the SP silver contacts on the front were fired through the SiN layer. Figure 10.5 shows the detailed belt-line process sequence and corresponding cell efficiency on mono-crystalline silicon. Total belt line processing time was less than 2 hours, which resulted in a cell efficiency of 17% on float zone silicon. This is virtually identical to what we obtained by single wafer RTP (Fig. 10.3).

In an attempt to exploit the full potential of the stack passivation, which gives surface recombination velocity of less than 20 cm/s on bare silicon surface, we have started investigating bifacial cells. Figure 10.6 shows the opportunity and challenge in fabricating gridded back screen-printed cell. Gridded back screen printed cells can simplify cell processing by permitting co-firing of contacts on both sides, prevent wafer warping due to full Al BSF if thin material (\cong 100 μm) is used, offer hydrogenation of defects from both sides due to the presence of SiN, and enhance the cell efficiency due to lower BSRV. The challenge is keep the series resistance and contact recombination small. Model calculations in Fig.10.7 show that 100 μm thick cell with a bulk lifetime of 20 μs can produce 17% efficient screen-printed cells without surface texturing, if the back surface recombination velocity is reduced to 100 cm/s. This approach can transform 12-15% efficient industrial cells on 300 μm thick Si today to greater than 17% cells on 100-200 μm thick silicon in the future.



17.3% on FZ 2.3 Ω-cm
17.8% on FZ 1.3 Ω-cm
18.2% on FZ 0.65 Ω-cm

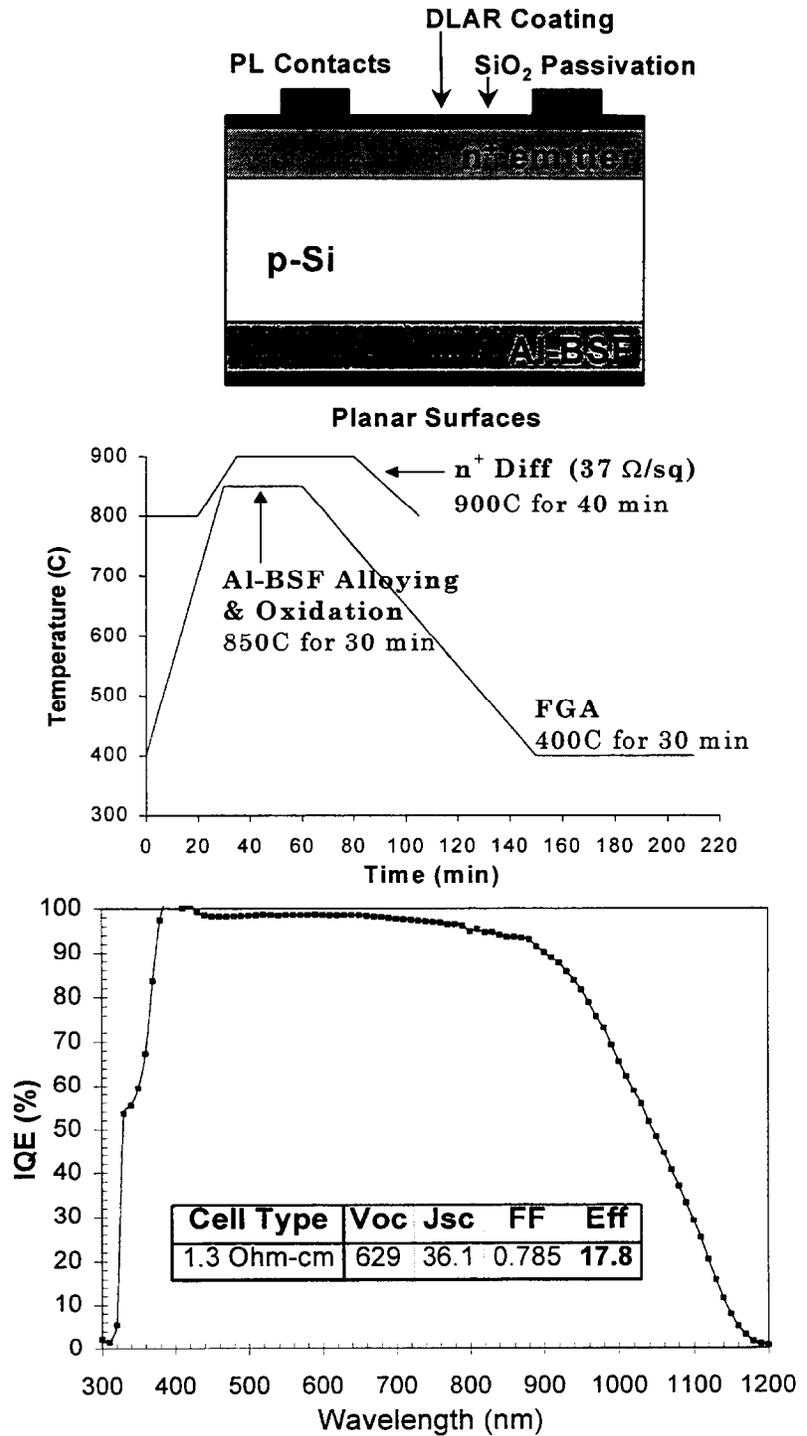
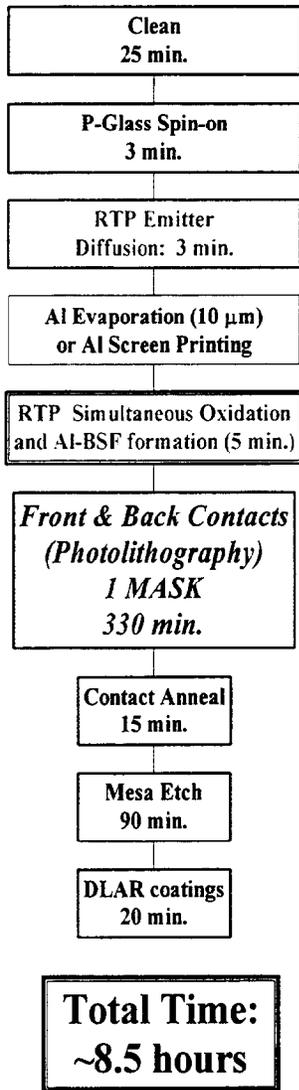


Figure 10.1: Baseline cell process sequence by conventional furnace processing and photolithography.



Best Cells:
 19.1% FZ
 18.4% Cz
 16.7% Solarex mc-Si

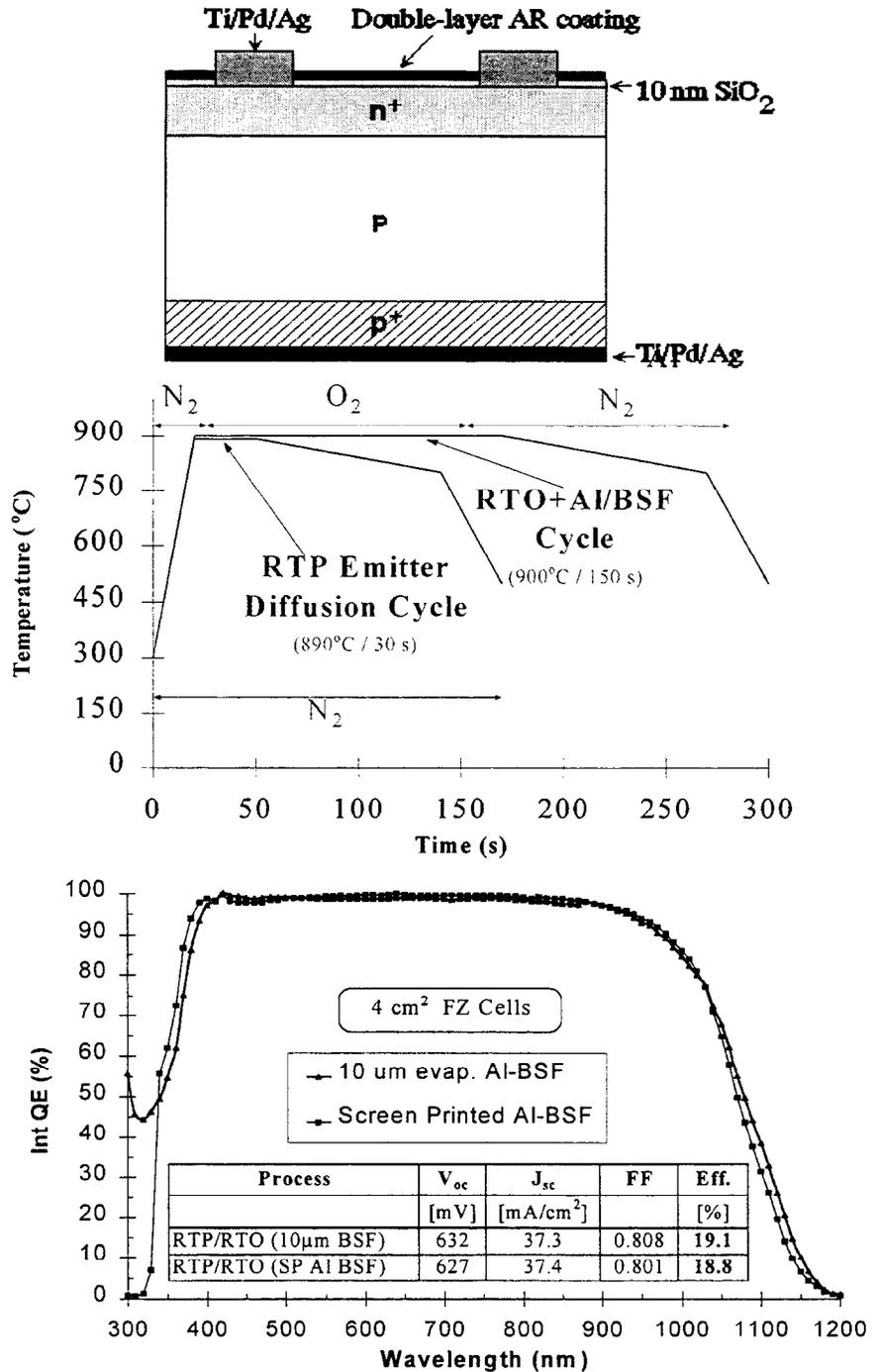


Figure 10.2: Rapid Thermal Processing (RTP) of cells with photolithography contacts

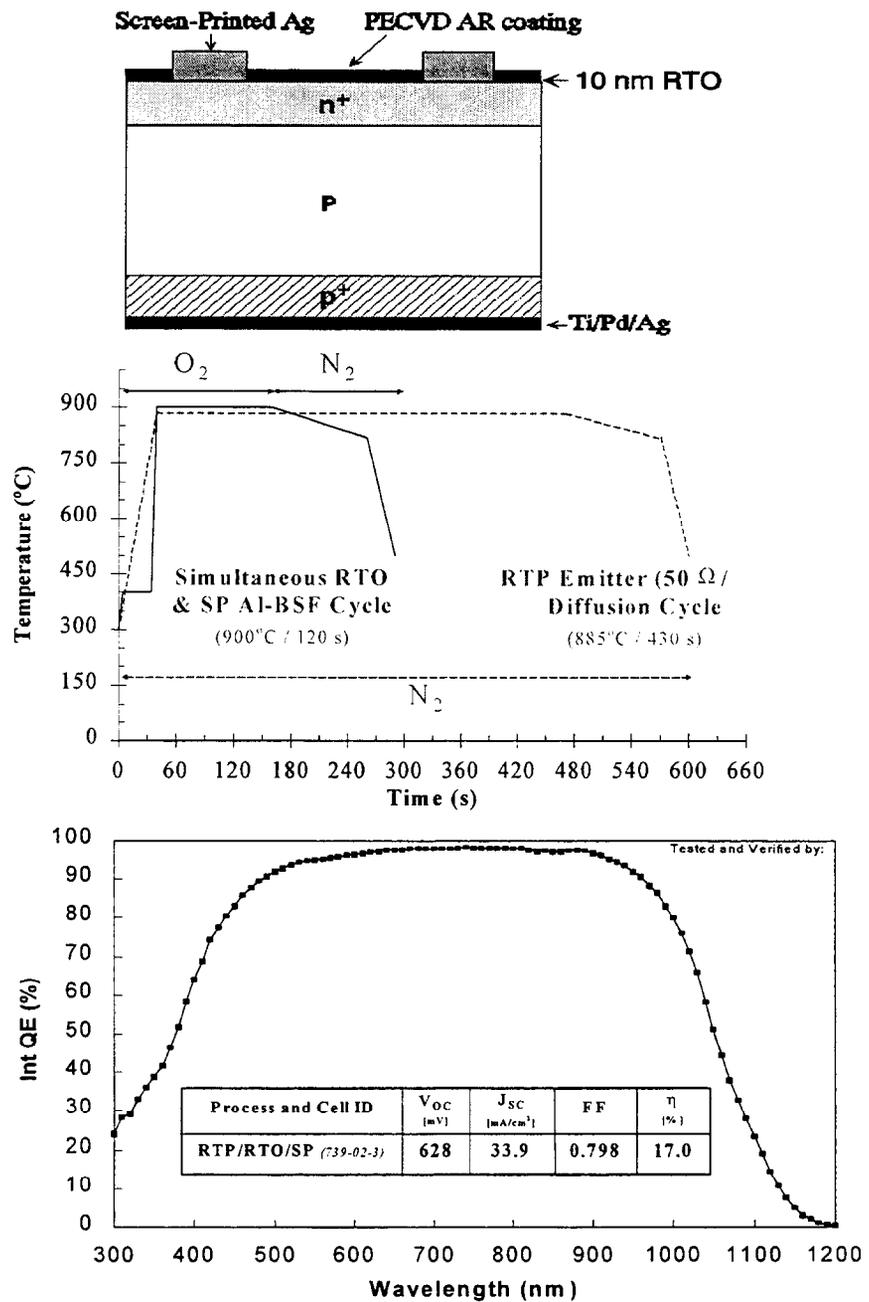
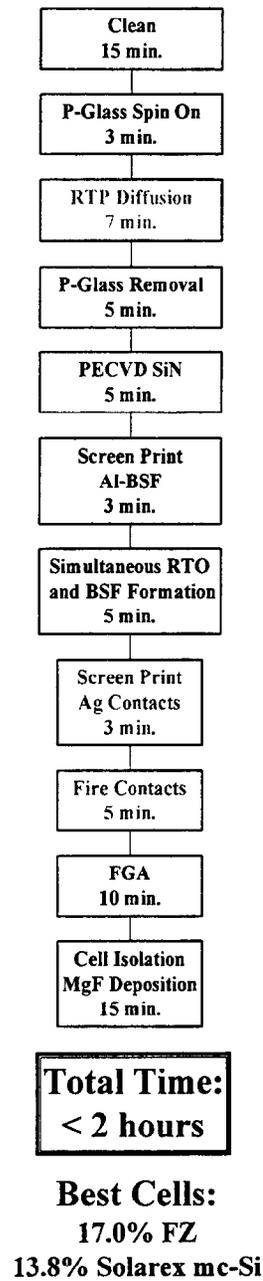


Figure 10.3: Rapid Thermal Processing of Cells with Screen-Printed Contacts

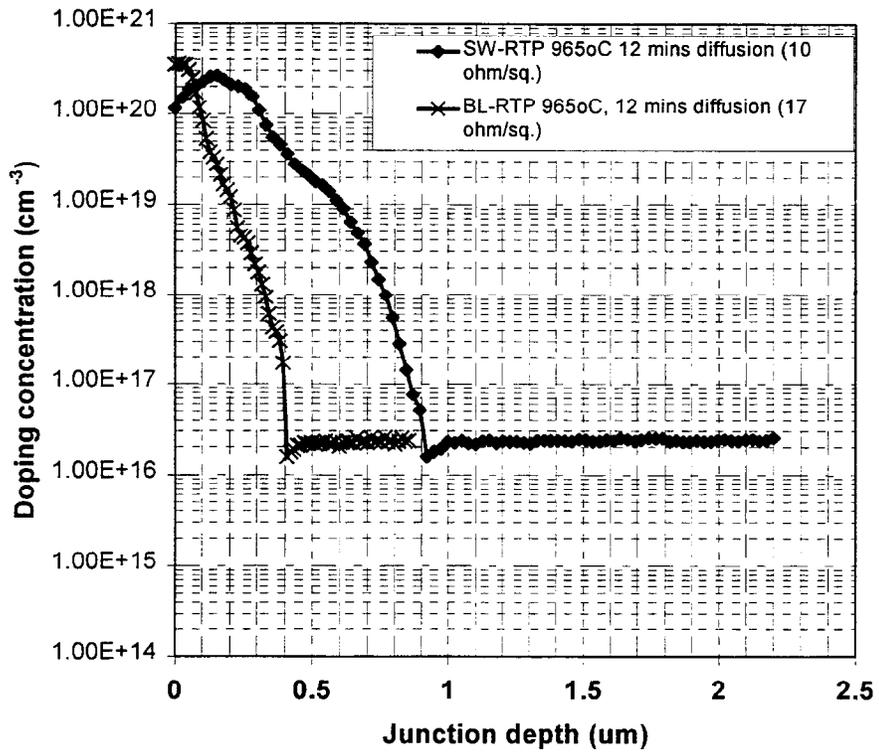
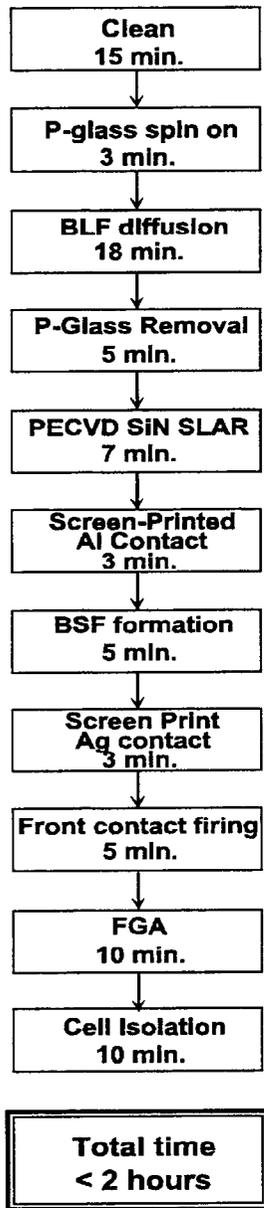


Figure 10.4: Comparison of the effective diffusivity of phosphorous in single wafer and BLP emitters at 965°C for 12 minutes.



**Best Cells:
17.0% FZ**

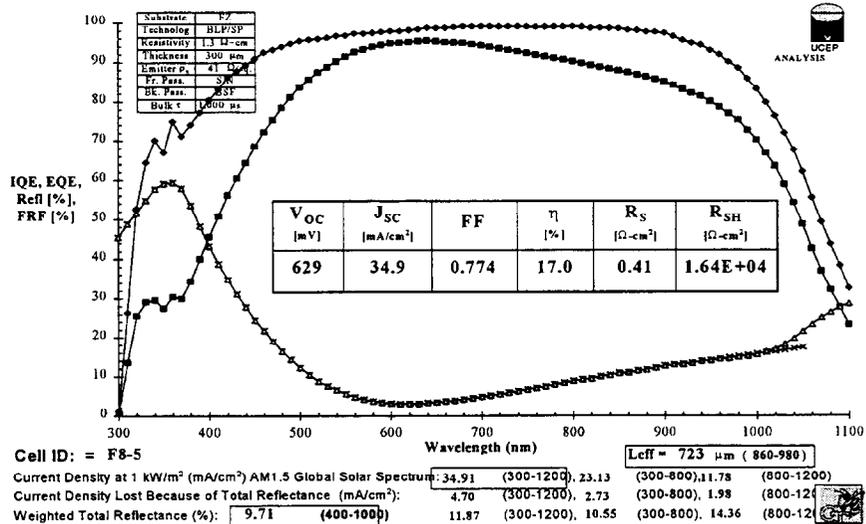
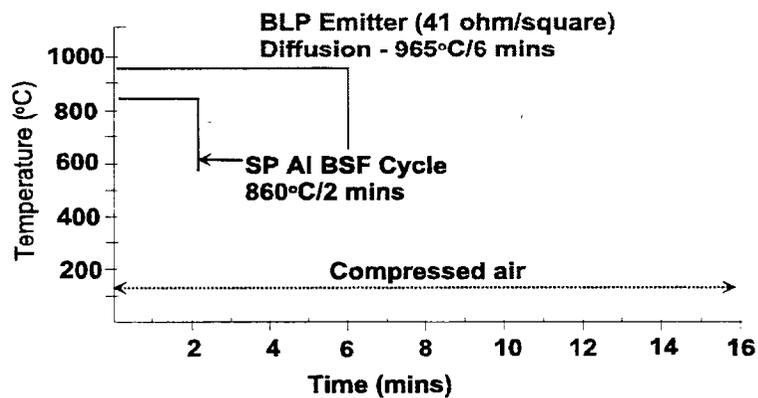
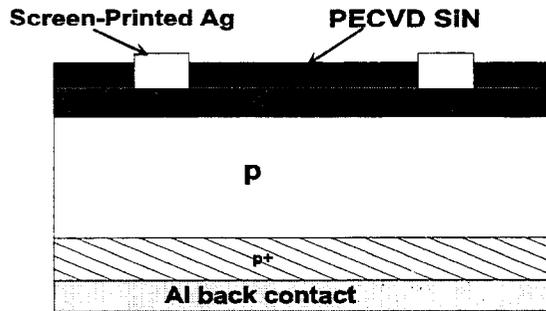
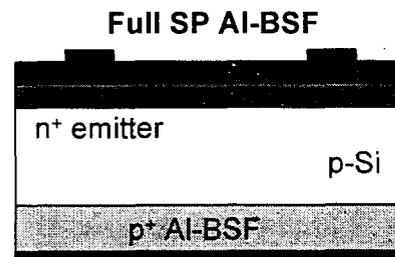
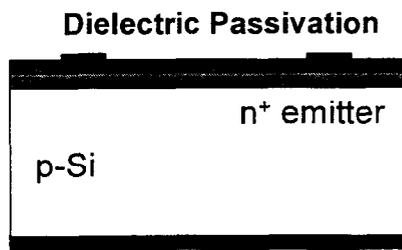


Figure 10.5: Belt line Processing of cells with screen-printed contacts



Advantages:

- No warping for thin wafers
- Lower surface recombination velocity
- Possibility of hydrogenation from the SiN on the back side
- Bifaciality

Challenges:

- Series resistance
- Contact recombination

Figure 10.6: Dielectric Passivation with Gridded Back Contacts vs Full Screen-Printed Al BSF.

(Model Calculations)

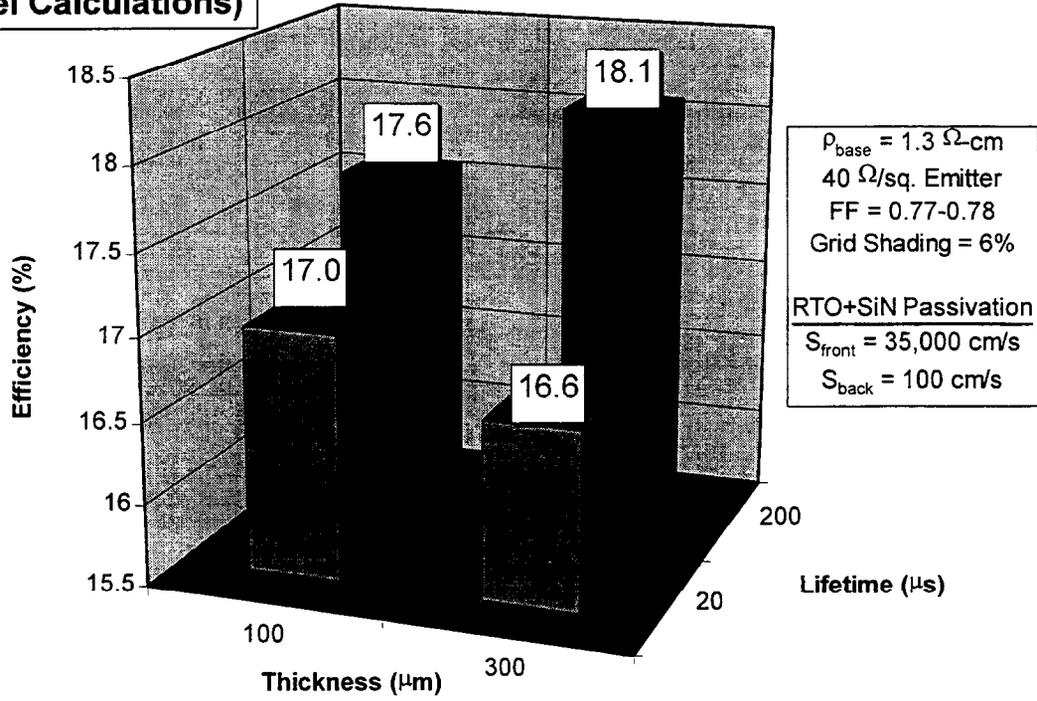


Figure 10.7: Modeling of Screen-Printed solar cells as a function of thickness and lifetime with S_{back} of 100 cm/s

Summary of Accomplishments

RESEARCH ACCOMPLISHMENTS OF THE GEORGIA TECH PV CENTER

- **Fabricated 4 cm² 20% FZ cells and 18.5% CZ planar cells by CFP/PL**
- **Fabricated 42 cm² 18.1% planar CFP/PL CZ cells**
- **Fabricated record high 18.6% planar multicrystalline CFP/PL Si solar cell**
- **Fabricated record high 16% EFG sheet Si CFP/PL cell**
- **Fabricated 4 cm² record high 16.2% string ribbon CFP/PL cell**
- **Fabricated 20% efficient FZ and 19.1% efficient CZ “STAR” cell**
- **Fabricated record high 19.3% rapidly processed RTP/PL FZ Si cells, and 18.5%-19% CZ and MCZ cells**
- **Fabricated 4cm² record high 17.3% dendritic web RTP/PL cell**
- **Fabricated 4cm² record high 17.6% low-cost screen printed planar Si solar cells**
- **Fabricated screen printed bifacial cells with record high rear illumination efficiency of 11-13%**

- **Fabricated ~17% 4cm² monocrystalline silicon cells by a low-cost manufacturable process using screen printing, beltline diffusion and PECVD SiN**
- **Fabricated 4 cm² 14.9% efficient belt-line screen printed manufacturable cell on String Ribbon silicon**
- **Fabricated 4 cm² 14.3% manufacturable n-type phostop, and 14.2% p-type BLP/PECVD/SP cells on dendritic web silicon**
- **Fabricated 100 cm², 15.1% efficient belt-line/RTP/SP cell on EFG Si**
- **Pioneered the field of RTP which reduces the cell processing time from 16 hrs to 2 hrs.**
- **Developed a novel “STAR” technology for simultaneous front and back diffusion and oxidation in a single furnace step**
- **Developed a rapid Al BSF which reduces back surface recombination velocity to 200 cm/s on 2 ohm-cm cells**
- **Developed a screen printing process that can produce very high fill factors of 0.795 on monocrystalline silicon**
- **Developed SP process to achieve 0.76-0.77 FF on mc-Si cells**
- ◆ **Developed a novel and very effective RTO/SiN stack for passivating silicon surfaces which reduces the surface recombination velocity to less than 20 cm/s, and can also withstand screen printing firing**
- **Developed and optimized manufacturable gettering and passivation techniques, including Al-enhanced hydrogen**

passivation, to achieve $>25 \mu\text{s}$ lifetime in most commercial substrates

- **Maintained and monitored 342 kW rooftop grid-connected PV system on the Georgia Tech Aquatic Center roof, which has so far produced more than one billion watt hr of electrical energy**

EDUCATIONAL ACCOMPLISHMENTS OF THE GEORGIA TECH PV CENTER

- **Taught one course (EE 64456) on Solar Cells each year**
- **Provided hands-on training to students in the area of modeling and fabrication of solar cells**
- **Graduated 10 Ph.D students and trained 10 more**
- **Trained more than 10 undergraduate students, including some from historically black colleges/universities**
- **Participated in graduate student exchange program with ISFH and Fraunhofer Institute**
- **Published 44 refereed journal papers, 42 refereed proceeding papers, and presented 21 invited presentations**
- **Awarded 4 United States patents**
- **Received Georgia Tech's best Thesis Award on the thesis pertaining to "Rapid Thermal Processing (RTP) of Silicon Solar Cells"**
- **Received SIAC Best Paper Award on the research on "Fundamental Understanding and Development of Screen Printed RTP Al BSF"**
- **Received Best Poster Paper Award – 1995 Nice, France, EUPVSC**

- **Received Best Poster Paper Award – 1996 Anaheim, CA, PVSC**
- **Received Best Special Paper Award – 1999 Japan, PVSEC**

PUBLICATIONS AND PRESENTATIONS

October 1996 – October 2000

- **44 JOURNAL PUBLICATIONS**
- **42 PROCEEDINGS PUBLICATIONS**
- **21 INVITED PRESENTATIONS**
- **4 US PATENTS**

SOLAR CELL COURSE OUTLINE

- I. Solar Cells and Sunlight**
 - A. The photovoltaic vision
 - B. Physical source of sunlight, solar constant and insolation data.
 - C. Direct and diffuse radiation

- II. Review of Semiconductor Properties**
 - A. Dynamics of electrons and holes
 - B. Generation and Recombination processes in semiconductors
 - C. Interaction of sunlight with semiconductors.
 - D. Reflectance and absorption of light.

- III. Junctions and Operating Principles of Solar Cells**
 - A. Homo and hetero-junctions
 - B. Dark and illuminated characteristics of solar cells
 - C. Internal quantum efficiency of solar cell
 - D. Equivalent circuit of solar cells
 - E. Solar cell output parameters

- IV. Efficiency Limits and Losses in Solar Cells**
 - A. Efficiency limits for black-body cells
 - B. Short-circuit current losses
 - C. Open-circuit voltage losses
 - D. Fill factor losses
 - E. Effect of temperature on cell performance
 - F. Practically achievable efficiency limit

- V. Silicon Solar Cell and Module Fabrication**
 - A. Promising photovoltaic silicon materials
 - B. Baseline silicon solar cell fabrication
 - C. Processing of advanced silicon solar cells
 - D. Photovoltaic module construction

- VI. Design of High Efficiency Silicon Solar Cells**
 - A. Surface recombination velocity and spectral response considerations
 - B. Heavy doping effects, junction depth, and emitter doping profile considerations.
 - C. Substrate doping, thickness and diffusion length considerations

- D. Grid design
- E. Back surface field design
- F. Antireflection coating design
- G. Textured surfaces for light trapping

VII. Heterojunction, Thin-Film and Other Promising Solar Cells

- A. Gallium arsenide solar cells
- B. Amorphous silicon thin-film solar cells
- C. Polycrystalline thin-film CdTe and CuInSe₂ cells
- D. Multijunction solar cells
- E. Concentrator cells

VIII. Photovoltaic Systems and Applications

- A. Stand alone PV Systems
- B. Utility-interactive PV systems
- C. Modeling and design of PV systems
- D. PV in buildings
- E. Cost analysis and future of PV systems

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