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W88 Integrated Circuit Shelf Life Program

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W88 Integrated Circuit Shelf Life Program

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Abstract

The W88 Integrated Circuit Shelf Life Program was created to monitor the long term performance, reliability characteristics, and technological status of representative WR ICs manufactured by the Allied Signal Albuquerque Microelectronics Operation (AMO) and by Harris Semiconductor Custom Integrated Circuits Division (CICD, Melbourne, FL). Six types of ICs were used. A total of 272 ICs entered two storage temperature environments (room ambient and +125 °C). The program began in 1989. Electrical testing and destructive physical analysis were completed in 1995.

During each year of the program, the ICs were electrically tested and samples were selected for destructive physical analysis (DPA). ICs that failed electrical tests or DPA criteria were analyzed. Fifteen electrical failures occurred, with two dominant failure modes: electrical overstress (EOS) damage involving the production test programs and electrostatic discharge (ESD) damage during analysis. Because of the extensive handling required during multi-year programs like this, it is not unusual for EOS and ESD failures to occur even though handling and testing precautions are taken. The clustering of the electrical test failures in a small subset of the test operations supports the conclusion that the test operation itself was responsible for many of the failures and is suspected to be responsible for the others. Analysis of the electrical data for the good (nonfailing) ICs found no significant degradation trends caused by the storage environments. Forty-six ICs were selected for DPA with findings primarily in two areas: wire bonding and die processing. The wire bonding and die processing findings are not surprising since these technology conditions had been documented during manufacturing and were determined to present acceptable risk. The current reliability assessment of the W88 stockpile assemblies employing these and related ICs is reinforced by the results of this shelf life program.

Data from this program will aid future investigation of 4/3 micron or MNOS IC technology failure modes. The remaining ICs will be retained as a unique and valuable resource for future stockpile evaluation and failure analysis efforts.

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Many people have been involved in this project, including those who contributed to the initial planning, those who worked on obtaining the ICs, those who implemented the storage and testing, and those who participated in the review and documentation of the results. The following is a partial list of the people who have been involved in this program.

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AS/KCD (now FM&T/KC): Urah Brown, Mike Diehl, and John Minihan.

SNL: Rich Anderson, Bill Dawes, Ted Dellin, Ed Graham, Cliff Evans, John Middleton, Bill Miller, Tim Mirabal, Bob Rieden, Bob Simpson, Jerry Soden, John Schwartz, and Charles Trauth.

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Summary

The W88 Integrated Circuit Shelf Life Program was created to monitor the long term performance, reliability characteristics, and technological status of representative WR ICs manufactured by the Allied Signal Albuquerque Microelectronics Operation (AMO) and by Harris Semiconductor Custom Integrated Circuits Division (CICD, Melbourne, FL). Six types of ICs were used. A total of 272 ICs entered two storage temperature environments (room ambient and +125 °C). The program began in 1989. Electrical testing and destructive physical analysis were completed in 1995. This report reviews the planning, procedures, findings, conclusions, and recommendations for this program.

ICs entering the shelf life program were of WR quality and were selected from production lots also used for WR system deliveries. Therefore, the shelf life program ICs were completely representative of the ICs that were assembled in W88 electronic assemblies. The availability of each IC type varied during each year of the shelf life program, so the quantities of each type were not all equal at the end of the program. During each year of the program, the available ICs were electrically tested and samples were selected for and submitted to destructive physical analysis (DPA). ICs that failed electrical test requirements or DPA criteria were analyzed.

The electrical testing resulted in a total of 15 failures. There appear to be two dominant failure modes, both of which involve test-induced damage to the ICs. One is electrical overstress damage that implicates the test process employed during testing for the shelf life program. The 4/3 micron and MNOS technologies are known to be susceptible to oxide breakdown and snapback failure mechanisms, so there was a predisposition for these ICs to fail in this manner when accidentally overstressed. Clustering of the electrical test failures in a small subset of the test operations also supports the conclusion that the test operation itself was responsible for many of the failures and is suspected to be responsible for the others. The other dominant failure mode is electrostatic discharge damage, which appears to have occurred during analysis of two of the failures. Analysis of the electrical data for the good (nonfailing) ICs indicated that there were no significant degradation trends caused by the storage environments.

Forty-six ICs were subjected to DPA with findings primarily in two areas: wire bonding and die processing. The wire bonding finding is a result of observations of poor bondwire clearance, poor bondfoot thickness, low bond pull strength, disturbed bondwires, and bondfoot cracks. The die process finding involves overetching and trenching of polysilicon and silicon due to low contact window area coverage by metal. Both of these have the potential to be reliability risks in the presence of other contributing factors. However, the wire bonding and die processing findings are not surprising since these technology conditions had been documented during manufacturing and were determined to present acceptable risk. Also, the criteria for acceptable wire bonding and die processing used during DPA were more critical than the criteria used during manufacturing. These criteria involve bondwire clearance from the die, bondfoot thickness, and contact window coverage by metal (discussed in detail in DPA Findings section VI).

The number of failures of electrical tests and DPA inspections during this shelf life program were higher than anticipated. However, analysis of these failures supports the conclusion that most, if not all, of the failures were either caused by the shelf life program activities themselves

or were due to the observation of known pre-existing conditions that, to varying degrees, have been previously investigated and determined to present acceptable risk. The current reliability assessment of the W88 stockpile assemblies employing these and related ICs is reinforced by the results of this shelf life program. It is also very important to observe that there have been no known failures of these ICs in any WR stockpile assembly. This is particularly significant for the W88, since each MC3811 programmer in the active stockpile is operated several times each year.

The remaining shelf life program ICs will be retained as a unique and valuable resource for future stockpile evaluation and failure analysis efforts. The 211 ICs remaining at the end of this program will be retained by the SNL Failure Analysis Department to support WR stockpile evaluation activities.

The following is a recommendation that results from this program.

Data from the W88 Integrated Circuit Shelf Life Program will be helpful for any future investigation of the failure modes of the 4/3 micron or MNOS IC technologies. The investigation of any failure or abnormal behavior of any W88 or other WR assembly IC from the 4/3 micron (Harris or SNL/AMO) or MNOS technologies should include a determination of whether such behavior involves the failure modes and mechanisms evaluated in the shelf life program. This includes the 4/3 snapback, MNOS oxide breakdown, and bond wire strength and clearance issues as described in this report. Although it is not expected, if evidence is found during stockpile testing or other activities of occurrences that relate to the shelf life program observations, then it is highly recommended that the reliability estimate for WR assemblies that contain these ICs be carefully reevaluated.

W88 Integrated Circuit Shelf Life Program

I. Introduction

The W88 Integrated Circuit Shelf Life Program was created to monitor the long term performance, reliability characteristics, and technological status of representative WR ICs manufactured by the Allied Signal Albuquerque Microelectronics Operation (AMO) and by Harris Semiconductor Custom Integrated Circuits Division (CICD). The program was operated by the AMO Quality Assurance organization and was later transferred to Allied Signal/Kansas City Division (AS/KCD, now Allied Signal FM&T/KC). A Shelf Life Program Committee was established to assure that coordinated recommendations and decisions were made regarding the scope and nature of this program. The committee was composed of representatives from each of the following organizations plus ad hoc members as required: AMO Quality Assurance (chairman), AMO Product Engineering, AMO Failure Analysis and Yield Enhancement, SNL IC Technology, SNL Failure Analysis, and SNL Weapons Evaluation. W88 ICs of six circuit types were selected from AMO and Harris WR production lots, based on availability, and subjected to a multi-year storage environment (room ambient and +125 °C temperatures). Annually, these ICs were electrically tested and samples were selected for destructive physical analysis. This report reviews the planning, procedures, findings, conclusions, and recommendations for this program.

II. Background

Planning for the shelf life program began in 1987. Meetings were held in the latter part of 1987 that described the general concepts and laid the foundation for the program. During 1988 and the first part of 1989, the details for the program were defined. During mid-1989, the types of ICs to be used were identified and their procurement began. The controlling document, Shelf-Life Program Specification BB390133, was created and IC testing began.

The objectives of the W88 Shelf Life Program were to:

- A. Measure the electrical performance and physical characteristics of a representative cross-section of W88 ICs as a function of time in two storage environments that were selected to bound the failure mechanism acceleration factors anticipated during weapon use conditions;
- B. Analyze trends and understand time-dependent variations (including failures) in these ICs as a function of storage time;
- C. Use this understanding to forecast potential problem areas and solutions prior to possible impact on customers;
- D. Maintain a reserve of representative, critical materials over the lifetime of their use that would be available for failure analysis or other studies, if this should prove necessary, based on either the results obtained from this program or those obtained from the SNL weapons evaluation program.

The ICs that entered the shelf life program were of WR quality and were selected from production lots also used for WR system deliveries. Therefore, the shelf life program ICs were completely representative of the ICs that were assembled in W88 electronic assemblies. The availability of each IC type varied due to production schedules during each year of the shelf life program, so the quantities of each type were not all equal at the end of the program.

The IC storage environments were chosen to be similar to that experienced in the Trident II application. Unpowered storage in both room temperature and +125 °C (the high temperature of the IC test specification) ambients simulated the use conditions reasonably well and were relatively easy to implement. Prior to being put into the storage environment, the ICs were subjected to a brief dynamic screen to simulate the War Reserve (WR) component manufacturing and acceptance process. Calculations by W. M. Miller, manager of SNL Reliability Physics Department 1276, indicated that subjecting the ICs to the dynamic screen environment (being used in production at that time for certain types of ICs) for 7 hours would simulate the manufacturing and acceptance conditions experienced by WR ICs. Following the dynamic screen, the ICs were electrically retested before entering the storage phase of the shelf life program.

The major goals of the program were accomplished through annual electrical testing of the stored ICs and Destructive Physical Analysis (DPA) of selected ICs from those in storage. ICs that failed electrical test requirements or DPA criteria were analyzed. Table 1 summarizes the information for the ICs that started into the program. A more detailed list of these is provided in the appendix.

Table 1
Information for ICs Starting the Program

W88 Subassembly	IC Type	IC Function	Year Started	# ICs Started
MC3811 Programmer	SA2998	1K MNOS RAM	1989	19
			1990	20
			1992	20
MC3811 Programmer	SA3000	SNL/AMO μ P	1989	20
MC3811 Programmer	SA3601	Harris μ P	1992	18
			1993	40
MC3811 Programmer	SA3001	2K SRAM	1989	20
			1993	20
MC3813 Force Balance Integrating Accelerometer	SA3230	A/D Converter	1989	18
			1990	20
			1991	20
MC3827 Clock	SA3246	Clock Counter	1989	17
			1990	20
Total				272

III. Electrical Test Procedures

Electrical tests were performed to evaluate the shelf life program ICs for potential changes in parametric or functional characteristics. The electrical test procedure is defined in BB390133 and consists of all of the electrical tests required by the current component product specification. Following electrical preconditioning, the ICs were subjected to an initial test that then constituted the baseline data against which subsequent test data were compared. These tests were performed at room, hot, and cold temperature using the currently specified tester and test tape. These tests were repeated for each shelf life program IC at approximately yearly intervals.

Table 2 is a summary of the number of ICs that were tested and that failed during each year.

Table 2
Number of ICs Tested and Failed by Year

	# ICs Tested / # ICs Failed					
Year Tested	1989	1990	1991/ 1992	1993	1994	1995
IC Type						
SA2998	19/0	39/8	56/4	47/0	41/0	-
SA3000	20/0	20/1	19/0	19/0	17/0	-
SA3601	-	-	18/1	57/0	55/0	36/0
SA3001	20/0	20/0	20/0	40/1	37/0	18/0
SA3230	18/0	38/0	58/0	58/0	52/0	-
SA3246	17/0	37/0	37/0	37/0	33/0	-
Total	94/0	154/9	208/5	258/1	235/0	54/0

IV. Electrical Test Findings

Table 3 shows IC SN, failure analysis (FA) references (in the appendix), and findings for the ICs that failed electrical tests during this program. Failure analysis was performed if there was an indication that a valid electrical failure occurred (failures that did not repeat were not analyzed if there was evidence that they were invalid, such as routine continuity test failures). All but one of the failures were investigated by AMO FA personnel; the last one (the SA3001) was analyzed by Sandia FA personnel.

Table 3
Information for Electrical Test Failures

IC Type	# Failed	Failure SN	Failure Information [references]
SA2998	5	17855 18243 18512 18550 19012	Apparently gate oxide shorts, failure mode similar to SNs 18250, 18557, and 18595. [M1-M4]
	3	18250 18557 18595	A5: Gate oxide shorts in n-well control inverter (NW2) due to transients during cold testing. [A5, R5, M1- M4]
	4	18120 18496 48493 49137	FA report not in project files (suspected cause is the test operations).
SA3000	1	25205	Damaged (continuity failure) during AMO FA; failure verified in 641-3 test lab.
SA3601	1	234	Failed dynamic screen at cold temp., apparently damaged by ESD during FA.
SA3001	1	25566	EOS damage of transistor source-drain junction due to snapback during electrical testing. [R2]
Total	15		

Review of electrical test data

The electrical test data for the parametric measurements (e.g., power supply current, output drive, etc.) in the Excel files provided by John Minihan (FM&T/KC) were analyzed for trends from one test year to the next. The SA3230 and SA3601 files contained the majority of the data and were analyzed first. The SA3230 parametric data at ambient, low, and high temperature were examined. No significant trends were observed. Next, the SA3601 parametric data at ambient, low, and high temperature were examined. Again, no significant trends were observed. Finally, the parametric data for the other types of ICs were analyzed and no significant trends were found for these either.

Review of electrical test failures

Eight SA2998Ds failed in 1990 after the first storage year. Three of these failed during low temperature tests immediately following high temperature tests. Initial investigation included the possibility that corrosion, contamination, or diode breakdown (walkout) might be responsible for these failures. Raman spectroscopy of one of the ICs from the high temperature environment suggested that a thin, conductive film, consisting of amorphous carbon, gold particles, and possibly also a hydroxyl-containing species had formed on the package pins [R5]. This film could have caused increased leakage current between the pins and could also have caused increased contact resistance (package to test socket). However, neither this failure mechanism nor diode walkout correlated well with the primary failure mode. Additional analysis of the three low temperature failures found that the *n*-well control inverter (NW2) of all three ICs had gate oxide damage. Silicon melt damage was found in both the drain diffusion and the substrate. Review of prior data indicated that these failures were not random and had occurred on other SA2998s (however, most of the prior failures were in the NW1 inverter). This and other information led to the conclusion that the SA2998 shelf life program failures were probably caused by the test operation [A5]. Four more SA2998s failed in 1992. Although it is suspected that these failures were also caused by testing, failure analysis information for these ICs was not in the project files.

SA3000 SN 25205 failed during testing in 1990 at AMO. Project file information for this failure indicates that during AMO failure analysis the part was damaged, resulting in a continuity failure on pin 21. This damage was verified in the FM&T/KC 641-3 test lab. The root cause of the initial failure is not known.

SA3601 SN 234 failed the dynamic screen in 1992 at -55 °C. Project file information for this failure indicated that it suffered electrostatic discharge damage in the FM&T lab during analysis. The root cause of the initial failure is not known.

SA3001 SN 25566 failed during electrical testing in November, 1992 (the 1993 testing cycle started in late 1992) at high temperature (95 °C). This IC had been in the 125 °C storage environment since 1989 and had passed annual electrical tests performed in 1991 and 1992. It failed due to high dynamic operating current (19.8 mA with a limit of 17.6 mA), and higher than normal I_{DDQ} (9 mA with a limit of 100 μ A). It passed all other tests, including all functional tests. The high current was due to electrical overstress damage to the metal and silicon in an *n*-channel transistor source region, forming a short from V_{SS} to the substrate (V_{DD}). The *n*-channel transistor was a driver for internal data bus bit 7 (the input circuit for the AD7 pin). The damage was attributed to snapback of

the n-channel transistor during the 95 °C dynamic operating current test. Snapback was probably initiated by a test-induced electrical transient during this test. ICs are more susceptible to snapback at elevated temperature.

Summary of electrical test findings

No trends or instabilities were observed in the parametric data. The failure analysis reports attribute most of the electrical test failures to test-induced causes, although some important failure analysis data cannot be located in the project files.

V. DPA Procedures

Destructive physical analysis was used to evaluate the shelf life ICs for potential problem areas (failure modes and mechanisms) that might not be discovered by electrical tests and to assist in determining possible reliability impact on systems. The DPA procedure was established and documented in SS390133 and BB390133. A standard industry approach was used, based on MIL-STD-883 procedures. A sample set consisting of two ICs for each type, production year, and storage environment (room ambient and +125 °C) were selected for analysis. One exception to this sampling plan was that the 2 SA2998 samples selected in 1994 were both from the room ambient storage group because all of the high temperature storage ICs had failed electrical tests. The DPAs were performed by Analytical Solutions Inc. (ASI) in Albuquerque. Table 4 is a summary of information for the DPAs performed. Although all but 2 of the DPAs failed at least one criterion, many of these were due to lid scratches, a known condition that is not a reliability concern (the lids were intentionally scratched to prevent use as WR material and there were additional scratches due to handling during this program). The findings involve conditions that existed prior to this program and are not related to aging of the ICs.

Table 4
DPA Information

IC Type	Year Started	Analysis Year	Number Analyzed	DPA Number
SA2998	1989	1993	2	9305-298-D
	1990	1993	2	9305-300-D
	1991	1993	2	9305-303-D
	1989	1994	2	9409-873-D
SA3000	1989	1993	2	9305-295-D
	1989	1994	2	9409-874-D
SA3601	1991	1993	2	9305-301-D
	1992	1994	2	9409-878-D
	1993	1994	2	9409-879-D
	1993	1994	2	9409-880-D
	1993	1995	2	9510-787-D
	1993	1995	2	9510-788-D
SA3001	1989	1993	2	9305-296-D
	1989	1994	2	9409-875-D
	1993	1994	2	9409-876-D
	1993	1995	2	9510-786-D
SA3230	1989	1993	2	9305-297-D
	1990	1993	2	9305-299-D
	1991	1993	2	9305-302-D
	1989	1994	2	9409-877-D
SA3246	1989	1993	2	9307-438-D
	1990	1993	2	9307-439-D
	1989	1994	2	9409-881-D

VI. DPA Findings

Table 5 shows the summary of the DPA analysis report numbers and findings. Two sample ICs were analyzed for each DPA. There are two areas of concern: wire bonding (poor bondwire clearance, poor bondfoot thickness, low bond pull strength, cracks in bondfoot, and disturbed bondwire) and die processing (low contact window area coverage). These items are highlighted in bold and are discussed next.

Table 5
DPA Findings

IC Type	DPA Number	Failed items
SA2998	9305-298-D	Lid scratches
	9305-300-D	Lid scratches, poor bondwire clearance, low contact window coverage
	9305-303-D	Lid scratches, poor bondwire clearance, low contact window coverage
	9409-873-D	Lid scratches, loosely attached particle, poor bondwire clearance
SA3000	9305-295-D	Lid scratches
	9409-874-D	Lid scratches, die attach voiding, poor bondwire clearance
SA3601	9305-301-D	Lid scratches
	9409-878-D	Lid scratches
	9409-879-D	Lid scratches
	9409-880-D	Lid scratches, die metallization damage
	9510-787-D	Pass
	9510-788-D	Lid scratches
SA3001	9305-296-D	Pass
	9409-875-D	Loosely attached particles on die attach, poor bondwire clearance
	9409-876-D	Lid scratches, die attach voiding, poor bondwire clearance
	9510-786-D	Die attach voiding, cracks in bondfoot, poor bondwire clearance
SA3230	9305-297-D	Poor bondwire clearance, poor bondfoot thickness, low bond pull strength
	9305-299-D	Poor bondwire clearance, poor bondfoot thickness
	9305-302-D	Lid scratches, poor bondwire clearance
	9409-877-D	Lid scratches, scrape on package ceramic, poor bondwire clearance
SA3246	9307-438-D	Lid scratches, poor bondwire clearance, poor bondfoot thickness, low contact window coverage
	9307-439-D	Lid scratches, lead contamination, poor bondwire clearance, poor bondfoot thickness
	9409-881-D	Lid scratches, poor bondwire clearance, disturbed bondwire, low contact window coverage

The DPA data were examined to determine the dominant failure conditions and organized them into categories. A new spreadsheet book (dpabook.xls) was derived from data in spreadsheet (dpa_loc.xls). This new spreadsheet book contains charts that show the twelve failure conditions (excluding lid scratches) found versus the frequency of occurrence for type of IC. One of the spreadsheets in the book, titled “DPA Defects,” shows the total count for each of the failure conditions. The results of this analysis are shown in Table 6. Table 6 shows the number of occurrences for the 13 failure conditions (including lid scratches), organized into four major failure categories.

Table 6
Categorization of DPA Failure Items

Failure Category	Failure Condition	# of Occurrences	Total for Category
Package lid marks	Lid scratches	17	17
Wire bonding	Poor bondwire clearance	28	39
	Poor bondfoot thickness	7	
	Low bond pull strength	2	
	Disturbed bondwire	1	
	Cracks in bondfoot	1	
Die processing	Low contact window coverage	8	8
Miscellaneous	Die attach voiding	3	9
	Particles on die attach	2	
	Loosely attached particle	1	
	Lead contamination	1	
	Die metallization damage	1	
	Scrape on package ceramic	1	

The DPA findings do not indicate a degradation of the ICs (packages or die) due to the shelf life environment. The findings involve conditions that existed prior to this program and are not related to aging of the ICs. Although all but 2 of the DPAs failed at least one criterion, many of these were due to lid scratches, a known condition not considered to be a reliability concern (the lids were intentionally scratched to prevent use as WR material and there were additional scratches due to handling during this program).

Fig.1 shows the bondwire clearance concern. This condition is in violation of MIL-STD-883/2010, 3.2.2a, Condition A, Class S, which requires a clearance of at least 1 mil between bond wires and unglassivated operating (biased) materials.

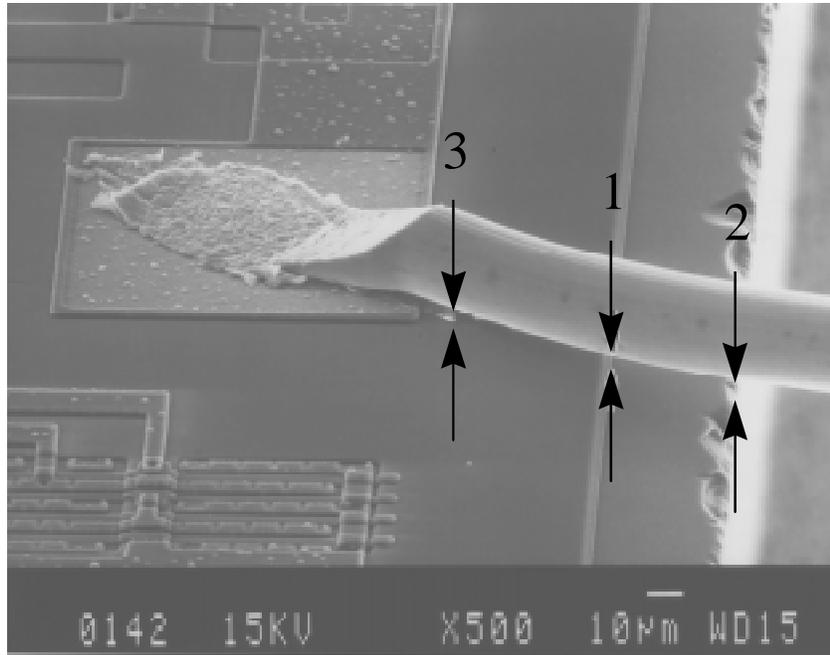


Fig. 1. SEM image of the poor bondwire clearance (~ 0.15 mil) between a bond wire and the passivation edge (location 1). Arrows point to measurement locations. Image from DPA 9305.297-D (pg. 16).

In Fig. 1, the arrows at location 1 show the clearance from the bottom of the wire to the passivation edge. This is the location where ASI usually measured the clearance, since the region beyond the passivation edge to the die edge (to the right of the arrows at location 1 in Fig. 1), is exposed silicon substrate biased at V_{DD} . This region, the die street, is where the overlying dielectric layers have been removed to delineate the die boundaries and to improve the die separation process (sawing for this packaging process). However, AMO measured the clearance from the bottom of the wire to the die edge (location 2 in Fig. 1). In several of the bondwire clearance failures identified by ASI, it appears that the wires had acceptable clearance using the AMO clearance location (die edge) because of the upward angle of the bond wires. In other cases, such as that shown in Fig. 1, the wires fail using either the passivation edge or die edge location. AMO used a reverse bonding process (package pad bond first, die bond last) which, combined with the type of packages used for these ICs, may have increased the likelihood of low clearance of the wires at the die bond pads.

The primary concern is whether the relatively low bondwire clearance increases the reliability risk. There are two aspects to this risk, both of which involve electrical shorts: #1. A bond wire might move enough to come into contact with the die surface, or #2. A

loose, conductive particle in the package cavity might lodge between the wire and the die surface.

Risk #1 seems the lesser of the two for several reasons. To short to the die, a wire would have to be in contact with the die surface since the voltages involved are low (5 to 10 V) and there is a native oxide of at least 1.5 nm on the silicon surface. Also, in order to contact the die in the street region, the wire would have to move from its as-bonded upward angle to below horizontal, due to the dielectric thickness at the passivation edge (a total of about 1.7 μm for field oxide, intermediate dielectric, and p-glass). This amount of movement seems relatively unlikely for normal wires. However, the disturbed bondwire observed in 9409-881-D and low bondfoot thickness observed in several DPAs may contribute to the risk that a wire may already be very close to the die or may move to contact the die (these are discussed further in the discussion later on bond wire strength). Another factor is that the bonding process can disturb or crack the dielectric layers next to the bond pad (location 3 in Fig. 1) [R2]. The probability of physical contact of the wire to the die surface is highest at this location. However, for a short to occur in this region, there would have to be contributing conduction mechanisms (such as corrosion, moisture, or contamination) since the dielectric material, even if damaged, should still have relatively low conductivity.

Risk #2 of a conductive particle lodging between the wire and the die, resulting in a short, is a more significant concern for these ICs. The reduced clearance between the wire and the die increases the likelihood of short if a loose, conductive particle is present in the package cavity. Particles were observed in packages of DPAs 9409-873-D and 9409-875-D. For DPA 9409-873-D, the particle was an aluminum sliver about 1.1 mil long at a wire bond to the IC pad. For 9409-875-D, the particles were AuSi slivers up to about 1.1 mil in length on the top of the AuSi die attach surface adjacent to the die. These particles are long enough to potentially cause a short if they were to come loose (both types of particles were described as “loosely attached”).

Fig. 2 shows the poor bondfoot thickness concern. Although the deformation of this particular bond is acceptable per the MIL-STD-883/2010 requirements, there is significant thinning of the bond. The bond foot thickness is less than 25 % (actually less than 10 %) of the wire diameter (1 mil). This condition is in violation of MCR-72-241, 5.1.1.4.3 (this is not a required specification for the DPA, but is used by ASI as a guide because it provides more detailed inspection criteria than MIL-STD 883 and has been used by Sandia satellite departments). This raises a significant concern about the strength and reliability of the wire bonds. For DPA 9305-297-D, the wirebond pull testing resulted in six bond wires of one IC fracturing at low forces (1.1 to 1.4 g). This fails the MIL-STD-883/2011, 3.2 requirement of 1.5 g. For this DPA, a total of 98 wires on the two ICs were tested with all other bonds fracturing from 1.6 to 4.8 g. These bond pull failures appear to be directly related to the overbonding observed during the DPA.

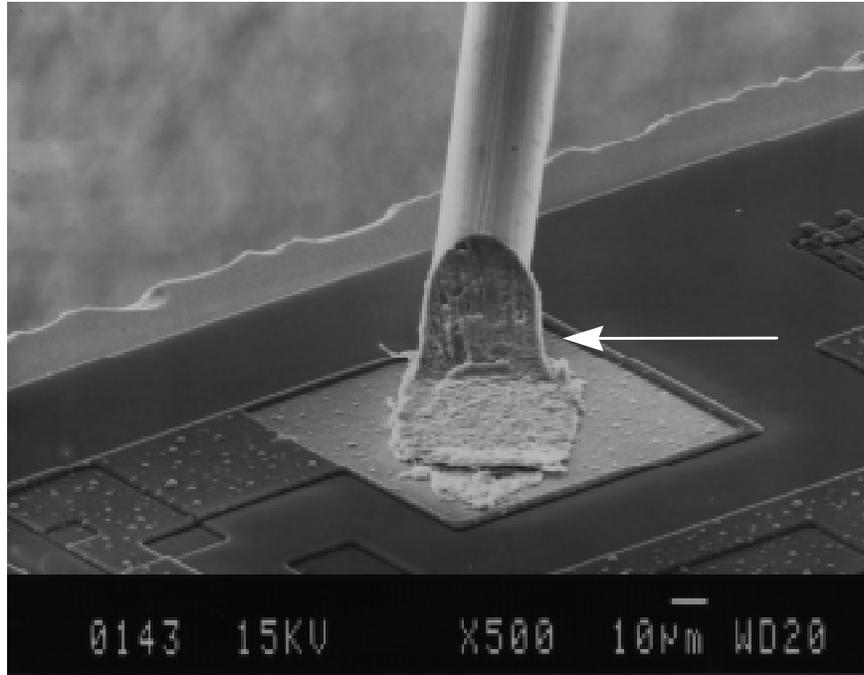


Fig. 2 SEM image of poor bondfoot thickness (same wire as that shown in Fig. 1 but from a different direction). Arrow points to bondfoot. Image from DPA 9305-297-D (pg. 15).

The bonding problems observed during the DPAs are interrelated in the following ways. The concern discussed previously of a wire moving down into physical and electrical contact with the die may be increased due to the observed low bondfoot thickness and pull strengths, since these may indicate an increased risk of the wire “sagging” into contact with the die. In addition, the observation of the disturbed bondwire (9409-881-D) indicates that there is a possibility that some wires may have been pushed closer to the die unintentionally during wirebonding or subsequent process operations prior to lid sealing.

This concern may be offset to some extent by the use during production of wire lifting to improve the wirebond clearance (resulting in the wire “kinks” noted in some DPAs). The wire lift procedure was used during production when deemed necessary to achieve the required wire clearance about the chip surface.

The other area of possible reliability risk involves the observation of low contact window area coverage. Misalignment of the metal contact windows to silicon and polysilicon resulted in significant overetching of the silicon and polysilicon for some ICs. This is shown in Figs. 3-6. The etch pit into silicon is a concern because it extends a considerable distance through the n^+ or p^+ junctions, creating the possibility of high junction leakage or junction shorting. The etch cut into the polysilicon appears deep enough to raise the concern that it might go all the way through the polysilicon. However, this is probably not as serious a concern, since it is likely that there would be sufficient intact polysilicon on at least one side of the contact window to assure electrical continuity even if the polysilicon were etched completely through. This might increase to some extent the electromigration risk for those sections of polysilicon that are used as interconnections (versus those used only as transistor gates).

During production, the criteria for contact window coverage was 75% or more coverage. This means that misalignment of the metal over silicon and polysilicon contact windows was allowed, permitting up to as much as 25% of the contact window area to not be covered. The exposed contact window areas shown in Fig. 3 and Fig. 5 are less than 25%, so they illustrate conditions that met the inspection requirement during production. In addition, no electrical failures are known to have occurred during production or W88 assembly testing due to mechanisms involving insufficient contact window coverage.

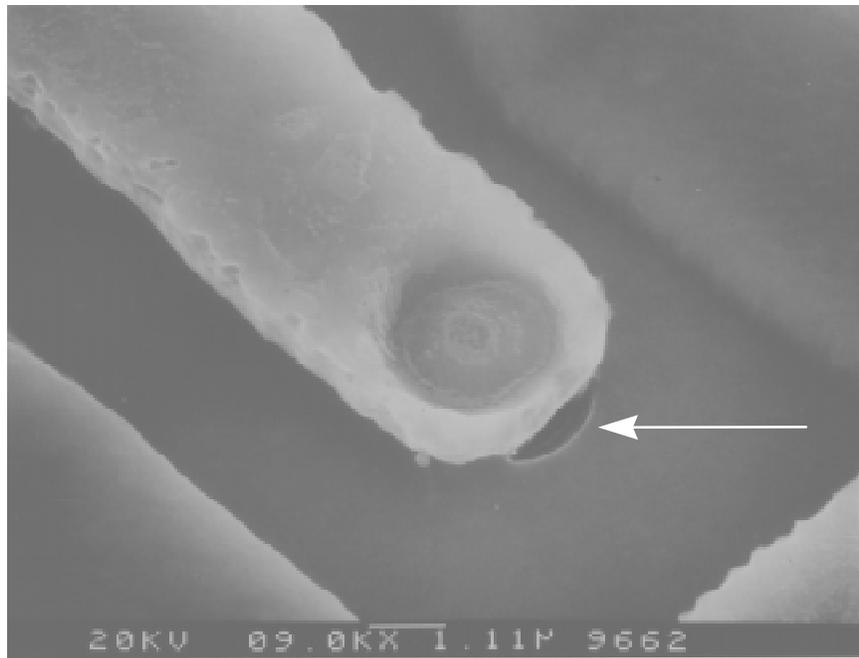


Fig. 3. SEM image of poor metal coverage of a contact window to silicon. Arrow points to contact window region not covered by metal. Image from DPA 9305-438-D (pg. 21).

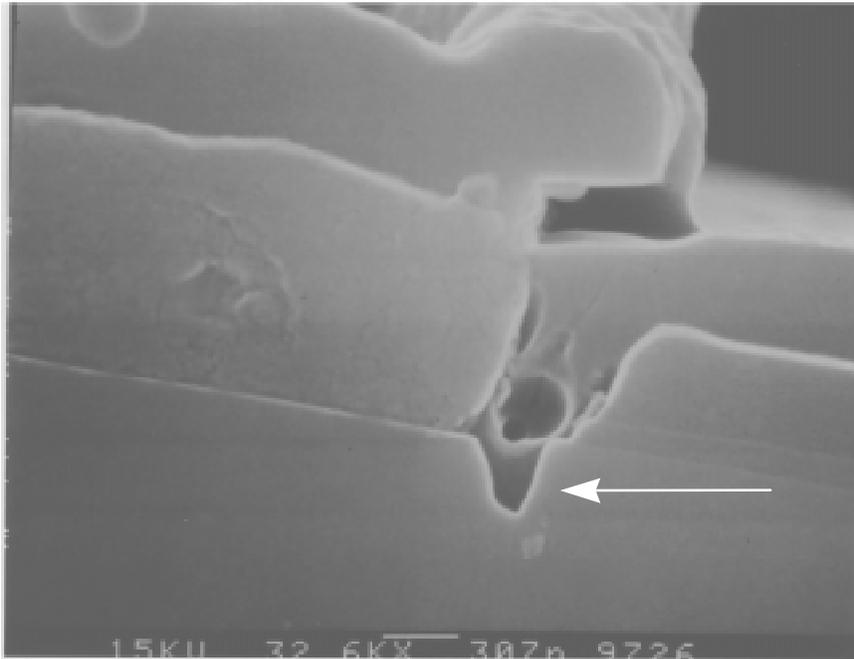


Fig. 4. SEM image of cross section of silicon etching due to poor metal coverage of contact window to silicon. Arrow points to etched silicon region. Image from DPA 9305-438-D (pg. 23).

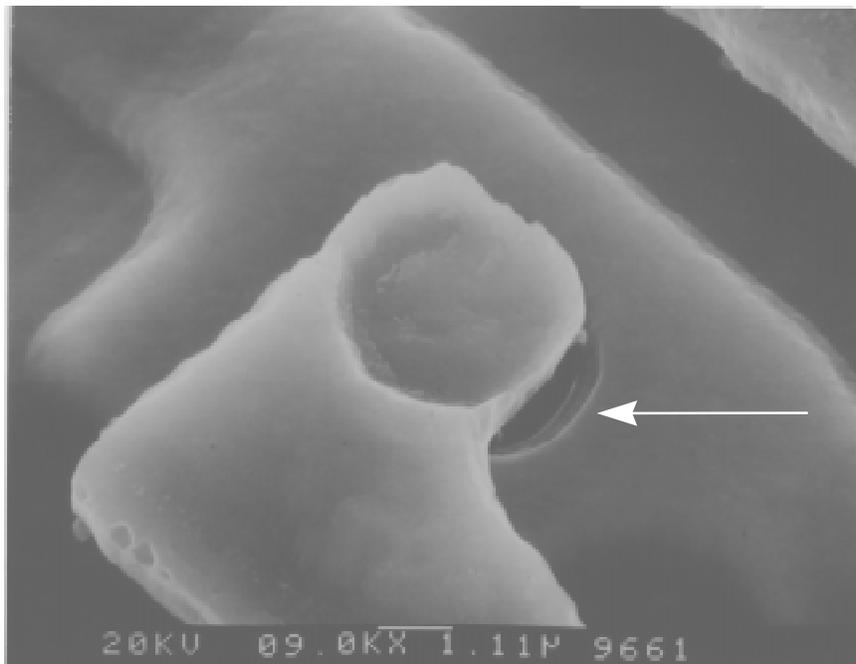


Fig. 5. SEM image of poor metal coverage of a contact window to polysilicon. Arrow points to contact window region not covered by metal. Image from DPA 9305-438-D (pg. 20).

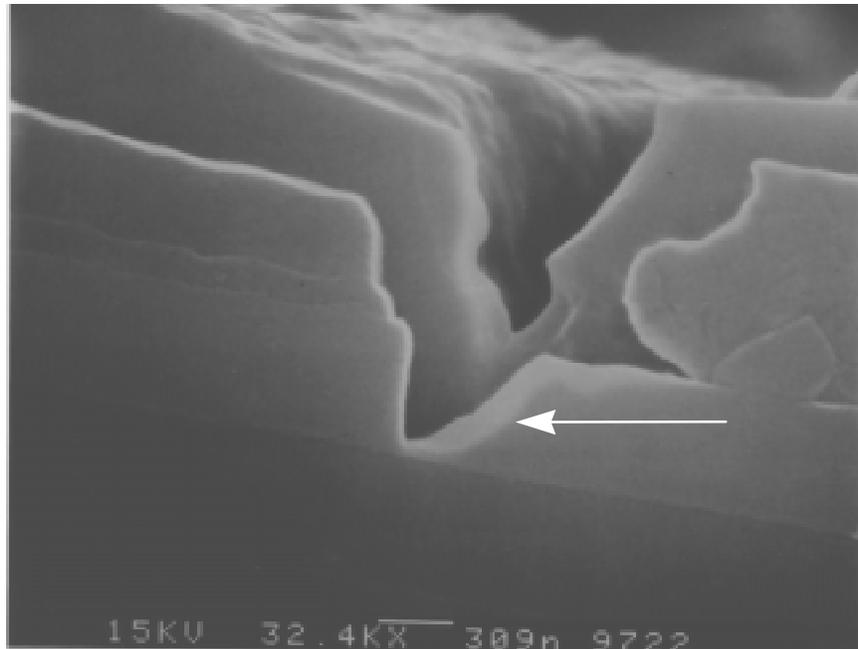


Fig. 6. SEM image of cross section of polysilicon etching due to poor metal coverage of contact window to polysilicon. Arrow points to etched polysilicon. Image from DPA 9305-438-D (pg. 24).

The following is a summary of reference A2, which is a review by Cathy Reber and Don Johnson in February, 1996 of the ASI reports (these two people are in SNL Advanced Packaging Dept. 1333 and had packaging responsibilities for these ICs during production). This summary provides a general perspective plus comments on specific issues, including bondwire clearance. Reference A2 also includes comments on specific DPA reports.

“In general, the DPA findings do not indicate a degradation of the ICs (packages or die) due to the shelf life environment, including testing and handling procedures. The majority of the observations are conditions that occurred for both the room ambient and +125 °C storage temperatures.

The following are comments about specific DPA issues.

- A. Lid scratches noted on almost every report. The scratches were obviously deliberate (or the result of shelf life program handling). The scratches have nothing to do with assembly, storage, or shelf life reliability.
- B. A positive observation is that the leak rates were good even for the ICs with small 40 pin chip carrier packages (a package design that violates known good design practices). Most leak rates were measured in the 1×10^{-9} range. Another positive observation is that die shear test results, in spite of some report comments regarding voiding, were all satisfactory.

- C. Nondestructive bond pull testing was not required during AMO production. Nondestructive wire lift was used when deemed necessary to achieve wire clearance above the chip edge. This caused the “kinks” referred to in some reports. According to these reports, wire lift should have been used more frequently.
- D. MCR-72-241 was used by ASI as a guide for bondfoot thickness but it was not a document of record for AMO during production, was not a Sandia-required document, and is not referenced in MIL-STD-883.
- E. Wire clearance, the observation that occurred repeatedly in the reports, is a very subtle and argumentative situation. The good aspect of this is that it is not considered to be directly related to shelf life degradation, rather it is an as-assembled condition. These ICs have undergone thermal cycling, centrifuge, PIND test, and burn-in without significant evidence of degradation. If wire clearance is considered a problem, current options for the lots involved here would be to repeat some or all of the acceptance tests. However, the determination of wire clearance acceptability (& whether it presents a W88 reliability risk) involves the methods used for DPA inspection versus the AMO production requirements. The DPA inspection used the clearance at the edge of the glassivated area, but the AMO assembly requirements measured the clearance at the die edge (sawed edge of the chip street) where silicon was exposed. Between the glassivation edge (basically the edge of the thick dielectric structure consisting of field oxide and p-glass passivation) and the die edge, one could argue that the die surface was somewhat protected by a natural (native) oxide and that it would take more than slight contact to cause a problem due to the relatively low voltage of these ICs (5 to 10 V). It is interesting to note that, in all but one of the reports, ASI used the glassivation edge as the point of reference and determined the clearance to be unacceptable. However, in one report (9409-878), the same reference was used as that used during AMO production (the sawed edge of the die) and the clearance was determined to be acceptable. A discussion with Norm Huling, the principal quality engineer for AMO packaging (now retired), supported this observation (that the shelf life ICs should pass the bond wire clearance requirement if inspected using the die edge instead of the glassivation edge).”

VII. Conclusions

The electrical testing and DPA analysis of these ICs produced several findings involving significant IC quality issues. However, none of these appear to indicate a severe reliability concern, rather they highlight known or preexisting testing and packaging issues that, to varying degrees, have been investigated and determined to present acceptable risk for the W88 stockpile assemblies.

There are two aspects of the electrical tests performed on these ICs: the implications of the electrical failures that occurred and the absence of degradation trends in the data. For the failures, there appear to be two dominant factors, both of which involve test-induced damage to the ICs. These are electrical overstress during the test process and electrostatic discharge (ESD) during failure analysis. The gate oxide shorts of the SA2998s and snapback of the SA3001 were apparently a result of how these ICs were tested. It should be noted that the MNOS and 4/3 technologies are known to be susceptible to oxide breakdown and snapback failure mechanisms, so there was a predisposition for these ICs to fail in this manner. ESD is a ubiquitous problem which all too often makes it difficult, if not impossible, to accurately determine the true root cause of failure. ESD prevention must be exercised at all times during testing and failure analysis. Considering the high level of handling and testing of these ICs over a number of years, the few ICs that were apparently damaged does not seem unusual. The absence of degradation trends in the electrical parameters of these ICs indicates that there are no early aging problems.

There are two dominant factors observed in the DPA results. These involve wire bonding and die processing issues. The wire bonding concern is a result of observations of poor bondwire clearance, poor bondfoot thickness, low bond pull strength, disturbed bondwire, and bondfoot cracks. The die process concern involves overetching of the polysilicon and silicon due to low contact window area coverage. Both of these have the potential to be significant failure mechanisms in the presence of other contributing factors.

The concern about wire bonding primarily involves the risk that a wire might break at the bond heel (causing an open circuit of this wire and possibly shorting to another wire) or that a wire might contact the die either directly or as a result of a conductive particle (causing a short circuit from the wire to the die). There are known cases of WR component failures due to bond wire and conductive particle shorts inside packages. One of the few confirmed IC failures during WR new material and stockpile weapon testing was due to a loose Pb/Au lid sealing solder sliver which intermittently shorted two or more bond wires during vibration testing of the W70 MC2764 MCCA in 1975 [R1]. In addition, there have been several environmental and destructive test (E-Test and D-Test) failures of the W88 MC3811 Programmer due to package failure mechanisms [R6, R7]. These failures occurred during or after the E-Test and D-Test mechanical shock and vibration conditions. The failures were caused by conductive particles inside transistor packages and a deformed (intermittently shorting) bond wire in a diode package (another failure occurred but did not repeat and the cause could not be determined). Because of these failures, an extensive Particle Impact Noise Detection (PIND) screen was instituted in MC3811 production. However, an MC3811 subsequently failed due to a foreign

particle, so the PIND screen apparently did not detect all ICs containing particles during production. All of the W88 ICs passed a PIND test during production.

The die processing concern about polysilicon and silicon etch pits resulting from low contact window area coverage involves primarily the possibility that these pits might lead to open circuits of the polysilicon or short circuits (or high junction leakage current) in the silicon. Of these, the junction shorts appear to have the highest risk. However, these regions should be reasonably well passivated by the overlying p-glass, making it unlikely that any significant change would occur in the magnitude of the leakage current. This is consistent with the absence of any significant increase in the power supply current (I_{DDQ}) for these ICs.

In summary, the electrical testing and DPA results for these ICs identified several noteworthy factors involving testing, handling, packaging, and die processing. These constitute significant issues for the ICs presently in W88 stockpile assemblies. However, these issues do not appear to change the reliability risks for these ICs, because they involve known or preexisting issues. The knowledge gained from the shelf life program is a valuable contribution to the data base for these ICs, because it reinforces and strengthens the methods used for W88 reliability estimates. It is also very important to observe that there have been no known failures of these ICs in any WR stockpile assembly.

VIII. Recommendations

The following is a recommendation that results from this program.

Data from the W88 Integrated Circuit Shelf Life Program will be helpful for any future investigation of the failure modes of the 4/3 micron or MNOS IC technologies. The investigation of any failure or abnormal behavior of any W88 or other WR assembly IC from the 4/3 micron (Harris or SNL/AMO) or MNOS technologies should include a determination of whether such behavior involves the failure modes and mechanisms evaluated in the shelf life program. This includes the 4/3 snapback, MNOS oxide breakdown, and bond wire strength and clearance issues as described in this report. Although it is not expected, if evidence is found during or stockpile testing or other activities of occurrences that relate to the shelf life program observations, then it is highly recommended that the reliability estimate for WR assemblies that contain these ICs be carefully reevaluated.

IX. References

Records for the W88 Shelf Life Program were organized by R. Anderson into six sections in a three ring binder. The following lists show the section titles and records in these sections. After this list is a summary of the meetings (dates and agenda items) referred to in the records in this binder.

A. Meetings (Project Memos and Records)

- A1. R. Anderson, Sandia memo, "W88 Shelf Life Program Final Report Requirements," 4/19/96.
- A2. C. Reber and D. Johnson, Sandia memo, "W88 Shelf Life Program DPA Review," 2/22/96.
- A3. R. Anderson, Sandia memo, "W88 Mk5 LSI Shelf Life Program DPA Reports," 10/21/94.
- A4. J. Schwartz, Sandia memo, "Test Plan for the W88/Mk5 LSI Shelf Life Program," 6/20/94.
- A5. D. Huffman, ASKCD memo, "SA2998D-2 Shelf Life Failure Analysis (KCD 413B No. 2004) Concerning S/N 18557 Date Code 8739, S/N 18595 Date Code 8739, and S/N 18250 Date Code 8738," 3/11/92.
- A6. E. Hollingsworth, ASAMO memo, "AMO Quality Assurance Shelf-Life Program Summary," 3/22/91.
- A7. D. Tallant and Morrison, Sandia Document, Micro-Raman spectroscopy report of dark areas on leadless chip carrier ceramic package surface near three pins, 2/19/91.
- A8. E. Hollingsworth, ASAMO memo, "Summary of the January 29, 1991, Meeting of the Shelf-Life Program Committee," 1/29/91.
- A9. G. Wagner, ASAMO Document, Summary of failure analysis: SA3000A, KCD660 #21286, Lots G2499B and G4904A; SA3001A, KCD660 #21285, Lot G0285A; SA2998D-2, KCD660 #21276, Lots J1902A, J19116A, J20106AA, and J20102AA, 1/24/91.
- A10. E. Hollingsworth, ASAMO memo, "Meeting of the Shelf-life Program Committee," 1/8/91.
- A11. G. Wagner, J. Mauth, and L. Suina, ASAMO memo, "G25005QSHLF SA3246C Shelf Life Failure Analysis Report," 9/25/90.
- A12. E. Hollingsworth, ASAMO memo, "Summary of the September 5, 1990, Meeting of the Shelf-Life Program Committee," 9/7/90.
- A13. E. Hollingsworth, ASAMO memo, "Meeting of the Shelf-Life Program Committee," 8/20/90.
- A14. W. Lewis, ASAMO Record, List of drawings for which AMO has responsibility and DTER status, 9/5/90.
- A15. E. Hollingsworth, ASAMO memo, "Shelf-Life Program Status Report," 8/9/90.
- A16. AMO Product Engineering Record, Shelf-Life Program Parameters (SA types with pin functions and names), 8/1/90.
- A17. AMO Product Engineering Record, W88 Program Devices (comparison of AMO and Harris SA numbers), 7/24/90.
- A18. P. Siegal, Information on SA2998 failure (SN 29520), 6 pages of hand written notes with no date, apparently related to R. Wagner's failure analysis report of 7/6/90.

- A19. G. Wagner, ASAMO memo, "SA2998 S/N 29520 Shelf Life Failure Analysis Report," 7/6/90.
- A20. E. Hollingsworth, ASAMO memo, "Shelf-Life Program Discussion," 6/4/90.
- A21. E. Saverino, ASAMO memo, "SA3230 Shelf life Test Failures," 12/13/89.
- A22. E. Hollingsworth, ASAMO memo, "Summary: Shelf-Life Committee Meeting of October 19, 1989," 10/23/89.
- A23. W. Lewis, W88 Shelf Life Program presentation material on AMO test equipment support (related to cessation of AMO production operations by September 1992, 10/19/89).
- A24. G. Wagner, ASAMO memo, "Analysis of SA3230 Shelf-Life Failures," 10/12/89.
- A25. E. Hollingsworth, ASAMO memo, "Summary of the Shelf-Life Committee Meeting of September 7, 1989," 9/8/89.
- A26. Hand written record of Shelf-Life Program Status for 1989, 9/7/89.
- A27. Hand written notes for SA2998D-2 SN 29520 failure, Sept. 1989.
- A28. Hand written SN list for SA3230C, Jan.-Mar. 1989.
- A29. Hale, "Meeting of the Shelf-Life Program Committee," 8/30/89.
- A30. Hand written record of Shelf-Life Program Status for 1989, 8/22/89.
- A31. Hand written record of Shelf-Life Program Devices, 6/5/89.
- A32. E. Hollingsworth, ASAMO memo, "Meeting of the Shelf-Life Program Committee," 5/4/89.
- A33. R. Anderson, "Meeting of Shelf Life Committee to Finalize Program Implementation," 3/1/89.
- A34. E. Hollingsworth, Hand written note of SA3230C sample requirements, 1/20/89.
- A35. R. Anderson and T. Dellin, "Recommendation for Changes in the Shelf Life Program to Enhance Implementation," 1/20/89.
- A36. W. Miller, "Equivalent Time/Temp./Voltage Values for Simulated Assembly II," 1/3/89.
- A37. W. Miller, "Equivalent Time/Temp./Voltage Values for Simulated Assembly," 12/22/88.
- A38. A. Tapia and D. Hartleben, Hand written notes on device availability, 1/3/89.
- A39. R. Anderson, "Meeting of Shelf Life Committee to Discuss Program Implementation," 1/16/89.
- A40. R. Anderson, Hand written notes on preferred devices for Shelf Life Program, end of 1988.
- A41. C. Trauth, "Meeting Regarding Necessary Actoions to Begin a Shelf-Life Program," 11/11/88.
- A42. D. Branscombe and R. Anderson, "Planning document for "Stockpile Mirror Program" of shelf life samples from 4/3 micron lots with evaporated metal used for WR system deliveries," 2/26/88.
- A43. C. Trauth, "Tomorrow's Presentation," 11/24/87.
- A44. R. Anderson, E. Savarino, and C. Trauth, presentation material for "A brief description of a proposed shelf-life program for CRM-related materials," 11/25/87.
- A45. B. Gregory, "CRM Shelf Life Program," 11/19/87.

B. AMO Activity (ASAMO activity reports containing information on the shelf life program).

B1. R. McClintock, March, 1992, 3/31/92.

B2. G. Hale, July 1989 - December, 1990.

C. PRs (Purchase Requisitions)

C1. Various cost and purchase documents for ICs used in the program.

D. Navy Programs

D1. L. Loudermilk, Sandia memo, "Open new reimbursable program cost objective (subproject only)," 7/11/91.

D2. W88 Component Shelf Life Project 3025, FY 91 and 92 Objectives.

D3. J. Middleton, Sandia memo, "PO 27-2247, Rev. 01 and 02 (attached), W88 Shelf Life with AS/KCD," 10/17/90.

D4. J. Middleton, Sandia memo, "Proposed FY91 Budget for W76/MK4 and W88/MK5 Weapon Evaluation Programs," 7/9/90.

D5. J. Middleton, Sandia memo, "Navy SSPO Reimbursable Cases," 8/7/89.

D6. J. Middleton, Sandia memo, "W88 Component Shelf Life Program," 4/27/89.

D7. J. Wirth, Sandia memo, "W88 Component Shelf-life," 2/15/89.

D8. R. Peurifoy, Sandia letter, "W88/Mk5 Trident II Component Shelf-life Program, Proposal #7280602LA," 2/17/89.

D9. J. Middleton, Sandia letter, Subject involves concerns and funding for shelf life program (attached is a draft of "Proposal for a shelf life program for selected Navy-funded components in the MC3810 AF&F for the W88/Mk5 RBA"), 11/22/89.

E. DPA Specifications

Note: R. Anderson created and maintained a Word table of W88 Shelf Life Program DPA submissions; the filename is "shelfdpa.doc."

E1. Sandia Procurement Contract, AR-3489, For destructive physical analysis per SS390133 by Analytical Solutions Inc, 10/27/95 (Performance Period 10/27/95-12/31/95).

E2. Anderson, Sandia memo, "Evaluation of Cost Quotation on RFQ AR-3489 Proposed Contract," 10/24/95.

E3. Ortiz, Sandia memo, "Evaluation of Cost Quotation on RFQ AR-3489 Proposed Contract," 10/23/95. R. Anderson, "Justification for Government Furnished Property on Purchase Requisition AR-3489," 10/3/95.

E4. Sandia Procurement Contract, AI-2068, For destructive physical analysis per SS390133 by Analytical Solutions Inc, 5/26/94, (work to be completed by Sep 30, 1994).

E5. Sandia Procurement Contract, AE-0795, For destructive physical analysis per SS390133 by Analytical Solutions Inc, 8/20/93, (work to be completed by Sep. 30, 1993).

E6. Anderson, Sandia memo, "Explanation and Approval for Converting Purchase Requisition AE-0795 into a Contract," 7/16/93.

E7. Sandia Procurement Contract, 14-3028, For destructive physical analysis per SS390133 by Analytical Solutions Inc, 5/8/91 (Cancelled).

E8. SS390133-000, Shelf-Life Program Destructive Physical Analysis, Issue B, 10/92.

E9. M. Strizich, Alliance Analytical letter, Response to request for DPA quote, 3/21/91.

E10. R. Anderson, Sandia memo, " Specification for Destructive Physical Analysis," 3/11/91.

- E11. SS390133-000, Shelf-Life Program Destructive Physical Analysis, Issue A, 3/91.
- E12. Alliance Analytical, Destructive Physical Analysis of Semiconductor Devices (CD-AA-003), Rev. A, 12/16/87.

F. Drawings

- F1. J. Middleton, "W88/Mk5 LSI Shelf-life Program Requirements Drawing," 1/18/91.
- F2. BB390133-000, "Shelf-life Program Requirements, AMO Manufactured LSI Components and Material," Issue B, 4/90.
- F3. BB390133, "Shelf-life Program Requirements, W88/MK5 LSI Components and Material," issue D, not dated.
- F4. BB390133-000, "Shelf-life Program Requirements, AMO Manufactured LSI Components and Material," Issue A, 6/89.
- F5. BBYYYYYY, "Shelf-life Program Requirements, Albuquerque Microelectronics Operation Manufactured LSI Devices and Material," Review draft, version 4.0, not dated.
- F6. C. Trauth, "Draft definition drawing for a CRM shelf-life program (version 4.0) and a revision of the planning document," 12/18/87.
- F7. CRM Shelf-Life Program Planning Document, issue A, 11/15/87.
- F8. C. Trauth, "Draft definition drawing for a CRM shelf-life program," 11/11/87.
- F9. C. Trauth, "Draft definition drawing for a CRM shelf-life program," 11/9/87.
- F10. C. Trauth, "Some observations about shelf-life sampling, testing, and DPA parameters," 11/6/87.
- F11. E. Saverino and R. Anderson, "CRM Shelf Life Program," 10/14/87.
- F12. G. Merren and C. Trauth, "Draft definition drawing for a CRM 4/3 Technology Shelf-Life program," includes draft BB drawing (version 1.0), 10/22/87.

G. Meetings (date and agenda items)

- G1. DPA Analysis Group; customer requirements for final report.
- G2. DPA Analysis Group; inspection failures.
- G3. Shelf Life Program Committee; program documents, electrical failures, and transfer of shelf-life program to KCD.
- G4. Shelf Life Program Committee; failure analysis report, DPA activity, transfer for program to KCD, parameters for trend analysis, and document changes.
- G5. Shelf Life Program Committee; funding, sampling, testing, DPA, and storage.
- G6. Shelf Life Program Committee; failure analysis and AMO production schedules.
- G7. Shelf Life Program Committee; status, dynamic screen, changes to BB390133, and SA3230C failures.
- G8. Shelf Life Program Committee; finalization of shelf-life specification and SA3230C first year activities.
- G9. Shelf Life Program Committee; package type selection, preconditioning, and definition of specifications.
- G10. Manpower and equipment status, budgets, changes to planning, and future "steering committee."
- G11. Overview of proposed shelf life program.
- G12. Shelf Life Program; sample selection, DPA planning, and program life.

The following are references from a file provided by Ron McClintock on 10/1/96.

- M1. M. Diehl and R. McClintock, ASKCD Memo, "SA2998D-2 Shelf-Life Failure Analysis Summary," 11/22/91.
- M2. J. Middleton, Sandia Memo, "Meeting on SA2998 High Current Anomaly in Shelf-Life Program," 11/15/91.
- M3. R. McClintock, Hand written notes on SA2998D-2 shelf life failure analysis summary, 10/15/91 attached to KCD-2663 Failure Analysis Request Form/Report #10080 (for 8 SA2998D-2 failures on 10/30/90).
- M4. R. McClintock, Memo, "SA2998D-2 Group-B N-Well Control Inverter Failures," 6/17/91.
- M5. P. Einerson, ASAMO memo, "SA2998 S/N 49788 Group B (OP6750) Failure Analysis Report," 10/26/90.
- M6. B. Berry, ASAMO Memo, "Lot J19014QGRPB (SA2998D-2) Failure Analysis Report," 7/17/90.
- M7. P. Dressendorfer, J. Rodriguez, R. Nasby, S. Everist, and T. Nguyen, "Final Report on SA2998 Manufacturability Studies," 5/30/89.

The following are additional references for this report.

- R1. J. Soden, "SA2141 LSI IC Weapon Stockpile Failure," Sandia Memo, Oct. 1, 1980.
- R2. J. Soden, "Gate Array Shorts," Sandia Memo, Feb. 11, 1986.
- R3. J. Soden and W. Witkowski, "Failure Analysis of SA3001A SN 25566," Sandia Memo, Nov. 12, 1993
- R4. A. Campbell, "Interim Failure Analysis Report for Customer Review," Sandia Memo, Jun. 25, 1990.
- R5. A. Campbell, "Apparent Contamination or Corrosion of W88 Shelf Life Parts," Sandia Memo, May 24, 1991.
- R6. N. Magnuson, Summary of MC3811 E-Testing and D-Testing Failures, one page of notes, Oct. 4, 1996.
- R7. N. Magnuson, "Component Reliability Assessment for the MC3811 Programmer," Sandia Document, Aug. 1996.
- R8. A. Campbell, "Interim Report: Analysis of SA3601 Dynamic Screen Failures," Sandia Memo, Jun. 25, 1990.
- R9. J. Soden, "4/3 Technology Snapback Information," Sandia Memo, Aug. 9, 1990.
- R10. A. Ochoa, et. al., "Snap-Back: A Stable Regenerative Breakdown Mode of MOS Devices," IEEE Trans. Nuclear Science, Vol. NS-30, No. 6, pp. 4127-4130, Dec. 1983.

X. Report Distribution

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W.M. Miller	D/1276	MS1081	
C.A. Reber	D/1333	MS1082	
M.J. Mundt	D/2314	MS0537	
N.D. Magnuson	D/12335	MS0830	
E.L. Saverino	D/12336	MS0637	
F.P. Freeman	D/12363	MS0633	
J.N. Middleton	D/12363	MS0633	
W.L. Schrader	D/12363	MS0633	
J.J. Schwartz	D/12363	MS0633	
S.M. Kohler, Attn: J.L. Wilcoxon	D/2334	MS0501	
W.H. Schaedla, Attn: D.R. Lyngen	D/2343	MS0533	
P.A. Sena, Attn: K. Shin	D/2151	MS0479	

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Dennis Lemon	D/416	FH40	
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X. Report Distribution (continued)

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XI. Appendix

Supplemental information.

Table 7
Data Files for the Program

File Name	File Size	Date Time	Creator	Content
SHELFDPA.DOC	38912	01/11/96 05:47:00PM	R. Anderson	Word summary of DPA info.
BB390133.DOC	4454912	05/15/96 11:36:04AM	C. Evans	Scanned version of issue C
QER01A.XLS	17408	05/05/96 02:23:00PM	C. Reber & D. Johnson	DPA info. and findings
OVERVIEW1.XLS	27648	05/06/96 08:31:00AM	J. Minihan	Summary of program activity
SA2998D1.XLS	393216	05/07/96 03:18:00PM	J. Minihan	SA2998 details & test data
SA3000D1.XLS	103424	05/06/96 03:26:00PM	J. Minihan	SA3000 details & test data
SA3001H1.XLS	94720	05/06/96 03:14:00PM	J. Minihan	SA3001 details & test data
SA3230D1.XLS	258048	05/07/96 07:22:00AM	J. Minihan	SA3230 details & test data
SA3246C.XLS	125952	05/07/96 08:09:00AM	J. Minihan	SA3246 details & test data
SA3601D1.XLS	120832	05/07/96 01:41:00PM	J. Minihan	SA3601 details & test data
SUMMARY1.XLS	24064	09/30/96 12:22:00PM	J. Minihan	Test programs & testers used

Table 8
Information for ICs in the Program

IC Type	IC Function	Year Started	# Started	# Elect. Failures *	# DPA samples	# Avail. for reuse **
SA2998	1K MNOS RAM	1989	19	10	4	5
		1990	20	2	2	16
		1992	20	0	2	18
SA3000	SNL/AMO μ P	1989	20	1	4	15
SA3601	Harris μ P	1992	18	1	4	13
		1993	40	0	8	32
SA3001	2K SRAM	1989	20	1	4	15
		1993	20	0	4	16
SA3230	A/D Converter	1989	18	0	4	14
		1990	20	0	2	18
		1991	20	0	2	18
SA3246	Clock Counter	1989	17	0	4	13
		1990	20	0	2	18
Total			272	15	46	211

* Unique SN's with presumed valid electrical IC failure modes that went to failure analysis.

** ICs that finished the program and are available for other use.