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## SAND DEVIL: A Digital Video Link for Telemetry Applications



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**SAND DEVIL:  
A DIGITAL VIDEO LINK FOR TELEMETRY APPLICATIONS**

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**ABSTRACT**

A digital video encoder/decoder has been built which is suitable for airborne telemetry. The system allows the use of multiple black and white or a single RGB camera. The spatial resolution, frame rate, and pixel compression algorithm can be tailored to specific mission requirements. The output bit rate of the encoder can be varied from 0.89 to 7.16 Mbit/sec, depending on test range capability and RF data link considerations. The digital output of the encoder can be encrypted for data security. The system architecture is flexible, yet very simple, leading to a compact design. Also, the entire system is implemented with off-the-shelf components, thus reducing development time and cost. The size of the encoder and decoder can be reduced substantially by using surface mount devices.

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## Glossary of Terms and Acronyms

ADC	Analog-to-digital converter
ALDPCM	Adaptive, logarithmic, differential pulse-code modulation: a class of algorithms for compression/decompression of digital data.
Air unit	The portion of the SAND DEVIL system that transforms the analog signals supplied by video cameras into coded, serialized, digital data. Also called the Encoder.
Back Porch	Part of an analog video signal: the time period between the trailing edge of the horizontal sync pulse and the beginning of the video line picture content. In color systems, this is where the color burst signals occur.
BCD	Binary-coded decimal: A format for representing base 10 numbers using binary digits. A number is represented with four bits per base 10 digit. For example, 19 (base 10) would be represented as "0001 1001."
DAC	Digital-to-analog converter
Decoder	See "Ground unit"
Encoder	See "Air unit"
EP1800	An erasable programmable logic device (EPLD) produced by Altera that contains logic arrays and storage elements. Used in SAND DEVIL for most control state machines.
EP910	An erasable programmable logic device produced by Altera, smaller than the EP1800. Used on the Decommutator board.
EPLD	Erasable programmable logic device: A chip containing logic arrays along with storage elements (latches and registers) all of which may be programmed to implement sequential logic circuits.
EPROM	Erasable programmable read-only memory. Used in SAND DEVIL to store data compression/decompression algorithms and a video test pattern.
Even Parity	A method of coding data for error detection in which an extra "parity" bit is appended to the end of a data word. When even parity is used, the value of the parity bit is selected such that there are an even number of 1's in the data word and the parity bit taken together. e.g. the data word "010" would receive a parity bit of "1" while the data word "110" would receive a parity bit of "0".
FF/OD	Freeze Frame / Overlay Decoder: Implemented in an EP1800 on the Frame Router board (ground unit). This

device is responsible for determining which frame memory should receive each incoming frame of data. It may "freeze" the picture on a screen by choosing not to write new data to a frame memory.

FIFO	First in, first out: a type of memory configuration useful for buffering data. Data is read from the memory in the same order that it was written to the memory.
Field	One half of an NTSC standard video frame. Two fields are interlaced to compose a frame.
Flight box	The package containing the SAND DEVIL air unit.
Frame	One complete NTSC standard video picture. Frames are produced at the rate of 30 per second in standard video signals.
Front porch	Part of an analog video signal: the period between the end of the picture content of a video line and the leading edge of the horizontal sync pulse for the next line.
Ground box	The package containing both the SAND DEVIL ground unit and an air unit used for testing purposes.
Ground unit	The entire unit that transforms the coded, serialized digital data into NTSC-compatible analog video signals. Also called the Decoder.
LED	Light emitting diode
lsb	Least-significant bit
msb	Most-significant bit
Mbps	Mega-bits per second
MSPS	Mega-samples per second
NTSC	National Television Standards Committee
OSSM	Omni Spectra sub-miniature coaxial connector; equivalent to the military designated SSMA connectors
PLL	Phase-locked loop
PWB	Printed-wiring board: the substrate on which all components are mounted.
RAM	Random access memory: a memory which may be read or written but loses its contents when power is removed.
ROM	Read-only memory: a memory which cannot be overwritten but holds stored data even when no power is supplied.
SAND DEVIL	Sandia digitally encrypted video link
SBE	Single Bit Error: in SAND DEVIL, an error in a 15-bit sync word in which exactly one bit is inverted.
VCO	Voltage-controlled oscillator
VCXO	Voltage-controlled crystal oscillator: more stable but less frequency range than a VCO.

**VDF** Video Data Formatter: an EP1800 on the Formatter Board (air unit). The primary purpose of this device is to format the video data for transmission. It also controls the A/D conversion of the video signal, the storage and retrieval of the digital data from the FIFO buffer, and the compression of the digital data.

**VSG/MC** Video Sync Generator / Memory Controller: an EP1800 on the Ground Controller board (ground unit). The primary purpose of this device is to generate the necessary video sync signals for the reconstruction of the analog video signal and to generate the majority of the control signals for the ground unit.

**VTPG** Video Test Pattern Generator: an EP1800 on the Test Pattern Board (air unit). The primary purpose of this device is to control the generation of an analog video signal for use as a test pattern. It also controls the synchronization of the encoder and the video cameras, and generates routing information for insertion at the start of each video frame.

## 1.0

## INTRODUCTION

The remote transmission of video images has two interesting general applications: reconnaissance, and motion analysis of a flight vehicle. Video information can be transmitted in either an analog or a digital form. The disadvantage of analog video is that it is not easily encrypted and is susceptible to noise and distortion. Digital video allows the use of digital encryption techniques and error correcting codes. However, digital video is not widely used in telemetry systems because it usually requires either a high bit rate or complex data compression circuitry. This report describes SAND DEVIL, a digital video encoder/decoder suitable for airborne telemetry. Some of its design goals include:

1. Low volume and power;
2. Compatibility with current range receiving and recording capabilities;
3. Flexibility, so the system can be adapted to a wide variety of scenarios;
4. Budget constraints (which preclude the development of custom chips); and
5. A specific mission requirement to multiplex several cameras to the encoder and have a test pattern generator for an end-to-end system ground check.

Figure 1 is a block diagram of the SAND DEVIL system. The air unit selects analog video input from one of three external cameras on a frame-by-frame basis. This signal is digitized and stored in a FIFO buffer. The data is read from the FIFO at one-third or one-sixth the bit transmission rate (depending on whether the pixels are to be compressed to three or six bits, respectively) and passed through a pixel compressor. The serial digital output may then be encrypted before being transmitted. The entire shaded area representing the air unit is controlled by the VTPG (video test pattern generator; not shown).

The ground unit accepts decrypted data through the decommutator. The decommutator strips synchronization information from the bit stream and passes valid data to the pixel expander. The expanded data is stored in the FIFO buffer to be read out at a high rate and stored in one or more frame memories as determined by the Frame Router. Each frame memory has its own D/A converter that generates an analog video signal from the digital data. The entire shaded area representing the ground unit is controlled by the VSG/MC (video sync generator/memory controller; not shown).

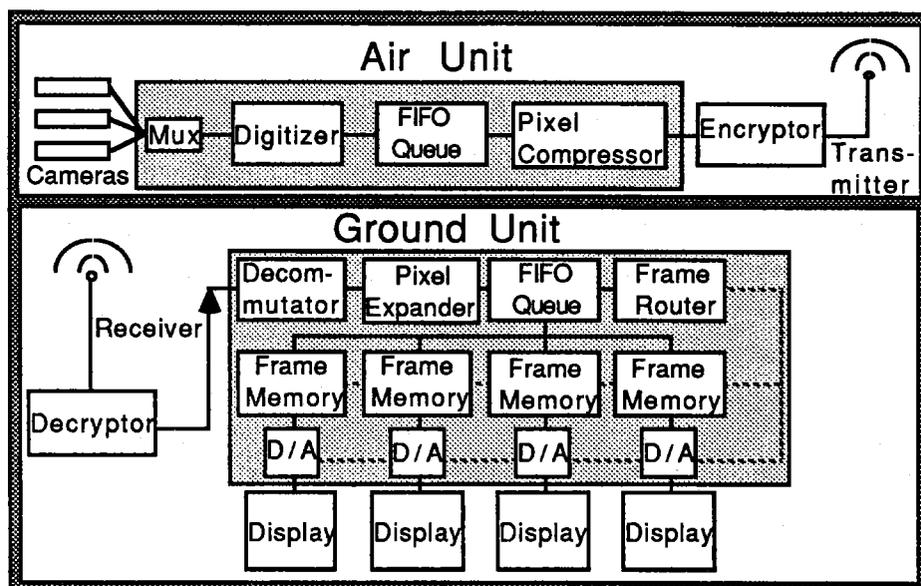


Figure 1: SAND DEVIL Block Diagram

It should be noted that while SAND DEVIL was designed for use as part of an airborne telemetry system, there may be a wide range of applications for a digitally encrypted video system.

The people responsible for the major portions of this project are as follows: Cory Ottesen did the initial system design and is responsible for the many features of SAND DEVIL; Mike Bell designed the Decommutator and Frame Router boards, built the first proto-type, and designed the layout for the printed circuit boards; James Meacham did the debugging of the proto-type and documented the project.

This report is organized in several sections. Chapter 2 discusses the data reduction/compression techniques used by SAND DEVIL. Chapter 3 describes the format of the transmitted data. Chapters 4 and 5 give an overview of the operation of the entire system. Chapters 6 and 7 then give a very detailed look at the functions of each of the boards in the system. Chapter 8 discusses the performance of the proto-type system and goes on to suggest how SAND DEVIL may be significantly reduced in size and power consumption. Several appendices contain relevant material. Appendix A contains board schematics along with notes where appropriate. Appendix B contains a discussion of the pixel compression algorithm used at the time of this writing along with the programs to generate the necessary data for storage in a EPROM. Finally, Appendix C is intended to be a user's manual. It describes the set-up and operation of SAND DEVIL in all of its different modes.

## 2.0

## DATA REDUCTION/COMPRESSION

Most of today's test ranges can not support digitized video rates. Digitized video requires transmission rates greater than 40 Mbits/sec, while current ground stations can only support rates of 1-10 Mbits/sec. The video bit transmission rate must be reduced to be compatible with existing ground stations.

SAND DEVIL uses three methods to modify its digital video transmission rate. First, a reduced rate of pixel sampling per frame decreases the spatial resolution (proportional to the number of pixels per unit area of the display) of the image. Second, a frame buffer allows entire video frames and/or individual video fields to be skipped, thereby reducing the temporal resolution and/or further reducing the spatial resolution of the image. Finally, a pixel compressor can reduce the number of bits per pixel based on various data compression algorithms.

Figure 2 illustrates an analog video signal for one full frame of video. This signal is nominally 1 V peak-to-peak. The figure shows the two major portions of the video signal, sync and video. There is a long series of sync pulses between "fields" and a single sync pulse between lines. Table 1 summarizes the NTSC standard video signal. Video cameras operating with this standard produce one picture "frame" every thirtieth of a second. A single video frame is composed of two sub-frames, or fields; each field contains 262-1/2 horizontal scan lines (with 525 lines per frame). The scan lines are interleaved such that one field fills in the missing information between the lines of another field. (Or, imagine odd-numbered fields as drawing odd-numbered lines and even-numbered fields as drawing even-numbered lines.) Each line is a continuous scan of image brightness. To digitize the image, the scan lines can be sampled with a 14.31818 MHz clock, which is the basis of the NTSC (National Television Subcommittee) standard [1]. At this sample rate, each line would contain 910 pixels. A full-resolution video system, therefore, could produce frames of 910 pixels by 525 lines (horizontal by vertical; "spatial resolution"), 30 times per second (frame rate; "time resolution"). Sampling at 7.16 MHz during analog-to-digital conversion cuts the horizontal resolution in half, reducing the total information per frame by half. Lower sampling rates would continue reducing the total data per frame, but also would reduce horizontal resolution.

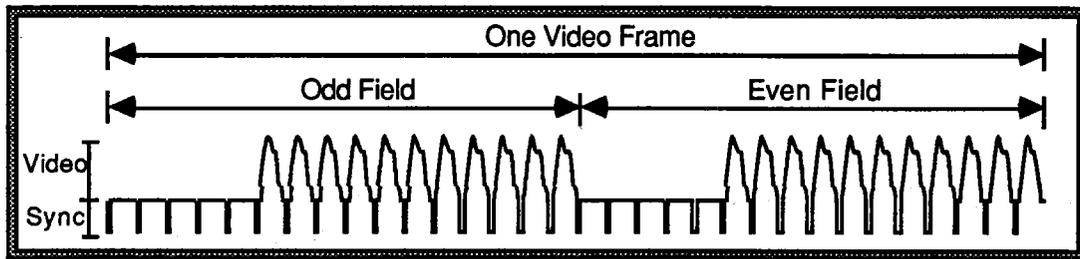


Figure 2: Analog Video Signal

Table 1: NTSC Standard Video Signal

Frame Rate	30 frames/sec
Fields per Frame	2
Total Lines per Field	262.5
Video Lines per Field	245.5
Sync Lines per Field	17
Digital Sampling Rate	14.31818 MHz
Total Samples per Line	910
Video Samples per Line	754
Sync Samples per Line	156

To further reduce the data per frame and maintain acceptable horizontal resolution, SAND DEVIL uses another technique that reduces vertical data as well. Reducing the vertical data by one-half is accomplished by digitizing every other field. Digitizing only every fourth field also reduces the frame rate by half, which further reduces the data rate. Digitizing fields even farther apart results in lower frame rates and data rates. Although A/D conversion continues at a high rate, a single digitized image (either a field or a frame) can be stored in memory and then read out at a lower rate (with data being transmitted continuously during both the used and unused fields). SAND DEVIL uses a FIFO memory as a frame buffer to reduce the complications of memory addressing.

Using the figures in Table 2, it can be seen that a 23% data reduction can be accomplished by digitizing only the parts of the analog signal with actual video content<sup>1</sup> (i.e. not digitizing the sync portion of the analog

<sup>1</sup> 
$$1.0 - \frac{(370,214 \text{ pixels of video content per standard frame})}{(477,750 \text{ pixels per standard frame})} = 0.23$$

**Table 2: Total Data by Format**

	Pixels per Line	Lines per Frame	Total pixels per frame
Standard video frame -	910	525	477,750
Actual video content -	754	491	370,214
Reduced frame -	640	490	313,600
Transmittable frame -	650*	490	318,500
"Hi-res" frame** -	325*	490	159,250

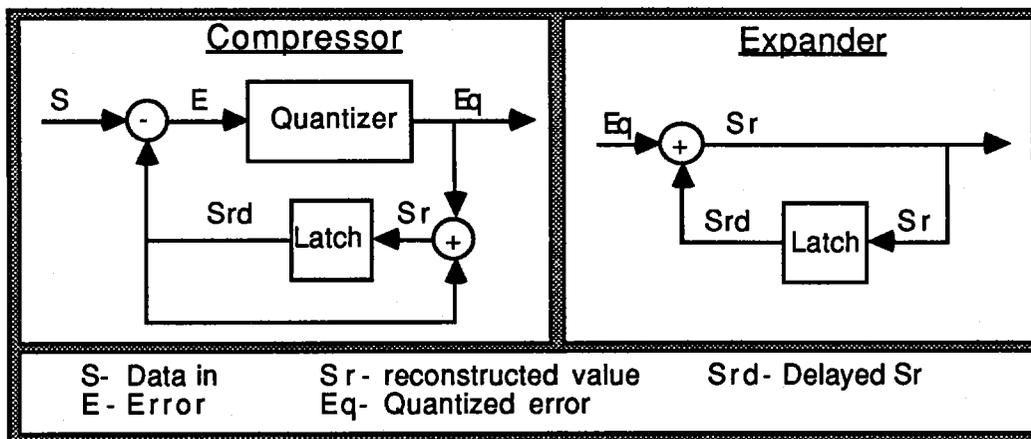
\* additional pixels per line for sync information  
 \*\* Highest resolution frame produced by SAND DEVIL

signal). Also, a "reduced frame" can be created if one of the 491 lines per frame with video content and 114 of the useable 754 pixels per line are not sampled (a 15% loss in video content<sup>1</sup>). Adding a sync word that is five pixels long to each line of the reduced frame creates a "transmittable frame" that is an integer sub-multiple of a full video frame. Thus the ratio of pixels per transmittable frame to pixels per standard frame is 2:3. SAND DEVIL's highest resolution frame contains one half as many pixels as the transmittable frame, so the minimum data reduction is exactly 1:3. The resolution of the video content left in this frame is 1/2 of the NTSC standard resolution since the data is sampled at 1/2 the standard rate. Further reduction of horizontal sampling rate and/or field sampling rate increases the reduction ratio to 1:6, 1:12, etc.

The data remaining after this reduction process is compressed to further reduce the bit rate. A block diagram of one compression technique possible with SAND DEVIL's hardware is shown in the left half of Figure 3. The right half shows the expansion algorithm. The main idea is to transmit the difference between adjacent pixels rather than the whole pixel value. S is the value to be compressed. The last pixel estimate, Srd, is subtracted from S to obtain an error E. Since SAND DEVIL only transmits three bits per pixel, this error E has to be quantized to one of the transmittable errors Eq. This mapping may be done in many ways including truncating all but the highest three bits of the error value, mapping the error to a fixed set of errors spaced evenly between the maximum and minimum values, mapping the error to a variable set of errors spaced logarithmically between the current value and the maximum and minimum values, etc. Once the error has been

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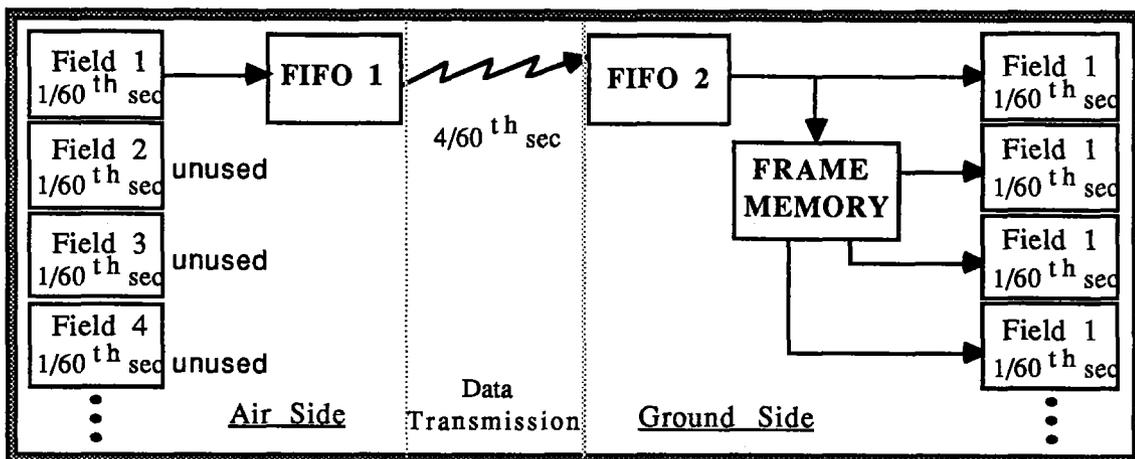
<sup>1</sup> 
$$1.0 - \frac{(313,600 \text{ pixels per reduced frame})}{(370,214 \text{ pixels of video content in standard frame})} = 0.15$$



**Figure 3: Pixel Compression/Expansion Block Diagram**

quantized, it is added to the last pixel estimate and stored in a latch for use in the next cycle. The expansion routine for this algorithm is simple: the received quantized error is added to the previous pixel estimate to form the new pixel estimate. This new pixel estimate is stored in a latch for use in the next cycle and also sent to the output. There are several variations on this theme. Appendix B describes the compression algorithm currently used by SAND DEVIL.

To reconstruct the video signal, data received by the ground unit is first passed through the 3-bit to 8-bit expansion algorithm, then written into the FIFO at a low rate. Data is read from the FIFO at the NTSC-required rate and is sent to a frame memory for storage and to a DAC for immediate display. The data stored in the frame memory is used to refresh the image on the monitor while the FIFO fills up again with the next frame. Figure 4 illustrates this process. Field 1 is sampled and stored in FIFO1 in 1/60th of a second. Transmission begins when the first pixel is sampled and takes 4/60th's of a second. Fields 2 through 4 pass unsampled. On the receiving end, FIFO 2 receives a frame in 4/60th's of a second. Data is read from FIFO 2 in 1/60th of a second and used to create Field 1 on the display as well as to fill the Frame Memory. Field 1 is refreshed from the frame memory over the next 3/60th's of a second as a new frame enters FIFO 2.



**Figure 4:** Example of data reduction & video reconstruction at half vertical resolution and half frame rate.

### 3.0

### DATA FORMAT

SAND DEVIL uses a fixed-length data format for the transmitted data. The system can be tailored to a specific application by selecting an appropriate format from Table 3. Note that while 325 pixels are transmitted per line as indicated in Table 2, five of these pixels are sync words. Therefore, the resulting image resolution is 320 pixels per line.

Data is transmitted with the frame format shown in Figure 5. A minor frame consists of 15 sync bits and 960 data bits. A horizontal video line is contained in one or two minor frames depending on the horizontal resolution and number of bits per pixel. A major frame consists of 245, 490, or 980 minor frames, depending on the vertical resolution and the number of minor frames per line. This data format allows a simple system architecture. A system using a fixed number of bits per pixel is much easier to implement (at the expense of lower compression ratios) than one using a variable bit per pixel algorithm. This format allows one image to be transmitted every 1, 2, 4 or 8 NTSC frames resulting in a frame rate of 30, 15, 7.5, or 3.75

**Table 3: Image Digitizing Formats**

Image Resolution	at	7.16	3.58	1.79	0.89	Mbits/second
320 H x 490 V x 6 bits/pixel =	7.5	*	*	*	*	frames/second
320 H x 490 V x 3 bits/pixel =	15	7.5	*	*	*	frames/second
320 H x 245 V x 6 bits/pixel =	15	7.5	3.75	*	*	frames/second
320 H x 245 V x 3 bits/pixel =	30	15	7.5	3.75	3.75	frames/second
160 H x 245 V x 6 bits/pixel =	30	15	7.5	3.75	3.75	frames/second

\* - Unsupported format

Major Frame Sync: 15 bits	Data: 1st 960 bits (160 6-bit or 320 3-bit pixels)
Minor Frame Sync: 15 bits	Data: 2nd 960 bits (160 6-bit or 320 3-bit pixels)
Minor Frame Sync: 15 bits	Data: 3rd 960 bits (160 6-bit or 320 3-bit pixels)
•	N = 245: 320H x 245V x 3bit/pix or 160H x 245V x 6bit/pix
•	N = 490: 320H x 245V x 6bit/pix or 320H x 490V x 3bit/pix
•	N = 980: 320H x 490V x 6bit/pix
Minor Frame Sync: 15 bits	Data: Nth 960 bits (160 6-bit or 320 3-bit pixels)

**Figure 5: Digital Video Frame Format**

frames per second respectively. Also, the ADC clock, output bit rate, and frame rate are all power of 2 sub-multiples of a 14.31818 MHz system clock, which is also the basis of the NTSC standard[1]. This allows easy synchronization to, and generation of, NTSC signals.

## 4.0

## DIGITAL VIDEO ENCODER OVERVIEW

The digital video encoder is shown in Figure 6 (next page). The encoder has inputs for three video cameras. Camera 1 is the master, and the encoder is phase-locked to it. The other cameras (slave cameras) lock onto the encoder. Alternately, the encoder can serve as the master and all cameras are locked to the encoder's free-running 14.31818 MHz system clock. The VTPG (Video Test Pattern Generator) provides addressing and control signals needed to reconstruct a test image stored in an EPROM. The resulting analog test image signal and the three video input signals from the cameras are fed to the video multiplexer. The VTPG controls which signal is passed through the video multiplexer. With no camera selected, the multiplexer is switched to the test image. When a single camera is selected, the multiplexer is switched to that camera. When more than one camera is selected, the selected cameras are time division multiplexed on a frame-by-frame basis. This allows near simultaneous digitization of up to three black and white cameras (or one RGB camera) by reducing the effective frame rate for each camera. A data tag identifying the source of the video is included on the first line of each digitized frame so that the ground unit will be able to sort the received frames. The multiplexed analog video signal is then digitized, buffered in a FIFO memory, compressed, and finally transmitted.

The format of the data is determined by jumper settings and the algorithm that is programmed into the pixel compressor. The Video Data Formatter (VDF) uses control signals from the VTPG to determine which digitized pixels will be saved in the FIFO. The VDF also recalls the data from the FIFO and passes it through the pixel compressor. The VDF then serializes the data and inserts sync words into the output bit stream.

The selection of the number of active cameras at any one time is controlled through an external device which will be called the flight controller. The flight controller may also initiate a timer reset sequence. When this occurs, a series of coded bits are inserted in the overlay line also used to identify the source of the video. This information is decoded by the ground unit which then resets a digital timer displayed to the operator of the ground unit. This allows events during the flight to be timed.



## 5.0

### DIGITAL VIDEO DECODER OVERVIEW

The digital video decoder is shown in Figure 7 (next page). Data enters the correlator which looks for possible sync words. In search mode, the correlator looks for sync words occurring at 975 bit intervals. When several consecutive sync words are found with the correct spacing, the correlator considers itself locked to the data. When locked, the correlator ignores spurious sync words, yet recognizes valid sync words with single bit errors and bit slips (i.e. the sync word is skewed by one or more bits from its expected position). The correlator outputs a sync pulse every time it expects a sync word. If the correlator misses several sync words in a row, it drops out of lock and enters the search mode. The correlator also performs a serial-to-parallel conversion and passes the resulting 15 bit data words to the multiplexer where it is parsed into 3 bit words. The data is then passed through the pixel expander and stored in the FIFO. The Video Sync Generator & Memory Controller (VSG/MC) uses the sync pulses from the filter to synchronize itself to the incoming data. The VSG/MC sends each frame of data from the FIFO to the proper frame memory. Each frame memory board contains a DAC (digital to analog converter) that continuously reconstructs video from the contents of its frame memory. The data transfer from the FIFO to the frame memory is done in a way that allows the same frame to be shown repeatedly until an entire new frame is ready to be displayed. The VSG/MC also provides all the DAC control signals and frame memory addressing. The PLL (phase-locked-loop) locks the 14.31818 Mhz system clock to a multiple of the incoming bit rate by comparing a divided down system clock generated by VSG/MC to the incoming bit clock. The FF/OD (Freeze Frame & Overlay Decoder) determines the source of each frame by decoding its data tag. The FF/OD also looks at a set of freeze frame switches which allow a frame of data from a particular camera to appear on the freeze frame monitor. Using the source information and the freeze frame switches, the FF/OD provides frame routing information to the VSG/MC. The FF/OD also controls a 999.9 second timer which is reset whenever a timer reset sequence is recognized in the data tag.

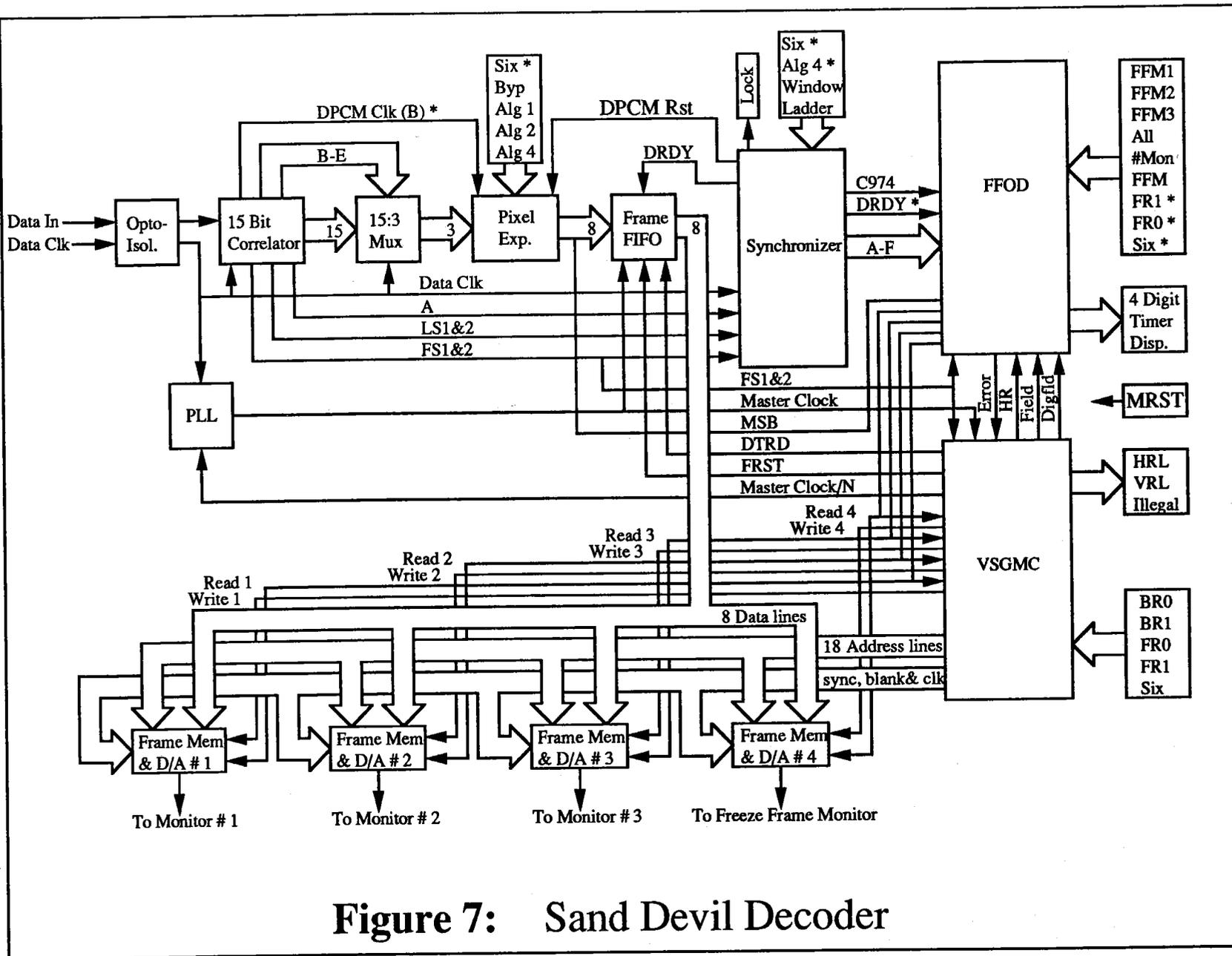


Figure 7: Sand Devil Decoder

## **6.0 DIGITAL VIDEO ENCODER DETAILED DESCRIPTION**

The digital video encoder is contained on three boards: the Formatter board, the Test Pattern board, and the Encoder FIFO board. Appendix A contains the schematics along with detailed notes. The following is a description of the major features and operations of each board.

### **6.1 Data Formatter Board**

#### **6.1.1 Overview**

The Formatter Board has four 75 ohm video inputs for up to three cameras and a test pattern as shown in Figure 6. The video inputs must conform to the NTSC standard except that they must not contain colorburst, chrominance, or audio signals and the video (luminance) signal should be band-limited to less than 3.58 MHz for best operation. The input video signals are "composite" signals, meaning that they contain both video information as well as sync information. The Formatter board extracts the sync information from the signal and digitizes only the video information. Smaller digital sync words are then inserted into the digitized video as it is transmitted so that the analog sync may be re-inserted in the video signal by the decoder.

The analog video signal from camera 1 (the master camera) is AC coupled to a sync separator which separates the sync signal from the analog video signal. The sync signals are used for synchronizing the air unit to the cameras and for DC restoration (setting a known portion of the AC signal to a known voltage) of the incoming video signal. All four video input signals are fed to the video multiplexer / amplifier. One of the four video inputs is selected by the multiplexer, amplified, and digitized by an A/D converter. The voltage reference to the A/D converter is selectable prior to a flight as either a fixed voltage derived from a 1.2 V reference or as a dynamic voltage derived from the sync-pulse amplitude. The latter option is useful if there is a wide disparity in the signal strengths between the input cameras. The output of the A/D converter can be tri-stated, allowing another source to drive the output. This feature is used to drive the A/D output with information on the

source of the frame during the first line of each video frame. This is called the "overlay" process.

The Formatter board also contains the pixel compressor. This is implemented with an EPROM and a feed-back latch as shown in Figure 8. The address to the EPROM is composed of the 8-bit data to be compressed and the last 8-bit pixel estimate. These two values create a unique address that identifies the 3-bit quantized error to be transmitted as well as the next 8-bit pixel estimate obtained when this error is added to the previous pixel estimate. In the 6 bit per pixel mode, the EPROM is programmed to compress an 8-bit pixel into a pair of 3-bit data words in two clock cycles. The compressor is initialized every minor frame by resetting the feedback data latch. This is done to synchronize the encoder and decoder and to minimize transmission error propagation. See Appendix B for a discussion of the algorithm(s) chosen for implementation.

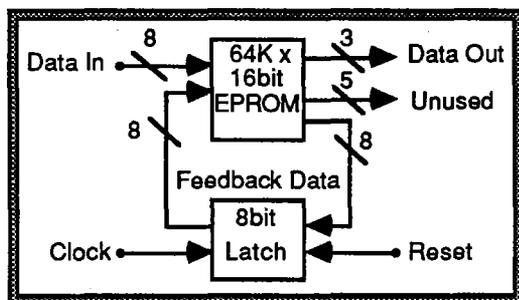


Figure 8: Pixel Compression Hardware

### 6.1.2 Video Data Formatter

The Video Data Formatter (VDF) is an EP1800 EPLD which implements the following functions:

**Bit Clock Generator** - The bit clock is the transmission data rate. It may be set by two jumpers to 7.16, 3.58, 1.79, or 0.89 Mbits/second. The bit clock is derived by dividing the main system clock by the value selected with the jumpers.

**Data Serializer** - The data serializer is responsible for serializing 3-bit or 6-bit data words at one-third or one-sixth the bit transmission rate, respectively. The data selected for serialization depends on the state of the signal BYPASS that is set by a jumper. When the signal BYPASS is not asserted, the data is taken from the output of the EPROM,

thus compressed data is being sent. Since data is serialized in 3-bit groups, data is compressed to six bits by two passes through the EPROM resulting in two 3-bit words. When the signal BYPASS is asserted, the data is taken directly from the FIFO output, bypassing the compression EPROM. Only the top three bits are serialized and transmitted in the 3-bit mode, resulting in only eight possible shades of grey. When the signal SIX is asserted, the bits 2-4 and 5-7 (of an 8-bit pixel with the bits numbered from 0 to 7; lsb to msb) are sent during alternate 3-bit periods, resulting in six of the eight bits from the FIFO being transmitted directly and a possible 64 shades of grey. Regardless of the transmission mode, the data is serialized such that the least significant bit is the first bit transmitted.

The serializer also inserts frame-sync and line-sync information into the data stream. The pixel and line counters are used to determine when these syncs should occur (see "Pixel Counter" and "Line Counter" sections). The sync word is [111 011 001 010 000] for line syncs and the logical inverse of this for frame syncs. The transmission order for the above sync word is from left to right.

**Pixel Clock Generator** - The pixel clock is used in clocking the pixel counter at one third of the transmission rate (also called bit rate). A pixel clock pulse is one system clock period wide and occurs once for every three bits transmitted. Note that this pixel clock is for pixels as they are being transmitted and is much slower than the pixel clock that controls the digitizing of the analog video signal (see section 6.2, "Test Pattern Board").

**Pixel Counter** - The pixel counter on the VDF chip is composed of the signals P1, P2,..., P256. This counter indicates which pixel in the current minor frame is being processed. The count starts at 0 and continues to 324. There are actually only 320 pixels encoded in each minor frame (or 160 pixels per frame in six bits per pixel mode). The additional five counts are accounted for by the sync word that is inserted at the beginning of each minor frame. The counter is synchronously reset after the count of 324 or when a master reset occurs. The clocking rate for the counter is one third the bit rate.

Figures 9a and 9b show the pixel counter sequence as related to a minor frame (a minor frame being a sync word and data block pair). As is shown, either a frame sync word or line sync word (fsync or lsync respectively) occupies the first five counts of each minor frame and the

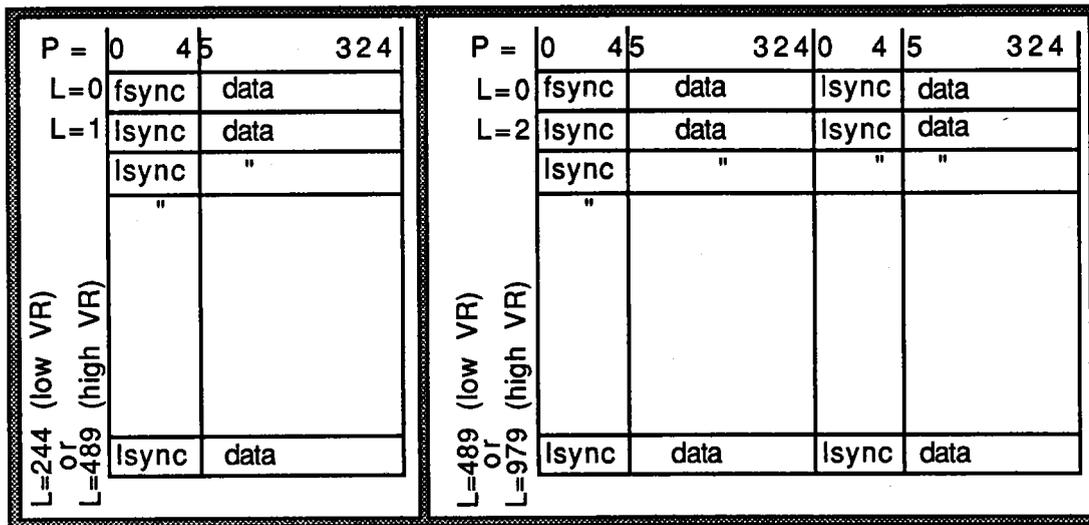


Figure 9a: One minor frame per video line

Figure 9b: Two minor frames per video line

next 320 counts indicate 3-bit data words. Figures 9a and 9b also show the two different ways in which these minor frames are combined to form a major frame. (See section 3.0, "DATA FORMAT" for a complete discussion of major and minor frames.)

**Line Counter** - The line counter on the VDF is composed of the signals L1, L2,..., L512. The line counter indicates in a complicated way which line is being processed. For modes in which one minor frame contains all the data for one line (three-bit, full; six-bit, half resolution) as illustrated in Figure 9a, the counter value is the line being processed. For modes in which two minor frames are required to transmit one video line (six bit, full horizontal resolution) as illustrated in Figure 9b, the line counter is twice the line currently being processed. When only one field per frame is transmitted (half vertical resolution), the maximum count is 244 in the former case and 489 in the latter. When both fields in a frame are transmitted (full vertical resolution), the maximum counts are doubled. The line counter is used to generate a frame sync flag during line count 0, causing the frame sync word to be inserted in that minor frame. This identifies that minor frame as the first in a major frame.

**A/D Controller** - The strobing rate of the A/D converter is the factor that determines the horizontal resolution. In the full horizontal resolution modes, the A/D converter is strobed at one half the master clock rate during portions of the picture that are to be digitized. The converter is not strobed during non-digitized lines, pixels, frames, or fields to conserve power. In the half resolution mode, the strobe is

generated at one fourth the master clock rate during these same periods. A straight division of the master clock by four causes the converter to be strobed at positions horizontally skewed by one pixel width on alternate lines causing vertical edges to appear jagged. The controller compensates by referencing the lowest bit of the line counter generated on the Test Pattern board. (Recall that the line counter on the Formatter Board is the line being transmitted, not the line being digitized.) This signal indicates whether the current line is an odd or even one. During odd lines, strobcs to the A/D are delayed by two clock cycles to vertically align them with strobcs during the even lines.

**FIFO Controller** - The FIFO acts as a buffer for the digitized video data being generated at a high rate by the A/D converter and being consumed at a lower rate by the Formatter board. Data is clocked from the A/D converter at the master clock frequency (14.32 MHz) divided by two or four for full or half horizontal resolution modes, respectively. The signal DRDY (Data Ready) is asserted for each pixel of the picture to be transmitted. The peak rate at which data is written to the FIFO is therefore 7.16 MHz. The data arrives in bursts due to the fact that only a fraction of the video frames available are digitized based on the resolution and bit transmission rate. For each video frame digitized, only a portion of each line is digitized, further contributing to the burst nature of the data.

In contrast, the encoder requires data at a steady rate determined by the bit transmission rate and the number of bits per digitized pixel. Data is requested from the FIFO by asserting DTRD (Data Read). The rate at which DTRD is asserted is equal to the bit transmission rate divided by three or six for three bits or six bits per pixel modes, respectively. (This is the effective pixel transmission rate.)

**Pixel Compressor Controller** - The pixel compressor, consisting of a 1-MBit EPROM and an 8-bit register, is controlled by the two signals DPCMRST and DPCMCLK. The first is a reset signal and the second is a clock signal. Both of these signals are supplied to the feedback register. This register is cleared at the start of every minor frame (during the sync word transmission) by DPCMRST to initialize the compression algorithm state. This keeps errors from propagating for more than one minor frame when the compression algorithm uses the feedback. The register is clocked once by DPCMCLK for every three bits transmitted. Note that this implies that the register is clocked twice during the transmission of a 6-bit pixel. Thus 3-bit compression algorithms are used for 6-bit resolution by performing two compression cycles on the

same data input. Therefore 6-bit per pixel modes encode two discrete jumps to arrive at the desired value as opposed to the single jump encoded in 3-bit per pixel modes.

## **6.2 Test Pattern Board**

The Test Pattern board generates an analog test pattern signal from data stored in an EPROM. It is also responsible for generating sync signals for the cameras as well as synchronizing the system clock with the video input. Additionally, the Test Pattern board determines which frames should be digitized, determines which camera should be the source for each frame, and generates a signal used to tag each digitized frame indicating its source.

### **6.2.1 Encoder Synchronization**

The Data Formatter board must be synchronized with the Test Pattern board. Depending on the selected operating mode, the Test Pattern board either generates the sync signals or is slaved to a master camera. In either case, the VTPG chip receives video field and line sync information stripped from the master video signal on the Formatter Board. The rising edge of the FIELDIN signal (occurring at the beginning of a video frame) ANDed with SYNCIN (to more definitely time the edge) is used to reset the pixel and line counters. These counters are used to generate a horizontal sync signal. With the air unit in the master mode, this sync signal is sent to all of the cameras. With the air unit in the slave mode, the phase-locked loop is used to compare the counter-generated sync with the sync stripped from the master camera. A difference in these two signals causes the on-board oscillator to be adjusted until the counter-generated sync pulse coincides with the stripped sync pulse. The generated sync is then sent to all of the slave cameras via the sync signal output connectors.

Once the above process is complete, the Formatter Board generated reset signal, VDFRST, occurs at the beginning of each digitized frame. VDFRST is used by the Formatter Board to reset its internal counters, keeping them synchronized with the counters on the Test Pattern board.

## 6.2.2 Video Test Pattern Generator Controller

The Video Test Pattern Generator Controller is implemented using an EP1800 EPLD called VTPG. The following functions are performed by the VTPG:

**Pixel Counter** - The VTPG contains a pixel counter that is different than the one on the VDF (video data formatter) that was described in section 6.1.2, "Video Data Formatter." The pixel counter described in this section operates at the frequency at which pixels are being digitized whereas the pixel counter on the VDF operates at the frequency at which pixels are being transmitted.

The pixel counter on the VTPG is composed of the signals P1, P2,..., P256, HL, and DIGPIX. It is a synchronously reset counter with resets occurring only when maximum counts are reached. The system clock drives the counter. The counter is synchronized to the incoming video signal through the actions of the phase-locked loop and VCO (voltage controlled oscillator). The action of the pixel counter is rather complex. A single video line can be partitioned as shown in Fig. 10. These partitions correspond to digitized and non-digitized portions of each half line and are identified by the signals HL and DIGPIX as shown. The pixel counter starts at zero at the beginning of each partition. At the end of the partition, the counter is reset and the signals HL and DIGPIX advance to the next state. There are a total of 910 pixel counts per line. Since the pixel counter advances at the rate of 14.31818 MHz, each pixel time is 69.8 nS. A single line lasts 910 pixels x 69.8 ns/pixel = 63.56 us.

The complex nature of this count is a result of the fact that the center of the video line is important since video fields and some vertical sync pulses can begin or end on a half line. Added complexity arises because only a portion of the video signal is digitized. The rest of the video, along with the sync portion of the signal, is unused. The sync signal is reconstructed in the ground unit.

Note that the pixel counter only indicates times during which the video signal *may* be digitized. The signal might not actually be digitized during that time period. The decision to digitize a particular portion of the video signal is made by other logic circuitry described later.

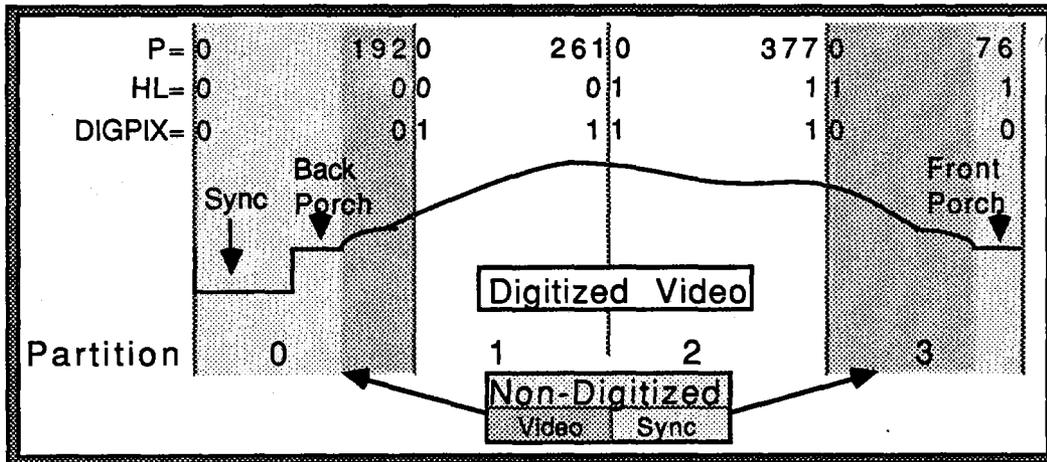


Figure 10: Pixel Counter Sequence

**Line Counter** - The line counter on the VTPG is composed of the signals L1, L2,...,L128, FIELD, and DIGLIN. The line counter has a complex sequence similar to that of the pixel counter reflecting digitized and non-digitized portions of the video signal. Figures 11a-c illustrate the operation of the line counter. It is reset to 3 on the rising edge of the FIELDIN signal stripped from camera 1. (The sync-stripper circuit used changes the state of the FIELDIN signal during the third line of a field.) Under normal operation the counter will be just reaching 3 at this time (see section 6.2.2, "Video Test Pattern Generator Controller"). The line counter then advances at the beginning of each line until it reaches either 16 or 17 depending on whether the field being digitized is the first or second in a video frame, respectively (recall that one video frame is composed of two interlaced "odd" and "even" fields). This region is the non-digitized portion of the video at the top of the screen. The counter is reset to 0, then it is incremented once per line to the count 244. This region is the digitized portion of the video signal. The counter is reset to 0 once again and is incremented once per line until the rising edge of the FIELDIN signal when the cycle is restarted. See Figure 11a for an illustration of this sequence.

Similar to the case for the pixel counter, the line counter indicates times during which the video signal *may* be digitized. The signal might not actually be digitized during that time period. The decision to digitize a particular portion of the video signal is made by other logic circuitry described later.

**Video Sync Generator** - The VTPG generates sync pulses which are buffered and sent to the slave cameras. The sync signal is also connected to the sync input of a video D/A converter to insert sync information into

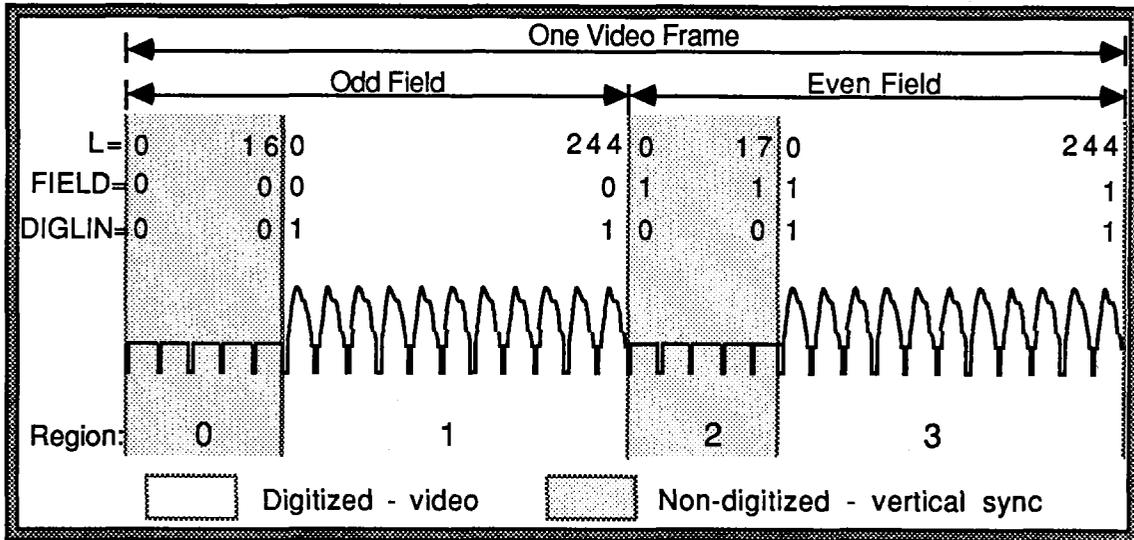


Figure 11a: Line Counter Sequence

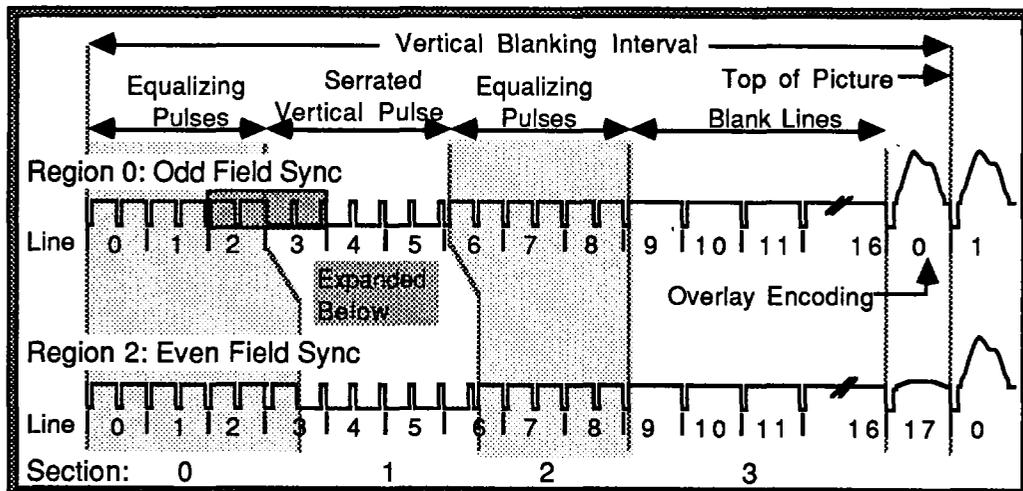


Figure 11b: Sync Pulses in Odd and Even Fields

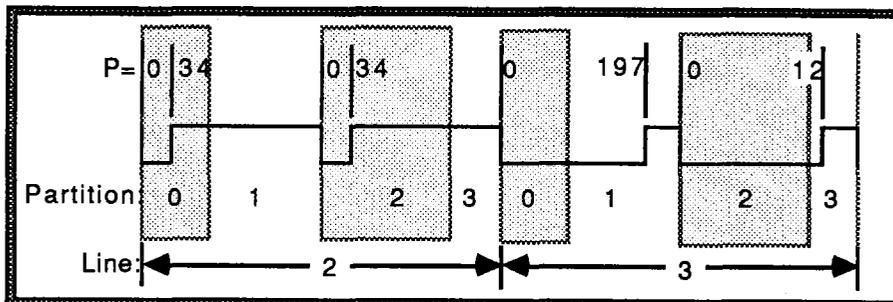


Figure 11c: Pixel Counts at Pulse Transitions

the test pattern signal generated by the Test Pattern board. These sync signals are designed to fall within the specifications of the NTSC standard.

A horizontal sync pulse is initiated at pixel count 76 when DIGPIX is low and HL is high (see Fig. 10). The signal changes on the next clock which is the beginning of a new line. The pulse lasts until pixel count 68 when both DIGPIX and HL are low. Assuming a 14.31818 MHz clock rate, this corresponds to a horizontal sync pulse lasting 4.75  $\mu$ s.

A vertical sync is indicated by a sequence of pulses as shown in Fig. 11b and expanded in Fig. 11c. As shown in Fig. 11b, the vertical sync period may be broken into four logical sections. Pulses in sections 0, 1, and 2 compose the vertical sync. Section 3 consists of ordinary horizontal sync pulses for lines that are "above" the top of a video screen and do not carry video content in the NTSC standard signal. The timing of the pulses is constant within each of these four sections. Moreover, sections 0 and 2 are identical. These facts are used by the VTPG to generate the vertical sync signal as illustrated.

This vertical sync sequence is generated on the VTPG chip by setting and clearing the signal SYNC according to the value of the pixel and line counters and the corresponding section. These counts, and their relations to the pixel counter partitions introduced in Figure 10, are indicated in Fig. 11c. The corresponding pulse widths may be computed by multiplying the count by the period of the system clock.

The signal SYNC generated by the VTPG is buffered and made available individually to the three cameras through three OSSM connectors.

**Test Pattern Generator Controller** - The test pattern generation hardware consists of an EPROM, a D/A converter, and two 8-bit registers (see "Test Pattern Generator" later in this section). The control signals needed for this hardware include addressing for the EPROM, clocking and output enabling of the two registers, a strobe for the D/A converter, and the video sync signals just discussed.

The D/A converter is always strobed at 7.16 MHz which is one half the system clock rate. (The generation of the test pattern is not affected by the mode of operation of the air unit since it is in effect simulating an independent camera.) The lowest order bit of the pixel counter is used as the strobe for the D/A converter since this signal has a period of one half the system clock's period. The data is recalled from the EPROM in

16-bit words and multiplexed into two 8-bit pixels by the registers. For this reason, the address to the EPROM need only change at a rate equal to one fourth the system clock rate. The output enables for the registers are therefore a function of the second lowest order bit of the pixel counter. The enable pulses are made shorter by logically ANDing them with bit 0 of the pixel counter to ensure that the two enables do not overlap. The clock is the same for both registers and is generated by the logical AND of the lowest two bits of the pixel counter resulting in a clock frequency one fourth the system clock rate and a 25% duty cycle. This allows the data from the EPROM plenty of time to settle at the inputs of the registers before being latched. Finally, the address to the EPROM consists of all the bits of the line counter and all but the lowest two bits of the pixel counter (which are the enable and clocking terms). Thus a unique address is generated for every pixel on the screen.

**Digitized Frame Controller** - One of the duties of the VTPG chip is to determine which frames from the input video signal (either from a camera or the Test Pattern board itself) should be digitized. A 3-bit counter (FRMC) is incremented at the beginning of each video frame. The value of this counter and the desired frame rate (determined by jumpers) are used to select one of every 1, 2, 4, or 8 frames. The signal DIGFRM is high for frames that are to be digitized and low for frames that are to be ignored.

**Input Source Selector** - There are four possible video input sources; three camera inputs and the Test Pattern board. One of these signals is selected through an analog multiplexer on the Data Formatter board. This multiplexer is controlled by the VTPG chip. A 3-bit counter (Q) which counts 0 to 5 is incremented on every digitized frame. The multiplexer select lines (S0, S1) are set based on the camera select inputs and the counter state. If no camera select inputs are asserted, the test pattern signal is passed through the mux for any value of Q. If only one camera select is asserted, that camera signal is passed for any value of Q. If two camera selects are asserted, those two camera signals are passed alternately through the mux based on odd or even values of Q. Finally, if all three camera selects are active, all camera signals are passed in a time-share fashion with camera one being passed during count Q=0, camera two during count Q=1, etc.

The Q counter was designed to have six states since six is divisible by both two and three. This allows for easy alternation between two or three cameras at a time.

**Digitized Pixel and Line Generator** - The pixel and line counters include the terms DIGPIX and DIGLIN which indicate the portions of the video signal that *may* be digitized and transmitted. Two extra signals, DIGFRM and DIGFLD (for Digitized Frame and Digitized Field), are used to determine if these portions of the signal actually are digitized. Section 6.2.2 entitled "Video Test Pattern Generator Controller" describes the operation of DIGFRM. DIGFLD is actually generated by the VDF chip on the Data Formatter board due to space and I/O considerations. When the system is operated in a full vertical resolution mode, both the even and the odd fields may be digitized, so DIGFLD is always active. In the half vertical resolution modes, only the odd (first) field of every frame may be digitized, so DIGFLD is active only when the signal FIELD is low.

The portions of the video signal that are actually digitized, buffered in the FIFO, and transmitted are determined by all of the signals DIGFRM, DIGFLD, DIGLIN, and DIGPIX being simultaneously active.

**Timer Reset Generator** - The ground unit contains a timer that may be reset by a message from the air unit. The timer may be used to record the elapsed time between two events by resetting it to zero during the first event, then noting the time (displayed in seconds by the ground unit) of the second. The reset message to this timer is coded in the video signal on line 17 (when the first line in the vertical sync sequence is numbered as line 0; see Fig. 11b in section 6.2.2). This line carries no video content in the NTSC standard signal. The VTPG logically divides this line into five regions (bars) in which five individual bits are encoded. A single bit is encoded in a bar by forcing every pixel in the bar to a pre-determined value. The first two bars are used to encode two bits (TRST1 and TRST2) representing the timer reset state.

SAND DEVIL uses a sequence of four states (coded by two bits) to indicate a timer reset. Using four states avoids spurious resets during noisy transmissions. The action is as follows: 1) The timer state is the default state of 11 (binary); 2) The flight controller asserts TRST (timer reset) for a minimum time equal to the transmission time of one video frame. (Thus the minimum time depends on the particular data format being used.) This action initiates the reset sequence. The timer state advances to 10 (binary) on the next digitized frame; 3) The timer state stays at 10 (binary) until the flight controller de-asserts TRST. 4) The flight controller de-asserts TRST. The timer state advances to 00 (binary) on the next digitized frame; 5) The timer state automatically advances to the states 01 (binary) and 11 (binary) on the next two digitized frames.

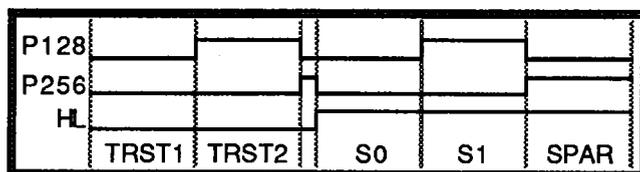
This sequence of events is controlled by a two-bit state machine made of D-flip flops on the VTPG chip. The bars are inserted in the video signal by the overlay generator which is discussed next.

**Overlay Generator** - There are several blank lines between the vertical sync sequence and the first visible line in the standard video signal. SAND DEVIL uses the line prior to the first video line to encode information regarding the state of the timer reset sequence and the camera from which the data in the current major frame originated. The signals TRST1 and TRST2 indicate the state of the timer reset sequence. The signals S0 and S1 indicate the camera of origin, while SPAR is an even parity signal based only on S0 and S1.

The bars are relative to pixel positions across the video line as shown in Figure 12. The bits P256, P128, and HL of the pixel counter are used to determine these positions as indicated. The signal OVERLAY directly drives the top two bits of the digitized pixels as they are stored in the FIFO. Thus a logical "1" is stored as the hexadecimal value "C0" and a logical "0" is stored as the hexadecimal value "00." These bars are continuous across each of the regions indicated in Figure 12.

There is a reason for using the top two bits of the pixel word as opposed to the top bit alone. The eight bit value will be compressed to a three bit value, then reconstructed as an eight bit value by the ground unit. This process introduces errors. If only the top bit were set, the hexadecimal value "80" could easily be corrupted to "7f" by the compression/expansion process. The overlay decoder on the ground unit would then see a cleared high bit and assume the value encoded is a "0" instead of a "1". By setting the two highest order bits, small errors introduced by the compression/expansion process will not corrupt the high bit. This allows the high bit to be used for easy decoding of the overlay values by the ground unit.

The reason for using this overlay scheme is that there is no good way to transmit a single bit from the air unit to the ground unit and be sure



**Figure 12: Overlay Bar Positions**

that it is received correctly. Noise may easily flip bits during transmission, bits may be lost entirely, and the pixel compression/expansion algorithm introduces errors in the data being sent. All of these facts compel the use of multiple pixels (bars) to encode a single bit. This bar may then be sampled multiple times by the ground unit and the probability of decoding the bit accurately is increased.

**Shutter Controller** - Some cameras have a shutter control input. A camera with a faster shutter speed will require higher incident light levels but will exhibit less smearing of fast-moving objects. SAND DEVIL produces a shutter output for controlling the shutter speed for cameras with shutter control inputs. A set of jumpers allows the system to be configured to operate the shutter at eight different speeds.

The output signal is a positive going pulse that starts at the beginning of the first line of a field (when the line counter is at zero and DIGLIN is active). The pulse ends when the line counter reaches a count determined by the jumper settings. The length of the pulse defines the period during which the shutter is "open" and ranges from 1/8000th to 1/60th of a second (see Appendix A for the derivation of these values). The shutter signal generated by the VTPG is buffered and made available to the cameras through OSSM connectors.

To our knowledge, there is not a camera currently available that can use a signal like the one just described. Rather, most cameras with controllable shutter speed have a few set speeds that are chosen by a digital input or inputs. SAND DEVIL may be modified to output a constant voltage by cutting and jumpering a trace as described in Appendix A. The described modifications may also allow the flight controller to set the level of the shutter control line allowing for dynamic adjustment of the shutter speed during a mission.

### 6.2.3 Test Pattern Generator

The pixel and line counters of VTPG are used to address a 16-bit wide EPROM which contains a test image. Each address contains two pixels which are latched by two 8-bit registers with tristate outputs. The register outputs are alternately enabled and latched by an 8-bit video D/A converter which produces the test pattern analog signal. The D/A converter also inserts sync and blanking information into the video output using the sync and blanking signals from VTPG.

#### **6.2.4 Phase Locked Loop**

The encoder can operate in two modes: master or slave. In the master mode, the system clock free-runs at 14.31818 MHz and VTPG generates the sync signal to which all cameras are locked. In the slave mode, the system clock depends on the master camera which is camera 1. The VTPG generated sync signal (based on the system clock) and the sync signal from camera 1 (based on the camera's internal oscillator) are inverted and sent to the comparator input of a phase-locked loop. The output of this chip drives a VCO (voltage controlled oscillator). Any differences in the two sync signals cause an adjustment of the system clock frequency which in turn affects the VTPG generated sync signal. By this method, the VTPG generated sync eventually coincides with the camera generated sync and a lock to the master camera is achieved. The VCO frequency is changed slowly during this process, spreading changes over several video frames. This prevents short glitches in the operation of the master camera from disrupting the entire system. The other cameras lock onto the encoder once the encoder is locked to the master camera.

#### **6.2.5 Opto-Isolators**

Opto-isolators are used on the camera select and timer reset input lines to break possible ground loops between the flight controller and the SAND DEVIL air unit and to protect the internal circuitry from high voltages due to incorrect connections. The differential inputs provide drive flexibility. Inputs from 2.9 to 5.5 V are acceptable in the current configuration. With the changing of a few resistors (see Appendix A), inputs from 18 to 42 V may be accepted.

#### **6.2.6 Output Drivers**

Shutter control signals, sync signals, the bit clock, and the serial data are all provided to OSSM connectors on the air unit package. These signals are all buffered by output drivers that are short-circuit protected, have 50 ohm source impedance, and will drive 2.5 V into 50 ohms. The drivers are built using two paralleled inverters in order to supply enough drive capability to withstand a short on the output.

### 6.3 Encoder FIFO

The Encoder FIFO is used to buffer the data which is produced at a high rate by the ADC and consumed at a slower rate by the pixel compressor and the data serializer. The FIFO is implemented using a FIFO RAM controller chip and four 16k x 4-bit CMOS static RAMs. The FIFO controller accepts "data request" and "data ready" signals and generates addressing and read/write signals for the RAM. The FIFO controller uses a buffered version of the system clock.

Due to the limited speed and address range of the FIFO controller, a byte-folding technique is used to increase the effective data rate and buffer depth. Figure 13 illustrates the byte-folding scheme using paired 8-bit registers and shows the data path through the FIFO. There are two separate paths. The data coming from the ADC is alternately written to even and odd memory. Since the data is written to the memory on every-other 8-bit store to the FIFO, the effective response time of the memory and the FIFO controller is doubled. Additionally, as there is a separate memory space for even and odd bytes, byte-folding doubles the total capacity given the same number of address lines from the FIFO controller.

The byte-folding procedure is implemented using a D-flip/flop in a toggling configuration clocked by the data ready (DRDY) signal. The resulting signal, DRDY divided by two, is used to clock the data registers. The flip/flop and the FIFO controller's input/output address registers are cleared at the start of each digitized frame by FRST (FIFO Reset). This prevents any misalignment between the input and output address registers, caused by missed DRDYs or DTRDs, from propagating to successive frames. On the first DRDY (after a FRST), the flip/flop's inverted output goes low which issues a write request to the FIFO controller. The data is also latched by Register 1. On the second DRDY, the data present at the input is latched by Register 2b, and the data in

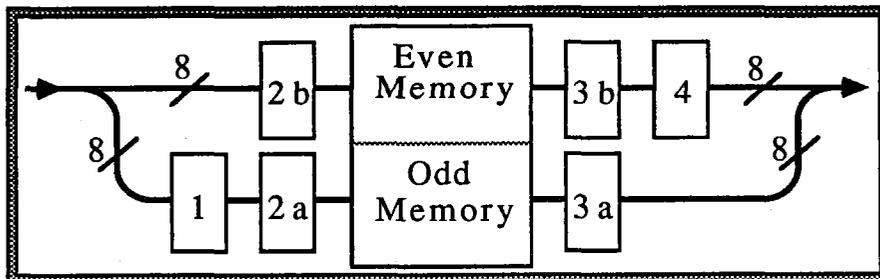


Figure 13: Byte Folding FIFO Expansion Technique

Register 1 is transferred to Register 2a. When the data is written to the FIFO at 7.16 MHz (full horizontal resolution), the latency of the FIFO controller causes the write signal (WR) to the RAM to be delayed until after the second DRDY is received, even though the request was initiated by the first DRDY. When the data is written to the FIFO at 3.58 MHz (half horizontal resolution), there is enough time between DRDYs that the signal WR is issued before the second DRDY occurs. The effect of this difference between the two cases is to shift the picture two pixels to the right when in the half horizontal resolution modes.

During the write to memory when WR is low, the RAM output drivers are tri-stated and the Registers 2a and 2b are enabled. To protect against possible bus contention, the output enable signal for the registers is generated by logically ORing WR with a 20 ns delayed copy of WR to delay only the leading edge of the active-low enable signal.

Data is read from the FIFO by asserting DTRD (data read). DTRD clocks a D-flip/flop which generates one FIFO read request for every two DTRDs. Since the FIFO output rate is relatively slow, the FIFO controller responds to a read request in the same DTRD cycle in which it is requested. On the first DTRD (after a FRST), the flip/flop enables the output of Register 3a placing it on the bus<sup>1</sup> and simultaneously transfers the data in Register 3b to Register 4. On the second DTRD, Register 4 is enabled and shortly thereafter new data is latched into Registers 3a and 3b. The FIFO controller responds to a read request by generating a RAM address and a RREGCK (Read Register Clock) signal. The active-low RREGCK is logically ORed with the system clock to delay latching of data into the read register pair by half of a clock cycle, allowing time for the RAM outputs to settle.

The capacity of this FIFO is 131,072 bytes (128k) and a full resolution video frame contains 156,000 pixels (320H x 490V). At the fastest bit rate (7.16 Mbps), data is read from the FIFO at half of the rate data is being written to the FIFO (on average). By the time a full frame has been written, half has been read back out and the FIFO does not overflow. At the next fastest bit rate, only one fourth will have been read out by the time a whole frame is written to the FIFO, etc. At slower bit rates, full resolution modes (320H x 490V) do cause the FIFO to overflow, disrupting the picture continuity in the lower portion of the video screen.

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<sup>1</sup> This actually puts out valid data because of a "pre-fetch" feature in the FIFO controller. On the first write request after a FRST, data is latched directly into the read registers instead of being written into memory.

## **7.0 DIGITAL VIDEO DECODER DETAILED DESCRIPTION**

The digital video decoder system consists of five to eight boards; the Ground Controller, Decommulator, FIFO, Frame Router, and one to four Frame Memories accomodating up to three real-time monitors and a freeze-frame monitor.

### **7.1 Ground Controller**

The Ground Controller is responsible for determining the mode of operation from the ground-unit's front panel switches, synchronizing the ground unit to the incoming bit stream from the receiver/decryptor, generating the data-read signals for the Decoder FIFO board, generating the memory addressing and enable signals for the Frame Memory boards, and generating the sync and strobe signals for the D/A converters on the Frame Memory boards.

#### **7.1.1 Opto-Isolators**

The data and clock inputs to the decoder are optically isolated, have 50 ohm input impedance and require a drive level between 2.3-5.0 volts. Greater than a 5.0 volt input signal with a 56% duty cycle will exceed the opto-isolator's maximum rating.

#### **7.1.2 Phase Locked Loop**

The system clock is divided down by an amount as determined by the bit rate switch settings to generate a local bit clock. This local bit clock and the incoming bit clock are fed to the comparator inputs of a phase-locked loop. The output of the phase-locked loop drives a voltage controlled oscillator. Any differences in the local and incoming bit clock signals result in an adjustment of the on-board oscillator which is the system clock. Altering the frequency of this oscillator alters the frequency of the local bit clock since the bit clock is a straight division of the system clock. Unlike the phase-locked loop in the air unit, this phase-locked loop responds very quickly to any discrepancies in the compared signals. In this way, the ground unit is synchronized to the

incoming bit stream and tracks it very closely. See the notes on the Test Pattern board in Appendix A for a more detailed description of the phase-locked loop.

### **7.1.3 Video Sync Generator / Memory Controller**

The Video Sync Generator / Memory Controller (VSG/MC) is an EP1800 EPLD that performs the majority of the control functions for the ground unit. A discussion of its specific functions follows:

**Pixel Address Counter** - The pixel address counter is composed of the signals P1, P2, P4, ..., P256, HL, and DIGPIX. For convenience, this will be called the pixel counter. Note that there are pixel counters within the air unit also. The context of the passage should make clear which counter is being referenced. The signals P2 through HL are used as address lines A0-A8, respectively, by the Frame Memory boards. Additionally, the pixel counter is used internally on the VSG/MC in the generation of sync signals, FIFO control signals, frame memory write signals, and the strobe signals for the D/A converters on the Frame Memory boards.

The operation of the pixel counter is very closely related to the operation of the pixel counter on the Test Pattern board in the air unit. Figure 10 (in section 6.2.2, "Video Test Pattern Generator Controller") illustrating the operation of the pixel counter through one cycle is valid for both counters. However, whereas the Test Pattern pixel counter is reset to zero only when a maximum count is reached, the Ground Controller pixel counter is also reset to zero on the occurrence of a frame-sync pulse. This difference is a manifestation of the method used to keep the Ground Controller operating in sync with the data coming from the air unit via the RF receiver. (See "Bit Rate Synthesizer" later this section.)

**Line Address Counter** - The line address counter (or line counter) is composed of the signals L1, L2, L4, ..., L128, FIELD, and DIGLIN. As was the case with the pixel counter, the operation of the line counter is nearly identical to the operation of the line counter on the Test Pattern board. Figure 11a (in section 6.2.2, "Video Test Pattern Generator Controller") accurately describes the operation of the line counter through one cycle.

The difference between the line counter on the Test Pattern board and the line counter on the Ground Controller is in the way the counter is synchronized to the incoming data. Section 6.2.2 entitled "Video Test Pattern Generator Controller" describes the synchronization of the line counter in the air unit. For the ground unit, the line counter is reset to 244 each time a frame-sync pulse occurs. A frame-sync pulse is created when the Decommulator board (discussed later) recognizes a frame-sync word in the incoming data stream. The action of the phase locked loop adjusts the system clock frequency so that the line counter should already be at the count 244 when the frame-sync pulse occurs, causing the count to be continuous. Using this synchronization technique, a vertical sync pulse sequence (illustrated in Fig. 11b) is initiated each time either a frame sync pulse is recognized by the Decommulator or the line counter reaches the count 244, or both.

There is an additional signal on the line counter produced by the Ground Controller line counter called A17. This signal is used as the high order address bit by the Frame Memory boards. In high vertical resolution modes, A17 operates exactly as FIELD does; alternately high and low with successive fields. In low vertical resolution modes, A17 is kept high continuously. Thus, only half of the frame memory is accessed in low vertical resolution modes as would be expected.

**Memory Read/Write Controller** - The VSG/MC produces the active low signals WRITE1-WRITE4, one signal for each of the four Frame Memory boards. These signals may be more appropriately referred to as Enable1-Enable4 since they control when the memory chips on the corresponding Frame Memory board are enabled regardless of whether the memory is being written or read. However, the nature of the signal WRITE<sub>x</sub> is dependent on whether the Frame Memory is being written or read.

First consider the case where the Frame Router board has indicated that Frame Memory X should use the data stored in its memory to reproduce the video picture during the current field. In this case, the signal READ<sub>x</sub> is active (high) for the duration of the field. The memory chips are enabled for the entire field (WRITE<sub>x</sub> is continuously low), even during sync periods. The data supplied to the D/A converter during the sync periods is simply ignored since the D/A converter is not strobed during these times (see section 7.1.3, "Video Sync Generator / Memory Controller").

Now consider the case where the Frame Router board has indicated that Frame Memory X should be written with the data from the FIFO during the current field. In this case, the signal READ<sub>x</sub> is held continuously low during the field. The signal WRITE<sub>x</sub> is active (low) when P1 (pixel counter lsb) is low, giving WRITE<sub>x</sub> a 50% duty cycle and allowing one pixel to be written to the memory for each address produced. The 50% duty cycle is used to ensure that the address has time to settle before the chip is enabled. Note that this signal is independent of the horizontal resolution, so in half horizontal resolution modes each pixel value is stored in two consecutive memory locations.

In either case, the signal WRITE<sub>x</sub> is held inactive (high) during periods when the signal DIGPIX is inactive. The signal WRITE<sub>x</sub> is also held inactive during all lines when DIGLIN is low. These time periods are when the video sync signals occur and WRITE<sub>x</sub> is disabled to prevent writing spurious data to memory during these times.

**Video Sync Generator** - The video sync signal (SYNC) produced by the VSG/MC is identical to the sync signal produced by the VTPG on the Test Pattern board as illustrated in Figures 11b and 11c (section 6.2.2, "Video Test Pattern Generator Controller"). The only difference between the two boards is that the VTPG uses the rising edge of the signal FIELDIN to reset the counter at the beginning of line 3, which is at the end of the first equalizing pulse section of the vertical sync sequence, while the VSG/MC expects the signal FSP (Frame-Sync Pulse) to occur at the end of line 244, which is at the very beginning of the vertical sync sequence. If either of these conditions are not met, the vertical sync sequence is longer or shorter than it should be and the frame may appear to "jump" vertically.

The signal BLANK is generated in conjunction with the signal SYNC. The purpose of BLANK is to indicate when there is no video content in the output analog video signal. BLANK is asserted during the entire vertical sync region illustrated in Figure 11b as well as during the shaded regions in Figure 10 (both in section 6.2.2, "Video Test Pattern Generator Controller").

**D/A Clock Generator** - The DAC converters on the Frame Memory boards require a strobe signal to indicate when the digital data is valid at the input of the converter. This signal, STROBE, is provided by the VSG/MC chip. The signal STROBE is the signal P1 (pixel counter lsb) inverted. This creates a rising edge every 139.7 nS, twice the period of the system clock. The data supplied to the input of the D/A converter

comes from the output of the FIFO board or from the memory chips on the Frame Memory board. When a new frame is to be written to a frame memory, data is taken directly from the FIFO board and is simultaneously sent to the DAC and written to the memory. Data is then supplied to the DAC from the memory on successive frames to refresh the picture on the monitor until a new frame is written to the memory. The data from the memory will change to a new value approximately 40 nS from the rising edge of P1 (when a new address for the memory is generated) and is valid until the next rising edge of P1. Data straight from the FIFO is valid approximately 20 nS from the rising edge of DTRD (which coincides with the rising edge of P1 in full horizontal resolution modes and only every other rising edge in half horizontal resolution modes), but is not guaranteed to be valid at the next rising edge of DTRD. This is because the FIFO controller may clock new data into the FIFO output registers at any time near the end of the cycle. Thus the inverted form of P1 is used as the strobe for the DAC to ensure the strobe is applied in the middle of the cycle when data is most likely valid.

This strobe is independent of the horizontal resolution of the data. This implies that in the half horizontal resolution modes, each 8-bit pixel value gets converted twice by the DAC before a new value appears at the converter's input. This may be noticeable on the monitor if the DAC has significant noise on the output (because two adjacent pixels that should be the same may end up different) but should be unnoticeable under normal conditions.

**FIFO Output Controller** - The VSG/MC chip creates the read-requests (pulses in the signal DTRD) for data from the FIFO. Data is written into the FIFO at a steady rate under the control of the Decommutator board (discussed later in section 7.2, "The Decommutator Board"). Depending on the frame rate and bit rate, the data is read from the FIFO once every 1, 2, 4, or 8 NTSC standard video frames.

The VSG/MC signal DIGFLD (Digitized Field) determines the fields during which DTRDs are issued. DIGFLD is a function of the frame rate jumper settings and the 3-bit frame counter FRMC. FRMC is advanced on the first line of each frame and simply "rolls over" to zero after every eighth frame. For example, in the 7.5 frames-per-second mode, DIGFLD is active for frames when the lower two bits of FRMC are high (every fourth frame.) DIGFLD is additionally limited by the vertical resolution which is a function of both frame rate and bit rate. For full vertical resolution modes, DIGFLD is active for both fields of the frames selected

using the frame counter. For half vertical resolution modes, DIGFLD is only active for the first field of the of the selected frames.

Once the fields during which DTRDs should be produced have been identified, the DTRD signals must be produced only during the portions of the video signal that contain video information. (Since no sync information is written to the FIFO, trying to read during sync periods would upset the system by resulting in more data being read from the FIFO than was written to it.) Additionally, DTRDs are produced at one half the desired pixel rate at the output of the FIFO since each DTRD recalls a 16-bit word, or two pixels. This second requirement is achieved in the full horizontal resolution modes (320H) by enabling DTRD signals when the lowest bit of the pixel counter is low. The requirement is met in the half horizontal resolution modes (160H) by enabling DTRD signals when the lowest bit of the pixel counter is low and the next to lowest is high during the first half of the video line, and when the lowest two bits of the pixel counter are low during the second half of the video line. This change at half-line in the half horizontal resolution modes is necessary since the number of pixels in the first half of the line is not evenly divisible by four.

The signal DIGPIX identifies the portions of the video line for which data is available. Therefore, it is used as an additional enable term for the DTRD signals. One slight deviation is that DTRD is disabled on the last bit of each line since no more data for the line is required, but DIGPIX does not go low until the next pixel clock.

In summary, DTRD signals are issued when DIGLIN, DIGFLD, and DIGPIX are active. The frequency of the DTRD signals is determined by the horizontal resolution and implemented using the lower two bits of the pixel counter as enable terms.

**Data Format Checker** - The signal ILLEGAL goes low to light an LED when the jumper settings create an unsupported combination of bit rate and frame rate. There are two modes which are not illegal but produce a partially obscured picture with approximately one third of the second field of each frame lost due to inadequate FIFO memory for buffering a total frame (see section 6.3, "Encoder FIFO"). These modes are when the selected frame rate is 3.75 frames per second and either the bit rate is 3.58 Mbps and there are 6 bits per pixel or the bit rate is 1.79 Mbps and there are 3 bits per pixel.

**Bit Rate Synthesizer** - The Ground Controller board uses a phase locked loop to adjust the frequency of the system clock in such a way that the ground unit is locked to the incoming data stream. This is done by comparing the incoming bit clock (supplied by a required external clock regenerator circuit following the RF receiver) to a comparison bit clock generated by the VSG/MC. The VSG/MC generates the comparison bit clock by dividing the system clock by the appropriate amount as determined by the bit-rate jumpers. The incoming and comparison bit rates are then compared by the phase locked loop. The oscillator in the loop then adjusts its operating frequency which is the system clock. In the locked condition, the system clock operates at just the right frequency such that the comparison and incoming bit rates are the same frequency.

## **7.2 The Decommulator Board**

The Decommulator Board is the front-end of the decoder system, providing both the data decommulator and pixel expander functions. The input to the ground unit is a continuous, serial data stream and its associated clock (which must be provided); no other control or timing signals are provided. The basic purpose of the Decommulator is to delineate groups and sub-groups of data and correlate them to pixel positions within a video frame. It also provides synchronization information in the form of clocking and control signals to the rest of the ground unit. To keep track of the data flow, the Decommulator identifies the frame-sync and line-sync bit patterns inserted by the air unit. It has the ability to detect corrupted sync patterns and filter false sync patterns that occur randomly in the data; and is provided with a scheme for dealing with synchronization problems that the filters can't handle.

The Decommulator is implemented using three EP910 EPLDs: the Correlator, the Data Multiplexer and the Synchronizer. The pixel expander is implemented with an AM27C1024 64k x 16-bit EPROM and an 8-bit register.

### **7.2.1 The Correlator**

There are three functional blocks in the Correlator; a 15-bit shift register, a divide-by-15 counter, and the line-sync and frame-sync correlators.

**Shift Register** - The shift register is basically a serial-to-parallel converter. Data is clocked into the shift register with an external bit clock (presumably supplied by a "bit synchronizer") which should have a 50% duty-cycle. The data is latched by the register on the positive going edge of the bit clock indicating that the data should be stable during this time. A serial-to-parallel converter only three bits wide is needed to process 3-bit pixel codes, but the larger 15-bit wide shift register is necessary to hold an entire sync word at one time so that it may be recognized. This was one of the driving factors in the selection of the data format (see Figure 5, section 3.0, "Data Format"), and the reason the number of bits per line is a multiple of fifteen.

**Divide-by-15 Counter** - The divide-by-15 counter is actually two counters (a 2-bit divide-by-three counter and a 3-bit divide-by-five counter) which together provide the desired 15 count. Instead of counting 0, 1, 2 as expected, the 2-bit counter counts 2, 3, 0. In binary form it can be seen that this is just the normal count, but with the msb inverted. This is done because the msb is used as a data latching signal in the Pixel Expander and must have a rising edge at the end of the cycle. The three-count is used for delineating each bit in a 3-bit pixel group (even in the 6-bits per pixel mode data is transmitted in groups of three). The divide-by-five counter counts from 0 to 4 in the normal fashion and is used to delineate the five pixels coded within the 15-bit groups. All the counter bits, except the lsb in the divide-by-three counter, are used by the Multiplexer as data selectors (see Fig. 14). Both counters are clocked by an inverted copy of the bit clock and are

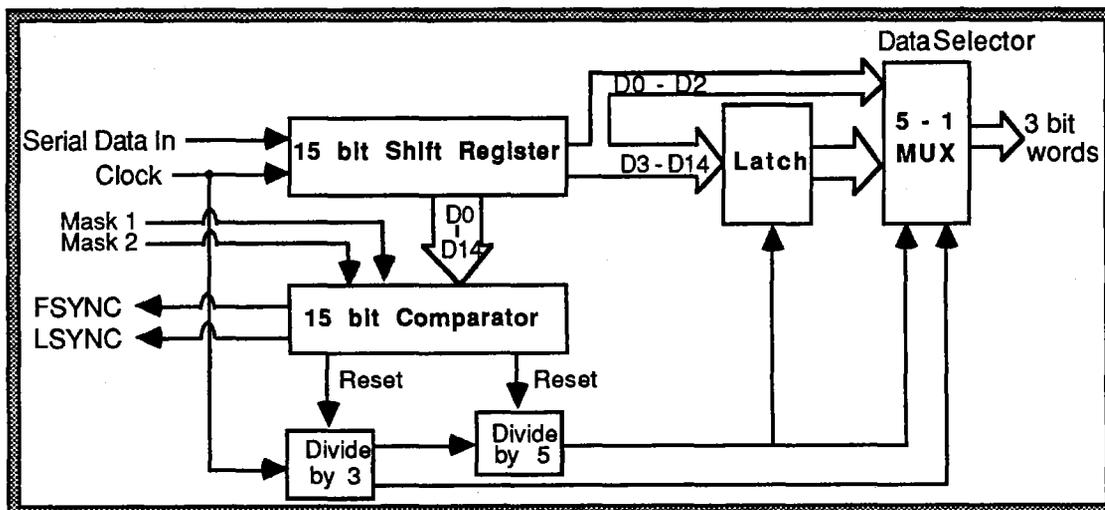


Figure 14: Decommutation of data

synchronously reset after reaching their highest count or when a sync word is detected. Normally both types of reset occur simultaneously; however, in the case of a bit-slip (from a missed or extra clock edge) separate resets will occur and the counters will be re-synchronized to the sync word.

**Line-sync and Frame-sync Correlators** - The line-sync and frame-sync correlators monitor data in the shift register and issue a line-sync or a frame-sync pulse lasting for one bit clock period when the correct 15-bit sequence is detected. These sync pulses can be inhibited by the Synchronizer. The correlators have the ability to detect a sync word even if one of the bits is inverted (a Single Bit Error) due to noise. A sync pulse will be issued in spite of a SBE unless the Synchronizer inhibits this function. Recognizing all cases of SBE requires more logic than is available to a single pin on the EP910 chips, so four sync-pulse lines are required: two to cover all possible frame-sync cases (FS1 & FS2) and two to cover all possible line-sync cases (LS1 & LS2). Frame-sync pulses are fed to the VSG/MC and the Overlay Decoder to indicate the beginning of a frame. The Synchronizer uses both the line-sync and the frame-sync pulses.

### 7.2.2 Data Multiplexer

The Data Multiplexer is simply three parallel 5-to-1 multiplexers and a 12-bit data register. (see data path through the Decommutator in Fig. 14.) The data register holds the twelve most-significant bits through an entire 15-bit cycle. The three least-significant bits are transferred immediately to the output registers at the beginning of the cycle, and the other twelve are multiplexed out through the rest of the cycle. From the output registers, the multiplexed data is presented at the input to the Pixel Expander.

### 7.2.3 Synchronizer

The overall purpose of the Synchronizer is to synchronize the ground unit with the incoming data format. Although this is primarily handled by sync-word detection in the Correlator, the Synchronizer supplements the process by filtering false sync words. It also provides a scheme for dealing with missed sync words, and the total loss of synchronization. Other logic components in the chip generate the reset signal for the Pixel Expander and control data flow into the FIFO.

**Sync Word Filter** - Filtering false sync words is very important, not only because they disrupt synchronization, but also because they are so prevalent. Since the data could be generated from any video image and is coded by a compression algorithm, it can be considered to be a random bit stream. As such, each group of 15 bits in the shift register at any time has a 2 in 32,768 chance<sup>1</sup> (or 0.000061) of imitating one of the two sync words. Over an entire line of 975 data bits, the odds<sup>2</sup> of receiving a false sync word jump to 0.0578; and for a single frame<sup>3</sup> of data, the chance of receiving a false sync word is 0.9999953 - almost a certainty! One way to eliminate false sync words is to detect them in the air unit and alter the code prior to transmission. This would require some way for the decoder to recognize and adjust to the changes, and this would not stop false sync words due to noise during transmission. Another method is needed.

The Synchronizer takes advantage of the fixed data format and only looks for sync words where they are expected - always 975 bits apart. A 10-bit counter driven by the bit clock is synchronously reset to zero after it reaches 974 or when the Correlator detects a sync word (both normally happen at the same time). The counter is used to create a "window"; a period of time identified by certain counts of the counter. While the window is "open," the Correlator can recognize sync words. When the window is "closed," sync words are masked. The size of the window can be selected by on-board jumpers so that the Synchronizer can tolerate bit-slips in the data. With no jumpers on the board, the Synchronizer accepts sync words at counts 971, 972, 973, 974, 0, 1, 2 and 3; a window eight bits wide. With the use of one jumper in either of two positions (see Appendix A), the window can be narrowed to six or four bits wide centered on counts 974 and 0. (The optimum window size will not be known until SAND DEVIL is tested in a field environment.)

The 10-bit counter is also used to provide sync information even when a sync word is not detected at the proper time. The Synchronizer

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<sup>1</sup> 2 sync words to match; 32,768 combinations of 15 bits

<sup>2</sup> To find the probability of getting a false 15-bit sync word in 975 bits, first calculate the probability of not getting an exact sync word in 15 bits. Then raise this value to the 975th power to compute the probability of not getting an exact sync word in 975 bits, and subtract from one. That is,  $P(\text{false sync in 975 bits}) = 1 - P(\text{no false 15-bit sync word in 15 bits})^{975}$ .  $P(\text{no false 15-bit sync word in 15 bits}) = (2^{15} \text{ words} - 2 \text{ sync words}) / (2^{15} \text{ words}) = .9999390$ . Therefore,  $P(\text{false sync in 975 bits}) = 1 - (.9999390)^{975} = 1 - 0.9422 = 0.0578$ .

<sup>3</sup> For this calculation, a frame is 245 lines. Thus, the  $P(\text{false sync word in one frame}) = 1 - P(\text{false sync word in one line})^{245} = 1 - (0.9422)^{245} = 0.99999535$ .

generates a reset signal for the Pixel Expander, with or without a sync word, at counts zero through 14. This initializes the algorithm at the beginning of each line and keeps the sync word from passing through the decoder as data. Bit-count information derived from this counter is also used by the Overlay Decoder.

**Sync Lock Ladder** - The Synchronizer filter dramatically reduces the possibility of receiving false sync words, but it is just part of the overall system for handling synchronizing problems. The sync lock ladder is in control of the whole process. It is a state machine which decides if the system is in sync or not, and determines the reliability of that decision. In hardware terms, it is a 3-bit counter that counts up everytime a sync word is detected when one is expected, and counts down when a sync word is expected but not detected. At the bottom of the "ladder" (see Fig. 15), when the system is first turned on, the Synchronizer is in the SEARCH mode; there is no window, all data is examined for the sync word pattern, and single bit errors are not accepted (only the exact 15-bit line-sync or frame-sync word is allowed). When a sync word is detected, the counter increments up the ladder. At this level the window function becomes effective - it is assumed that the system is now synchronized to the data, although the level of confidence is low since it could have been a false sync word. Single bit errors are still not allowed. If another sync word is found in the first open window, the counter

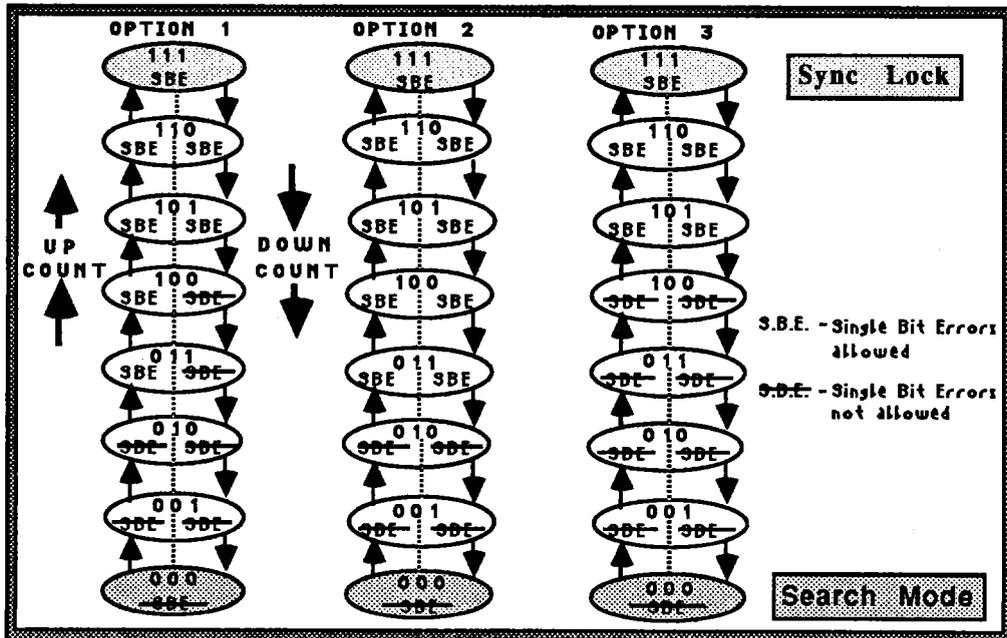


Figure 15: Sync-lock ladder options

increments to a higher level of confidence. If not, it decrements back down to the SEARCH mode level, the window function is disabled, and the process starts over.

When in the SEARCH mode, a true sync word eventually must be detected. Then, unless there is excessive noise, consecutive sync words will be found in the open windows, and the counter will increment up the ladder. At some count, the confidence level will be high enough that single bit errors should be allowed, improving the system's immunity to noise. After eight sync words are detected in a row, the confidence level is at its maximum and the system is considered to be "sync-locked."

Once sync-locked, the system should stay that way, unless the data format is disrupted by excessive transmission noise or by a power drop-out to the air unit. In either case, the Synchronizer will not find sync words in the open windows and start dropping down the ladder. At some count, the confidence level will have dropped low enough to disallow single bit errors. (Since there are 15 ways to have a SBE for each sync word, sync words with SBEs are 15 times more likely to occur in random data than an exact sync word.) Unless confidence is improved with exact sync words, the Synchronizer should go to the SEARCH mode as quickly as possible so that the system can be re-synchronized to the new data format.

To implement this pattern of detecting sync words, the Synchronizer generates two masking signals which become part of the sync-word detection logic in the Correlator. MASK2 is the simpler term, which is used for masking out exact sync words (no SBE). Since exact sync words are allowed at all levels of the ladder, its only function is to mask sync words while the window is closed; it is inactive in the SEARCH mode when the window is always open. MASK1 only applies to sync words with Single Bit Errors. Its function is dependent on the count in the Sync Lock Ladder. At the lower levels where SBE's are not allowed, it is actively masking during the entire line. At the higher levels, it masks while the window is closed. The point on the ladder that transitions from allowing to disallowing Single Bit Errors is arbitrary at this time. Once again, it will require field testing to find the optimum points. It is merely a matter of programming the EPLDs to implement the final decision. In the meantime, and to help with field testing, the circuit is designed to allow selection of three pre-programmed options using a jumper. The ladder options are illustrated in Figure 15. Note that the count direction, as well as the count level, can be a deciding factor, as in Option 1. With no jumper in place, Option 2 is selected.

**FIFO Input Controller** - The Synchronizer generates DRDY (Data Ready), a control signal for writing data into the FIFO. It is similar to the signal that controls the data flow into the Pixel Expander, except that it is phase-shifted to allow for the ROM's access time. (It uses the lsb from the Correlator's 2-bit counter.) In the six bits per pixel mode, since the pixel expander only processes three bits at a time, every other DRDY is masked to allow the data to have two passes through the Pixel Expander.

### 7.2.4 Pixel Expander

The pixel expander consists of a 64K x 16 bit EPROM and an 8-bit latch as shown in Figure 16. The incoming 3-bit quantized error code, the 8-bit feedback containing the last pixel estimate, and the five select lines all compose the address to the EPROM. Each possible address identifies an 8-bit output value and an 8-bit feedback value which are determined by the selected algorithm. Two of the select switches are dedicated to the functions of BYPASS for uncompressed data and SIX for data in the form of six bits per pixel. In the BYPASS mode, the incoming three bits are not interpreted as an error code. Instead, they are taken to be the top three bits of a truncated pixel. The output is therefore the incoming three bits shifted to the top of an 8-bit pixel. Since the output does not depend on the previous pixel, the feedback value is inconsequential. In the SIX mode, the expansion is accomplished by using two successive error codes to arrive at one pixel value. The algorithm can therefore disregard the SIX signal in most cases since it only affects when the data is latched, not how the output is computed. The special case is when both SIX and BYPASS modes are selected concurrently. Now the first three bits to be received are passed to the feedback latch. The next three bits to be received are then combined with the three bits in the feedback latch to form a 6-bit output value. A zero is sent to the feedback latch at this point to indicate that the next three bits will be the

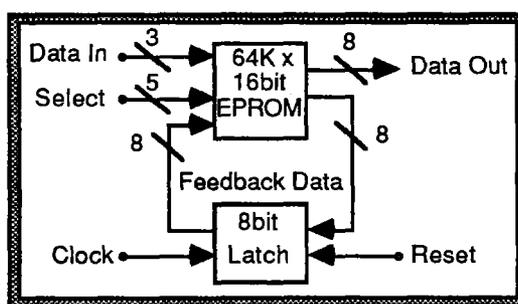


Figure 16: Pixel Expander Hardware

first of six and the process repeats. The other three switches may be used to select one of many expansion algorithms. In order for these selections to work, the expansion algorithm must be compatible with the compression algorithm performed on the data by the air unit. One way this may be accomplished is to use the switches to select among differing degrees of low-pass filtering on the output. Appendix B contains a discussion of the filtering process and the particular algorithm implemented in SAND DEVIL at the time of this writing.

### 7.3 The Decoder FIFO

The Decoder FIFO is used to buffer the data which is produced at a slow rate by the Decommutator and consumed at a high rate by the Frame Memory. The Decoder FIFO is very similar in implementation and operation to the Encoder FIFO in the air unit. The input stage is identical in the two FIFOs. Since the input to the Decoder FIFO always arrives at a relatively slow rate, a WR (RAM write signal) is issued by the FIFO controller during the same DRDY cycle in which it was requested.

The output stage of the Decoder FIFO uses one less 8-bit register than the output stage of the Encoder FIFO and there is a 2 to 1 multiplexer not found in the Encoder FIFO. (Figure 13 in section 6.3, "Encoder FIFO," is valid for the Decoder FIFO if Register 4 is ignored.) These differences are due to the high rate at which the data is read from the Decoder FIFO when the system is operating in the full horizontal resolution modes. In these modes, the latency of the FIFO controller causes the read requested by an initial DTRD to be filled *after* a second DTRD has been received. To deal with this case, a read request is issued to the Decoder FIFO controller by the first DTRD received after a FRST (FIFO reset) through the selection of the flip/flop's inverted output through the mux as the read request signal. The output of Register 3a is enabled at this time<sup>1</sup> placing an "odd" byte on the output bus. A subsequent DTRD causes the output of Register 3b to be enabled, placing an "even" byte on the output bus. The RDCLK fulfilling the read request is issued by the FIFO controller just as the next DTRD comes along, clocking new data into Registers 3a and 3b. This process is then repeated.

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<sup>1</sup> This register contains valid data at this time due to the "pre-fetch" actions of the FIFO controller: the first word written to the FIFO is stored directly in output registers without going through a memory cycle.

When the system is operating in a half horizontal resolution modes, the read request is filled during the same DTRD cycle in which it is initiated. This case is handled through the selection of the flip/flop's positive output through the mux as the read request signal. Now the first DTRD enables the output of Register 3a. The second DTRD enables the output of Register 3b and initiates the read request. This read request is filled (RDCLK is issued) just as the next DTRD comes along, clocking new data into Registers 3a and 3b. This process is then repeated.

## **7.4 Frame Router**

The Frame Router board performs essentially two functions: it determines which frame memory (if any) should receive the current incoming frame of data, and it provides timer control for a four-digit LED clock which is mounted on the front panel of the ground unit. Since the incoming frames could have any one of four video input sources, the frames must be de-multiplexed in the Decoder and sent to the appropriate frame memories. The source ID-tag overlaid on line 17 of each frame along with the setting of the front panel switches for Single/Multiple Monitors and Freeze Frame are used by the Overlay Decoder to determine the destination frame memory. The Timer clock displays elapsed time in tenths of a second up to 999.9 seconds. The clock is reset when a specific set of reset signals is decoded from the overlay line of four consecutive frames. A special-purpose chip implements the timer functions, drives the LEDs, and is the interface between the Overlay Decoder and the timer display.

### **7.4.1 Overlay Decoder**

An EP1800 called the Freeze-Framer/Overlay Decoder (FF/OD) functions as the overlay decoder, freeze-frame/frame-route state machine, and the timer controller. The Overlay Decoder looks at the digital data as it is being written into the FIFO. This is the first point where uncompressed data is available, and it allows the Overlay Decoder to decode the frame routing information well before the data is to be routed to the appropriate frame memory (which is when it exits the FIFO). The frame-sync and line-sync signals from the Decommutator are used to identify the overlay line. Then, with input from the Synchronizer bit-counter to sub-divide the overlay line, the Overlay Decoder translates the encoded bits for timer reset state (T1 and T2), video source (S0 and S1), and parity (PAR). The relative positions of

where these bits are encoded in the minor frame(s) are shown in Figure 17. To filter errors in the code from noise on the data line or from the data compression routine, each of the coded "bits" is sampled at three points. A value greater than or equal to 128 is interpreted as a logical "1" while a value less than 128 is interpreted as a logical "0." The common logical value at two or more of the sample points is taken to be the logical value of the bit being decoded.

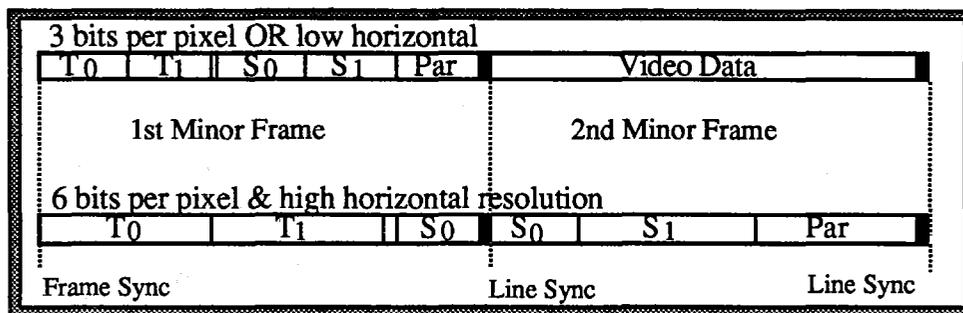


Figure 17: Overlay Line Formats

#### 7.4.2 Freeze Framer and Frame Router

The freeze-frame/frame-route state machine (or Freeze Framer) ultimately uses the video source information from the Overlay Decoder to decide where, or if, the incoming frame should be routed. To make the proper choice, it must look at the settings of the Single/Multiple Monitor switch, the Freeze Frame Monitor switch and Freeze Frame switches on the front panel. In the "Single Monitor" mode, all video is sent to Frame Memory #1 regardless of the source. For time-division multiplexing, this may not be a good idea; but it can be quite useful and a less expensive option if various cameras are to be selected at appropriate intervals. When the switch is set to "Multiple" (two or three monitors), the source ID-tag is used to route the frame to the corresponding frame memory. (If three cameras are to be used, three monitors are necessary; if two cameras are to be used, the third monitor would be idle.) An ID-tag of "00" indicates the source was the test pattern and the frame is routed to all frame memories that are not in the freeze-frame state. The Freeze Frame Monitor switch is also involved in the routing decision. Without an extra "freeze frame monitor," a freeze frame request causes the Frame Router to stop routing new data to the appropriate frame memory. This freezes the image on the monitor; anything of interest that may follow will not be seen until the freeze frame request is removed. With a freeze frame monitor, the frame memory continues to be updated when a Freeze Frame switch is thrown,

and the image immediately following the freeze frame request is sent to Frame Memory #4, which is used exclusively by the Freeze Frame Monitor. There are four Freeze Frame switches on the front panel; three of the numbered switches are used to freeze images coming from their respective video sources. The fourth switch, labeled "ALL," is specifically designed to freeze color video, but may be used with black-and-white. The action of the switches depends on the setting of the Freeze Frame Monitor switch. With a Freeze Frame Monitor present, only the action of throwing the switch is important. A freeze-frame occurs regardless of the direction the switch is thrown, and the last image sent to Frame Memory #4 is retained until a Freeze Frame switch is thrown again. Conversely, when the action is frozen on a source monitor, it is important that the monitor be able to again display incoming video. For this reason, a freeze-frame only occurs when the switch is in the up position and normal video resumes when the switch is down. Also, the Freeze Framer never freezes in the middle of an image; any action resulting from changing a switch setting only occurs after the current frame routing cycle is complete.

Another issue for the FF/OD to resolve is how to handle freeze-framing with respect to time division multiplexing. The data bus between the FIFO and the frame memories was not designed to allow data flow between frame memories. Therefore, when the Freeze Frame #1 switch (for example) is thrown, the last image from Frame Memory #1 is not sent to Frame Memory #4; instead, when the next frame from Camera #1 is received, the data is sent to both the freeze-frame and source frame memories. The time delay between these events may or may not be apparent to the user depending on the frame rate and the degree of multiplexing. When the ALL switch is thrown, the next full frame, regardless of its source, is sent to both its respective frame memory and Frame Memory #4. Of course, in the No Freeze Frame Monitor switch setting, none of this is a consideration - after a freeze-frame request, subsequent video information for the corresponding frame memory is blocked; and following an ALL freeze frame request, all incoming video is blocked. It should also be noted that when switched to Single Monitor, Freeze Frame switches #2 and #3 are inactive; and the Freeze Frame #1 switch behaves exactly like the ALL switch. When using an RGB camera, SAND DEVIL must be switched into the "Multiple Monitor" setting. If a Freeze Frame Monitor is desired, keep in mind that only the luminance from one color can be sent to that monitor, whether it is a color monitor or black-&-white; this may prove to be of some use, however, since the color can be chosen by use of the appropriate Freeze Frame switch.

After the Freeze Framer determines how an incoming frame is to be routed, it implements this decision by affecting output signals READ1 through READ4 (corresponding to each frame memory). VSG/MC uses these signals to generate the WRITE1 through WRITE4 enabling signals for the frame memories. The individual READ lines are also used by the frame memories directly to put the RAM chips into the appropriate read/write mode.

The Freeze Framer also has the Parity "bit" from the Overlay Decoder available for making routing decisions. Its purpose was to help prevent incorrect routing of an image. However, even though it is successful at detecting errors, a clear scheme for dealing with the errors was never apparent. The bit remains unused at this time, although it is routed to VSG/MC in the event a useful scheme is conceived.

### 7.4.3 Timer Controller

The timer controller portion of the FF/OD chip requires minimal logic to drive the timer/display-driver. The timer/display-driver is a special-purpose chip with a decade counter that can directly drive multiplexed 7-segment LED displays. The timer is clocked at 10 Hz (to provide tenth-of-a-second accuracy) by dividing the 30 Hz signal FIELD (which comes from VSG/MC) by three. The timer/display-driver can be reset and its timer/counter registers loaded with preset values. To detect a reset condition, the two timer bits from the Overlay Decoder are pipelined through two sets of 3-bit shift registers. A state machine then issues a reset when the proper sequence of timer-bit states is detected based on the two current timer bits and the six previous bits. The state machine is designed to allow an error in any one of the four states. This is so the circuit will not only reject false resets, it will also recognize true resets corrupted by noise. When a reset is issued, a 4-digit BCD value is loaded into internal registers in the timer/display-driver. This value depends on the switch settings for frame rate. All four possible values were predetermined to *roughly* compensate for the delay created by the four-frame reset sequence, and the average delay between the time the flight controller raises TRST and the start of the next frame. The timer/display-driver uses an internal oscillator to multiplex-drive the four LED digits at about 2.5 kHz. Through this multiplexing mechanism, only seven signals are needed to drive the segments for all four digits, minimizing the number of off-board signals to the display unit. Output signals D1 through D4 are common-anode drive lines that select each

digit; D1 also provides the FF/OD timer controller with the timing information for loading the timer preset value.

The timing display system is a simple, rather humble way of providing elapsed-time information. Since the purpose of SAND DEVIL is to watch video on a monitor, it would be better to have the timing information displayed on the monitor also. Complexity and time constraints did not allow this type of display system to be incorporated into the initial SAND DEVIL design. However, the basis for such a system was investigated, and SAND DEVIL was modified so that a video display timer could be incorporated in the future by modifying only the Frame Router board. This is evident by the WHITE and BRITE lines between the FF/OD and the frame memory boards. Either line could be driven by a modified Frame Router board with the timer/display-driver replaced by microprocessor-based or state-machine-based timer display circuitry to place numbers and/or text on the monitor. Besides just elapsed-time, the source camera number and other information could be added to the monitor display. The FF/OD chip would remain on the Frame Router board unchanged except the timer control section.

## **7.5 Frame Memory Boards**

SAND DEVIL uses from one to four frame memory boards to support from one to three "real-time" monitors and an optional "freeze-frame" monitor. Each Frame Memory board consists of enough RAM to store the digitized video of one video frame and a D/A converter to provide a continuous analog video signal. All Frame Memory boards are identical whether they supply a "real-time" monitor or a "freeze-frame" monitor.

The frame memory itself is composed of eight 16k x 4-bit static CMOS RAM chips organized as 64k words of 8-bit pixel values. The upper half of this memory is only used for images with full vertical resolution. The address lines are generated directly from the pixel and line counters on the Ground Controller board. Due to the sequence of these counters, some RAM locations are never accessed.

Each Frame Memory board contains a video D/A converter. The signals STROBE, BLANK, and SYNC are generated by the VSG/MC on the Ground Controller board and have been described earlier (see section 7.1.3, "Video Sync Generator / Memory Controller"). The signals WHITE and BRITE are for future use by the FF/OD board in generating an on-screen timer display. The signals BLANK, SYNC, WHITE, and BRITE override the

digital inputs when they are active and force the output of the DAC to NTSC standard levels. The digital inputs to the DAC are supplied by a bus common to both the memory outputs and the FIFO output.

The input signal READ (active high) is buffered with a spare decoder. When READ is low, the RAMs are write enabled and the FIFO input is used to drive the inputs to the D/A converter and the RAM. This allows the data from the FIFO to concurrently update the memory and construct the video output in real-time. A frame memory board operates in this mode when a new frame has been received for the monitor corresponding to that particular frame memory. When READ is high, the FIFO input is disabled and the RAM chips drive the inputs to the D/A converter. A frame memory board operates in this mode most of the time, refreshing the monitor at the NTSC standard frame rate with the picture last written to the frame memory. The VSG/MC (video sync generator/memory controller) and FF/OD (freeze-frame/overlay decoder) chips decide on a frame-by-frame basis which frame memory boards are to receive the incoming frame and which are to simply refresh their monitors.

The input signal WRITE should more appropriately be called ENABLE, for the RAM chips are enabled for either reading or writing when WRITE is low and disabled for both operations when WRITE is high. When WRITE is low, input signals A16 and A17, supplied by the VSG/MC chip, determine which two of the eight RAM chips are enabled. Two chips are enabled at a time since each chip is only four bits wide, enabling the storage of eight bit pixels.

## 8.0

## SYSTEM PERFORMANCE

The system performance is directly related to the algorithm used for data compression/expansion. Using a dual-adaptive 3-bit logarithmic differential PCM (DALDPCM) algorithm geared for space flights produces pictures with excellent response on high-contrast edges but noticeable amounts of overshoot in terrestrial pictures. A DALDPCM algorithm has been created which is suitable for terrestrial use and exhibits little overshoot. An averaging filter can be applied to any three bit per pixel algorithm and helps reduce overshoot and noise. The transmission of uncompressed video with six bits per pixel creates an image of equal or better quality than compressed video and produces no overshoot or error propagation at the expense of lower resolution for a given data rate. Other algorithms[2, 3] can be programmed into the pixel compressor.

The system has been tested to determine its immunity to loss of the bit clock. Each bit clock edge that is missed causes a shift of the affected line by one pixel. If the bit clock is lost for an extended period of time, significant data loss will occur. However, the bit clock may drop out for any period of time and the system will be able to regain synchronization within one frame of data (assuming noiseless data transmission).

Immunity to noise in the data stream has been tested in two ways. First, frame sync and line sync words were inserted into the data stream at random positions with an average of one sync word per line. The sync word filter worked very well, allowing the system to achieve sync and ignore the false sync words. Removal of the sync word filter resulted in the display being severely disrupted, demonstrating the effectiveness of the filter. Secondly, a percentage of data bits were inverted to simulate transmission errors. Tests in the range from a .1% to a 2% bit error rate resulted in significant "snow" in the uncompressed data modes and there were large disturbances to the picture in the compressed data modes. Additionally, frames were frequently routed to the wrong monitor in the multiple monitor mode. Once the bit error rate was set to .01% or less, the disturbance to the picture was minimal and frames were very frequently mis-routed. In none of the above cases did the system have trouble achieving sync.

The flight box (shown in Appendix C) is 37.6 cubic inches in size. The entire flight unit (Encoder and associated 28v to 5v and -5v DC converters) typically consumes 6.5 watts with a worst case consumption of 10.3 watts.

## 9.0

### SIZE REDUCTION PLAN

There are many situations where size is very important for telemetry instruments. In recognition of this fact, a study has been performed on methods to reduce the size of the SAND DEVIL flight unit. The goal is to take the flight unit and the three cameras it supports and reduce it to a single camera system with an encryption device all integrated in one unit. This reduced flight unit will be minimized with respect to size, cost, and power considerations. The size reduction methods fall into two basic groups: reducing the amount of total hardware and the size of the remaining hardware.

Considerable size reductions may be made through hardware elimination. The most obvious reduction is the elimination of all but one camera. This reduces the system size not only by elimination of the cameras themselves but also by reduction of the complexity of the circuitry which dealt with the multiple video inputs. Once it is decided that only one camera is necessary, it becomes obvious that a flight controller is not needed to select which cameras are active. (Doing away with the flight controller also removes the remote mission timer-reset capability, but this is insignificant.) Without a flight controller to select cameras, the built-in test pattern signal may no longer be selected so the test pattern generation circuitry may be removed. If SAND DEVIL is used in the master mode (it generates the sync signals for the camera), no phase-locked loop is necessary.

After the above reductions, the only parts left on the Test Pattern Board are the oscillator for the system clock and the VTPG (Video Test Pattern Generator), which still generates some signals important to digitizing the incoming video signal and storing it in a FIFO (first-in, first-out) memory. If the flight unit is restricted to one mode of operation (a single bit rate and frame rate combination), the jumpers that set the mode of operation may be removed and fewer I/O pins are required on the controller chips. This fact combined with the elimination of the test pattern allows the VTPG and VDF (Video Data Formatter) chips to be combined on one programmable or semi-custom part.

The next logical step in the hardware reduction process is to note that the camera inserts sync signals in its NTSC video signal, which the flight

unit is also producing. Integration of the camera into the flight unit itself can eliminate duplicated hardware. There are two specific functions that may be removed from the camera. The first function is the output signal conditioning (which adds sync information to the analog video signal) and the circuitry generating sync signals. The second function is a phase-locked loop on the camera for locking to an external sync source. If the camera is integrated into the flight unit, it may use the same system clock produced by the flight unit, and no phase locking is necessary.

The FIFO used to buffer the data prior to transmission is now a large portion of the remaining flight unit. The FIFO in the present system is also a large consumer of power due to the complex controller needed. One reason that the FIFO was necessary in the first place was that the signal received from the camera was an NTSC signal that had to be sampled in a set time while the actual transmission of the data took much longer. With the camera integrated into the flight unit, it can be driven at a slower rate. If the camera were able to produce pixels at a constant rate without interruption, no FIFO would be necessary. Unfortunately, a camera with an electronic shutter cannot produce pixels during the shutter period. Additionally, it is very expensive to have a custom camera made with the exact resolution needed (320 pixels by 245 lines) to make this steady data flow possible. Therefore, a FIFO cannot be eliminated entirely. However, once the camera is integrated into the rest of the system, the rate at which information is read from the camera can be controlled, using the image storing device in the camera itself as a short-term memory. Therefore, the FIFO need only buffer enough information to maintain the data flow during the shutter period. If the shutter period is selected to be 1/1000th of a second, the FIFO can be reduced to only one chip, as opposed to 14 chips in the current FIFO!

The second method for reducing the total size of the system is to reduce the size of the components themselves. One of the larger individual components is the EPROM that implements the data compression algorithm. If it is decided that each pixel is to be digitized to six bits rather than eight bits and that the feedback path in the compression algorithm is to be five bits, the 64k x 16 EPROM may be replaced by a 2k x 8 EPROM. This smaller EPROM not only takes up less board area and consumes less power, but it can operate much faster than the larger EPROM. This increase in speed allows data compression to be performed before the data is written into the FIFO rather than as it is

read out. This in turn means that the FIFO need only be three bits wide instead of eight.

The compression scheme with the smaller EPROM has been simulated with the current SAND DEVIL system by masking the lower two bits of the input to the compressor and the lower three bits of the feedback. The test was successful by showing that a gain in speed and a reduction in size can be achieved with minimal loss in picture quality.

Another reduction in the size of the components can be realized if a hybrid circuit is used. This allows the die portion of each chip to be mounted directly to a surface without the bulky packaging. Several such chips may be mounted on a single substrate along with external components such as resistors and capacitors. This high density hybrid circuit can then be mounted in the flight unit as a single large chip. For components not placed on the hybrid circuit, simply using surface mounted devices which typically have a much smaller footprint than hole mounted devices would greatly reduce board area.

Figure 18 shows the block diagram of the reduced flight unit. The customized camera assembly consists of a CCD (charge coupled device) imaging array, drivers for the CCD, and amplifiers/filters for the output analog video signal. This video signal is digitized to 6-bit pixels and compressed to 3-bit pixels. These 3-bit pixels are stored in a FIFO until they are read by the controller and serialized. The serialized data is then sent to the encryptor along with a bit clock. The data output can be sent to a telemetry unit which will actually transmit the data.

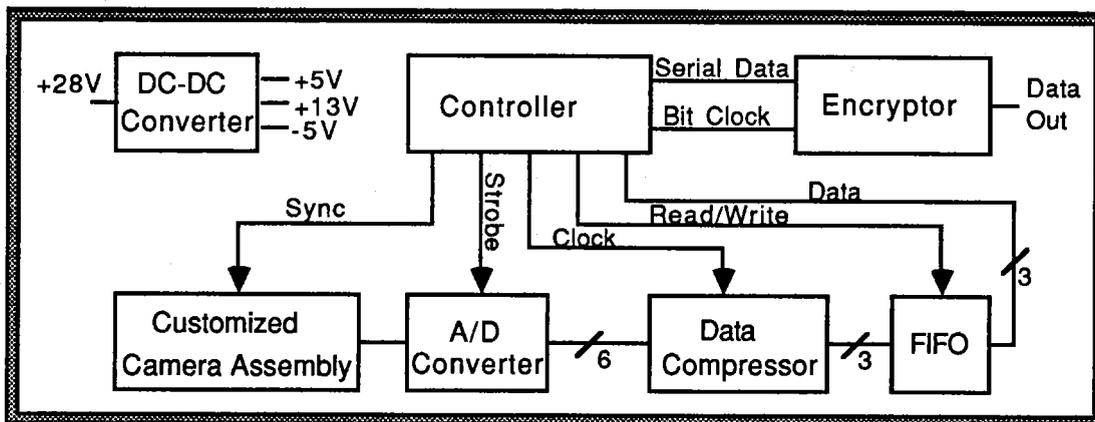


Figure 18: Size Reduced Flight Unit

Figure 19 shows the expected shape and size of the reduced flight unit. The CCD driver/signal conditioner, CCD imaging board, camera power supply, and lens mount sizes are based on information from Pulnix, a maker of electronic cameras. These pieces are collectively referenced as "the camera." The controller board would be a Sandia designed hybrid. One integrated circuit on this hybrid will perform the functions of the controller shown in Figure 18. This chip would likely be a standard cell logic chip if a large number of units are made. Smaller production quantities may warrant the use of programmable logic chips. An itemized power consumption estimate is given in Table 4.

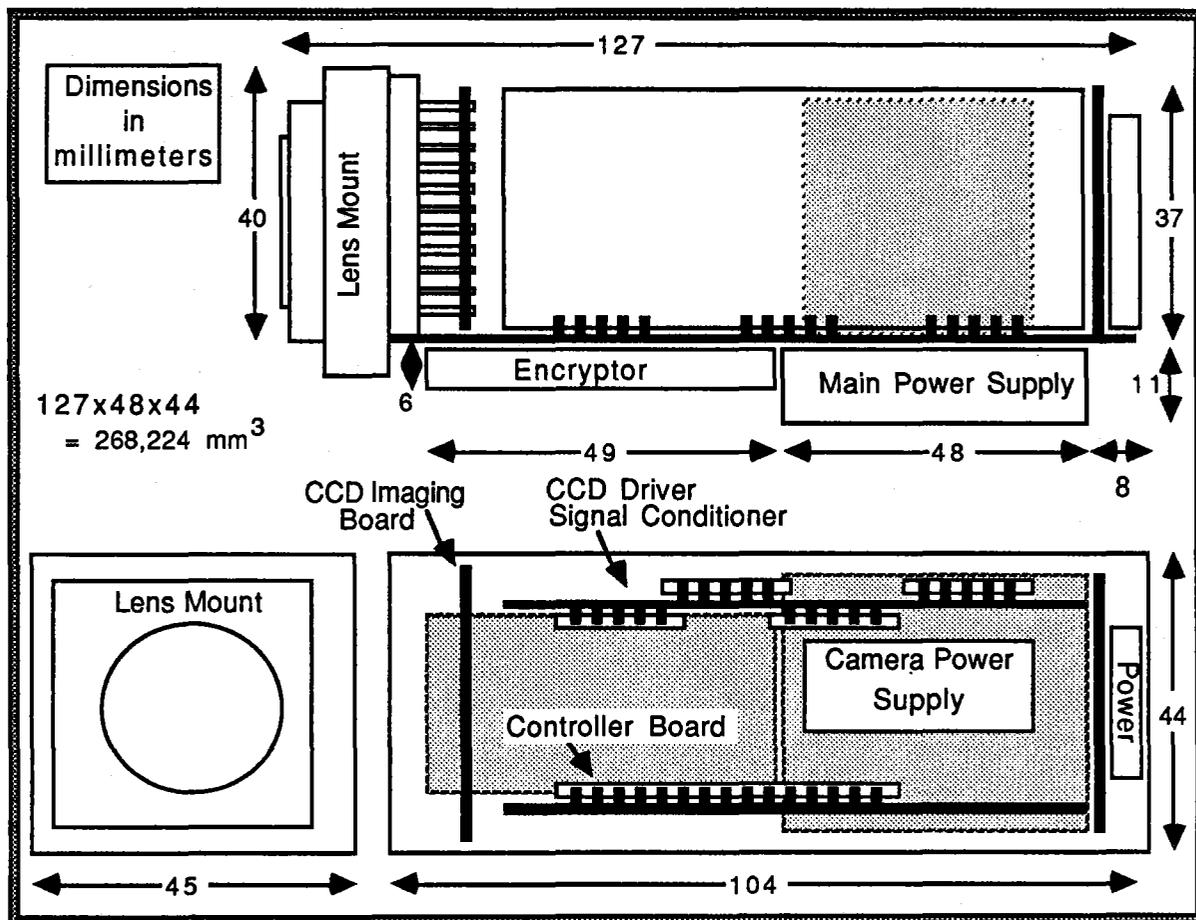


Figure 19: Reduced Flight Unit Mechanical Design

**Table 4: Reduced Flight Unit Power Consumption Estimates**

<u>Part</u>	<u>Power (mW)</u>
Encryptor	220
Compressor	600
FIFO	575
Controller	500
A/D conversion	225
Camera	2,640
Printed board	---
<u>Hybrid package</u>	<u>---</u>
subtotal	4,760
<u>Power converter</u>	<u>x1.33</u>
Total	6,347 mW

As a summary, the reduced flight unit differs from the normal flight unit in that it supports only one camera instead of three and there is no test pattern available. The reduced flight unit has a fixed transmission rate of 3.58 Million bits per second which results in a video frame rate of 15 frames per second. The camera and the encryptor are integrated into the reduced flight unit whereas they are external to the normal flight unit. Even so, the reduced flight unit (camera and encryptor included, lens excluded) is 16.4 cubic inches in volume, 21.2 cubic inches smaller than the normal flight unit (which excludes cameras and the encryptor), and consumes 6.35 watts, 3.65 watts less than the normal flight unit. It is estimated that such a device could be mass produced relatively inexpensively.

## REFERENCES

1. "Broadcasting and Recording", *Reference Data for Radio Engineers*, Sixth ed. (Howard W. Sams & Co., Inc., Indianapolis, 1981), pp 13-15.
2. R. H. Stafford, "Bandwidth Reduction," Digital Television: Bandwidth Reduction and Communications Aspects (John Wiley & Sons, Inc., New York, 1980).
3. T. J. Lynch, Data Compression: Techniques and Applications (Lifetime Learning Publications, Belmont, 1985).

## **Appendix A**

### **SAND DEVIL Schematics and Associated Notes**

The following notes give detailed descriptions of analog components as well as jumper settings and their effects. Some boards do not have any notes in this appendix because their operation is fully explained in the main text. When referencing jumper settings, the following terms will be used: Up, Down, Left, Right, Open, and Closed. These may be abbreviated by their first letter. The first four are used when there are three vertical posts and two are selected for connection by the jumper. The directions are valid when viewing a PWB with the card fingers down and the component side facing the viewer. The last two terms are used when there are only two vertical posts and a jumper is either present (Closed) or absent (Open). The jumpers are all named on the boards as they are in the following discussions for easy reference.

**Test Pattern Board Notes:** (This board is part of the encoder.)

**Digital-to-Analog Converter** - The pixel and line counters of VTPG are used to address an AM27C1024 64k by 16-bit EPROM which contains a test image. Each address contains two pixels which are latched by two 74AC574 octal D flip-flops with tri-state outputs. The 74AC574's outputs are alternately enabled and latched by a BT102 8-bit video D/A converter which then outputs the pixels. The BT102 also inserts sync and blanking into the video output using the sync and blanking signals from VTPG. T1, R3 and C3 form a 1.23V reference for the BT102 and R2 sets its video output to be 1 Vp-p max.

**Phase Locked Loop** - The encoder can operate in two modes: master or slave. See Table A1 for the jumper settings for each mode. In the master mode, the encoder system clock, a STUGCA 14.31818 MHz VCXO, free-runs and VTPG generates the sync signal to which all cameras are genlocked. The VCXO frequency can be trimmed by adjusting VR1. Camera 1 is not locked to the encoder in slave mode, but vice versa. The VTPG sync and sync from camera 1 are inverted and sent to PC2 (phase comparator 2) of a 74HC4046 phase locked loop. There are two phase comparators on the 74HC4046 chip, PC1 and PC2. PC2 is used for two reasons: 1) there is no phase difference between its inputs when the loop is in lock, and 2) it only uses leading edges for phase comparison so it does require that the input signals have a 50% duty cycle. This second feature is important because the sync signals that are compared do not have 50% duty cycles. The output of PC2 passes through a loop filter comprised of R12, R13, and C6 and enters the 74HC4046 VCO input where it is buffered and drives the VCO. The

**Table A1:** Master/Slave mode jumper settings

<u>Mode</u>	<u>VCXOIN</u>	<u>SYNCIN</u>	<u>CLKOUT</u>
Master, Standard	R	L	L
Slave, Standard	L	R	L
Master, Non-Standard	R	L	R
Slave, Non-Standard	L	R	R

VCO frequency is set by R14, R16, and C7. The buffered loop filter also drives the VCXO and R15 via the demodulator output. The loop is completed by setting the clock jumper to VCXO or VCO. The VCXO (Standard) setting should be used whenever possible since the VCXO provides the greatest encoder stability. For a master camera with a horizontal scan rate not within +/-50 ppm of the NTSC standard, the VCO

(Non-standard) setting must be used. However, the loop filter values for R12, R13, and C6 are for the VCXO and other values must be used with the VCO setting. The other cameras lock on to the encoder once the encoder is locked to the master camera.

**Opto-Isolators** - The HCPL-2631 opto-isolators are used on the camera select and timer reset lines to break possible ground loops and provide protection to the system from over-voltages on the inputs. The differential inputs provide drive flexibility. The input current limiting resistors, R8, R9, R10, and R11 can be changed depending on the input drive level: 270 ohm for 2.9-5.5 V inputs and 2.7k ohm for 18-42 V inputs. R4, R5, R6, and R7 are pull-up resistors for the opto-isolator outputs.

**Sync, Shutter, and Output Drivers** - All output drivers are short-circuit protected, have 50 ohm source impedance, and will drive 2.5 V into 50 ohms. The drivers are built using two paralleled inverters from a 74AC04. Each inverter circuit has approximately 10 ohms internal impedance and 91 ohms external impedance. Two inverter circuits in parallel have an effective impedance of 50 ohms and together provide the necessary drive capability to withstand a continuous short on the output.

**Shutter Control** - Most video cameras that are compact and light-weight use CCD (charge-coupled device) arrays to store charge accumulated from photo-diodes and transfer this charge to the output. From there this charge is used to generate the video signal. The effective shutter speed is the time that the photo-diodes are allowed to accumulate charge (from exposure to the incident light) before that charge is transferred to the CCD array. There does not need to be any physical device that blocks the incident light. Rather, the charge may be read from the photo-diodes twice in rapid succession, with the interval between the readings being the effective shutter speed.

The shutter control output signal currently generated by SAND DEVIL is a positive going pulse that starts at the beginning of the first line of a field (when the line counter is at zero and DIGLIN is active). The pulse ends when the line counter reaches the jumper selected count as shown in Table A2. The duration of this pulse is the desired time between charge dumps from the photo-diodes to the CCD array. The shutter speeds listed in the table are rounded. The actual time the shutter is "open" may be computed by multiplying the line count at which the shutter is closed by 63.56 uS, the time between successive lines.

**Table A2: Shutter Speed Jumper Settings**

SS2	Jumper		Shutter Speed (Pulse time in Sec)	Pulse Duration (In lines)
	SS1	SS0		
R	R	R	1/60th	245
R	R	L	1/125th	128
R	L	R	1/250th	64
R	L	L	1/500th	32
L	R	R	1/1000th	16
L	R	L	1/2000th	8
L	L	R	1/4000th	4
L	L	L	1/8000th	2

To our knowledge, there is not a camera currently available that can use a signal like the one just described. Rather, most cameras with controllable shutter speed have a few set speeds that are chosen by digital inputs. SAND DEVIL may be modified to output a constant voltage by cutting the trace from U1 pin G10 to U12 pins 1, 2, 3, 5, 9,11 and 13. The trace going to U12 may then be tied to ground or Vcc. Alternatively, the trace going to U12 may be tied to a wire connected to the D15 external connector on the air unit box. This configuration allows the flight controller to choose dynamically the level of the shutter control line, which is then inverted, buffered, and sent to the cameras.

**Data Formatter Board Notes:** (This board is part of the encoder.)

**Video Inputs** - The Formatter board has four 75 ohm video inputs for cameras 1, 2, and 3 and a test pattern. R25, R26, R27, and R28 are the termination resistors for the video inputs and can handle up to 3 Vrms. The inputs are protected from transients by the termination resistors (which absorb the transient energy) and R5, R6, R7, R8, and R9 (which limit current through the IC protection diodes). The video inputs must conform to the NTSC standard except that they must contain no color burst, chrominance or audio signals and preferably the video (luminance) signal should be band-limited to less than 3.58 MHz for best operation.

**Sync Separator** - The video from camera 1 (the master camera) is AC coupled through C4 to the input of the LM1881 sync separator. The reference voltage for the LM1881 is set by R9 and decoupled by C9. R9 is set to 560 k-ohm instead of the standard 680 k-ohm to shorten the

BURST output pulse as much as possible without causing improper operation of the LM1881 with standard video timing. The shorter BURST output pulse allows the DC-restoration (see next section) of a video signals with a shorter than standard back porch and a slight amount of skewing between the cameras.

**Multiplexer Amp** - The four video inputs are AC coupled through C5, C6, C7, and C8 and fed to the four inputs of the MAX454 video multiplexer / amplifier and also to the four switches in the 74HC4316 quad bilateral switch. The opposite side of each switch is connected to ground. When the BURST pulse occurs, the switches close and tie the inputs of the multiplexer to ground, forcing a set voltage across the AC coupling capacitors. This switching action DC restores the video signals by setting the back porch of each video signal to ground potential. If the video signals contain colorburst (which normally occurs during the back porch in NTSC color video) or the back porches are too narrow or not adequately synchronized, then the DC restoration will be imprecise. One of the four video inputs is selected by a two bit binary address (S1 and S0). The output of the multiplexer is buffered by a non-inverting video op-amp. The gain of the op-amp is set to 3.4 by R16 and R18. A gain of 3.4 amplifies the nominal 715 mV black to white part of the video signal to 2.43 V. This allows a +/-3 dB variation of the video signal without clipping the op-amp (+3 dB = 3.44 V, MAX 454 video mux/amplifier clips at 3.5 V) or increasing the A/D non-linearities (-3dB = 1.72 V, larger input voltage ranges result in lower non-linearities). R20 keeps the op-amp from ringing by isolating it from the switched 50pF capacitive load of the A/D input. C16 compensates for stray capacitance on the non-inverting op-amp input which would normally cause high frequency peaking. R29 helps provide an optimal load for the op-amp.

**Analog-to-Digital Converter** - The A/D is a CA3318 8-bit flash converter operating at 7.16 MSPS (or 3.58 MSPS in half-horizontal resolution modes). The reference voltage for the A/D is provided by a NE5230 low voltage op-amp set in the inverting mode by R15 and VR1. The input to the op-amp can come from one of two places. Table A3 shows the jumper settings for selecting the desired mode. In the fixed mode, the input to the amplifier comes from T1, R12 and C15 which form a -1.23V reference. VR1 is adjusted to set the amplifier gain to -1.98 which sets the A/D full scale voltage at 2.43V. Note this is the optimum voltage for a standard video input signal. However, if the input signal is larger or smaller than expected, VR1 would have to be adjusted or the digitized image will appear washed out (in the case of too large an input signal) or dark (in the case of too small an input signal).

**Table A3: A/D Reference Level Options**

<u>Mode</u>	<u>Vref</u>	<u>Comp</u>	Note: Vref and Comp are
Fixed Reference	L	O	unlabeled on the PWB.
Sync Based AGC	R	O	They are along the top
Compensated AGC	R	C	edge on the left and
Illegal	L	C	right, respectively.

The second reference mode available is the sync based AGC (Automatic Gain Control) mode. In this mode, the circuit is designed to dynamically adjust the voltage reference to the optimal level for the video input. This is useful in the case of several cameras with different amplitude video outputs. The input to the circuit is the video signal passed through a negative peak hold circuit formed by D2 and C15. The peak hold circuit charges to the sync tip amplitude. In the NTSC standard, this is 0.4 times the black to white amplitude. VR1 is adjusted to set the amplifier gain to -2.5 ( $1 / 0.4 = 2.5$ ). Ideally, this will create a voltage reference just equal to the black to white amplitude. However, there is an offset voltage introduced into the peak hold circuit by the non-ideal characteristics of D2. This offset voltage is nulled out by a diode reference formed with D1, R13 and C14. The diode reference is proportional to the offset introduced in the peak hold circuit and will track it with temperature. The compensation is accomplished by jumpering R14 to the summing node of the amplifier. The ratio of R14 to R15 is the same as the ratio of the offset voltage to reference voltage. The AGC mode is sync derived and is independent of the picture. It is the responsibility of the camera to provide the proper sync to picture ratio. A picture derived peak AGC could have been built using a diode-capacitor peak hold circuit on the overflow output of the A/D and buffering the output with an op-amp in order to drive the reference input of the A/D. It was determined that for this encoder, sync derived AGC was more desirable than picture derived AGC. In either fixed or AGC mode, VR1 can be adjusted in case the camera does not conform closely to the NTSC standard.

To insert the overlay tag on the first digitized line of each frame, the two most significant bits of the A/D, B7 and B8, are multiplexed with the overlay generator by tying B7 and B8 together with R1 and tying B8 and the overlay generator together. Normally the overlay generator is tri-stated and R1 is large enough that it does not interfere with proper operation of B7 and B8. On the first line, B7 and B8 are tri-stated and

the overlay generator is active. R1 is small enough that B7 tracks B8 which is driven directly by the overlay generator.

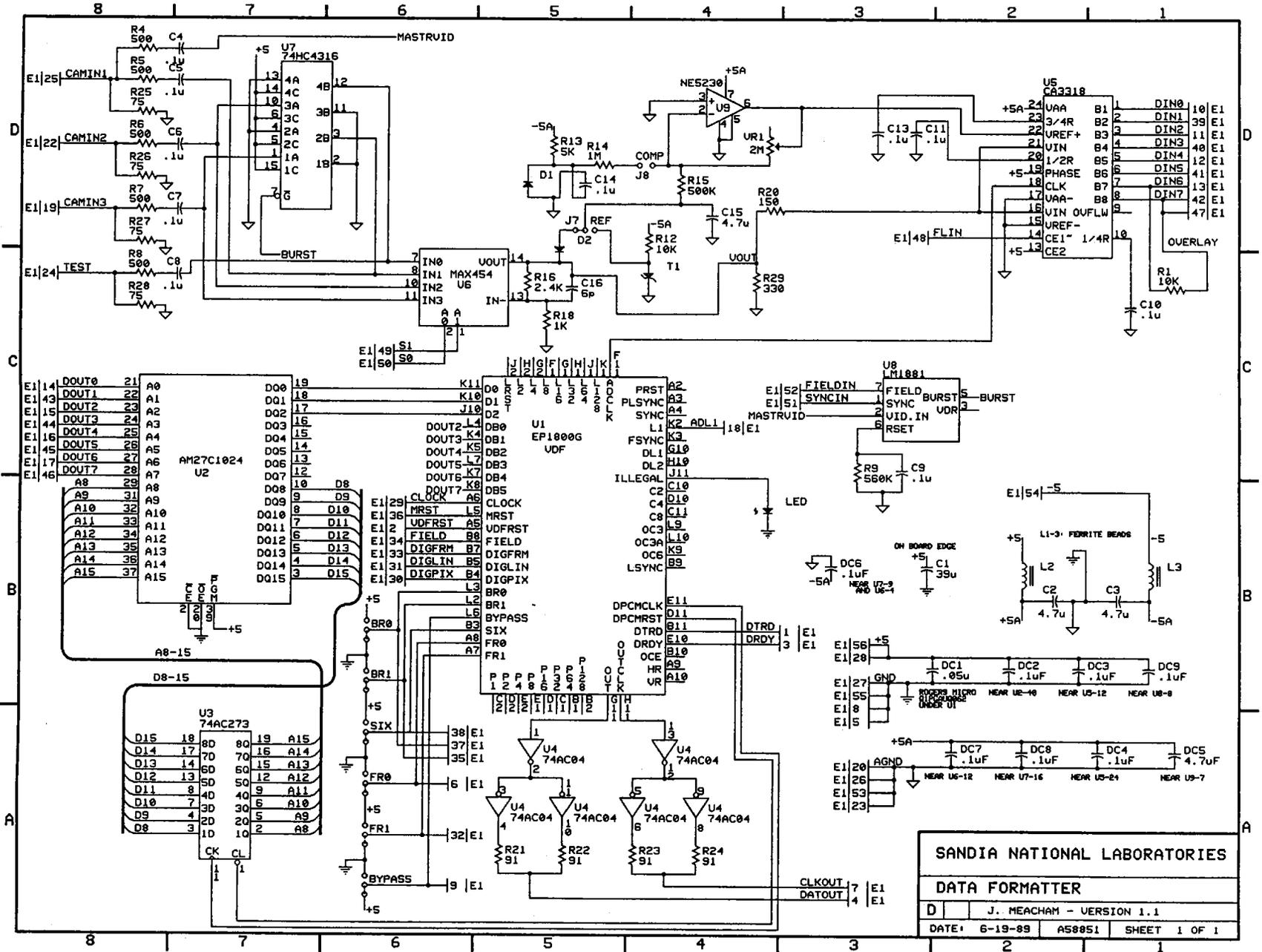
**Data Format Selection** - SAND DEVIL allows a wide range of bit rates and frame rates to be selected along with a data format of three or six bits per pixel. Each mode results in either half or full (H or F) vertical and horizontal resolution separately. The legal modes and their jumper settings are shown in Table A4. If the compression algorithm is to be used, the BYPASS jumper should be to the right. If it is to be bypassed, the jumper should be to the left.

**Table A4: Valid Operating Modes and Associated Jumper Settings**

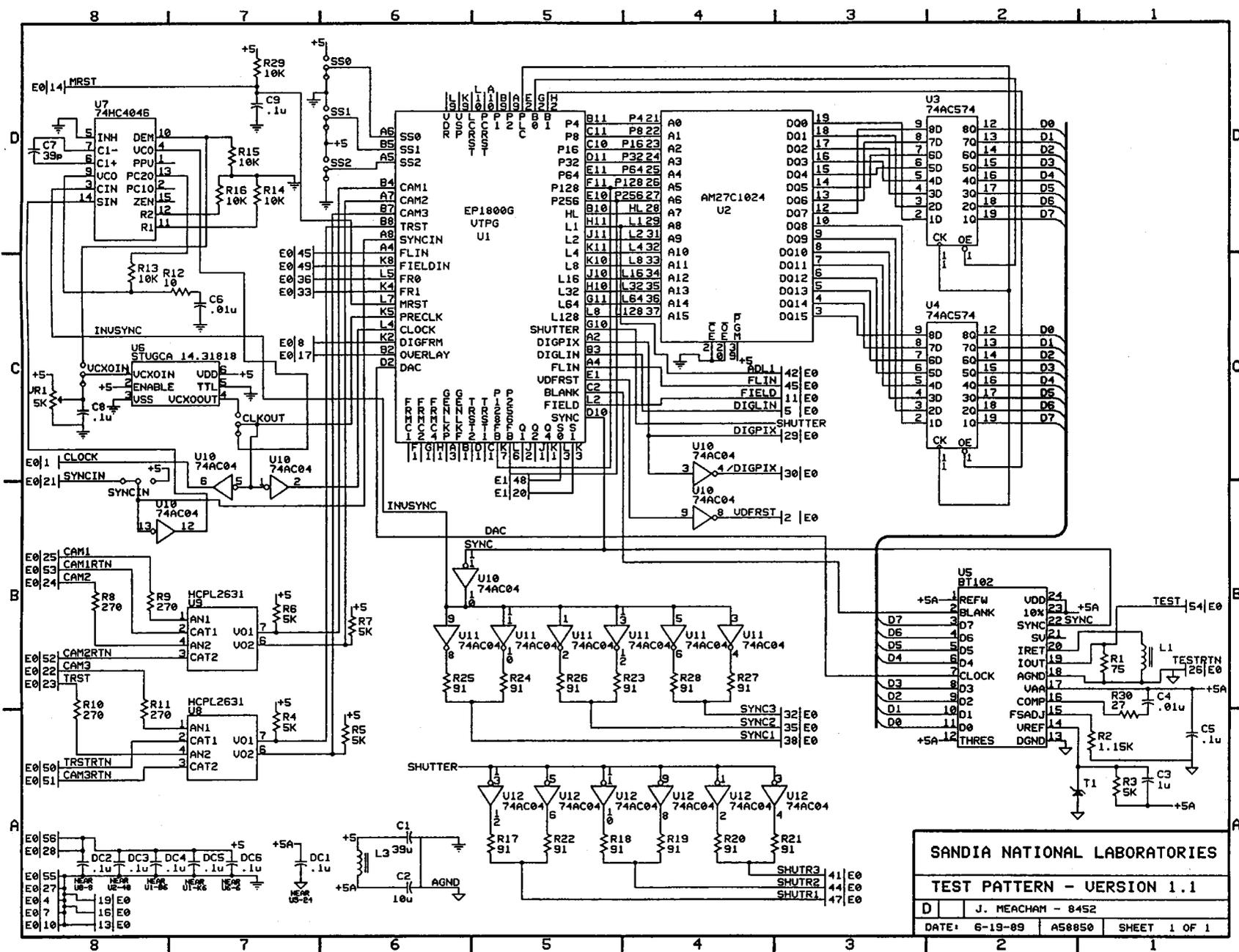
SIX	BR1	BR0	FR1	FR0	Bit Rate	Frame Rate	HR	VR
R	R	R	R	R	.895 Mbps	3.75 fps	F	H
* R	R	L	R	R	1.79	3.75	F	F
R	R	L	R	L	1.79	7.50	F	H
R	L	R	R	L	3.58	7.50	F	F
R	L	R	L	R	3.58	15.0	F	H
R	L	L	L	R	7.16	15.0	F	F
R	L	L	L	L	7.16	30.0	F	H
L	R	R	R	R	.895	3.75	H	H
L	R	L	R	R	1.79	3.75	F	H
L	R	L	R	L	1.79	7.50	H	H
* L	L	R	R	R	3.58	3.75	F	F
L	L	R	R	L	3.58	7.50	F	H
L	L	R	L	R	3.58	15.0	H	H
L	L	L	R	L	7.16	7.50	F	F
L	L	L	L	R	7.16	15.0	F	H
L	L	L	L	L	7.16	30.0	H	H

\* - Modes with partial picture loss

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SANDIA NATIONAL LABORATORIES			
DATA FORMATTER			
D	J. MEACHAM - VERSION 1.1		
DATE:	6-19-89	AS8851	SHEET 1 OF 1

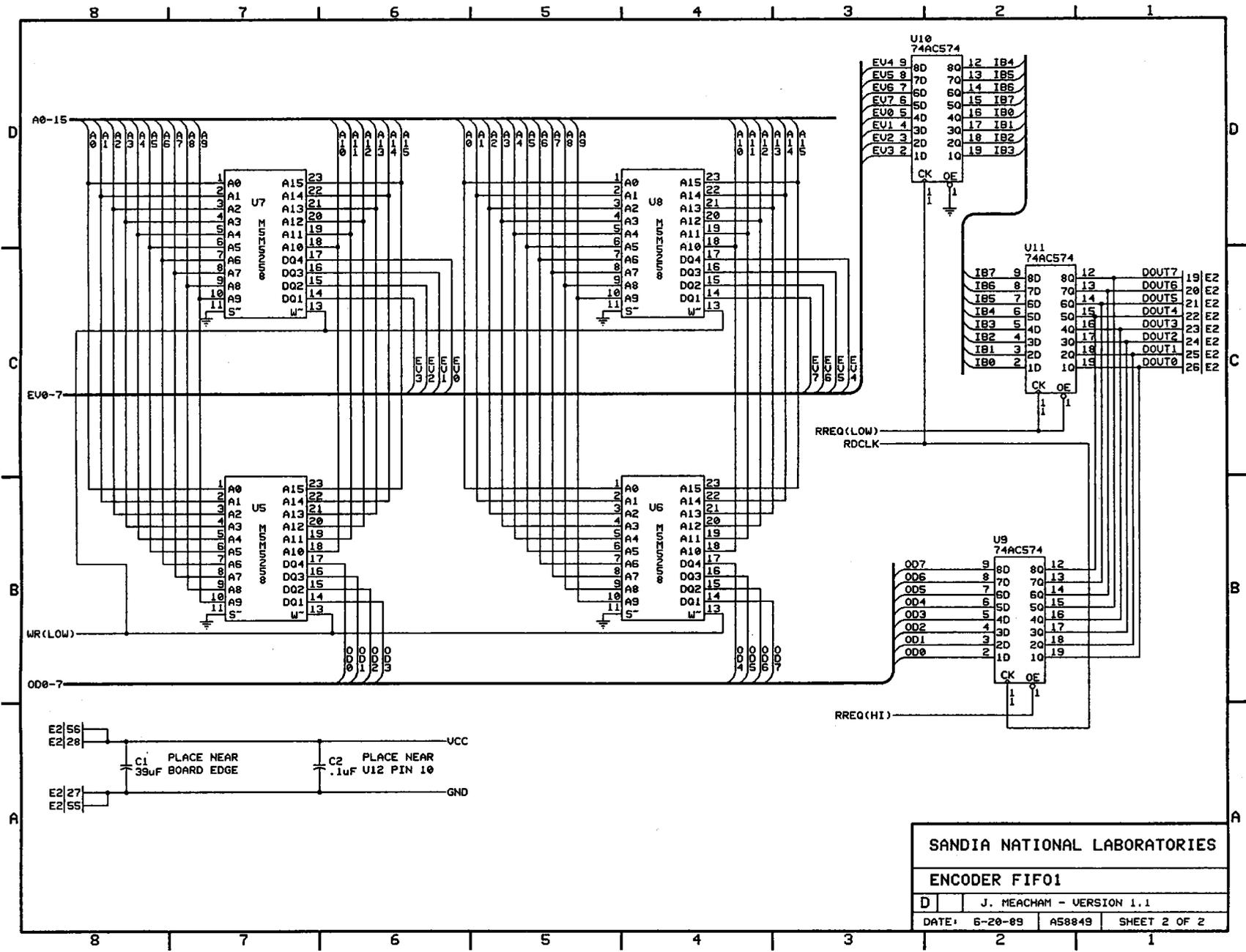


**SANDIA NATIONAL LABORATORIES**

**TEST PATTERN - VERSION 1.1**

D	J. MEACHAM - 8452
DATE: 6-19-89	AS8850 SHEET 1 OF 1





SANDIA NATIONAL LABORATORIES  
ENCODER FIFO1  
D J. MEACHAM - VERSION 1.1  
DATE: 6-20-89 A58849 SHEET 2 OF 2

**Ground Controller Notes:** (This board is part of the decoder.)

**Opto-Isolators** - The HCPL-2631 opto-isolators are used on the serial data and bit clock inputs to break possible ground loops between the decoder unit and the receiver as well as to protect the decoder from over-voltages on the inputs. The resistor pairs of R1 with R2 and R3 with R4 along with the photo-diodes provide an average input impedance of 50 ohms to an input signal that has an amplitude of 5V. Resistors R10 and R11 are pull-up resistors for the opto-isolator outputs.

**Phase Locked Loop** - The decoder is phase-locked to the incoming bit clock through the actions of the 74HC4046 phase locked loop. The incoming bit clock is compared with a bit clock (called the local bit clock) generated by the VSG/MC chip. The local bit clock is a derivative of the 74HC4046 VCO frequency which is the local system clock. The two bit clocks are compared using PC1 (one of the two phase comparators on the 74HC4046 chips). The output of this phase comparator is PC1O and is the exclusive-or the two input signals. This output signal is passed through a low-pass filter composed of R5, R6, and C2. The output of the filter is used as the controlling voltage for the VCO. When the system is in lock, the local bit clock and the incoming bit clock will be the same frequency but 90 degrees out of phase.

PC2 can only be used if the signals to be compared have a 50% duty cycle. In this case, both bit clocks do have a 50% duty cycle, so this condition is met. PC1 does not have the duty cycle restriction; it uses on the rising edge of the input signals. PC1 was not used because of the possibility that the edges produced by the opto-isolator may not be as well defined (due to the rise-time of the output) as the width of the pulse.

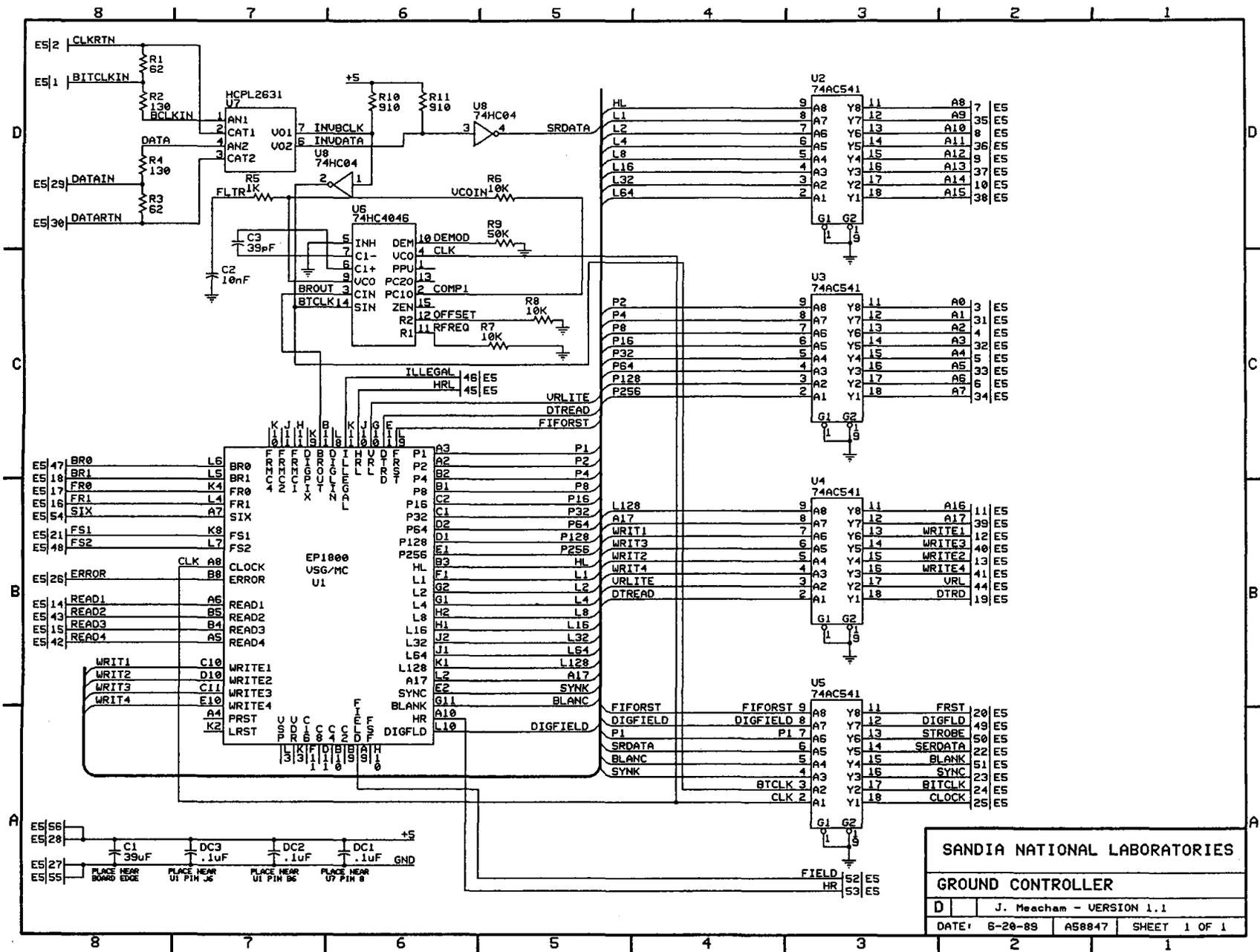
**Decommutator Notes:** (This board is part of the decoder.)

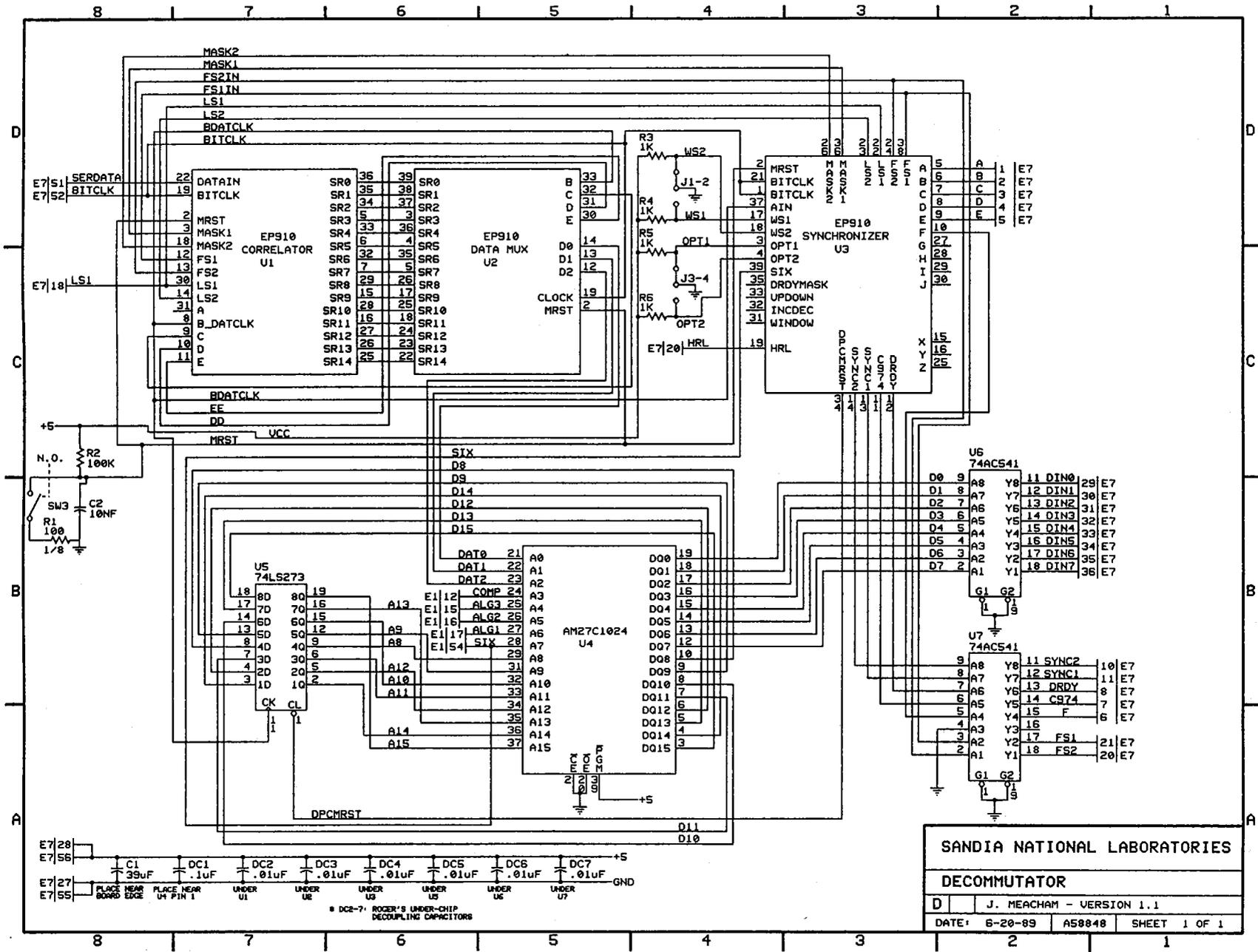
There are four jumpers on this board labeled J1, J2, J3, and J4. J1 and J2 cannot be both in place at the same time, nor can J3 and J4. Each jumper controls a single signal. The signal associated with the jumper is normally high due to a pull-up resistor but goes low with the jumper in place. Jumpers J1 and J2 control the window size option (see main text section 7.2.3.1, "Sync Word Filter"). Jumpers J2 and J3 control which sync lock ladder is used (see main text section 7.2.3.2, "Sync Lock Ladder"). The valid jumper settings and their effects are listed in Table A5.

All four jumpers are along the left edge of the decommutator board, with two set in slightly from the others. The two posts closest to the bottom of the board are J2. The center post is common to both J1 and J2 (physically ensuring that both are not present at once). The bottom two posts of the inset group are J3. The center post is common to both J3 and J4.

**Table A5: Deccommutator jumper settings**

<u>J1</u>	<u>J2</u>	<u>Window Size</u>	<u>J3</u>	<u>J4</u>	<u>Ladder Option</u>
O	O	8 bits	O	O	2
O	C	4 bits	O	C	3
C	O	6 bits	C	O	1
C	C	illegal	C	C	illegal





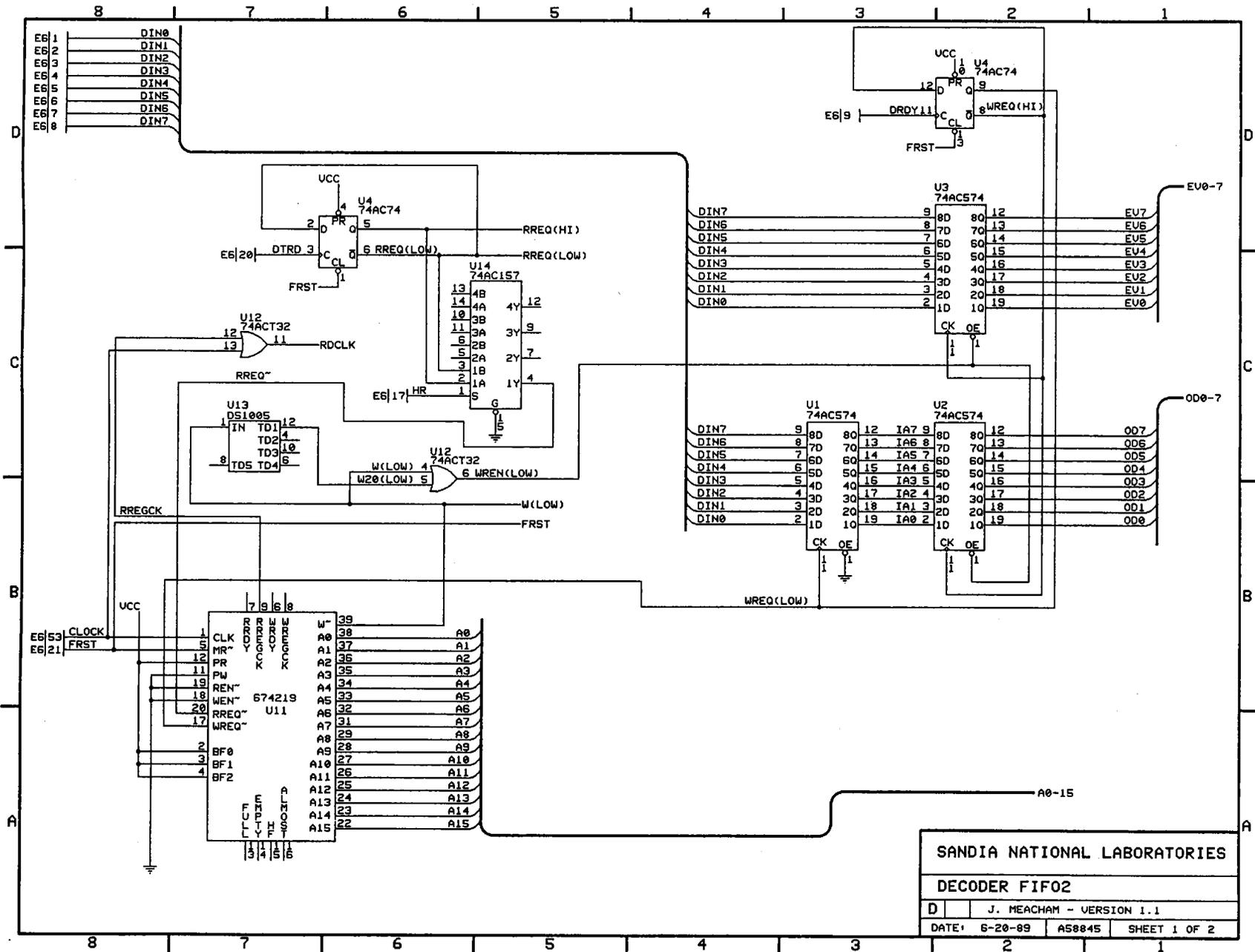
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D  
C  
B  
A

D  
C  
B  
A

E7|28  
E7|56  
E7|27  
E7|55

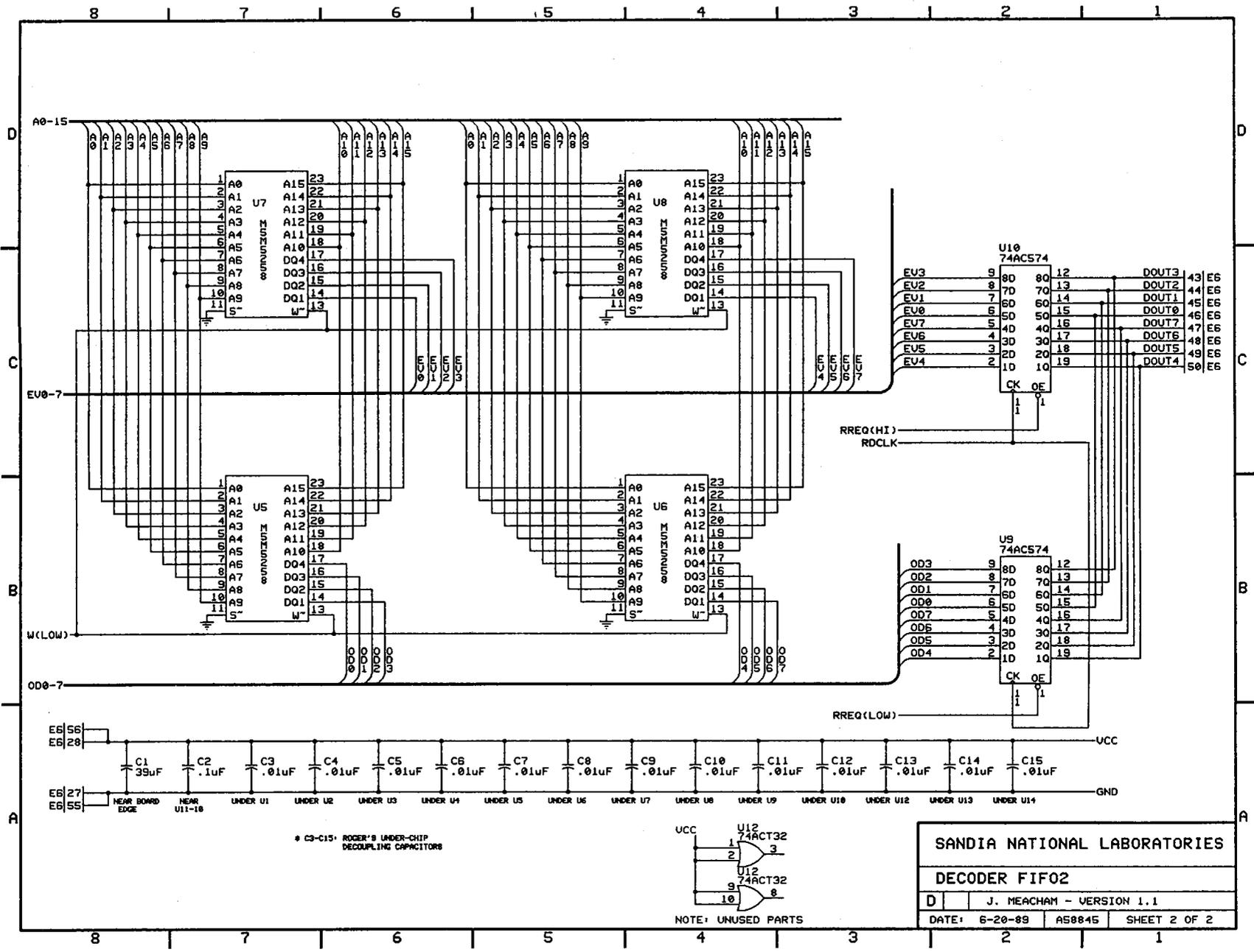
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

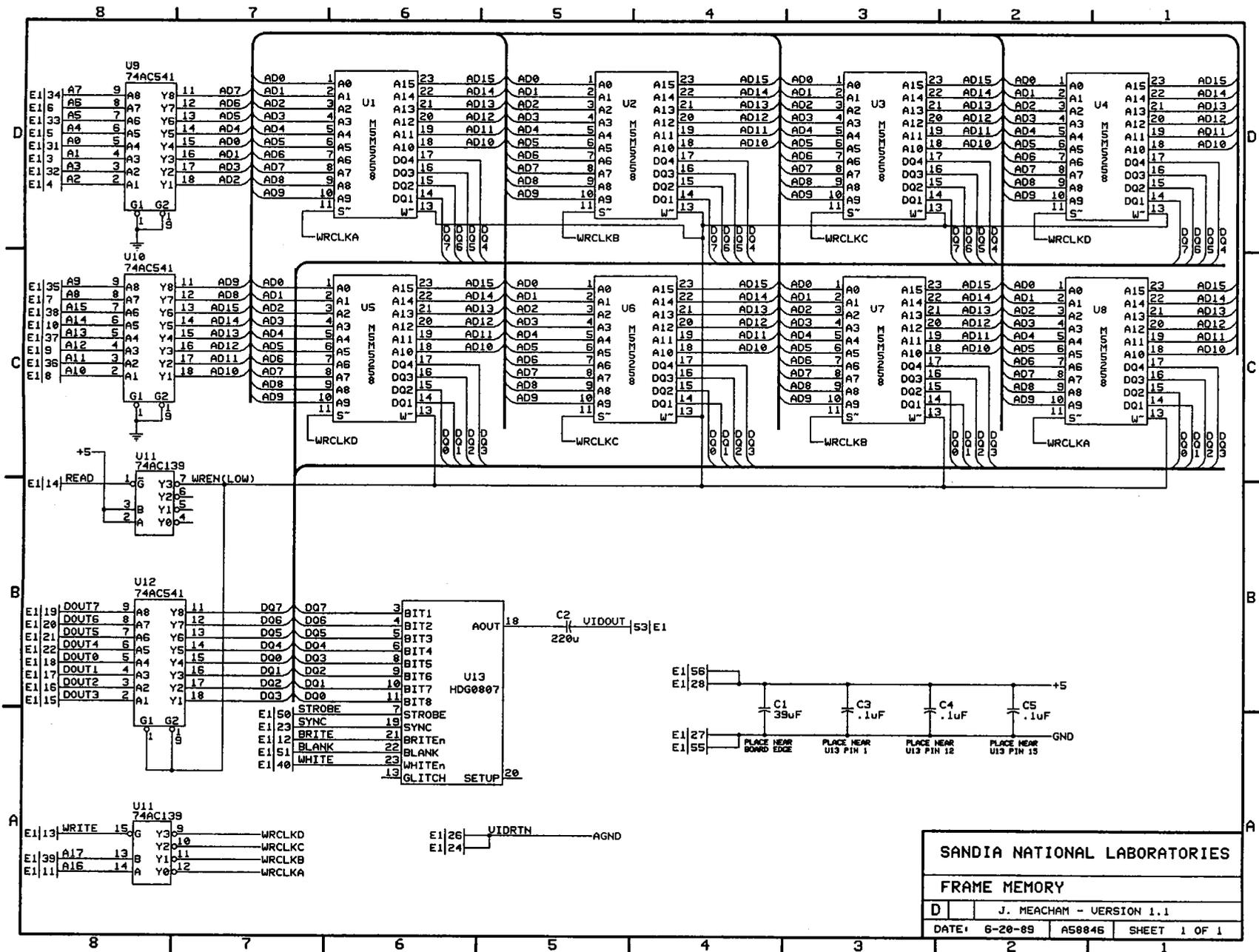


**SANDIA NATIONAL LABORATORIES**

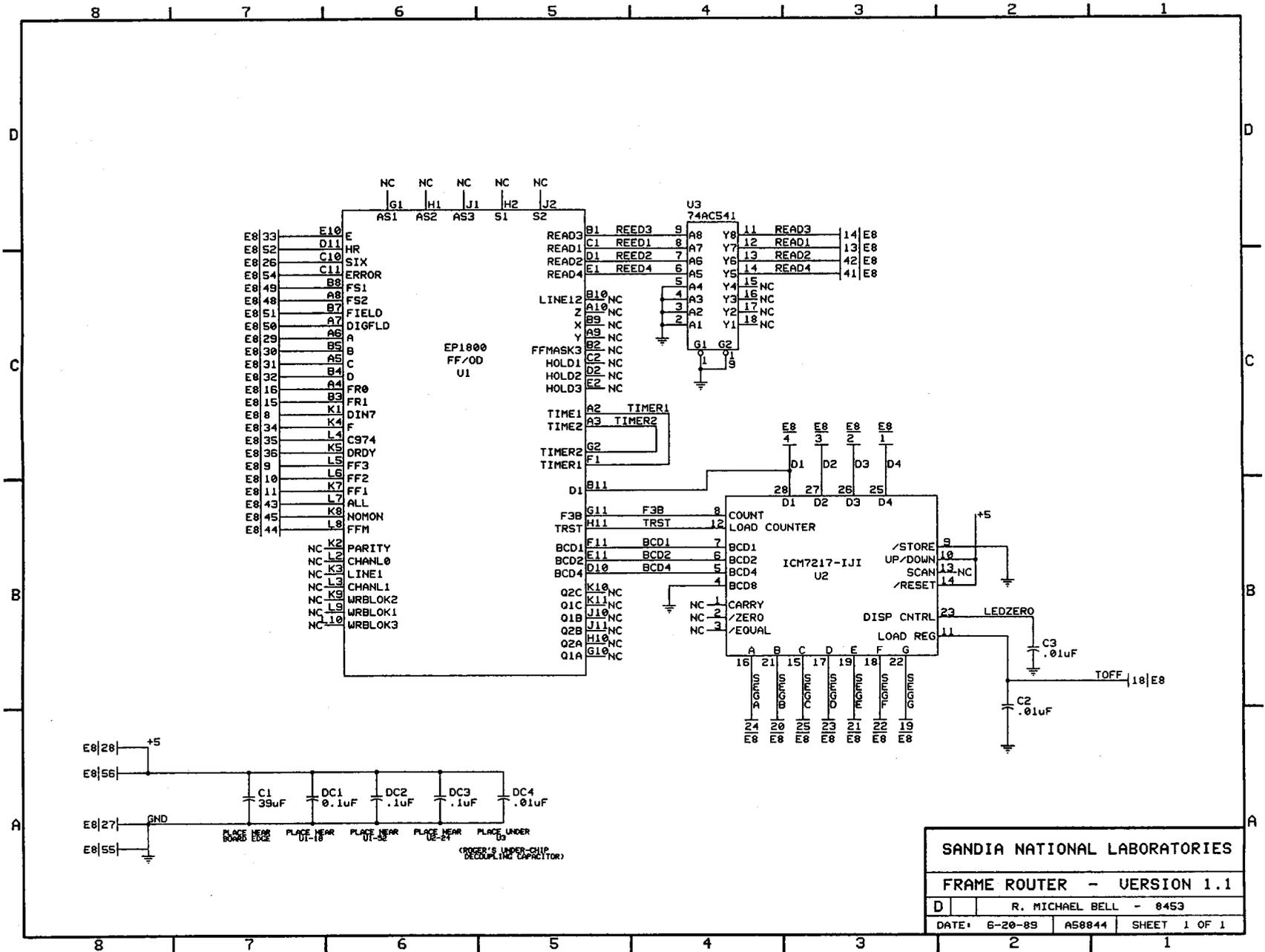
**DECODER FIFO2**

D	J. MEACHAM - VERSION 1.1		
DATE:	6-20-89	AS8845	SHEET 1 OF 2





SANDIA NATIONAL LABORATORIES			
FRAME MEMORY			
D	J. MEACHAM - VERSION 1.1		
DATE:	6-20-89	A58046	SHEET 1 OF 1



SANDIA NATIONAL LABORATORIES  
 FRAME ROUTER - VERSION 1.1  
 D R. MICHAEL BELL - 8453  
 DATE: 6-20-89 AS8844 SHEET 1 OF 1

## APPENDIX B

### Compression/Decompression Algorithms and Generation Programs

The compression/expansion scheme currently used on SAND DEVIL is a filtered, dual-adaptive, logarithmic, differential pulse code modulation (FDALDPCM) algorithm. This rather lengthy name describes the major features of the algorithm which compresses 8-bit pixels to 3-bit pixels. This appendix discusses exactly what these features are, how they were derived, and how they are implemented.

One way to compress eight bits of data into three is to simply truncate the lower five bits. This is exactly what is done in SAND DEVIL when it is operating in the Bypass mode (selected by one of five algorithm select lines; see main text section 2.0, "Data Reduction/Compression"). This scheme only produces eight grey levels. A better way is to use a differential scheme: given the last pixel value encoded and the next value to be encoded, simply transmit the algebraic difference between the two. With three bits, differences of -4 to +3 may be transmitted directly. This system is inadequate because it would take 85 passes through the algorithm to jump from 0 to 255! Instead of using the three bits as a direct value to add to the present value, the three bits may be used to encode specified steps. For example, the three bit value 010 may mean "add 25 to the last value," 111 might mean "subtract 100 from the last value," etc. An algorithm of this type would select a jump value from the set of available jump values to add to the old pixel value. The jump value selected would be the one that makes the sum closest to the pixel value being encoded. When selecting the set of available jumps, it makes sense to use a logarithmic scale so that both small and large jumps are available. Using a logarithmic scale therefore allows for subtle changes in picture shade as well as creating sharp edges where they occur. Such a scheme is well suited to the human eye.

The algorithm used in SAND DEVIL goes a few steps further: instead of using a pre-determined set of possible jump values, it adapts the sizes of the available jumps depending on the present pixel value. For example, if the present value is 20, there is no need for a jump value of, say, -50. Therefore all jumps are based on a logarithmic division of the interval between the present pixel value and the values 0 and 255. This correctly implies that there is a different scale for positive and negative jumps. A logarithmic jump scale is desirable since it contains small jumps for fine variations in a picture as well

as large jumps for hard edges. Assuming that there are four positive and four negative jump codes, the compression algorithm is as follows:

If new > old	This jump is positive:
logstep = LOG(255 - old) / 4;	Divide log of difference between maximum value and old value by number of positive jumps.
logdif = LOG(new - old);	Determine log of difference between new and old values.
If old > new	This jump is negative:
logstep = LOG(old) / 4;	Divide log of difference between old value and minimum value (0) by number of negative jumps.
logdif = LOG(old - new);	Determine log of difference between old and new values.
jump = logdif / logstep;	Determine the number of logarithmic steps to take.
old = EXP(jump * logstep) + old;	Determine new "old" value for feedback.

Here "jump" will be converted to an integer and be transmitted. The value "old" is the value the decoding algorithm will generate when it receives "jump." The value of "old" is feedback for the next iteration of the algorithm. Since the logarithm of 0 and division by the logarithm of 1 (division by 0) are both undefined, the actual algorithm has provisions for special cases. There is yet one more twist to the algorithm used in SAND DEVIL: the number of jumps in either direction (positive or negative) are not fixed. Consider the case where the old pixel value is 10. Having four available jumps in either direction results in much smaller jumps (much higher accuracy) between 10 and 0 than between 10 and 255, yet the odds are that the next pixel will be between 10 and 255. The algorithm handles this by allocating seven of the eight available jump codes between positive and negative jumps based on the old pixel value. The number of jumps allocated is then substituted in place of the "/ 4" terms in the above equations. The eighth jump code is reserved for jumps of zero. The jump of zero is used if the difference between two pixels is less than 2. This does two things: 1) avoids some of the special cases mentioned, and 2) keeps the algorithm from continuously "bouncing" (which results in alternately lighter and darker pixels) along a line of constant luminance. The number of jumps allocated in each direction are determined by the following equations:

```
positive = ((255 - old) / 256) * 2.0 + 3.0;  
negative = 7.0 - positive;
```

These equations result in 3 or 4 jumps in either direction since the fraction  $((255 - \text{old}) / 256)$  is never quite equal to 1.

Scaling the jumps between the current value and the maximum and minimum values is ideal for space images where the image is usually white or black since only one jump is required to reach these values from any other value. However, it results in severe "overshoot" for normal terrestrial pictures. This overshoot can be reduced by limiting the maximum step to half of the full scale. While an algorithm with this restriction will require two jumps to go from black to white, it results in greater resolution for fine variations in a picture and reduces the overshoot problem. The algorithm currently in use does not use this limitation on the maximum jump size.

The 64k x 16 chip implementing the encoding algorithm can only implement one algorithm since it has sixteen address lines and eight are needed for both the incoming pixel value and the feedback value. The program that produces the algorithm simply produces each possible address in order, determines the incoming and feedback pixel values that would produce the address, determines the jump code set for that particular feedback value, and then outputs the appropriate three-bit jump code and the value obtained by adding the encoded jump to the incoming pixel for feedback to the next cycle.

The expansion (or decoding) algorithm is just the inverse of the procedure described. If there are no errors in transmission of the jump codes, the encoder and decoder both have the same "old" pixel value. Therefore the decoder can determine the number of jumps in either direction and the size of each jump using the same equations given for the encoder. The decoder then simply adds the jump value to the old pixel value to arrive at the new pixel value. This new pixel value is then output and fed back as "old."

The 64k x 16 chip implementing the expansion algorithm can actually implement up to 32 different options because there are five unused address lines (16 lines total; eight used for feedback, three for incoming jump code.) External switches on SAND DEVIL are used to set the values of these lines which select specific address ranges for each option. Two lines are dedicated to SIX and BYPASS modes. There are therefore three "free" switches on the ground unit allowing up to eight additional separate algorithms to be programmed. Since only one algorithm may be present at any time in the air unit and it requires dis-assembling the air unit to change the algorithm, how might these switches be used? One way is to implement an "output filter" with

the degree of filtering selectable by the three switches. The "filter" is implemented by making the output byte a weighted average of the old value and the new value obtained by adding the jump to the old value. Changing the switches changes the weighting.

Note that while the pixel compressor in the air unit is not used in the BYPASS mode, the pixel expander is never "bypassed": it merely interprets the incoming data according to its programming. The program that produces the decoding algorithm again produces each possible address in order, then determines the jump code, feedback value, and switch settings that would produce the address. The inverse of the appropriate algorithm (as selected by the switches) is then applied to arrive at the output and feedback values.

The inverse of the Bypass algorithm depends on the number of bits per pixel. In the three bits per pixel mode, the incoming three bits are output as the highest three bits in a byte with the low order bits set to zero. The feedback is ignored in this case. In the six bits per pixel mode, the first three incoming bits (indicated by a zero feedback byte) are put out as the low order bits of the feedback byte, and the msb of the feedback is set. When the second three bits arrive (identified by the feedback msb being set), they are combined with the lower three bits of the feedback byte and output as the highest six bits in a byte with the lowest two bits set to zero. The feedback is set to zero and the cycle repeats.

## **Appendix C**

### **SAND DEVIL Operations Manual**

This manual will describe the steps necessary to set-up and operate SAND DEVIL. It is important that the SAND Report describing SAND DEVIL's capabilities is understood before deciding the mode in which SAND DEVIL will be used.

The set-up will occur in three steps: 1) Deciding mode of operation, 2) Configuring air-unit, and 3) configuring the ground unit and making proper external connections. How to operate the system will then be discussed.

#### **MODES OF OPERATION**

There are three basic configurations of the SAND DEVIL system: 1) stand alone mode, 2) remote test mode, and 3) full remote mode. The ground-based box of SAND DEVIL contains a complete encoder (air unit) as well as the decoder (ground unit). The ground unit requires a clock input and a data input. In the stand alone mode, these inputs are tied directly to the clock and data outputs of the air unit in the ground box. In the remote test mode, the air unit in the ground box is unused and the clock and data inputs to the ground unit are supplied by a separate air unit in a flight box. The flight box and ground box are also connected together through 15-pin connectors, allowing some switches on the ground unit to act as a flight controller. In the full remote mode, the clock and data inputs to the ground box are supplied by a receiver/clock regenerator. A separate air unit in its flight box connected to a transmitter and a flight controller completes the full remote system.

The advantage of the stand alone system is that all the different operating modes may be demonstrated with little effort since all the on-board jumpers in the air unit that determine the data format are available as switches on the front panel of the ground box. It is best to configure SAND DEVIL in this manner and test the desired operating mode before using the remote set-up. It is obvious that the full remote mode is the way in which SAND DEVIL will operate in any actual mission.

## SETUP PROCEDURES FOR THE AIR UNIT

**System clock configuration** - The SAND DEVIL air unit must be synchronized with the cameras to function properly. The air unit may be the "master" and determine the sync signals to which all cameras are locked; or camera 1 may be the master (making the air unit a "slave"), whereby the air unit and the other camera(s) lock to the sync signals of camera 1. Using the air unit as the master is the preferred mode of operation due to the fact that if the master camera fails, the rest of the system does not go out of synchronization. However, if the cameras are not quite standard and require an operating frequency out of the range of the air unit's VCXO, the air unit will have to be slaved to the master camera.

To configure the air unit in the master mode, set the jumpers as shown in Table A1. The Test Pattern board in the air unit has a variable resistor labelled VR1 on the schematic. This resistor must be adjusted while the system clock frequency is being monitored. The desired operating frequency for standard video cameras is 14.31818 MHz.

To configure the air unit in the slave mode, again set the jumpers as shown in Table A1. Adjustment of VR1 is not necessary in this case.

**Shutter Speed Control** - The air unit has three outputs dedicated for camera shutter speed control. If the cameras to be used have no such control input, this section may be ignored. The shutter speed control output signal is a positive going pulse with the pulse width determining the "open" time for the shutter. The width of this pulse may be set with three jumpers as shown in Table A2.

The camera in use may have a shutter control input that requires a DC voltage: high for one shutter speed or low for another. The detailed notes to the schematics in Appendix A describe how SAND DEVIL may be modified to produce such an output.

**Digitizing Reference Level** - The A/D converter on the Formatter board in the air unit requires a reference voltage to set the white level on the incoming analog video signal. This may be set according to a fixed reference or through a sync-based AGC (automatic gain control) circuit. One of these modes must be selected by setting the jumpers on the Data Formatter board according to the selections in Table A3. The fixed reference is preferable in most cases since it results in a more reliable reference level and is not subject to producing moire patterns in the

picture as the AGC reference sometimes does. The only reason the AGC reference should be considered is if multiple cameras are being used that have widely different output levels in the overall signal (including the sync pulses). If the AGC reference is chosen, there is the option of using temperature compensation. It is probably a good idea to use the compensation, but the system should be tested in this mode over a range of temperatures. The cameras used in this test should be the cameras to be used in the mission to determine if there are any problems.

**Data Format Selection** - The bit rate, frame rate, bits per pixel, and compression method all must be chosen in conjunction with each other to produce a legal operating mode with the desired resolution. One of the compression options is the bypass mode in which the data is uncompressed. This may be a bad choice since most communications systems require an AC signal and uncompressed data may produce a DC signal (if, for example, the picture is all black as might occur in space). If a compression algorithm is to be used, a PROM programmed with the appropriate algorithm (see Appendix B) must be installed on the Formatter board. In the compressed modes, three bits per pixel is the best choice as the six bits per pixel algorithms cause reduced resolution with very little improvement in picture quality.

Use of full vertical resolution appears to be only marginally better than half vertical resolution and should therefore be used only in cases where vertical resolution is of high importance.

With the above in mind, the favored modes are those using compression, full horizontal resolution, and half vertical resolution. The desired bit rate may then be selected, and the frame rate will be fixed. The valid modes and their jumper settings are shown in Table A4. Note that none of the data format jumpers should be installed in the air unit internal to the ground box since the switches on the front panel drive these signal lines.

## CONFIGURING THE GROUND UNIT AND MAKING CONNECTIONS

**Ground unit set-up** - The only adjustment required on the ground unit is the setting of the switches on the front panel to agree with the jumper settings in the air unit. The switches of concern are those which set the frame rate, bit rate, bits per pixel, and compression selection. Additionally, a PROM programmed with the appropriate de-compression algorithm(s) (see Appendix B) must be installed on the Decommulator board.

**Making the connections** - Figures D1 and D2 (next page) show the flight box and the available external connectors. The air unit flight box has external connections for the cameras and the data and bit clock outputs. The camera inputs should be used in the order they are numbered. That is, if only one camera is to be used, it should be connected to the camera 1 port; if two cameras are used, they should be connected to camera ports 1 and 2, etc. If the air unit is operated in the slave mode, the sync input for camera one should be left *disconnected*. The sync inputs to cameras 2 and 3 (if present) should be connected to the outputs on the air box at all times. The shutter control connections may be left unused.

The bit clock and data outputs should be connected to the encryption module if used, otherwise they should go straight into the transmitter. If the system is being operated in the stand alone mode, the clock and data outputs from the air unit should be connected directly to the clock and data inputs on the ground unit (with both units housed in the ground box).

There is a 15-pin MDM connector to the flight box. This is for the +28V power supply and the inputs from the flight controller. The pins are numbered as shown in Fig. D2b and are connected as in Table D1. The three inputs labeled cam1 - cam3 are the camera select lines. These lines should be asserted high when the appropriate camera is to be selected. Note that the flight controller can change which cameras are being used dynamically during a flight. The cameras do not require any less power if they are not selected, but higher frame rates may be obtained from the cameras still in use if other cameras are not selected. If all the camera select lines are low, the test pattern is transmitted. The last input on the 15-pin connector is the timer reset input. If the flight controller

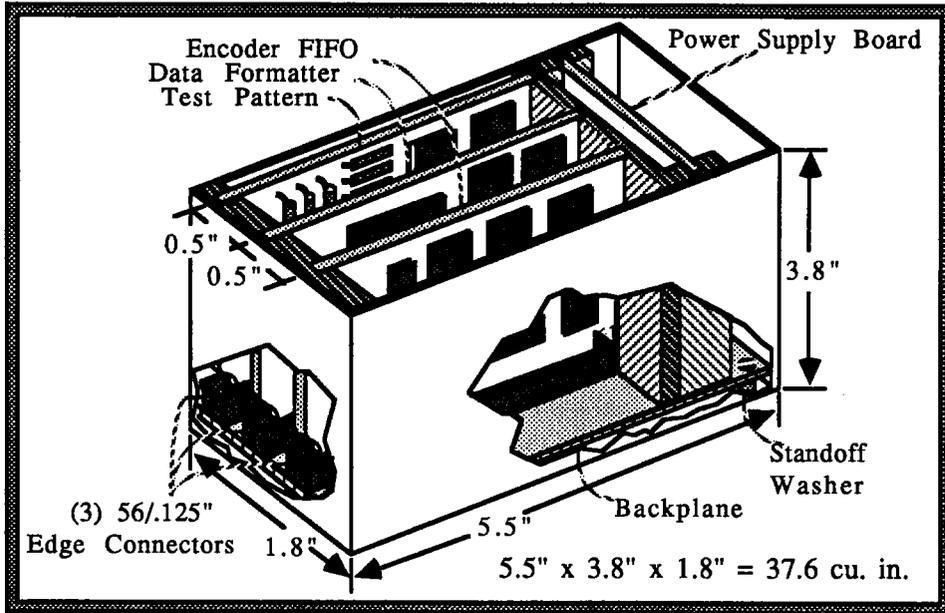


Figure D1: Flight box overview

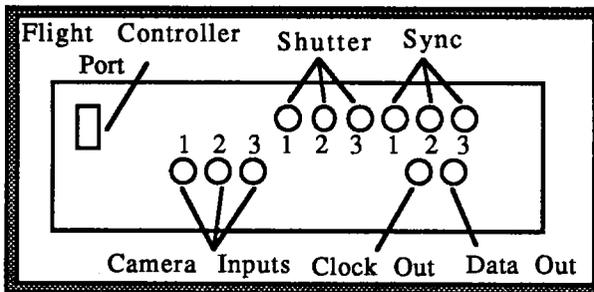


Figure D2a: Flight box; bottom view

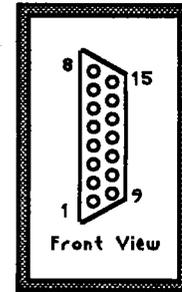


Figure D2b: Controller Port pin numbering

Table D1: Flight Controller Port Pin Connections

Pin	Signal	Pin	Signal
1	+28 V	9	ground
2	unused	10	unused
3	unused	11	unused
4	unused	12	return; cam 3
5	select; cam 3	13	return; cam 2
6	select; cam 2	14	return; cam 1
7	select; cam 1	15	return; timer reset
8	timer reset		

asserts this line, the air unit transmits a reset sequence to the ground unit which in turn resets the mission timer. This reset line must be asserted for a minimum time equal to the transmission of one frame in the chosen mode of operation. This is to guarantee that the air unit sees the reset request. At the lowest frame rate, half vertical and full horizontal resolution (the format requiring the longest time to transmit a frame), the minimum time the reset line must be asserted is 267 mS (79,625 pixels per frame \* 3 bits per pixel / .89 Mbits per second).

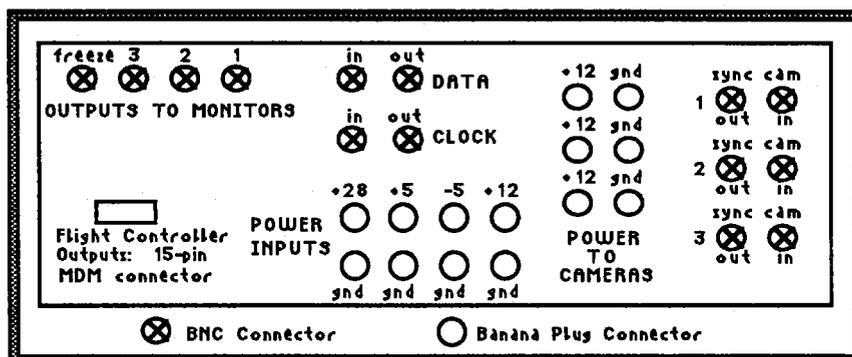


Figure D3: Ground box back panel

Figure D3 shows the connectors on the back panel of the ground box. Four pairs of connectors are for power inputs. The +5 input should be connected to a power supply operating between 4.8 V and 5.2 V and capable of delivering 3.0 amps. The -5 input should be connected to a power supply operating between -4.9 V and -5.1 V and capable of delivering .021 amps. The +12 V input is unused when the system is operated in the remote mode. When in the stand alone mode, the +12 V input is used only to supply the cameras with power. The exact input voltage and current requirements are set by the number and type of cameras used. The +28 V input is for supplying the air unit when operated in the remote mode. It is unused in the stand alone mode.

There is a 15-pin MDM connector on the back of the ground unit. The pin-out for this connector is listed in Table D1. These outputs may be connected to the 15-pin connector on the air unit when the system is operated in the remote mode and there is not a separate flight controller available. When this is done, the camera select and timer reset switches on the front panel of the ground box act as the flight controller and operate the camera select and timer reset inputs to the air unit. The +28 V supply to the air unit is also supplied through this connector and is switched by the power switch on the ground box.

Two of the inputs on the ground box are for the bit clock and serial data. These inputs may come from the air unit contained in the ground box (stand alone mode), from a separate air unit with the clock and data outputs tied directly to the inputs on the ground box (remote test mode), or from an RF receiver/clock regenerator unit (full remote mode).

There are four video outputs for use by up to four monitors. The first three are for monitors dedicated to each of the cameras. The system may be used with only one monitor, but it must be connected to the monitor #1 output. The fourth video output is for an optional dedicated freeze-frame monitor. This optional monitor may be used with any number of monitors dedicated to individual cameras (or even a single monitor displaying video from all cameras). There are switches on the front panel that must be set to indicate the number and type of monitors connected to the system (discussed later).

The rest of the connections on the back of the ground box are the same as the connections on the back of the flight box and are used by the air unit internal to the ground box. These are used only when the system is being tested in the stand alone mode.

**Diagnostic connector** - There is an un-populated edge connector in the ground unit. This connector is for diagnostic purposes. The signals that drive the LEDs on the face-plate of the ground unit, the switch inputs, and several internal signals are available through this connector. Table D2 lists the pins and associated signal names. These signal names are as they appear in the schematics in Appendix A. Simple diagnostics may be performed on the system by probing these signals.

**Table D2: Diagnostic port connections**

Pin	Signal	Pin	Signal	Pin	Signal
1	E	20	DTRD	39	FF1
2	ILLEGAL	21	FS1	40	READ1
3	HRL	22	DIGFLD	41	ALG2
4	VRL	23	SERDATA	42	ALG1
5	F	24	BITCLK	43	FR1
6	N/C	25	CLOCK	44	FR0
7	N/C	26	ERROR	45	BR1
8	DRDY	27	GND	46	BR0
9	SYNC2	28	VCC	47	SEGG
10	SYNC1	29	D4	48	SEGB
11	COMP	30	D3	49	SEGE
12	ALG3	31	D2	50	SEGF
13	ALL	32	D1	51	SEGD
14	FFM	33	A17	52	SEGA
15	NOMON	34	WRITE1	53	SEGC
16	LS1	35	C974	54	SIX
17	DOUT7	36	DIN7	55	N/C
18	SYNC	37	FF3	56	VCC
19	N/C	38	FF2		

## OPERATION OF SAND DEVIL

The switches on the front of the ground box can be lumped in three groups: 1) Configuration switches, 2) Operations switches, and 3) Flight Control switches. The configuration switches are in bank 2 as shown in Figure D4. These switches are to be set to match the jumper settings in the air unit when the system is in the remote mode. When the system is in the stand-alone mode, these switches simultaneously control both the air and the ground units. The operations switches are in bank 3 as shown in Fig. D4. (Switch 14 may also be considered a member of this group.) These switches affect only the operation of the ground unit. While they may be changed at any time, the switches determining the number of monitors will probably remain unchanged. The freeze-frame switches and the algorithm switches are the only switches likely to be used during an actual mission. The flight control switches are in bank 1 as shown in Fig. D4. These switches are tied directly to the air unit in the ground box and to the 15-pin connector on the back of the ground box.

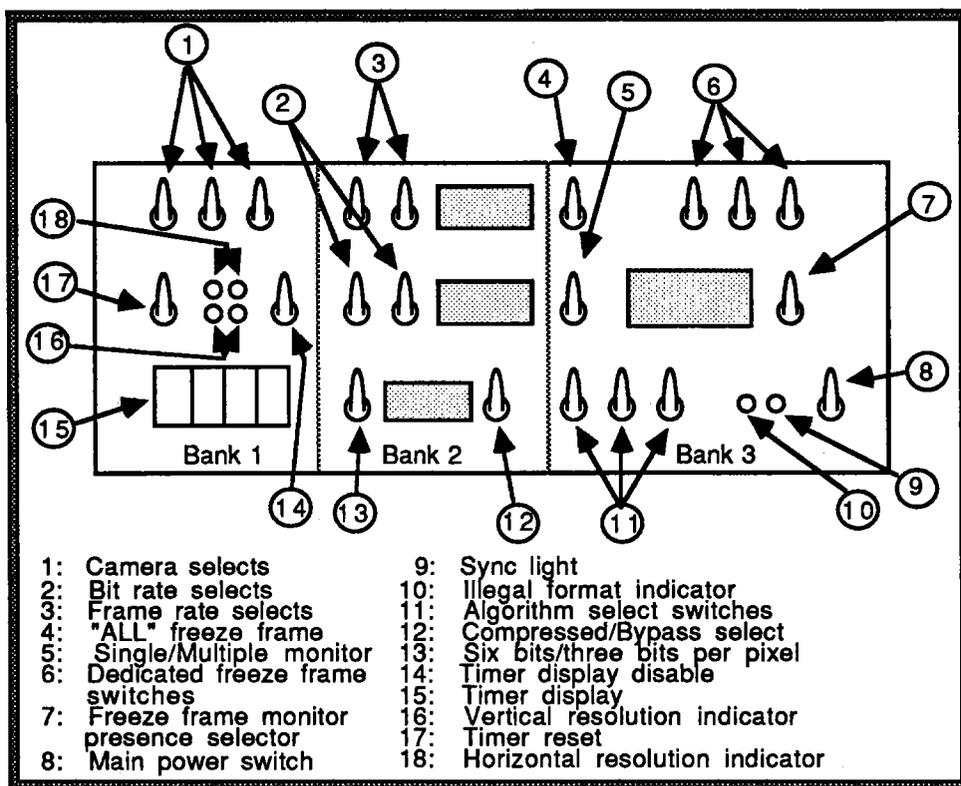


Figure D4: Ground box front panel

If the system is being operated in the remote test mode, this connector is used to connect the ground unit to the remote air unit. The switches are always connected to the air unit in the ground box for use in the stand alone mode. In either case, these switches emulate the actions of a flight controller by allowing dynamic selection of which cameras are active and initiation of a timer reset sequence.

The operator should first indicate whether there is a single monitor or multiple monitors connected to the ground unit using the switches in bank 3. If there are only two monitors and one is used solely as the dedicated freeze-frame monitor, the switch should be in the single-monitor setting. A second switch should be set to indicate the presence or absence of the dedicated freeze-frame monitor.

The main power switch controls all power to the air and ground units in the ground box. If a remote air unit is connected to the ground box via the 15-pin connector, the +28 V to the air unit is also controlled by the main power switch. If the air unit is in the full remote mode, it will require its own +28 V supply. The air unit and ground unit may be powered up in any order. Once both units are powered up, there may be

a time period from five to thirty seconds while the air unit first synchronizes with the camera(s), then the ground unit synchronizes itself with the air unit. The pictures on the monitors will tend to jump and/or roll during this time.

There are several indicator lights on the front panel of the ground box. The sync light ("9" in Fig. D4) indicates when the ground unit has synchronized to the incoming data. This light is red when the system is in the search state (out of sync), green when it is in the sync-lock state (the desired state), and yellow when the system is somewhere between these two states (see the discussion of the sync-lock ladder in the main body of this report). The illegal light ("10" in Fig. D4) glows red when an illegal configuration is chosen with the switches in bank 2. The vertical resolution indicators ("16" in Fig. D4) indicate full resolution when they are both lit and half resolution when they are both off. The horizontal resolution indicators ("18" in Fig. D4) indicate full resolution when they are both lit and half resolution when only one is lit.

Once the system has been correctly configured and powered up, the only operations that can be performed are the freeze-framing of pictures and the selection of different decoding algorithms. The selection of different algorithms is valid only if the EPROM in the ground unit is programmed to implement different algorithms which are compatible with the compression algorithm installed in the air unit. This may be the case if the different algorithms in the ground unit implement various degrees of high frequency filtering. In this case, a noisy picture may be smoothed somewhat by selection of another algorithm.

The freezing of video frames is performed in different ways depending on the number of monitors. If only a single monitor is present, throwing either the freeze-frame switch #1 or the "all" switch to the up position results in the last received video frame being held on the monitor. The picture is freed when both switches are in the down position. If there is a single real-time monitor and a freeze-frame monitor, throwing a numbered switch causes the next video frame received from the corresponding camera to be sent to and held by the freeze-frame monitor. If the "all" switch is thrown, the next video frame received is held by the freeze-frame monitor, regardless of its source. In either case, the real-time monitor continues to display all the incoming frames. If frames are being received from more than one camera, the pictures will be time-division multiplexed on the single monitor. In the case of multiple real-time monitors and no freeze-frame monitor, each monitor has its own switch. When that switch is thrown to the up position, the

last video frame received is held on the respective monitor until the switch is returned to the down position. If the "all" switch is used, all monitors hold the last received frame. Finally, in the case with multiple monitors and a freeze-frame monitor, the operation of the individual freeze-frame switches is the same as for the operation of switch #1 in the case where there is a single real-time monitor and a freeze-frame monitor. Using the "all" switch in this mode gives unpredictable results in that the next frame received is sent to the freeze-frame monitor regardless of its source. Therefore, it cannot be predicted from which camera the frozen frame originated.

The above operations are the only operations that may be performed when the system is in the full remote mode. If the system is in the remote test mode (the air unit is connected to the ground box via the 15-pin connector) or the stand alone mode, the camera select and timer reset switches may also be used. When a camera select switch is in the down position, the corresponding camera is essentially ignored and no video frames from it are digitized and transmitted. When a camera select switch is in the up position, data is acquired from the corresponding camera. When there is more than one camera, frames are taken from them each on rotating basis and time-division multiplexed for transmission. If no cameras are selected, a test pattern is transmitted. The timer reset switch is operated by moving from the down position to the up position, holding it momentarily, then returning it to the down position. This produces the necessary pulse on the timer reset line to initiate a timer reset sequence. Once the ground unit has received the timer reset sequence and decoded it, the timer on the front panel of the ground box will be reset. The timer display disable switch ("14" in Fig. D4) can be used to turn off the LED displays to conserve power.

The above operations are the only operations that may be performed with the system configured in the remote test mode. All of the above operations and more may be performed with the system in the stand alone mode. When the system is in the stand alone mode, the switches in bank 2 affect both the ground unit and the air unit internal to the ground box. Thus, different bit rate, frame rate, bits per pixel, and compressed/uncompressed formats may be selected. Note that only a few of all the possible combinations result in legal formats. The illegal light on the front panel of the ground box indicates whether the selected mode is legal or not.

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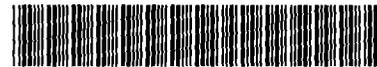
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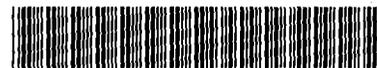
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