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SANDAC V Hardware Reference Manual

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L. J. Dalton, Editor

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SANDAC V Hardware Reference Manual

L. J. Dalton, Editor
Guidance and Control Division II

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Albuquerque, NM 87185

Abstract

This manual describes the hardware of the SANDAC V embedded computer designed and built at Sandia National Labs.

Acknowledgment

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1. PRODUCT DESCRIPTION

1.1 GENERAL

The Sandia Airborne Computer (SANDAC) V is a third-generation embedded computer developed for applications in hard real-time environments (those in which systems must continuously observe critical timing constraints). Specifically, SANDAC V has been tailored by Sandia National Laboratories for executing strap-down navigation and control algorithms. With a Sandia-designed Roll-Stabilized Inertial Measuring System (RIMS), SANDAC V performs inertial navigation and attitude reference control on reentry vehicles. SANDAC V has also been used in land-vehicle experiments for navigation and digital map display and is being evaluated for autonomous vehicles, robotic controls, and vision applications.

To provide the flexibility for a wide range of applications, SANDAC V has a modular architecture that is expandable in the number of processors and I/O ports and the amount of memory. A SANDAC V can be configured with as many as 15 Processor Modules so that an application can be divided into logically independent activities.

SANDAC V application code and data are stored in battery-backed RAM. (Powerup code is stored in ROM.) Because RAM is used for code storage, an application program must be downloaded into SANDAC V from a nearby portable computer, known as the Gateway, before a mission. The download path is a serial channel between the Gateway and SANDAC V.

1.2 ARCHITECTURAL OVERVIEW

SANDAC V's modular architecture lets the user configure a system with the appropriate type and number of hardware modules for a specific application. The following types of modules are available:

- Processor
- Utility
- Global Memory
- Expansion Memory
- System I/O
- MIL-STD-1553B

Within a system, Processor Modules, the Utility Module (required in every system), and Global Memory Modules reside on the global bus. Expansion Memory Modules, System I/O Modules, and MIL-STD-1553B Modules reside on the local bus associated with a Processor Module. These modules physically connect to a Processor Module's local bus, expanding it. The modules are referred to generally as expansion modules, and the

extended local bus is designated the local expansion bus. A third bus, the global serial bus, connects all Processor Modules to an external port located on the Utility Module. (The Gateway communicates with SANDAC V via this port.)

Because of signal propagation delays, a SANDAC V is limited to a maximum of 20 interconnected modules. This total includes all global bus modules (Utility, Processor, and Global Memory) and all modules connected to Processor Module local buses (Expansion Memory, System I/O, or MIL-STD-1553B).

In configuring a system, the following considerations apply:

- One Utility Module is required for every system.
- A system supports a maximum of 15 Processor Modules.
- A Processor Module can have a maximum of four expansion modules attached to its local bus. The modules can include the following types in the quantity indicated:
    - 1 System I/O Module
    - As many as 4 Expansion Memory Modules
    - As many as 4 MIL-STD-1553B Modules

The modular SANDAC V architecture is illustrated in Figure 1-1, which shows a typical system configuration. The bus system and the hardware modules are described in the following paragraphs.

1.2.1 Bus System

SANDAC V contains the following buses:

- Global bus
- Local buses associated with each Processor Module
- Global serial bus

The global bus is a parallel bus with 32 address lines and 32 data lines that interconnects all Processor Modules, the Utility Module, and any Global Memory Modules. Processor Modules access the resources on the Utility and Global Memory Modules over the global bus. To avoid contention problems when more than one Processor Module at a time tries to use this bus, an arbitration system gives bus control to the module with the higher priority. Module priority is set with hardware jumpers (see Subsection 4.4.1).

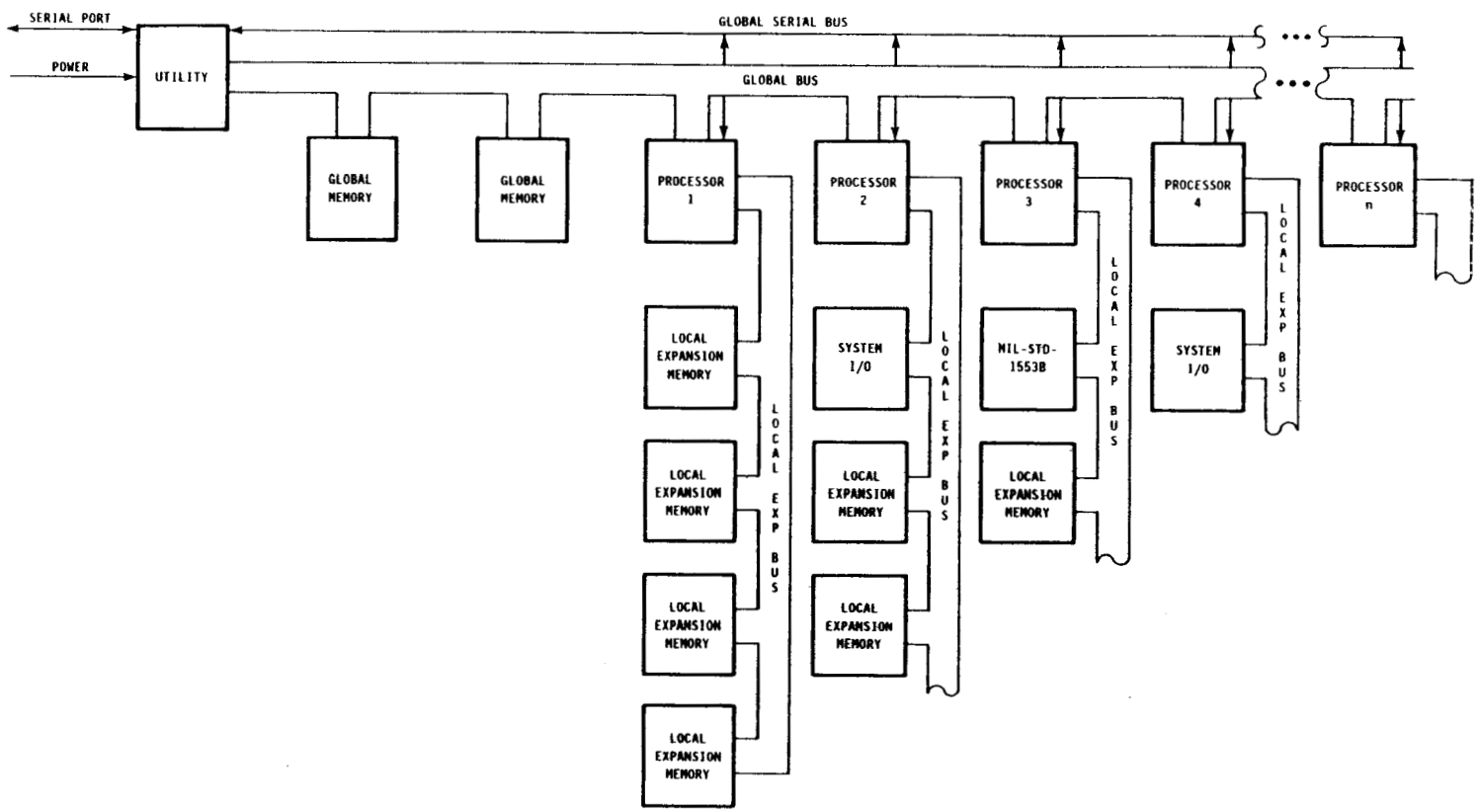


Figure 1-1. SANDAC V Architecture

The local bus on each Processor Module is a parallel bus with 32 address lines and 32 data lines that provides the module's Motorola MC68020 microprocessing unit (MPU) with access to memory and I/O resources. Additional memory and I/O can be added to the local bus by attaching Expansion Memory, System I/O, or MIL-STD-1553B Modules to the Processor Module.

The global serial bus connects all Processor Modules to an external port on the Utility Module. This port is used for loading application code into the SANDAC V and is also a window into the system for debug operations. The Gateway terminal interfaces with the SANDAC V via this port. Software running on the Gateway communicates with individual Processor Modules over the global serial bus and loads application code or performs debug operations.

1.2.2 Processor Module

The Processor Module uses the Motorola MC68020 MPU and the Motorola MC68881 Floating-Point Coprocessor. Processing is supported with a variety of local resources supplied by the following:

- 128K Bytes of RAM
- 1 VLSI Gate Array
- 1 512-Byte First-In-First-Out (FIFO) Buffer
- 1 Motorola MC68901 Multi-Function Peripheral

The Processor Module resides on the SANDAC V global bus. Access to global resources is through the global bus interface, which includes bus arbitration logic. The module's local memory and I/O resources can be expanded by attaching as many as four additional SANDAC V expansion modules. Section 4 describes the Processor Module.

1.2.3 Utility Module

SANDAC V requires one Utility Module (Section 5). This module provides the system with the following:

- Power
- Clocks
- Global Serial Bus Interface
- Global Resources
  - 256K Bytes of EPROM
  - 128K Bytes of RAM
  - 32-bit Timer
  - Status Register

1.2.4 Global Memory Module

The Global Memory Module provides 512K bytes of battery-backed RAM on the global bus. SANDAC V has address space for 30 Global Memory Modules, but the number installed is subject to the limitations discussed in Subsection 1.2. The module includes an access monitor that, if enabled, can detect an overwrite in a user-selected area of the RAM. Section 6 describes the Global Memory Module.

1.2.5 Expansion Memory Module

The Expansion Memory Module provides 2M bytes of battery-backed RAM on a Processor Module's local bus. A Processor Module has address space for six of these modules, but because of electrical drive limitations, only four can be supported. The address monitor included on the host Processor Module provides monitoring for any attached modules. Section 7 describes the Expansion Memory Module.

1.2.6 System I/O Module

The System I/O Module attaches to a Processor Module's local bus and provides the following resources:

- 1 parallel port
- 5 async/sync serial channels
- 4 16-bit counter/timers
- 4 8-bit counter/timers
- 2 baud-rate generators
- 8 input discretes
- 8 output discretes
- 8 input/output/interrupt discretes
- 4 DMA channels
- 4 digital phase-locked loops (DPLLs)
- 4 general-purpose isolated input buffers
- 14 general-purpose nonisolated input/output buffers

With the exception of the parallel port, these resources are provided by the following devices:

- 2 Signetics SCN68562 Dual Universal Serial Communications Controllers
- 1 Motorola MC68901 Multi-Function Peripheral
- 1 Hitachi HD63450 Direct Memory Access Controller

Section 8 describes the System I/O Module.

1.2.7 MIL-STD-1553B Module

The MIL-STD-1553B Module attaches to a Processor Module's local bus and provides a dual-redundant interface for the MIL-STD-1553 command/response data bus. To support this interface, the module uses the following devices:

- BUS-66300 II MIL-STD-1553-to-Microprocessor Interface Unit
- 4K × 16-bit RAM
- BUS-65600 MIL-STD-1553 Bus Controller, Remote Terminal, Bus Monitor
- BUS-63125 Dual Transceiver

Section 9 describes the MIL-STD-1553B Module.

1.3 MECHANICAL DESIGN

Each SANDAC V module is a printed circuit board framed with aluminum rails. This frame is keyed so that only one orientation is possible when interconnecting modules.

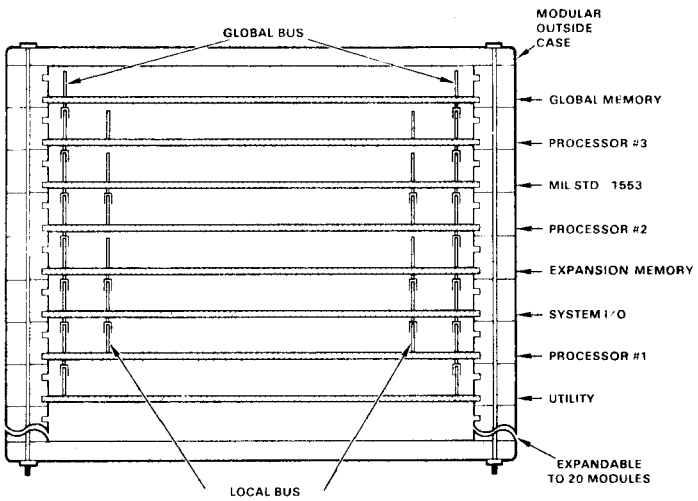
NOTE

> The aluminum rails are stamped with information that identifies the type of module and provides other configuration data. This information is detailed in Appendix A.

In a system, groups of modules are interconnected by rows of pins and sockets on the circuit boards. Rows of pins and sockets on two outer edges of the modules provide the global bus between all system modules.

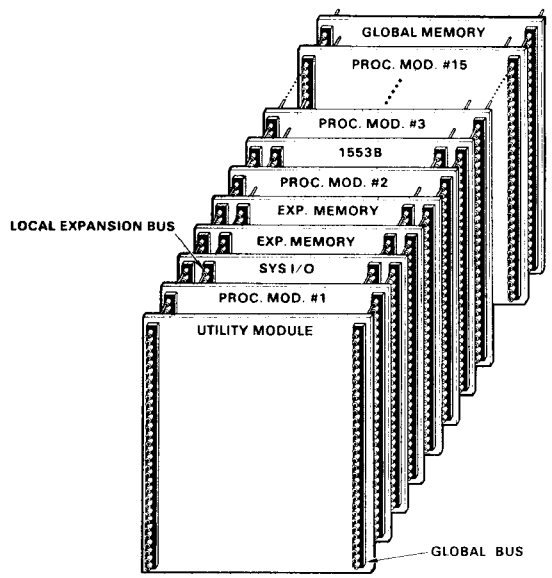
A second set of pins and sockets on Processor Modules and expansion modules (Expansion Memory, System I/O, MIL-STD-1553B) inside the global bus provides the local expansion bus. Expansion modules must be mated to the component side of the host Processor Module; expansion modules can be placed in any order on a Processor Module's expansion bus. A Processor Module and its associated expansion modules can be placed anywhere in a SANDAC V stack. For electrical continuity, expansion modules pass the global bus signals through, but do not connect to any of these signals. The interconnection scheme for SANDAC V is illustrated in Figure 1-2a. A physical arrangement of modules is shown in Figure 1-2b.

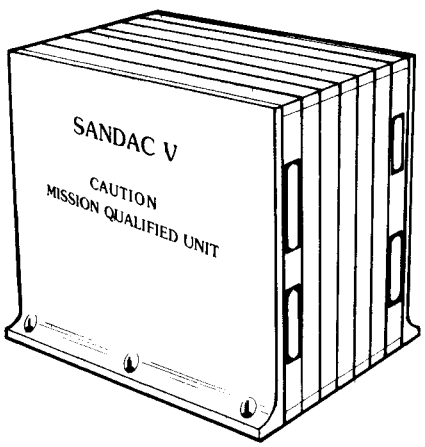
Once a set of modules is interconnected, the set is assembled between two end plates. An assembled SANDAC V is shown in Figure 1-2c.



(a) INTERCONNECTION SCHEME

(b) PHYSICAL MODULE ARRANGEMENT





(c) ASSEMBLED SANDAC V

Figure 1-2. SANDAC V Mechanical Design

1.4 SPECIFICATIONS

SANDAC V specifications are given in Table 1-1.

TABLE 1-1. SANDAC V SPECIFICATIONS

Size (per module)	6.25 H x 7.0 W x 0.57 D in
Weight (per module)	1 lb (typical)
Power Dissipation (per module)	5 W (maximum)
Modules per System	2 to 20
Shock (flight-qualified system)	Minuteman and Polaris A3 Payload
Vibration (flight-qualified system)	18 g rms random from 20 Hz to 2 kHz
Operating Temperature	-20° C to +70° C (case temperature)
External Power Requirement	8 to 12 Vdc

2. OPERATIONAL CONCEPTS

2.1 SYSTEM ADDRESS MAP

Logically, SANDAC V has an address space of 4 gigabytes. This space is divided into four areas:

- Utility Module address space
- Global Memory Module address space
- Processor Module address space
- Local Processor Module alias space

The address map for SANDAC V is shown in Figure 2-1. Descriptions of the four areas listed above are given in the following subsections.

2.1.1 Utility Module Address Space

The global resources provided by the Utility Module, EPROM, RAM, 32-bit timer, and status register, reside in the first megabyte of SANDAC V address space. Detailed descriptions of these resources are given in Section 5.

2.1.2 Global Memory Module Address Space

Thirty blocks of 512K bytes each are reserved for Global Memory Modules. The size of the individual blocks (512K bytes) corresponds to the storage capacity of a single Global Memory Module. The addresses that a module responds to are determined by hardware jumpers; thus, a Global Memory Module can be placed in any of the 30 reserved blocks. The address map for Global Memory Modules is shown in Figure 2-2. A detailed description of the Global Memory Module is given in Section 6.

2.1.3 Processor Module Address Space

A SANDAC V can be configured with as many as 15 Processor Modules. Each of the 15 possible modules is assigned a 16 megabyte block of address space. The particular block used by a Processor Module is determined by the module's identification (ID) number, which is set with hardware jumpers. The four-bit Processor ID, or hardware ID (HWID), can be from 0001 (1) through 1111 (15). The four bits that form the ID correspond to address bits 27 through 24 of the module's address space. Therefore, the 16 megabytes of space assigned to each Processor Module is defined by starting address 0n,000,000 hex and ending address 0n,FFF,FFF hex, where "n" is the Processor ID (HWID) in hex. The address map for Processor Modules is shown in Figure 2-3.

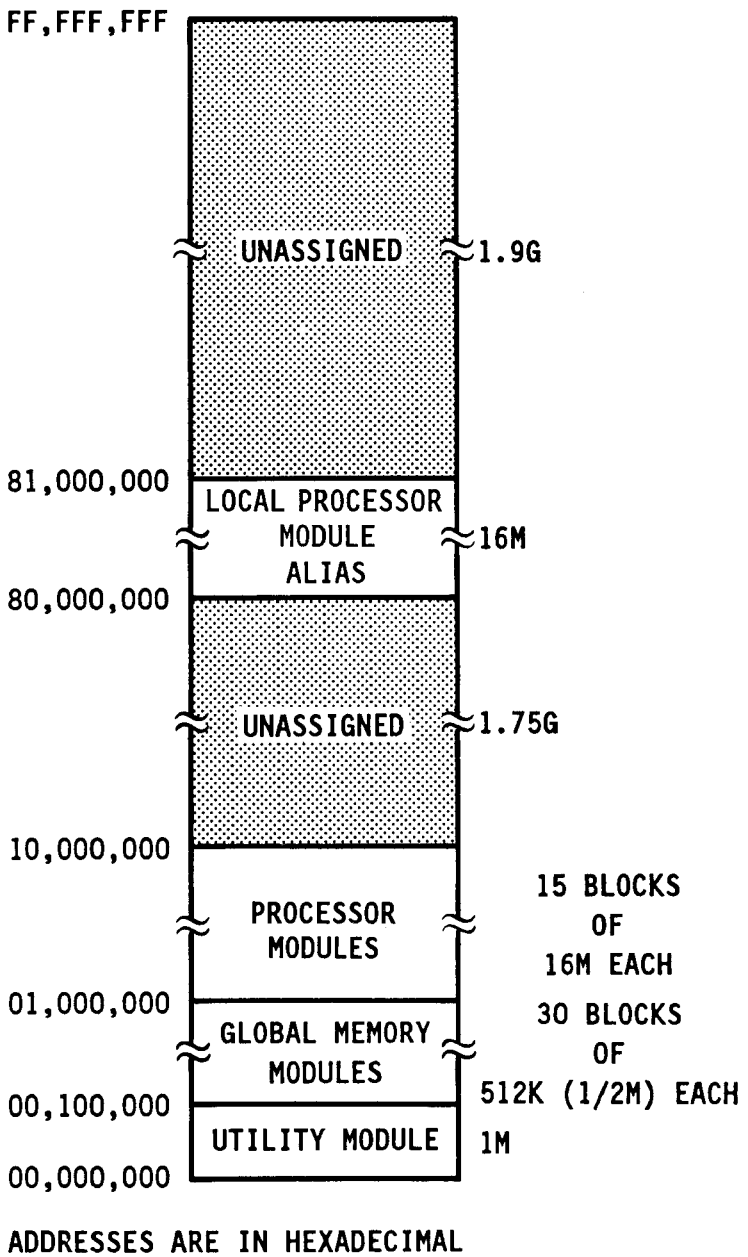


Figure 2-1. SANDAC V Address Map

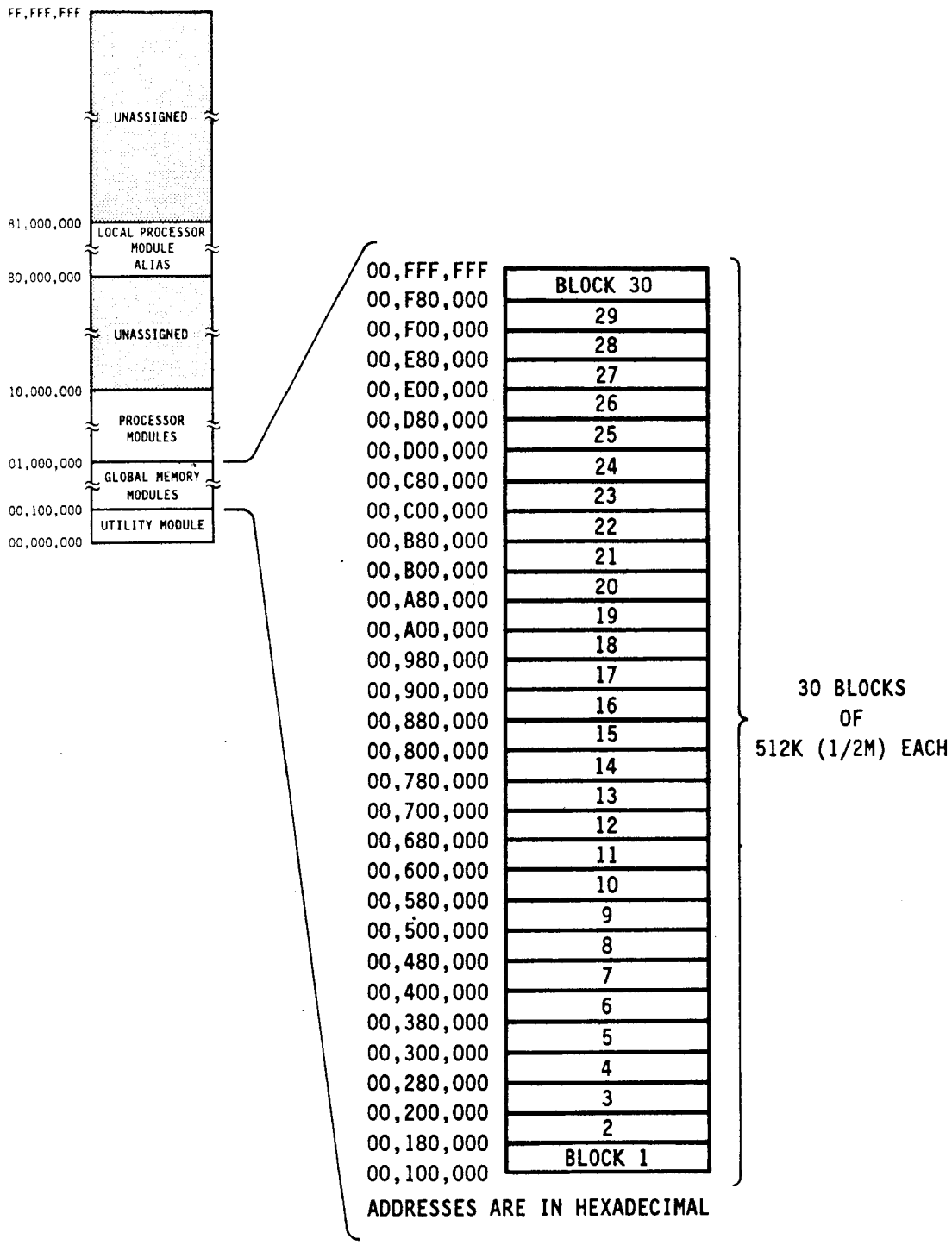


Figure 2-2. Global Memory Module Address Map

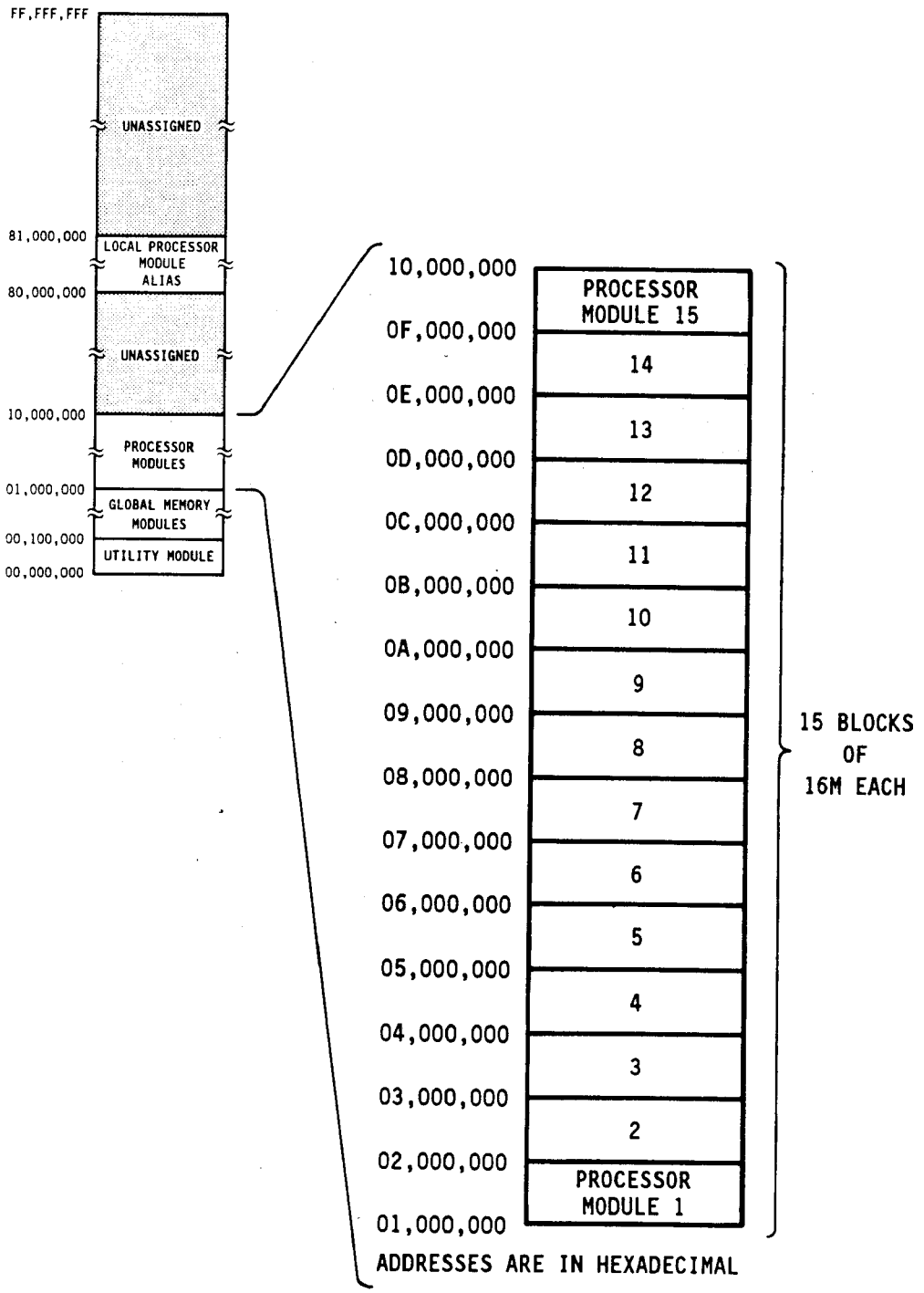


Figure 2-3. Processor Module Address Map

2.1.4 Local Processor Module Alias Space

The 16 megabyte local Processor Module alias at 80,000,000 hex is a logical entity only; no physical memory is present. It is included in the SANDAC V address map to support software development in a multiple processor environment.

When a Processor Module issues an address that is within the 16 megabyte alias space, the bus cycle generated will access the corresponding address in that Processor Module's own 16 megabyte address space. For example, if the Processor Module with the ID of 1 issues an address for location 80,000,1FE hex, the actual access is of location 01,000,1FE hex, a location in its own address space. By the same token, if the Processor Module with the ID of 2 issues an address for location 80,000,1FE hex, the actual access is of location 02,000,1FE hex, a location in *its* own address space.

This feature permits code with a base address of 80,000,000 hex to be independent of the Processor ID.

2.2 GLOBAL RESOURCES

The Utility Module and Global Memory Modules reside on the global bus, and the resources they provide are referred to as global resources. The following is a list of SANDAC V global resources:

- 256K Bytes of EPROM (Utility Module)
- 128K Bytes of RAM (Utility Module)
- 32-Bit Timer (Utility Module)
- Status Register (Utility Module)
- Battery-Backed RAM (512K Bytes per each Global Memory Module)

Detailed descriptions of these resources are in the sections on the Utility Module (5) and the Global Memory Module (6).

2.3 LOCAL RESOURCES

The Processor Module's MPU is supported by several memory-mapped resources located on the local bus and local expansion bus. These are known as local resources. The following is a list of local resources resident on the Processor Module (Section 4):

- Hardware Identification Register
- 15 Configuration Registers
- 128K Bytes of RAM
- 512-Byte FIFO
- Command/Status Register
- 8 Software Interrupts
- 68901 Multi-Function Peripheral

To provide additional local resources, the following expansion modules can be attached to a Processor Module:

- Expansion Memory Module (Section 7)
- System I/O Module (Section 8)
- MIL-STD-1553B Module (Section 9)

2.4 ACCESSING RESOURCES

Although SANDAC V contains global resources on the global bus and local resources on Processor Module local buses, *the address space for the entire system is linear.* The 32-bit addressing capability of the 68020 MPU gives each Processor Module an address range of 4 gigabytes, and the global bus provides access to all SANDAC V address space. By issuing the proper address, any Processor Module can access any global or local resource, including its own local resources (local access), any resource on the global bus (global access), or the local resource of any other Processor Module (global-to-local access). The different types of accesses are described below:

Local	A Processor Module's 68020 MPU issues an address within its local address space. Access of the location is via the local bus or local expansion bus.
Global	A Processor Module's 68020 MPU issues an address assigned to a global module (Utility or Global Memory). Access of the location is via the global bus.
Global-to-Local	A Processor Module's 68020 MPU issues an address within the address space of another Processor Module. Access of the location is via the global bus and the local bus of the addressed module.

2.4.1 Global Bus Arbitration

With multiple Processor Modules, two or more may try to use the global bus at the same time, so each Processor Module has a user-defined priority to determine which can use the bus first. A module's priority is related to its HWID as shown below:

HWID	Address Space (hex)	Priority
1	01,000,000-01,FFF,FFF	Lowest
2	02,000,000-02,FFF,FFF	.
3	03,000,000-03,FFF,FFF	.
4	04,000,000-04,FFF,FFF	.
5	05,000,000-05,FFF,FFF	.
6	06,000,000-06,FFF,FFF	.
7	07,000,000-07,FFF,FFF	.
8	08,000,000-08,FFF,FFF	.
9	09,000,000-09,FFF,FFF	.
10	0A,000,000-0A,FFF,FFF	.
11	0B,000,000-0B,FFF,FFF	.
12	0C,000,000-0C,FFF,FFF	.
13	0D,000,000-0D,FFF,FFF	.
14	0E,000,000-0E,FFF,FFF	.
15	0F,000,000-0F,FFF,FFF	Highest

Before using the global bus, a Processor Module initiates bus arbitration, comparing its priority to the priority of other modules requesting the global bus. If the bus is not busy, the module with the highest priority becomes the bus master.

SANDAC V has two modes of global bus arbitration. These modes, which are selectable with software (Subsection 4.4.2.1) are described below:

Priority Mode The Processor Module with the highest priority (highest ID number) is granted access to the global bus.

Fair Mode After a Processor Module has been the global bus master, it cannot make another request until the bus has been free for at least one clock cycle. Therefore, when two or more Processor Modules contend for the bus, the highest priority module is served first, but it is prevented from acquiring the bus again until the lowest priority module has been allowed access.

2.4.2 Bus Mastership

After a Processor Module is given global bus mastership through arbitration, it has exclusive use of the bus for a single access cycle. If the resource accessed is in the address space of another Processor Module, the accessing module must also gain control of the accessed module's local bus. If local bus mastership is granted, the accessing

module then has exclusive use of the accessed module's address space for a single access cycle.

2.4.3 Access Time

If an access is within the Processor Module's own local space, the 68020 MPU can run at maximum speed. If an access is of a global resource, three wait states are required for global bus arbitration if the global bus is idle. If there is bus contention, the wait time depends on the priority of the requesting Processor Module and the access time of the higher priority module. If the access is of a location in another Processor Module's address space, three wait states are required for global bus arbitration, and another six wait states are required to gain control of the local bus. This assumes the local MPU is idling. Additional wait states may be required by the resource being accessed.

2.4.4 Watchdog Timer

The Processor Module includes a circuit known as the watchdog timer. The timer terminates the bus cycle when there is no response to a local, global, or local-to-global access.

For a local access, the timer starts when the access starts; for a global and access, the timer starts after the Processor Module has gained control of the global bus. If a resource does not respond within 512 MPU clock cycles, the timer times out and generates a bus error, which terminates the bus cycle.

3. GLOBAL BUS

3.1 GENERAL DESCRIPTION

The SANDAC V global bus is the system-wide parallel bus connecting all Processor Modules, the Utility Module, and any Global Memory Modules. The Expansion Memory, System I/O, MIL-STD-1553B Modules do not reside on the global bus but do contain a full set of global bus connectors to pass signals through for continuity. Expansion modules draw power from the global bus.

The bus is comprised of 68020 MPU address, data, and control signals; power lines; clock signals; bus arbitration signals; and interrupt request lines. Physically, the bus consists of 126 interconnect pins divided between two connectors, J1 and J2. These connectors are on all SANDAC V modules, including expansion modules.

3.2 SIGNAL DESCRIPTION

Global bus signals are described in Table 3-1.

TABLE 3-1. GLOBAL BUS SIGNALS

Conn.-Pin	Mnemonic	Description
J1-1	-	Not Used
J1-2	GA2	Global Address Bit 2 - Global address bus (GA31-GA0) contains address for bus transfer.
J1-3	GA3	Global Address Bit 3
J1-4	GA4	Global Address Bit 4
J1-5	GA5	Global Address Bit 5
J1-6	GA6	Global Address Bit 6
J1-7	GA7	Global Address Bit 7
J1-8	GA8	Global Address Bit 8
J1-9	GA9	Global Address Bit 9
J1-10	GND	Dc power return and signal ground
J1-11	GND	
J1-12	GA10	Global Address Bit 10 - Global address bus (GA31-GA0) contains address for bus transfer.
J1-13	GA11	Global Address Bit 11
J1-14	GA12	Global Address Bit 12

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J1-15	GA13	Global Address Bit 13 - Global address bus (GA31-GA0) contains address for bus transfer.
J1-16	GA14	Global Address Bit 14
J1-17	GA15	Global Address Bit 15
J1-18	GA16	Global Address Bit 16
J1-19	GA17	Global Address Bit 17
J1-20	VCC	System power, +5 Vdc nominal
J1-21	VCC	
J1-22	GA18	Global Address Bit 18 - Global address bus (GA31-GA0) contains address for bus transfer.
J1-23	GA19	Global Address Bit 19
J1-24	GA20	Global Address Bit 20
J1-25	GA21	Global Address Bit 21
J1-26	GA22	Global Address Bit 22
J1-27	GA23	Global Address Bit 23
J1-28	GA24	Global Address Bit 24
J1-29	GA25	Global Address Bit 25
J1-30	GA26	Global Address Bit 26
J1-31	GA27	Global Address Bit 27
J1-32	GA28	Global Address Bit 28
J1-33	GA29	Global Address Bit 29
J1-34	GA30	Global Address Bit 30
J1-35	GA31	Global Address Bit 31
J1-36	GRW	Global Read/Write - Defines direction of data transfer. High level is a read; low level is a write.
J1-37	$\overline{\text{GIRQW}}$	Global Interrupt Request W (active low)
J1-38	$\overline{\text{GIRQX}}$	Global Interrupt Request X (active low)
J1-39	$\overline{\text{GIRQY}}$	Global Interrupt Request Y (active low)
J1-40	$\overline{\text{GIRQZ}}$	Global Interrupt Request Z (active low)
J1-41	$\overline{\text{GDS}}$	Global Data Strobe (active low) - During a read, indicates that device being read should drive data bus. During a write, indicates that data bus has valid data.
J1-42	$\overline{\text{GAS}}$	Global Address Strobe (active low) - Indicates that global bus has valid address, function code, size, and read/write state information.

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J1-43	$\overline{\text{GDSACK0}}$	Global Data Transfer and Size Acknowledge Bit 0 (active low; wire-OR output) - $\overline{\text{GDASCK0}}$ and $\overline{\text{GDSACK1}}$ indicate data transfer complete and also port size (8, 16, or 32 bits) of device accessed.
J1-44	$\overline{\text{GDSACK1}}$	Global Data Transfer and Size Acknowledge Bit 1 (active low; wire-OR output)

$\overline{\text{GDSACK1}}$	$\overline{\text{GDSACK0}}$	Transfer Status
0	0	Cycle complete; 32 bits
0	1	Cycle complete; 16 bits
1	0	Cycle complete; 8 bits
1	1	Cycle not complete; insert wait states

J1-45	$\overline{\text{GBERR}}$	Global Bus Error (active low) - Indicates problem with bus cycle.
J1-46	GA0	Global Address Bit 0 - Global address bus (GA31-GA 0) contains address for bus transfer.
J1-47	GA1	Global Address Bit 1
J1-48	GSIZ0	Global Data Transfer Size Bit 0 - GSIZ0 and GSIZ1 indicate number of operand bytes to be transferred during bus cycle.
J1-49	GSIZ1	Global Data Transfer Size Bit 1

GSIZ1	GSIZ0	Data Size (Bytes)
0	0	4 (long word)
0	1	1 (byte)
1	0	2 (word)
1	1	3

J1-50	$\overline{\text{GRMC}}$	Global Read-Modify-Write Cycle (active low) - Indicates current bus cycle is a read-modify-write. Signal is active for duration of operation.

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J1-51	GFC0	Global Function Code Bit 0 - GFC2, GFC1, and GFC0 identify MPU's execution level (user or supervisor) and the address space accessed.
J1-52	GFC1	Global Function Code Bit 1
J1-53	GFC2	Global Function Code Bit 2

GFC2	GFC1	GFC0	Address Space
0	0	0	Reserved
0	0	1	User data
0	1	0	User program
0	1	1	User defined
1	0	0	Reserved
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	CPU space

J1-54	GCLK2	Global Clock, 2.4576 MHz; synchronous to GCLK14
J1-55	VCC	System Power, +5 Vdc nominal
J1-56	GCLK14	Global Clock, 14.7456 MHz
J1-57	GND	Dc power return and signal ground
J1-58	GCLK16	Global Clock, 16 MHz
J1-59	GND	Dc power return and signal ground
J1-60	GCLK8	Global Clock, 8 MHz; synchronous to GCLK16
J1-61	GND	Dc power return and signal ground
J1-62	GCLK4	Global Clock, 4 MHz; synchronous to GCLK16
J1-63	-	Not Used

(End of J1)

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J2-1	VCC	System power, +5 Vdc nominal
J2-2	PRAM	Power, RAM - System RAM backup power. Vcc ±100 millivolts at powerup; +3.1 Vdc minimum after power down with battery backup.
J2-3	GD0	Global Data Bit 0 - Global data bus (GD31-GD0) forms data path for bus transfers.
J2-4	GD1	Global Data Bit 1
J2-5	GD2	Global Data Bit 2
J2-6	GD3	Global Data Bit 3
J2-7	GD4	Global Data Bit 4
J2-8	GD5	Global Data Bit 5
J2-9	GD6	Global Data Bit 6
J2-10	GD7	Global Data Bit 7
J2-11	GND	Dc power return and signal ground
J2-12	GND	
J2-13	GD8	Global Data Bit 8 - Global data bus (GD31-GD0) forms data path for bus transfers.
J2-14	GD9	Global Data Bit 9
J2-15	GD10	Global Data Bit 10
J2-16	GD11	Global Data Bit 11
J2-17	GD12	Global Data Bit 12
J2-18	GD13	Global Data Bit 13
J2-19	GD14	Global Data Bit 14
J2-20	GD15	Global Data Bit 15
J2-21	VCC	System power, +5 Vdc nominal
J2-22	VCC	
J2-23	GD16	Global Data Bit 16 - Global data bus (GD31-GD0) forms data path for bus transfers.
J2-24	GD17	Global Data Bit 17
J2-25	GD18	Global Data Bit 18
J2-26	GD19	Global Data Bit 19
J2-27	GD20	Global Data Bit 20
J2-28	GD21	Global Data Bit 21
J2-29	GD22	Global Data Bit 22
J2-30	GD23	Global Data Bit 23

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J2-31	PRAM	Power, RAM - System RAM backup power. Vcc ±100 millivolts at powerup; +3.1 Vdc minimum after power down with battery backup.
J2-32	GND	Dc power return and signal ground
J2-33	GD24	Global Data Bit 24 - Global data bus (GD31-GD0) forms data path for bus transfers.
J2-34	GD25	Global Data Bit 25
J2-35	GD26	Global Data Bit 26
J2-36	GD27	Global Data Bit 27
J2-37	GD28	Global Data Bit 28
J2-38	GD29	Global Data Bit 29
J2-39	GD30	Global Data Bit 30
J2-40	GD31	Global Data Bit 31
J2-41	GRAMPROT	Global RAM Protect - Inhibits selection of system RAM during power down.
J2-42	PWRIN	Power In - External, unregulated power to SANDAC V, 8-12 Vdc.
J2-43	GST	Global Serial Bus Transmit (wire-OR output) - Transmit data path for global serial bus.
J2-44	GSR	Global Serial Bus Receive - Receive data path for global serial bus.
J2-45	PRAMCTL	Backup Power Control - Disconnects Vcc and connects PRAM to system memory during power down.
J2-46	$\overline{\text{GRRUN}}$	Global Rerun (active low; wire-OR output) - Asserted by a Processor Module attempting a global read-modify-write when accessed by global bus master. Asserting this signal causes global master to retry access, thus allowing module to complete read-modify-write.

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J2-47	PWRST	Global Powerup Reset (active low) - Active following powerup and causes local reset signals to be generated. Active for 512 clock cycles minimum.
J2-48	-	Reserved
J2-49	-	
J2-50	-	
J2-51	-	
J2-52	-	
J2-53	$\overline{GPRI3}$	Global Priority Bit 3 (active low; wire-OR output) - $\overline{GPRI3}$-$\overline{GPRI0}$ are active during bus arbitration and indicate Processor Module's global bus priority. Priority is associated with the Processor ID.
J2-54	$\overline{GPRI2}$	Global Priority Bit 2 (active low; wire-OR output)
J2-55	$\overline{GPRI1}$	Global Priority Bit 1 (active low; wire-OR output)
J2-56	$\overline{GPRI0}$	Global Priority Bit 0 (active low; wire-OR output)

HWID	$\overline{GPRI3}$	$\overline{GPRI2}$	$\overline{GPRI1}$	$\overline{GPRI0}$	Priority
1111	0	0	0	0	Highest
1110	0	0	0	1	.
1101	0	0	1	0	.
1100	0	0	1	1	.
1011	0	1	0	0	.
1010	0	1	0	1	.
1001	0	1	1	0	.
1000	0	1	1	1	.
0111	1	0	0	0	.
0110	1	0	0	1	.
0101	1	0	1	0	.
0100	1	0	1	1	.
0011	1	1	0	0	.
0010	1	1	0	1	.
0001	1	1	1	0	Lowest
-	1	1	1	1	Idle

TABLE 3-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J2-57	$\overline{GBAR}$	Global Bus Arbitration Request (active low; wire-OR output) - Asserted when Processor Module requires global bus.
J2-58	$\overline{GBW}$	Global Bus Winner (active low; wire-OR output) - Asserted when Processor Module is the highest priority module requesting the bus. Assertion of signal negates $\overline{GBAR}$ and the $\overline{GPRI}$ signals. The bus winner waits for the negation of $\overline{GBLC}$ before assuming bus mastership.
J2-59	$\overline{GBLC}$	Global Bus Lock (active low; wire-OR output) - Asserted when global bus winner takes control of global bus. As long as $\overline{GBLC}$ is active, no other Processor Module can use bus. $\overline{GBW}$ is negated when this signal goes active.
J2-60 J2-61	- -	Reserved
J2-62	VCC	System power, +5 Vdc nominal
J2-63	GND	Dc power return and signal ground

3.3 LOADING SPECIFICATIONS

Loading specifications for global bus signals are given in Table 3-2. The specifications include the effects of the following:

- Input and output buffers
- Pull-up and pull-down resistors
- Bus pins and sockets
- Circuit board traces

TABLE 3-2. GLOBAL BUS LOADING SPECIFICATIONS

Global Bus and Expansion Modules	20 maximum
Capacitive signal load per module (except power and ground)	25 pf maximum
Pull-up resistor load per module (wire-OR)	2 KΩ minimum
Logic threshold	TTL Compatible

3.4 SIGNAL TERMINATION

Global bus signals are terminated as shown in Table 3-3. Termination resistors are located on the Utility Module.

TABLE 3-3. GLOBAL BUS SIGNAL TERMINATION

Signal	Terminating Resistor (Pull-up)
GA31-GA0	2.2 KΩ
GD31-GD0	2.2 KΩ
GRW	2.2 KΩ
$\overline{\text{GRMC}}$	2.2 KΩ
$\overline{\text{GDS}}$, $\overline{\text{GAS}}$	1 KΩ
$\overline{\text{GRRUN}}$	470 Ω
GFC3-GFC0	2.2 KΩ
$\overline{\text{GDSACK1}}$, $\overline{\text{GDSACK0}}$	470 Ω
GSIZ1, GSIZ0	2.2 KΩ
$\overline{\text{GBERR}}$	470 Ω
$\overline{\text{GIRQW}}$-$\overline{\text{GIRQZ}}$	2.2 KΩ

3.5 GLOBAL BUS ARBITRATION

When more than one Processor Module attempts to use the global bus, global bus arbitration circuits on each module resolve contentions using a scheme that gives the module with the highest priority bus mastership.

Priority is determined by a Processor Module's ID (Processor ID or HWID), which is set with hardware jumpers. HWIDs are from 1 to 15, corresponding to 15 possible SANDAC V Processor Modules. The module with HWID 15 (1111) has the highest priority; HWID 1 (0001) has the lowest priority.

3.5.1 Bus Arbitration Algorithm

The Processor Module uses the following signals for bus arbitration:

- Bus Arbitration Request ($\overline{BAR}$)
- Priority ($\overline{PRI3}$, $\overline{PRI2}$, $\overline{PRI1}$, $\overline{PRI0}$)
- Bus Winner ($\overline{BW}$)
- Bus Lock ($\overline{BLC}$)

These signals are driven onto the global bus by open-collector buffers. On the global bus, they become the following wire-ORed signals:

- $\overline{GBAR}$ (J2-57)
- $\overline{GPRI}$n (J2-53 through J2-56)
- $\overline{GBW}$ (J2-58)
- $\overline{GBLC}$ (J2-59)

Global bus arbitration is controlled by a Processor Module's gate array. When the gate array decodes an address issued by the local MPU that is outside the local address space, arbitration for the global bus begins.

Under control of the gate array, bus arbitration proceeds in two cycles, fast and normal. During the fast cycle, Processor Module PRIn bits are driven onto the global bus, and then each Processor Module compares its priority to the wire-OR result of the $\overline{GPRI}$n bits on the global bus. A module with local priority equal to global priority is the bus winner. If there is no bus winner, the normal cycle is entered. In this cycle, priority bits are compared one at a time until there is a bus winner.

The flowchart in Figure 3-1 details global bus arbitration activity.

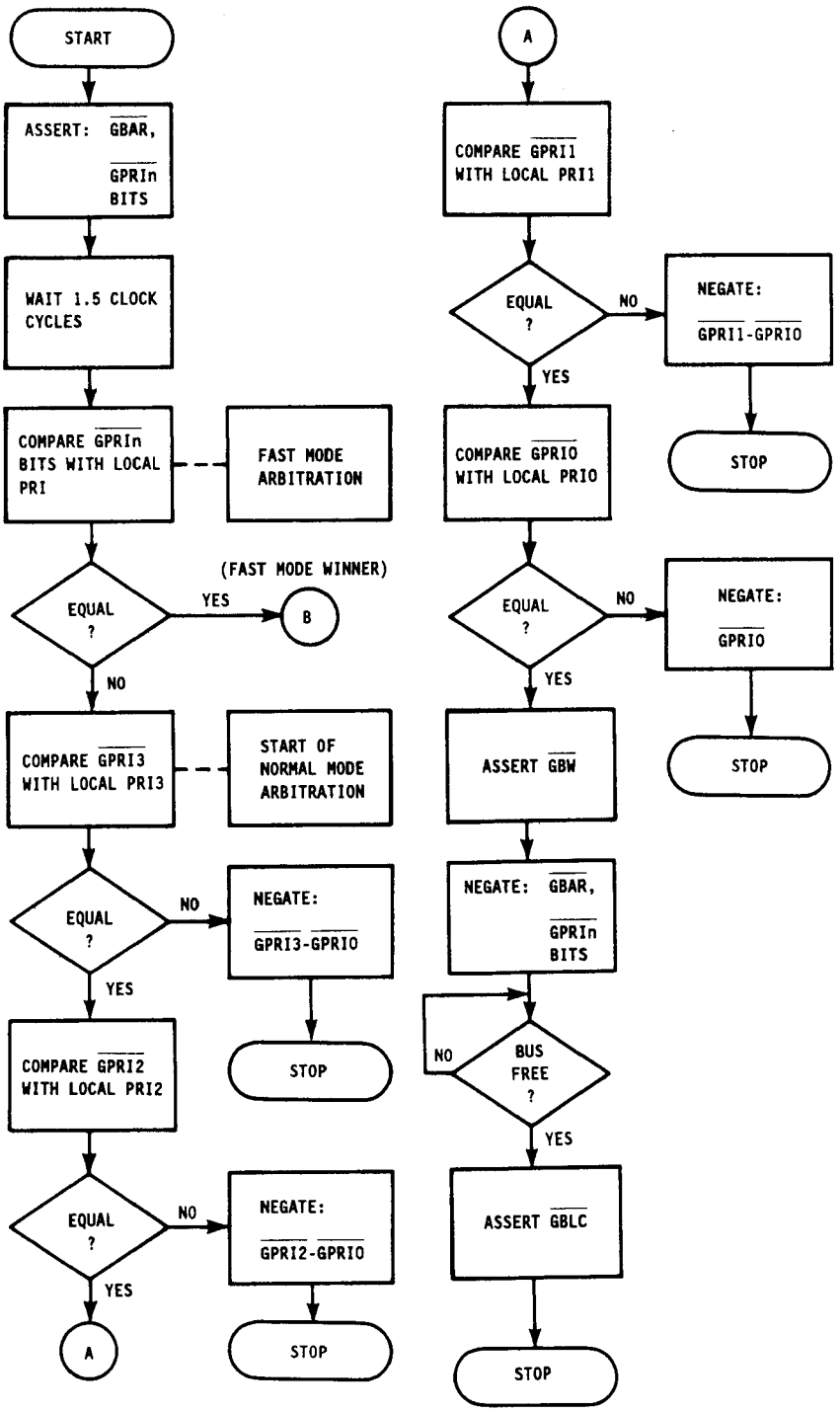


Figure 3-1. Global Bus Arbitration

3.5.2 Global Bus Arbitration Timing

Timing diagrams for bus arbitration are shown in Figure 3-2. These diagrams show activity for the fast cycle and for the normal cycle. Global bus arbitration time is calculated from the assertion of $\overline{BAR}$ until the next arbitration cycle starts. This assumes that the global bus is free at the end of the arbitration cycle so that the bus winner can become the bus master immediately and the next arbitration cycle may start.

NOTE

After a Processor Module has become the bus master and takes control of the global bus, another round of arbitration may start during the current bus master's cycle. When the master completes the bus cycle, the next global bus winner is waiting to take control.

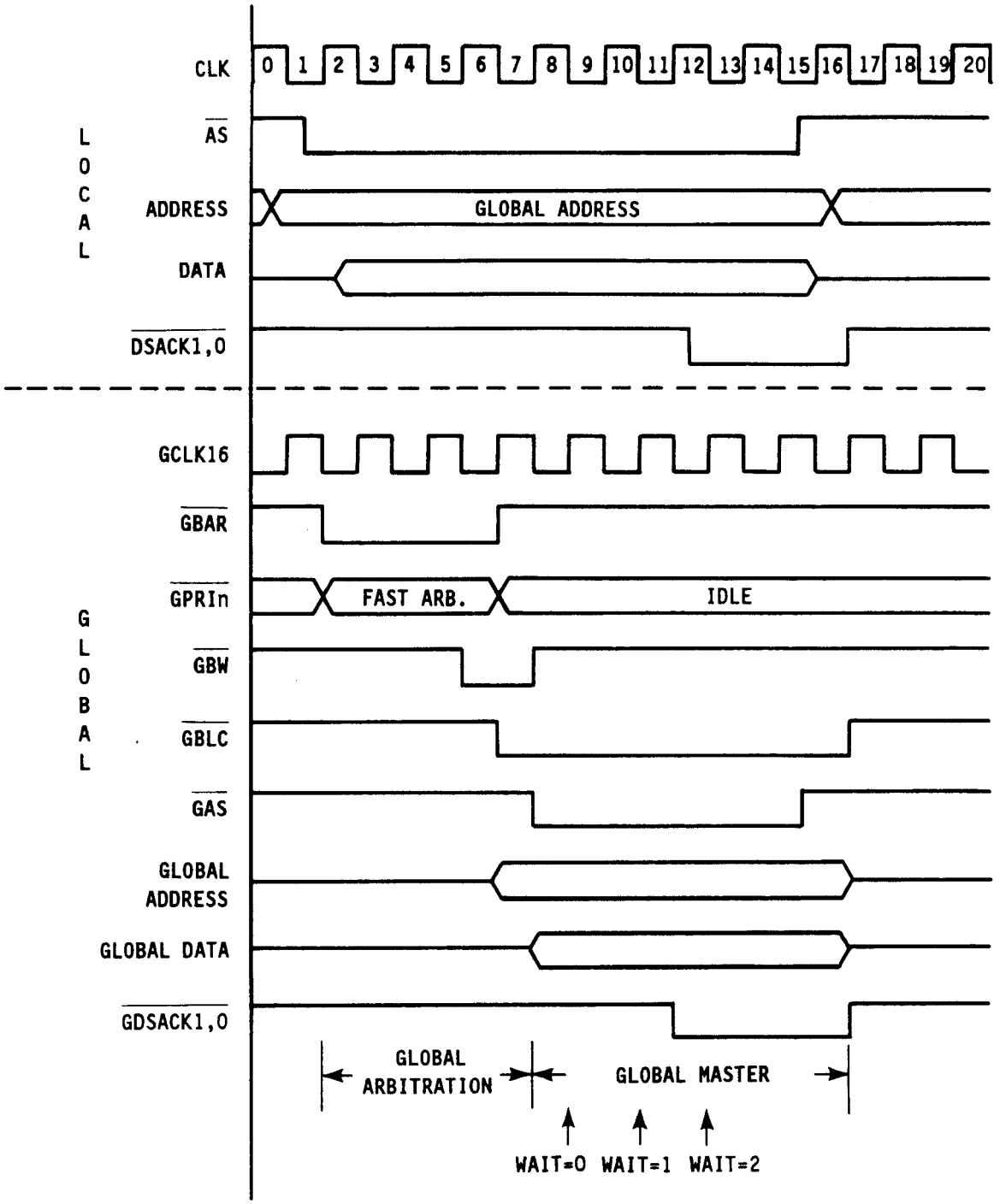


Figure 3-2a. Bus Arbitration Timing (Local-to-Global, Fast Arbitration, 2 Wait States).

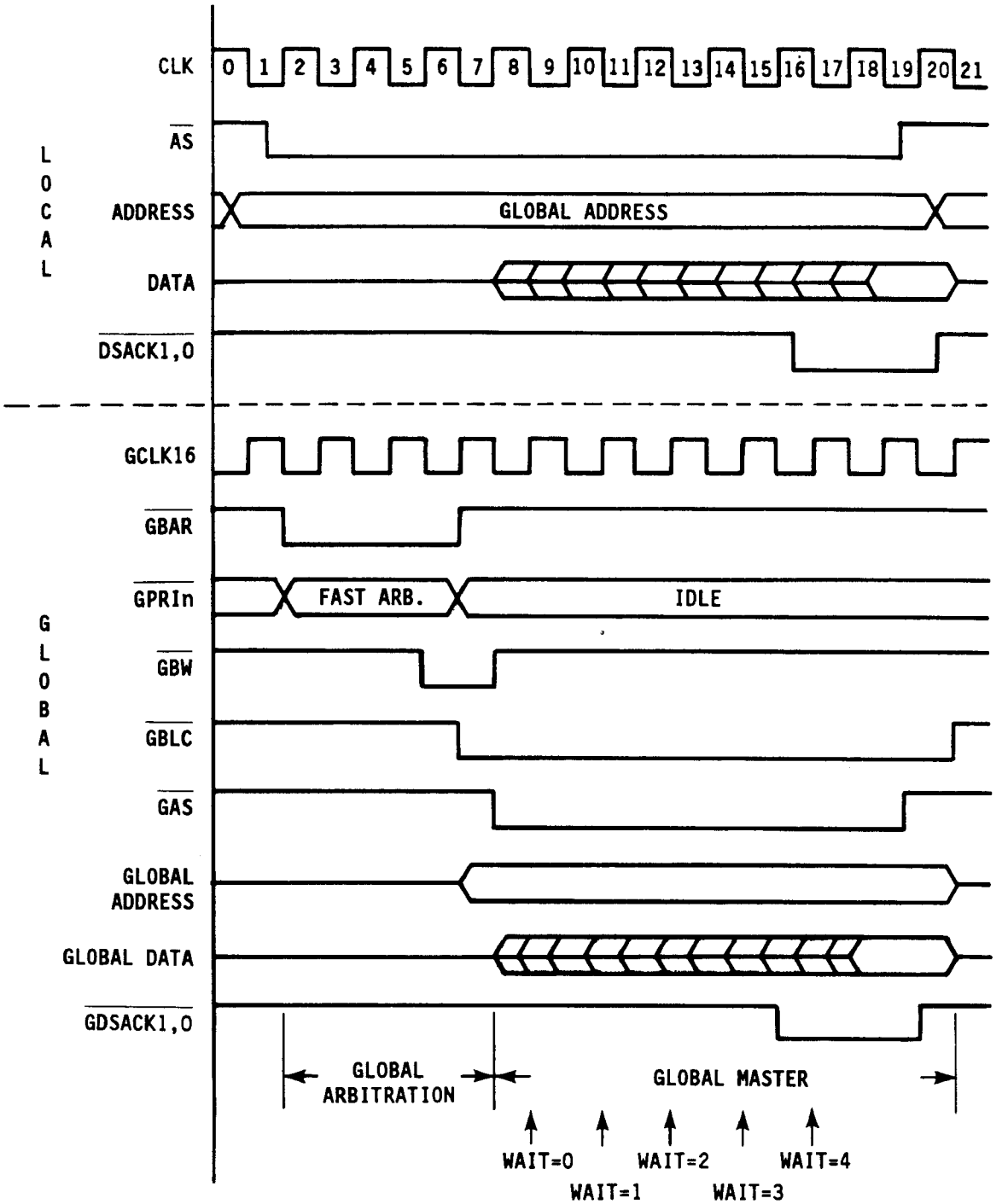


Figure 3-2b. Bus Arbitration Timing (Local-to-Global, Fast Arbitration, 4 Wait States).

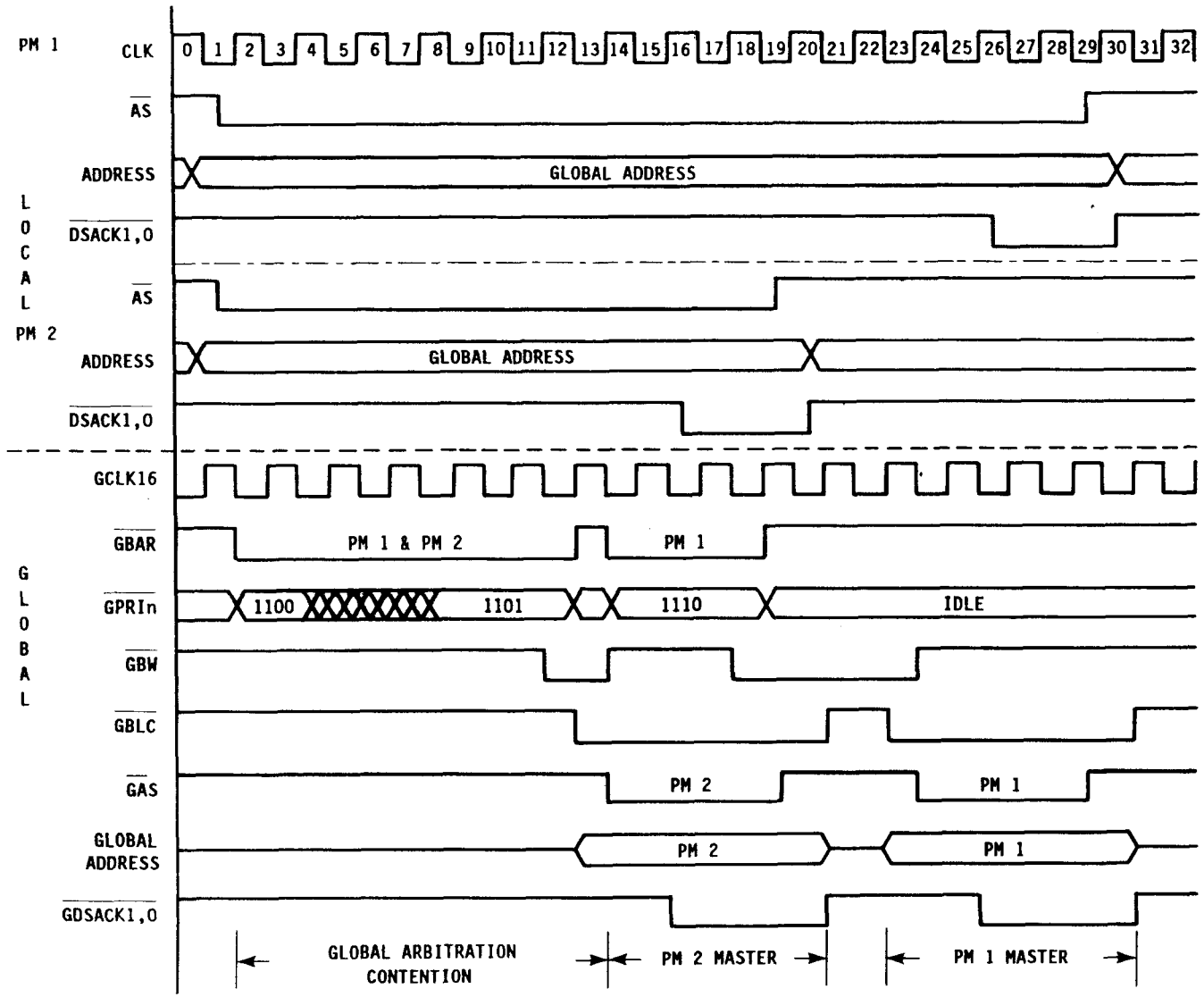


Figure 3-2c. Bus Arbitration Timing (Local-to-Global, Normal Arbitration, 1 Wait State).

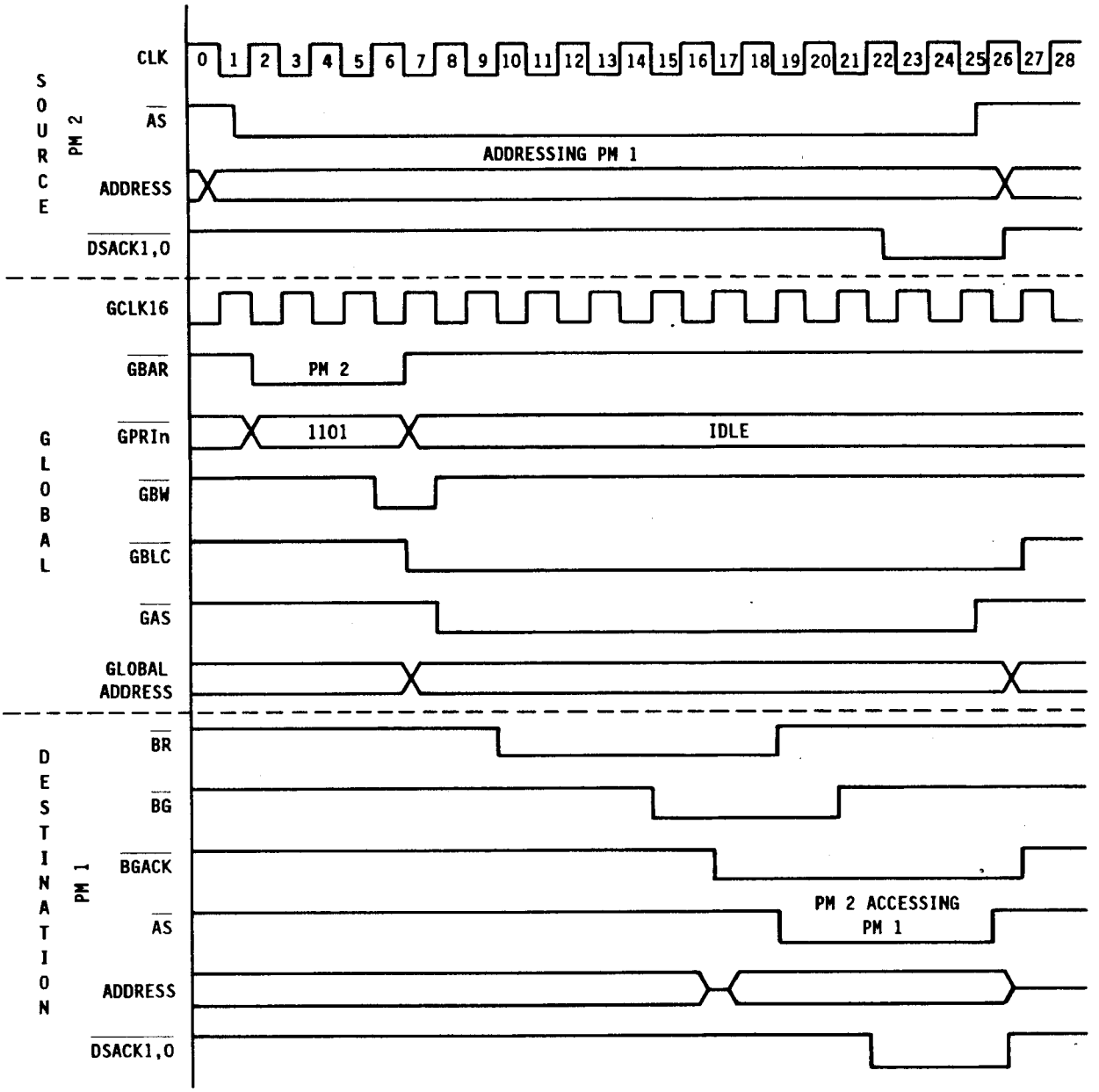


Figure 3-2d. Bus Arbitration Timing (Processor Module 2 Accessing Processor Module 1, Fast Arbitration, Processor Module 1 Idle, 1 Wait State).

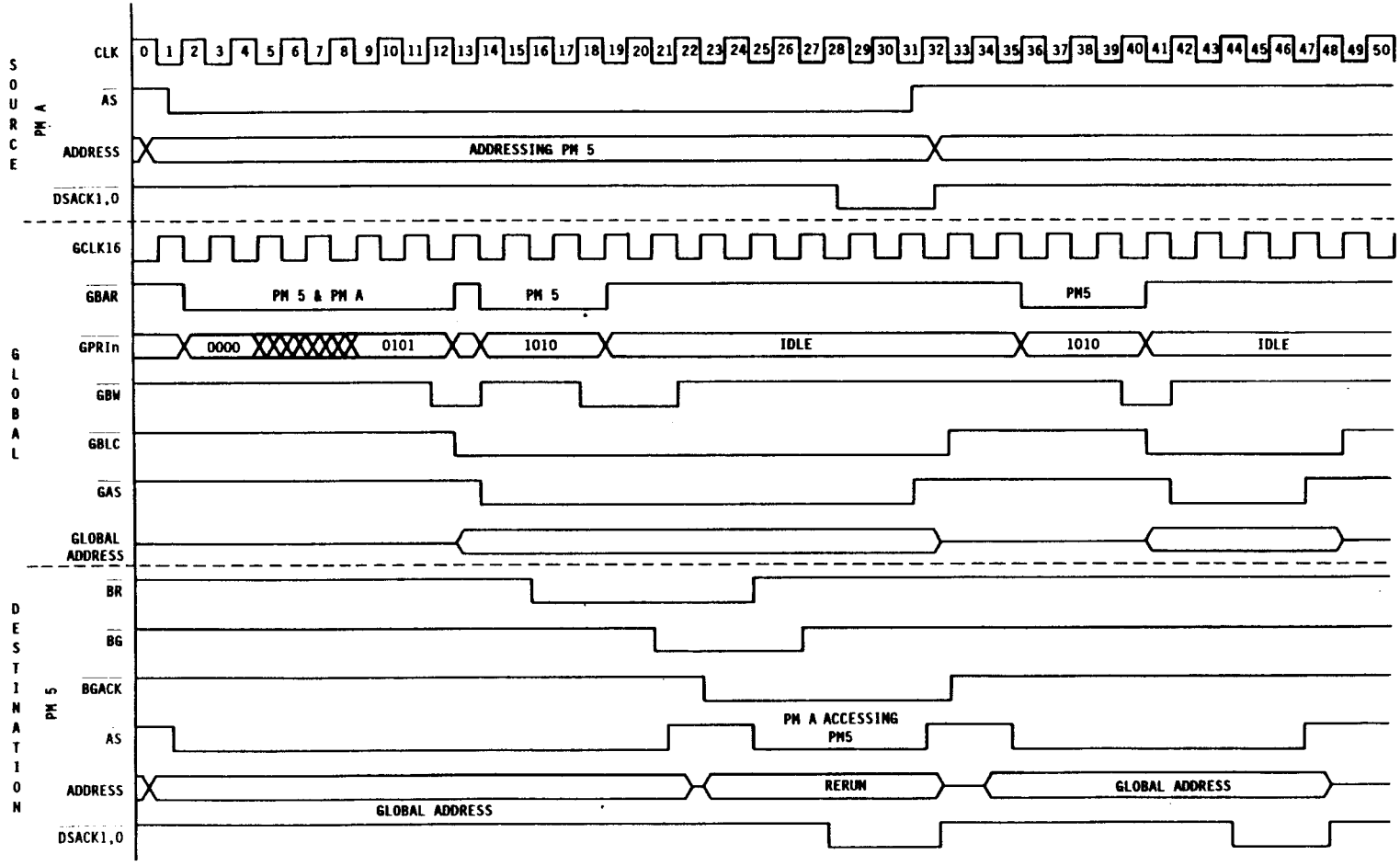


Figure 3-2e. Bus Arbitration Timing (Processor Module A Accessing Processor Module 5, Normal Arbitration, 1 Wait State).

Arbitration time also depends on whether a winner is established in the fast cycle or in the normal cycle. During the normal cycle, additional clock cycles are required to evaluate individual priority bits. The SANDAC V system configuration should take advantage of fast arbitration whenever possible. The following example shows how HWID assignments can speed up the bus arbitration process.

Example: A system includes two Processor Modules with HWIDs of 1100 and 1000. When these two Processor Modules are competing for the global bus, the module with HWID = 1100 will always win in the fast cycle because the wire-ORed $\overline{GPRIn}$ signals will be 1100. However, if the HWIDs of the modules are 1100 and 0011, the wire-ORed $\overline{GRPIn}$ signals will be 1111. There will be no winner during the fast cycle and the normal cycle will begin. After bit comparisons, the module with HWID = 1100 will eventually be the bus winner.

The following shows how to assign HWIDs for maximum performance, depending on the number of Processor Modules in the system:

Extant Processor Module	HWID
1st	1111
2nd	1110
3rd	1100
4th	1000
5th	0100
6th	0110
7th	0111
8th	1101
9th	0010
10th	1010
11th	1011
12th	0001
13th	1001
14th	0101
15th	0011

For example, if a system contains only five Processor Modules, the first five IDs shown above should be used.

3.5.3 Global Bus Bandwidth

Global bus bandwidth depends on the time required for bus arbitration and the time required for the bus master's operation. Since these two operations may be in parallel,

bandwidth is a function of the activity that requires more time. In SANDAC V, the fastest arbitration time takes four clock cycles, and the fastest bus master operation takes five clock cycles. Therefore, assuming a 16 MHz clock, the fastest global bus bandwidth is 3.2 million bus cycles per second. With a bus arbitration time of seven clock cycles, as in the normal bus arbitration mode, the global bus bandwidth drops to 2.3 million bus cycles per second.

NOTES

4. PROCESSOR MODULE

4.1 OVERVIEW

The SANDAC V Processor Module uses the Motorola MC68020 microprocessing unit (MPU) and MC68881 floating-point coprocessor. These two devices are interconnected for full 32-bit data transfer and logically form a single processing unit. Complete information on the 68020 and the 68881 is in the following Motorola publications:

- *MC68020 32-Bit Microprocessor User's Manual*
- *MC68881 Floating-Point Coprocessor User's Manual*

Processing is supported by the following Processor Module (local) resources:

- Hardware Identification (HWID) Register
- Configuration Registers (15)
- 128K Bytes of RAM
- 512-Byte First-In-First-Out (FIFO) Buffer
- Command/Status Register
- Software Interrupts
- 68901 Multi-Function Peripheral (MFP)

Additional local resources can be added by attaching SANDAC V expansion modules. The Processor Module also has a programmable interrupt system and a global serial bus interface.

The major hardware component on the Processor Module is a VLSI gate array that contains several of the local resources and provides most of the module's "glue" logic.

The architecture of the Processor Module is shown in Figure 4-1. A detailed description of the module is given in the following subsections.

NOTE

The circuit diagram of the Processor Module is Sandia National Laboratories drawing CK-S64650. In the following text, all component number and signal references are from this drawing.

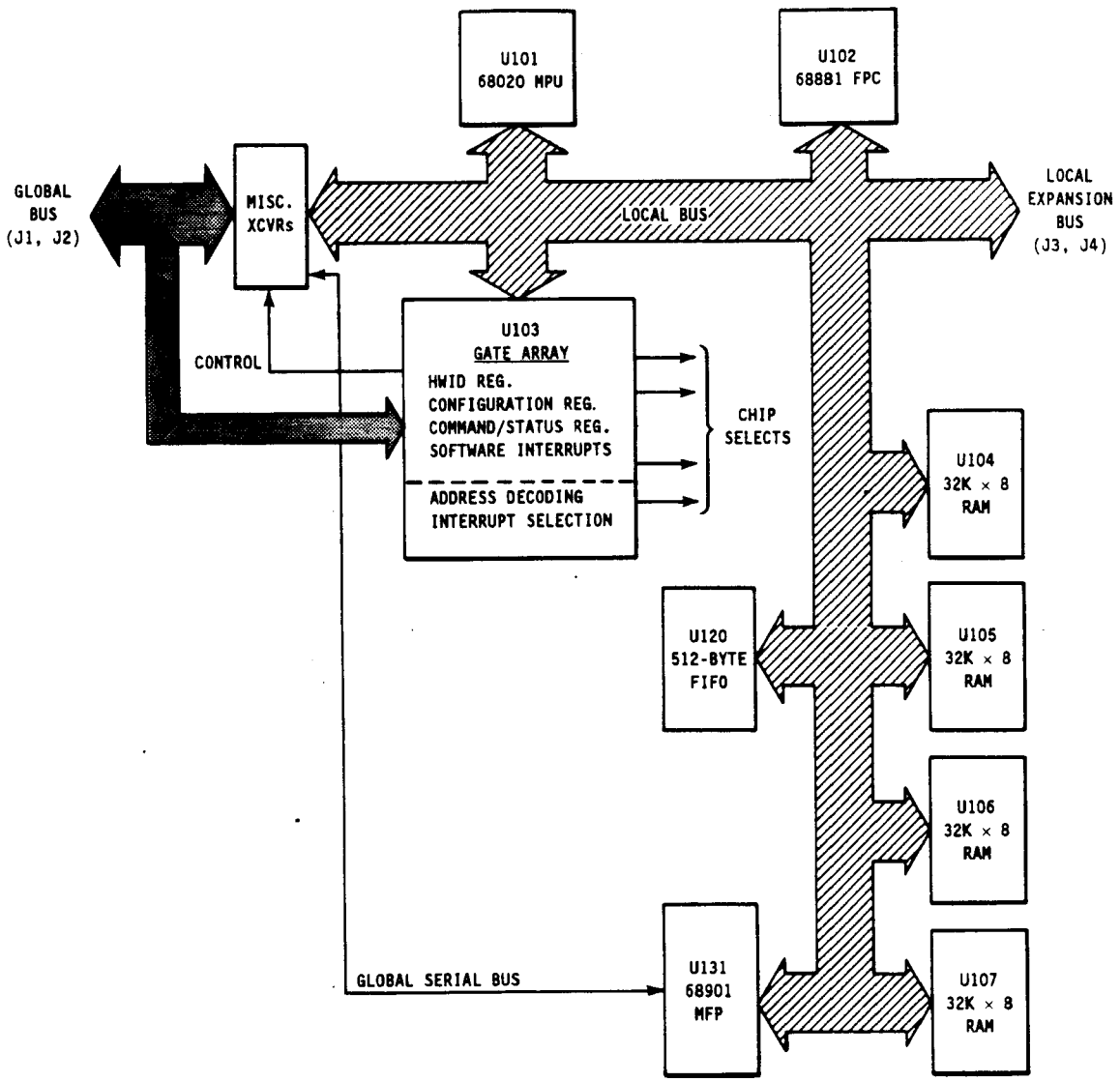


Figure 4-1. Processor Module Architecture

4.2 LOCAL BUS

The local bus connects the 68020 MPU with the local resources. The bus is comprised of 68020 MPU address, data, and control lines; power lines; clocks; resource select lines; and interrupt request lines.

The local bus, which runs throughout the Processor Module, is also connected to 126 interconnect pins divided between two connectors, J3 and J4. These connectors extend the local bus into the local expansion bus and allow expansion modules to be connected to the Processor Module. The local expansion bus includes the same signals as the local bus, with one exception: the interrupt acknowledge daisy chain line is on the expansion bus only.

4.2.1 Signal Description

A description of local and local expansion bus signals is given in Table 4-1.

TABLE 4-1. LOCAL/LOCAL EXPANSION BUS SIGNALS

Conn.-Pin	Mnemonic	Description
J3-1	-	Not Used
J3-2	A2	Local Address Bit 2 - Local address bus (A31-A0) contains address for bus transfer.
J3-3	A3	Local Address Bit 3
J3-4	A4	Local Address Bit 4
J3-5	A5	Local Address Bit 5
J3-6	A6	Local Address Bit 6
J3-7	A7	Local Address Bit 7
J3-8	A8	Local Address Bit 8
J3-9	A9	Local Address Bit 9
J3-10	GND	Dc power return and signal ground
J3-11	GND	
J3-12	A10	Local Address Bit 10 - Local address bus (A31-A0) contains address for bus transfer.
J3-13	A11	Local Address Bit 11
J3-14	A12	Local Address Bit 12
J3-15	A13	Local Address Bit 13

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J3-16	A14	Local Address Bit 14 - Local address bus (A31-A0) contains address for bus transfer.
J3-17	A15	Local Address Bit 15
J3-18	A16	Local Address Bit 16
J3-19	A17	Local Address Bit 17
J3-20	VCC	Module power, +5 Vdc nominal
J3-21	VCC	
J3-22	A18	Local Address Bit 18 - Local address bus (A31-A0) contains address for bus transfer.
J3-23	A19	Local Address Bit 19
J3-24	A20	Local Address Bit 20
J3-25	A21	Local Address Bit 21
J3-26	A22	Local Address Bit 22
J3-27	A23	Local Address Bit 23
J3-28	A24	Local Address Bit 24
J3-29	A25	Local Address Bit 25
J3-30	A26	Local Address Bit 26
J3-31	A27	Local Address Bit 27
J3-32	A28	Local Address Bit 28
J3-33	A29	Local Address Bit 29
J3-34	A30	Local Address Bit 30
J3-35	A31	Local Address Bit 31
J3-36	RW	Local Read/Write - Defines direction of data transfer. High level is a read; low level is a write.
J3-37	$\overline{\text{EMEM4}}$	Expansion Memory Board 4 Select (active low)
J3-38	$\overline{\text{EMEM3}}$	Expansion Memory Board 3 Select (active low)
J3-39	$\overline{\text{EMEM2}}$	Expansion Memory Board 2 Select (active low)
J3-40	$\overline{\text{EMEM1}}$	Expansion Memory Board 1 Select (active low)
J3-41	$\overline{\text{DS}}$	Local Data Strobe (active low) - During a read, indicates that device being read should drive data bus. During a write, indicates that data bus has valid data.

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J3-42	$\overline{AS}$	Local Address Strobe (active low) - Indicates that global bus has valid address, function code, size, and read/write state information.
J3-43	$\overline{DSACK0}$	Local Data Transfer and Size Acknowledge Bit 0 (active low; wire-OR output) - $\overline{DASCK0}$ and $\overline{DSACK1}$ indicate data transfer complete and also port size (8, 16, or 32 bits) of device accessed.
J3-44	$\overline{DSACK1}$	Local Data Transfer and Size Acknowledge Bit 1 (active low; wire-OR output)

$\overline{DSACK1}$	$\overline{DSACK0}$	Transfer Status
0	0	Cycle complete; 32 bits
0	1	Cycle complete; 16 bits
1	0	Cycle complete; 8 bits
1	1	Cycle not complete; insert wait states

J3-45	$\overline{BERR}$	Local Bus Error (active low) - Indicates problem with bus cycle.
J3-46	A0	Local Address Bit 0 - Local address bus (A31-A0) contains address for bus transfer.
J3-47	A1	Local Address Bit 1
J3-48	SIZ0	Local Data Transfer Size Bit 0 - SIZ0 and SIZ1 indicate number of operand bytes to be transferred during a bus cycle.
J3-49	SIZ1	Local Data Transfer Size Bit 1

SIZ1	SIZ0	Data Size (Bytes)
0	0	4 (long word)
0	1	1 (byte)
1	0	2 (word)
1	1	3

J3-50	$\overline{RMC}$	Local Read-Modify-Write Cycle (active low) - Indicates that current bus cycle is a read-modify-write. Signal is active for duration of operation.

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J3-51	FC0	Local Function Code Bit 0 - FC2-FC0 identify MPU's execution level (user or supervisor) and the address space accessed.
J3-52	FC1	Local Function Code Bit 1
J3-53	FC2	Local Function Code Bit 2

FC2	FC1	FC0	Address Space
0	0	0	Reserved
0	0	1	User data
0	1	0	User program
0	1	1	User defined
1	0	0	Reserved
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	CPU space

J3-54	CLK2	Clock, 2.4576 MHz; synchronous to CLK14
J3-55	VCC	Module power, +5 Vdc nominal
J3-56	CLK14	Clock, 14.7456 MHz
J3-57	GND	Dc power return and signal ground
J3-58	ECLK16	Expansion Bus Clock, 16 MHz
J3-59	GND	Dc power return and signal ground
J3-60	CLK8	Clock, 8 MHz; synchronous to ECLK16
J3-61	GND	Dc power return and signal ground
J3-62	CLK4	Clock, 4 MHz; synchronous to ECLK16
J3-63	-	Not Used

(End of J3)

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J4-1	VCC	Module power, +5 Vdc nominal
J4-2	PRAM	Power, RAM - Module RAM backup power. Vcc ±100 millivolts on powerup; +3.1 Vdc minimum after power down with battery backup.
J4-3	D0	Local Data Bit 0 - Local data bus (D31-D0) forms data path for bus transfers.
J4-4	D1	Local Data Bit 1
J4-5	D2	Local Data Bit 2
J4-6	D3	Local Data Bit 3
J4-7	D4	Local Data Bit 4
J4-8	D5	Local Data Bit 5
J4-9	D6	Local Data Bit 6
J4-10	D7	Local Data Bit 7
J4-11	GND	Dc power return and signal ground
J4-12	GND	
J4-13	D8	Local Data Bit 8 - Local data bus (D31-D0) forms data path for bus transfers.
J4-14	D9	Local Data Bit 9
J4-15	D10	Local Data Bit 10
J4-16	D11	Local Data Bit 11
J4-17	D12	Local Data Bit 12
J4-18	D13	Local Data Bit 13
J4-19	D14	Local Data Bit 14
J4-20	D15	Local Data Bit 15
J4-21	VCC	Module power, +5 Vdc nominal
J4-22	VCC	
J4-23	D16	Local Data Bit 16 - Local data bus (D31-D0) forms data path for bus transfers.
J4-24	D17	Local Data Bit 17
J4-25	D18	Local Data Bit 18
J4-26	D19	Local Data Bit 19
J4-27	D20	Local Data Bit 20
J4-28	D21	Local Data Bit 21
J4-29	D22	Local Data Bit 22
J4-30	D23	Local Data Bit 23

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J4-31	PRAM	Power, RAM - Module RAM backup power. Vcc ±100 millivolts on powerup; +3.1 Vdc minimum after power down with battery backup.
J4-32	GND	Dc power return and signal ground
J4-33	D24	Local Data Bit 24 - Local data bus (D31-D0) forms data path for bus transfers.
J4-34	D25	Local Data Bit 25
J4-35	D26	Local Data Bit 26
J4-36	D27	Local Data Bit 27
J4-37	D28	Local Data Bit 28
J4-38	D29	Local Data Bit 29
J4-39	D30	Local Data Bit 30
J4-40	D31	Local Data Bit 31
J4-41	RAMPROT	RAM Protect - Inhibits selection of system RAM during power down.
J4-42	PWRIN	Power In - External, unregulated power, 8 to 12 Vdc.
J4-43	EPCOM	Expansion Coprocessor Communication
J4-44	$\overline{\text{EXIO}}$	Expansion I/O Module Select (active low).
J4-45	$\overline{\text{ESIO}}$	System I/O Module Select (active low).
J4-46	$\overline{\text{HALT}}$	Local Halt (active low) - When asserted by a device external to the MPU, causes 68020 to stop bus activity. When asserted by the 68020, indicates 68020 bus is stopped.
J4-47	$\overline{\text{RESET}}$	Local Reset (active low) - Active following powerup and causes local reset signals to be generated. Active for 512 clock cycles minimum.
J4-48	$\overline{\text{BGACK}}$	Local Bus Grant Acknowledge (active low) - Indicates a device other than the MPU has become the bus master.

TABLE 4-1. CONTINUED

Conn.-Pin	Mnemonic	Description
J4-49	$\overline{EBR}$	Expansion Bus Request (wire-OR input; active low) - Indicates that a device on the local expansion bus requires bus mastership.
J4-50	$\overline{EBG}$	Expansion Bus Grant (active low) - Indicates that the 68020 will release the bus at the completion of the current bus cycle.
J4-51	$\overline{BR}$	Local Bus Request (wire-OR input; active low) - Indicates that a device on the local bus requires bus mastership.
J4-52	-	Not Used
J4-53	$\overline{EIACKDC}$	Expansion Bus Interrupt Acknowledge Daisy Chain (active low) - Propagates interrupt acknowledge signal from one expansion module to another.
J4-54	$\overline{EIRQW}$	Expansion Bus Interrupt Request W (active low)
J4-55	$\overline{EIRQX}$	Expansion Bus Interrupt Request X (active low)
J4-56	$\overline{EIRQY}$	Expansion Bus Interrupt Request Y (active low)
J4-57	$\overline{EIRQZ}$	Expansion Bus Interrupt Request Z (active low)
J4-58	$\overline{EIACKW}$	Expansion Bus Interrupt Acknowledge W (active low)
J4-59	$\overline{EIACKX}$	Expansion Bus Interrupt Acknowledge X (active low)
J4-60	$\overline{EIACKY}$	Expansion Bus Interrupt Acknowledge Y (active low)
J4-61	$\overline{EIACKZ}$	Expansion Bus Interrupt Acknowledge Z (active low)
J4-62	VCC	Module power, +5 Vdc nominal
J4-63	GND	Dc power return and signal ground

4.2.2 Loading

Loading specifications for the local expansion bus signals are given in Table 4-2. The specifications include the loading effects of the following:

- Input and output buffers
- Pull-up and pull-down resistors
- Bus pins and sockets
- Circuit board traces

TABLE 4-2. LOCAL EXPANSION BUS LOADING SPECIFICATIONS

Expansion Bus Modules	4 maximum
Capacitive signal load per module (except power and ground)	25 pf maximum
Pull-up resistor load per module (wire-OR)	2 KΩ minimum
Logic threshold	TTL compatible

4.3 ACCESSING LOCAL RESOURCES

4.3.1 Local Bus Arbitration

Resources on the local bus can be accessed by any of the following:

- Local 68020 MPU
- An "alternate local bus master" such as the System I/O Module DMA controller (refer to Section 8)
- 68020 MPU of another Processor Module (remote processor) that has gained control of the global bus through global bus arbitration

To handle possible contentions for mastership of the local bus, the Processor Module has a local bus arbitration circuit implemented in the gate array (U103).

The local MPU has the lowest priority with respect to the other possible bus masters. When a remote processor (global bus master) or an alternate local bus master requests the local bus, the local MPU always relinquishes control after the completing the current bus cycle.

Local bus arbitration uses the standard 68020 bus arbitration scheme as shown in the flow diagram in Figure 4-2. The top portion of the figure shows a remote processor requesting the bus; the lower portion shows an alternate local bus master.

4.3.2 Resource Access

Once a bus master has been established through arbitration, the access of a resource proceeds as shown in Figure 4-3. Addresses are decoded by the gate array (U103), which then generates the proper resource select signal. For some resources, the gate array generates the 68020 $\overline{\text{DSACK}}$n signals inserting any required wait states; for other resources, the selected device handles this. For wait states generated by the gate array, one additional wait state is inserted when the access is by the alternate local bus master or a remote processor. Table 4-3 summarizes this activity.

TABLE 4-3. $\overline{\text{DSACK}}$n AND WAIT STATE GENERATION

Resource	$\overline{\text{DSACK}}$ From	Wait States (Local MPU)	Wait States Alternate Local Bus Master or Remote MPU
68881 Coprocessor	Device	Varies	Varies
Hardware ID Register	Gate Array	3	4
Configuration Registers	Gate Array	3	4
RAM	Gate Array	0-3*	1-4*
FIFO	Gate Array	3	4
Command/Status Register	Gate Array	3	4
68901 MFP	Device	Varies	Varies
Software Interrupts	Gate Array	3	4
Expansion Modules	Module	Varies	Varies

*The number of wait states inserted when RAM is accessed is selectable with hardware jumpers. Appendix B details the setting of these jumpers.

REMOTE PROCESSOR **LOCAL GATE ARRAY** **LOCAL 68020 MPU**

1. Drive global bus with signals for access.

1. Decode GA31-GA24 as this module's ID.
2. Assert $\overline{BR}$ to local 68020.

1. Assert $\overline{BG}$.
2. Relinquish the bus at the end of the current cycle.

1. Assert $\overline{BGACK}$ to local 68020.
2. Enable global transceiver.

1. Take control of other Processor Module's local bus.

ALT. LOCAL BUS MASTER **LOCAL GATE ARRAY** **LOCAL 68020 MPU**

1. Assert $\overline{EBR}$.

1. Assert $\overline{BR}$ to local 68020.

1. Assert $\overline{BG}$.
2. Relinquish bus mastership at the end of the current cycle.

1. Drive $\overline{EBGACK}$ on expansion bus.

1. Assert $\overline{BGACK}$.
2. Take control of local bus.

Figure 4-2. Local Bus Arbitration

BUS MASTER	LOCAL GATE ARRAY	RESOURCE
1. Drive signals required for access.		
	1. Decode address. 2. Generate select signal. 3. Assert $\overline{DSACK}$n/insert wait states for some resources. (Add one additional wait state for access by remote processor or alternate local bus master.)	
		1. Input or output data. 2. Assert $\overline{DSACK}$/insert wait states (some resources).
1. Complete bus cycles. (Alternate local bus master negates $\overline{BGACK}$; for a remote processor, the gate array negates $\overline{BGACK}$ and returns bus mastership to the local MPU.)		

Figure 4-3. Resource Access

4.3.3 Restrictions

Local bus access by a remote processor is limited to one bus cycle unless it is a read-modify-write (RMW) cycle.

NOTE

Only three 68020 instructions generate RMW cycles: TAS (Test-and-Set), CAS (Compare-and-Swap), and CAS2 (Compare-and-Swap 2).

Access by the alternate local bus master is not limited to a single bus cycle; it may maintain local bus mastership as long as Bus Grant Acknowledge ($\overline{BGACK}$) is asserted.

If the global master requests the local bus while an alternate local bus master has control, it is up to the alternate local bus master whether it will honor the bus request and relinquish control. If the alternate local bus master makes the global master wait more than 512 clock cycles, the watchdog timer of the global master will time out and generate a bus error forcing the global bus master to terminate its cycle.

4.3.4 Contention Resolution

Contention occurs when a Processor Module makes a global access at the same time the current global master requests a local bus access on that Processor Module. When this happens, retry or rerun operations are attempted by the contention resolver circuit in the gate array (U103).

4.3.4.1 Retry Operation. When a Processor Module makes a normal global access, that is, executing any instruction other than TAS, CAS, or CAS2, and, at the same time, the current global master requests a local bus access, the local 68020 MPU bus cycle is retried. The Bus Error ($\overline{BERR}$) and Halt ($\overline{HALT}$) signals of the Processor Module that is not the global bus master are asserted simultaneously to force the local 68020 to retry the instruction. This allows the global master to arbitrate for control of the local bus.

4.3.4.2 Global Rerun Operation. The retry operation is not adequate to resolve contention if the Processor Module that is not the global bus master is running a global access RMW cycle. Once the RMW cycle has started, the MPU can be halted or forced to retry; but it will not relinquish control of the local bus until the RMW cycle is completed, and the global master will not be able to gain control of the local bus. Therefore, the global master is forced to relinquish the global bus and let the Processor Module running the global RMW cycle control the global bus. This is accomplished by

asserting the Global Rerun ($\overline{GRRUN}$) signal, which causes the global master to retry. At the same time, the Processor Module running the RMW cycle "steals" global bus mastership.

NOTE

> If there are two Processor Modules running RMW cycles to each other's memory simultaneously, neither will relinquish local bus control, and a true deadlock will occur until the watchdog timers time out and bus errors are generated. This condition can be avoided if RMW operations are restricted to global memory.

4.4 LOCAL RESOURCES

The resources located on the Processor Module or on expansion modules are mapped into a Processor Module's 16 megabyte address space as shown in Figure 4-4. Local resources are described in the following subsections.

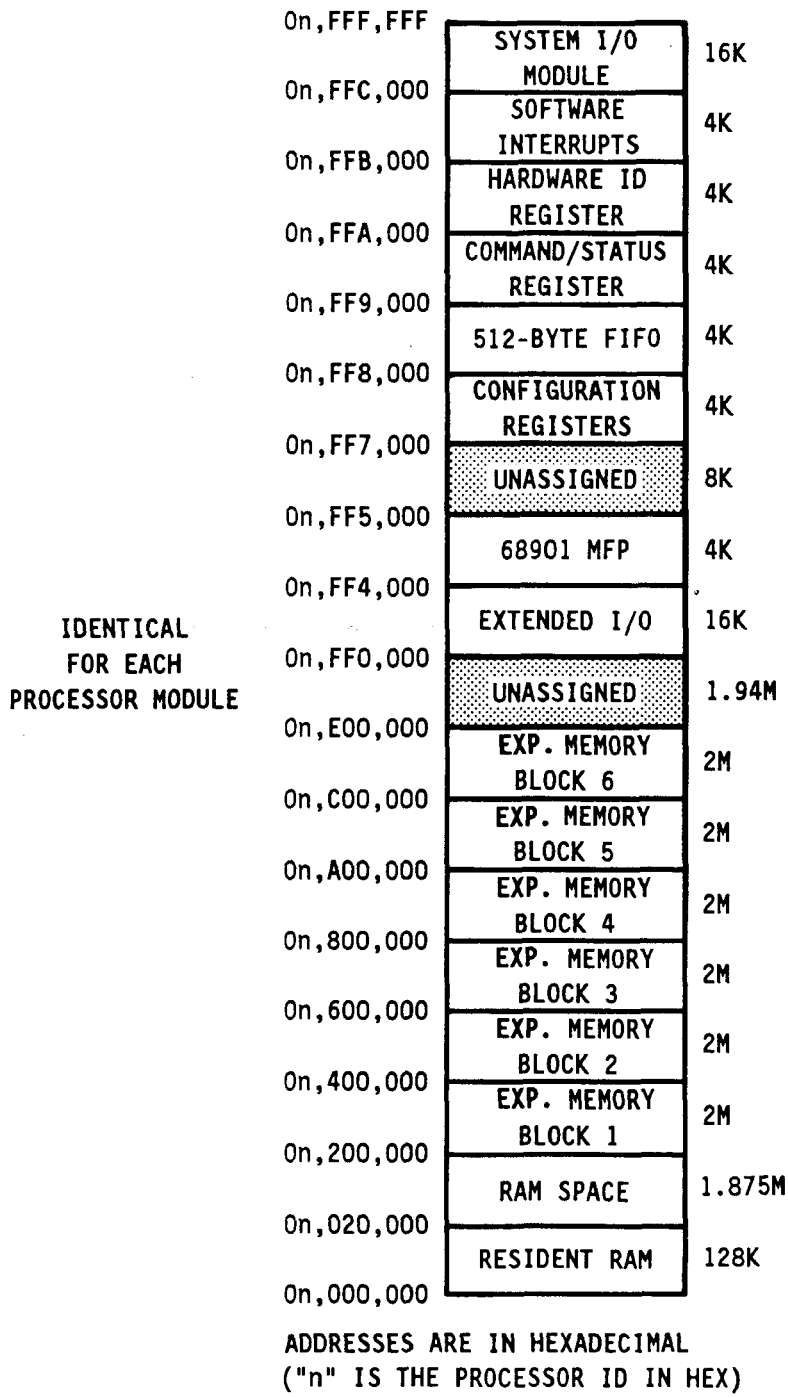


Figure 4-4. Local Resource Address Map

4.4.1 Hardware Identification (HWID) Register

The Hardware Identification (HWID) Register, located in the gate array (U103), is an 8-bit register that contains the revision level of the gate array VLSI and also reflects the setting of the hardware jumpers that form the Processor Module identification number (Processor ID or HWID). (Appendix B details the setting of these jumpers.) The four-bit ID, from 0001 (1) through 1111 (15), is unique for each Processor Module in SANDAC V. The ID defines a Processor Module's global address and also specifies the module's priority for global bus arbitration. The format of the HWID Register is shown below:

HWID Register

7	6	5	4	3	2	1	0
R3	R2	R1	R0	ID3	ID2	ID1	ID0

Address: On,FFA,000 (n = Processor ID in hex)
Access Level: Supervisor (Read-only)

Rn REVISION - The four-bit revison level of the gate array VLSI. R3 is the most-significant bit.

IDn IDENTIFICATION - The four-bit Processor ID (HWID) that defines a Processor Module's global address and also specifies the module's global bus arbitration priority as shown below:

ID3	ID2	ID1	ID0	HWID	Address Space (hex)	Priority
0	0	0	1	1	01,000,000-01,FFF,FFF	Lowest
0	0	1	0	2	02,000,000-02,FFF,FFF	.
0	0	1	1	3	03,000,000-03,FFF,FFF	.
0	1	0	0	4	04,000,000-04,FFF,FFF	.
0	1	0	1	5	05,000,000-05,FFF,FFF	.
0	1	1	0	6	06,000,000-06,FFF,FFF	.
0	1	1	1	7	07,000,000-07,FFF,FFF	.
1	0	0	0	8	08,000,000-08,FFF,FFF	.
1	0	0	1	9	09,000,000-09,FFF,FFF	.
1	0	1	0	10	0A,000,000-0A,FFF,FFF	.
1	0	1	1	11	0B,000,000-0B,FFF,FFF	.
1	1	0	0	12	0C,000,000-0C,FFF,FFF	.
1	1	0	1	13	0D,000,000-0D,FFF,FFF	.
1	1	1	0	14	0E,000,000-0E,FFF,FFF	.
1	1	1	1	15	0F,000,000-0F,FFF,FFF	Highest

4.4.2 Configuration Registers

The gate array (U103) contains a group of 15 registers known collectively as the configuration registers, which support the following functions:

- Bus arbitration
- Address monitoring
- Interrupt selection

Table 4-4 summarizes the configuration registers. Detailed descriptions of the bus arbitration and address monitor registers are given in the following subsections. The interrupt select registers are described in Subsections 4.5.2 and 4.5.3.

4.4.2.1 Bus Arbitration Mode Control. Half of CONFIG1 controls the two modes of global bus arbitration:

Priority Mode The Processor Module with the highest priority (highest ID) controls the bus for as long as it requests it.

Fair Mode After a Processor Module has been the bus master, it is prohibited from making another request until the bus has been free for at least one cycle. Therefore, when two or more modules contend for the bus, the highest priority module is served first, but it is prevented from acquiring the bus again until the lowest priority module has been allowed access.

The mode of bus arbitration is selected by the setting of bit 4 in CONFIG1. The format of the register is shown below:

CONFIG1

7	6	5	4	3	2	1	0
*	*	*	PRI	**			

*Not Used
**Used by Address Monitor

Address: On,FF7,001 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: Fair Mode (00 hex)

PRI PRIORITY - 1 = Priority mode; 0 = Fair mode.

TABLE 4-4. CONFIGURATION REGISTER SUMMARY

Register	Function	Address*
CONFIG1	Bus Arbitration: Mode select Address Monitor: Mode select	0n,FF7,001
CONFIG2	Address Monitor: Upper address most-significant byte	0n,FF7,002
CONFIG3	Address Monitor: Upper address middle byte	0n,FF7,003
CONFIG4	Address Monitor: Upper address least-significant byte	0n,FF7,004
CONFIG5	Address Monitor: Lower address most-significant byte	0n,FF7,005
CONFIG6	Address Monitor: Lower address middle byte	0n,FF7,006
CONFIG7	Address Monitor: Lower address least-significant byte	0n,FF7,007
CONFIG8	FIFO, 68901 interrupt priority select	0n,FF7,008
CONFIG9	Local Interrupt W, X priority select	0n,FF7,009
CONFIG10	Local Interrupt Y, Z priority select	0n,FF7,00A
CONFIG11	Global Interrupt W, X priority select	0n,FF7,00B
CONFIG12	Global Interrupt Y, Z input select	0n,FF7,00C
CONFIG13	Software Interrupt 0, 1 input select	0n,FF7,00D
CONFIG14	Software Interrupt 2, 3 input select	0n,FF7,00E
CONFIG15	Software Interrupt 4, 5 priority select	0n,FF7,00F

*Addresses are in hex; "n" is the Processor ID.

4.4.2.2 Address Monitor. Half of CONFIG1 and CONFIG2 through CONFIG7 form a programmable address monitor that covers the entire 16 megabytes of Processor Module address space. The address block and types of accesses to be monitored are specified by programming the configuration registers. When a specified access is detected, a bus error is signaled. A bit in the Command/Status Register (Subsection 4.4.5) indicates an address monitor bus error.

Access types are specified with CONFIG1. The format of this register is shown below:

CONFIG1

7	6	5	4	3	2	1	0
*	*	*	**	U	S	R	W

*Not Used
**Used for Arbitration Mode

Address: On,FF7,001 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: Monitor Disabled (00 hex)

U USER-LEVEL ACCESS - If this bit is set, the address monitor forces a bus error when a user-level access of the selected address block occurs. This bit can be set concurrently with the S bit.

S SUPERVISOR-LEVEL ACCESS - If this bit is set, the address monitor forces a bus error when a supervisor-level access of the selected address block occurs. This bit can be set concurrently with the U bit.

R READ ACCESS - If this bit is set, the address monitor forces a bus error when a read access of the selected address block occurs. This bit can be set concurrently with the W bit.

W WRITE ACCESS - If this bit is set, the address monitor forces a bus error when a write access of the selected address block occurs. This bit can be set concurrently with the R bit.

NOTE

The address monitor is disabled when R=0 and W=0 or when U=0 and S=0; this is the initial state for both bit pairs.

The boundaries of the address space to be monitored are set with CONFIG2 through CONFIG7. Three of the registers hold the 24 bits that specify the upper address, and three hold the 24 bits of the lower address. The formats of the address monitor boundary registers are shown below:

CONFIG2 (Upper Address Most-Significant Byte)

7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19	A18	A17	A16

Address: On,FF7,002 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG3 (Upper Address Middle Byte)

7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8

Address: On,FF7,003 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG4 (Upper Address Least-Significant Byte)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Address: On,FF7,004 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG5 (Lower Address Most-Significant Byte)

7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19	A18	A17	A16

Address: On,FF7,005 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

CONFIG6 (Lower Address Middle Byte)

7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8

Address: On,FF7,006 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

CONFIG7 (Lower Address Least-Significant Byte)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Address: On,FF7,007 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

4.4.3 RAM AND RAM SPACE

The first 512K bytes of Processor Module address space is reserved for RAM on the Processor Module. This space is divided into four 128K byte blocks. Only the first 128K byte block contains actual RAM (U104, U105, U106, U107). This RAM is 32 bits wide and is accessible at either the user or the supervisor level. The addresses for the 128K bytes of resident RAM are "aliased" in the other three 128K byte blocks; addresses issued to locations in these blocks access the corresponding location in the lower 128K byte block.

Directly above the four 128K byte blocks reserved for RAM is a 1.5 megabyte space that is reserved for future expansion. Any access of this area causes a bus error. Directly above this space are six blocks of 2 megabytes each reserved for Expansion Memory Modules (Section 7), which attach to the Processor Module. The size of the individual blocks corresponds to the storage capacity (2M bytes) of a single module. In configuring a system, as many as four of these modules can be attached to a Processor Module.

The following is a summary of Processor Module RAM space:

Address (hex)	Location	Implementation
0n,000,000-0n,01F,FFF	Processor Module	U104-U107
0n,020,000-0n,07F,FFF	Processor Module	RAM Alias (3 times)
0n,080,000-0n,1FF,FFF	Reserved	Reserved (Bus Error)
0n,200,000-0n,3FF,FFF	Expansion Bus	Expansion Memory Module
0n,400,000-0n,5FF,FFF	Expansion Bus	Expansion Memory Module
0n,600,000-0n,7FF,FFF	Expansion Bus	Expansion Memory Module
0n,800,000-0n,9FF,FFF	Expansion Bus	Expansion Memory Module
0n,A00,000-0n,BFF,FFF	Expansion Bus	Expansion Memory Module
0n,C00,000-0n,DFF,FFF	Expansion Bus	Expansion Memory Module

n = Processor ID in hex

4.4.4 512-Byte FIFO

The 512-byte first-in-first-out (FIFO) buffer, U120, is 8 bits wide (bit 9 is not used) and 512 locations deep. This 8-bit buffer is writable and readable at the supervisor level. Anytime the FIFO contains data, an interrupt request is generated by the gate array (U103).

Writing to the FIFO when it is full causes a bus error and the data are not written. If the local MPU is responsible for the write, a bit in the Command/Status Register (Subsection 4.4.5) is set to indicate the cause of the bus error. If a global bus master is

responsible for the write, the bit is not set, and there is no indication of the cause of the bus error. FIFO "empty" and "half-full" status is reflected by two bits in the Command/Status Register. A summary of FIFO access is given below:

Address: 0n,FF8,000 hex (n = Processor ID in hex)
Access level: Supervisor
Initial state: Indeterminate

4.4.5 Command/Status Register

The Command/Status Register, located in the gate array (U103), is a single register that serves two functions. When bits in the register are set with a write operation, commands are issued to the 68020 MPU (Command Register). When the register is read, various status conditions are returned (Status Register). The format of the register is shown below, separated into command and status functions:

Command Register

7	6	5	4	3	2	1	0
RST	HLT	TBE	ABE	FBE	CD	*	*

*No Command Function

Address: 0n,FF9,000 hex (n = Processor ID in hex)
Access Level: Supervisor (Write-only)
Initial State: 00 hex

RST RESET - When this bit is set, the local 68020 MPU is held in the reset state. It is removed from the reset state only when another device accesses (read or write, any location) its memory space after a minimum of 256 clock cycles has elapsed since the bit was set. An access prior to 256 clock cycles causes a bus error on the originating Processor Module. Once the MPU is removed from the reset state, it proceeds with the normal powerup reset sequence; thus, there is no need to clear this bit. The reset command implemented through this register is intended for software diagnostic purposes only.

HLT HALT - When this bit is set, the 68020 MPU enters the halted processing state. Another Processor Module must clear this bit to remove the MPU from the halted state.

TBE TIMEOUT BUS ERROR - Clearing this bit clears the corresponding TBE flag in the Status Register.

ABE ADDRESS MONITOR BUS ERROR - Clearing this bit clears the corresponding ABE flag in the Status Register.

FBE FIFO BUS ERROR - Clearing this bit clears the corresponding FBE flag in the Status Register.

CD CACHE DISABLE - Setting this bit disables the 68020 MPU internal instruction cache. This is a hardware disable and causes the cache to be bypassed regardless of the state of the 68020 Cache Control Register (CACR). Clearing the bit enables the cache, assuming that it is first enabled through the CACR.

Status Register

7	6	5	4	3	2	1	0
HTD	HLT	TBE	ABE	FBE	CD	FHF	FMT

Address: On,FF9,000 hex (n = Processor ID in hex)
Access Level: Supervisor (Read-only)
Initial State: 01 hex

HTD HALTED - When this bit is set, it indicates that the 68020 MPU is in the halted processing state. The MPU may have entered this state as a result of writing to the HLT bit in the Command Register or because of a double bus error. To determine the cause, the user should examine the HLT bit (see below). If HLT is set, then the HTD condition is the result of the Command Register; if HLT is cleared, the HTD condition is the result of a double bus error.

HLT HALT - This bit echoes the state of the HLT bit in the Command Register.

TBE TIMEOUT BUS ERROR - When this bit is set, it indicates that a bus error was caused because there was no response to an MPU address within 512 clock cycles. This flag is cleared by writing a 0 to the corresponding bit in the Command Register.

ABE ADDRESS MONITOR BUS ERROR - When this bit is set, it indicates that a bus error was caused by the address monitor (Subsection 4.4.2.2)

detecting an illegal memory access by the local MPU. An illegal access by a global bus master is not flagged. This flag is cleared by writing a 0 to the corresponding bit in the Command Register.

FBE FIFO BUS ERROR - When this bit is set, it indicates that a bus error was caused by the local MPU writing to the FIFO when it was full. A write-when-full by a global bus master is not flagged. This flag is cleared by writing a 0 to the corresponding bit in the Command Register.

CD CACHE DISABLE - This bit echoes the state of the CD bit in the Command Register.

FHF FIFO HALF FULL - When this bit is set, it indicates that the 512-byte FIFO (Subsection 4.4.4) contains at least 257 bytes.

FMT FIFO EMPTY - When this bit is set, it indicates that the 512-byte FIFO (Subsection 4.4.4) is empty.

4.4.6 68901 MFP

The 68901 Multi-Function Peripheral (MFP), U131, is a Motorola 68000-family device that provides the following resources for MPU support:

- 4 timers (Timers A, B, C, D)
- 1 Universal Synchronous/Asynchronous Receiver-Transmitter (USART)
- 8 programmable I/O lines with interrupt capability
- 1 16-source interrupt controller

On the Processor Module, these resources are utilized as follows:

- Timers A and B are general purpose
- USART and Timers C and D form the global serial bus interface
- 8 I/O lines are used as inputs to the interrupt controller
- Interrupt controller handles as many as 16 requests for the module's programmable interrupt system (Subsection 4.5)

These resources are described in the following paragraphs. Complete information on the 68901 MFP is in the Motorola publication, *MC68901 Multi-Function Peripheral.*

4.4.6.1 General-Purpose Timers. Only two of the four timers in the 68901, Timers A and B, are available for general-purpose use. The hardware configuration of the timers on the Processor Module is shown in Figure 4-5. Each timer is an 8-bit prescaler/counter type. As shown, the timers are interconnected to form a single 16-bit timer. Timer A can also function independently as an 8-bit timer. The input clock frequency at Timer A is 2.4576 MHz.

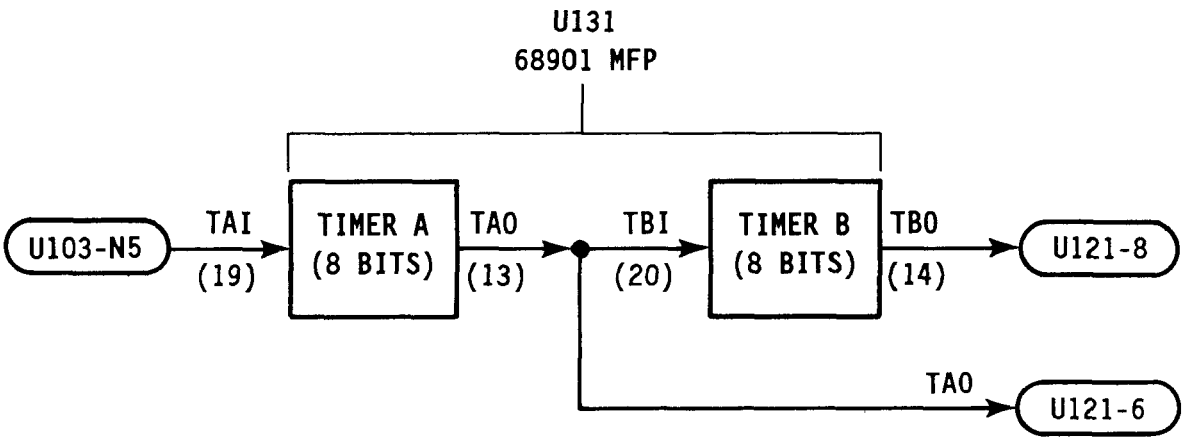


Figure 4-5. General-Purpose Timer Hardware Configuration

4.4.6.2 Global Serial Bus Interface. The global serial bus interface is implemented with the 68901 USART and Timers C and D, which are hardwired to supply the USART receive and transmit clocks, respectively. A block diagram of the interface is shown in Figure 4-6.

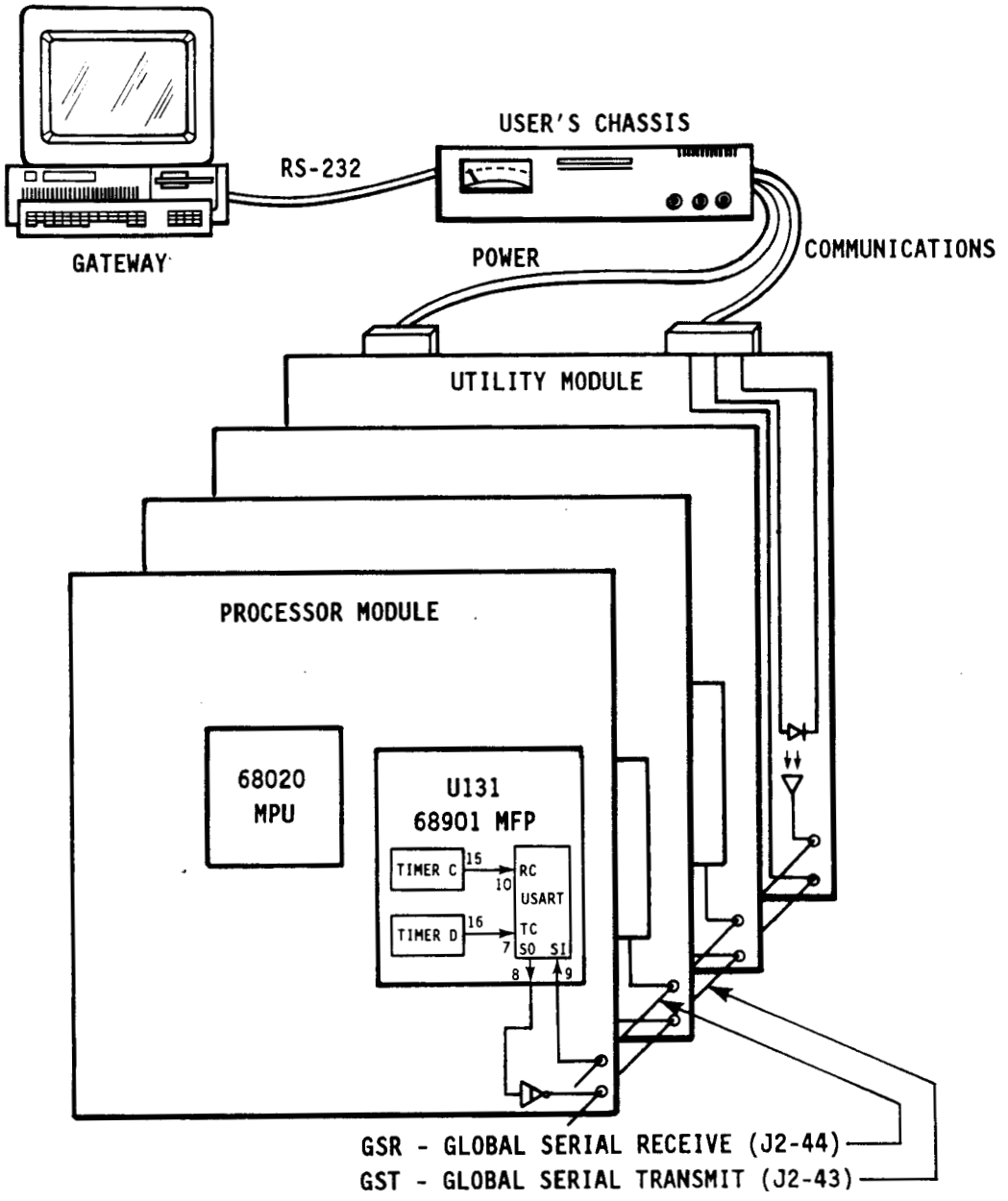


Figure 4-6. Global Serial Bus Interface

4.4.6.3 Programmable I/O Lines. The eight programmable I/O lines are used only to connect external interrupt requests to the 68901 interrupt controller and therefore cannot be used for general-purpose I/O operations.

4.4.6.4 Interrupt Controller. The 68901 interrupt controller has 16 prioritized channels for handling interrupt requests. The requests are generated by sources internal to the 68901 and by external sources. The internal sources include the 68901 timers and USART. The external sources are routed to the controller on the eight programmable I/O lines, I0 through I7, and the Timer A external input, TAI.

The 16 interrupt controller channels are prioritized. The channel assignments for the interrupt controller and their priorities are as follows:

Channel	Interrupt Request	Priority
1111	Input 7 (I7)	Highest
1110	Input 6 (I6)	.
1101	Timer A	.
1100	USART (receive buffer full)	.
1011	USART (receiver error)	.
1010	USART (transmit buffer empty)	.
1001	USART (transmitter error)	.
1000	Timer B	.
0111	Input 5 (I5)	.
0110	Input 4 (I4)	.
0101	Timer C	.
0100	Timer D	.
0011	Input 3 (I3)	.
0010	Input 2 (I2)	.
0001	Input 1 (I1)	.
0000	Input 0 (I0)	Lowest

When interrupt requests are presented to the interrupt controller, the controller responds to the highest priority source first and causes the 68901 to generate a single vectored interrupt request. During the 68020 interrupt acknowledge cycle, the 68901 furnishes an interrupt vector with the format shown below:

68901 Interrupt Vector Format

7	6	5	4	3	2	1	0
V3	V2	V1	V0	CH3	CH2	CH1	CH0

Vn VECTOR - The four bits in this field are copied from the 68901 Vector Register (VR). The bits are loaded into the VR when the 68901 is initialized to designate the interrupt vector the device will use.

CHn CHANNEL - The four bits in this field designate the interrupt controller channel that made the interrupt request.

4.5 INTERRUPT SYSTEM

The Processor Module interrupt system serves the following functions:

- Selecting and prioritizing interrupt requests to the resident 68020 MPU
- Generating interrupt requests to other Processor Modules

A block diagram of the interrupt system is shown in Figure 4-7. The operation of the system is described in the following paragraphs.

4.5.1 Interrupts to the 68020

The following are sources of interrupt requests to the resident 68020 MPU:

- 512-byte FIFO
- Local expansion bus interrupt W, X, Y, or Z
- Global bus interrupt W, X, Y, or Z
- Software interrupts
- 68901 MFP

As shown in Figure 4-7, some of the sources present their requests to the input of a programmable 10×7 crossbar switch. The switch is controlled by configuration registers CONFIG8 through CONFIG11 and CONFIG15. These registers are user programmable and assign a 68020 interrupt priority level to the requests.

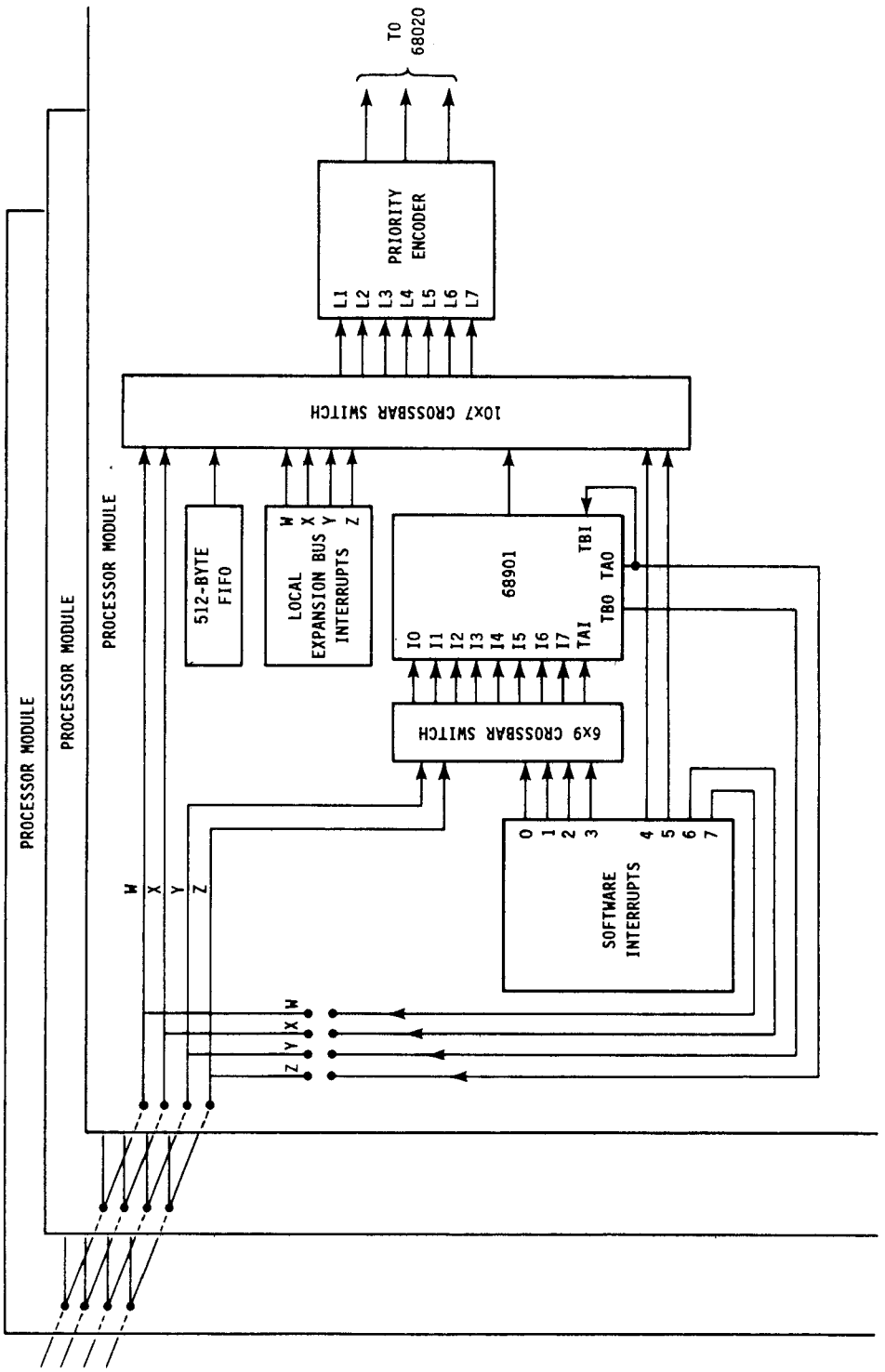


Figure 4-7. Processor Module Interrupt System

The interrupt sources that are not presented to the 10×7 crossbar switch are presented to a 6×9 crossbar switch that is controlled by configuration registers CONFIG12 through CONFIG14. These registers are user programmable and connect the interrupt sources to the external inputs of the 68901 interrupt controller. Interrupt requests generated by these sources are presented to the 10×7 crossbar switch as the composite 68901 interrupt request.

A description of the interrupt sources and the associated crossbar switches follows.

4.5.1.1 512-Byte FIFO Interrupt. The 512-byte FIFO (Subsection 4.4.4), U120, generates an interrupt request whenever it contains data. This interrupt request is directed to the 10×7 crossbar switch.

4.5.1.2 Local Expansion Bus Interrupts. The local expansion bus includes four interrupt request lines that send requests from expansion modules to the Processor Module as shown below:

$\overline{\text{EIRQW}}$	J4-54
$\overline{\text{EIRQX}}$	J4-55
$\overline{\text{EIRQY}}$	J4-56
$\overline{\text{EIRQZ}}$	J4-57

Interrupt requests are directed to the 10×7 crossbar switch.

4.5.1.3 Global Bus Interrupts. The global bus includes four interrupt request lines that send interrupt requests from one Processor Module to another as shown below:

$\overline{\text{GIRQW}}$	J1-37
$\overline{\text{GIRQX}}$	J1-38
$\overline{\text{GIRQY}}$	J1-39
$\overline{\text{GIRQZ}}$	J1-40

Interrupts W and X are directed to the 10×7 crossbar switch; interrupts Y and Z are routed to the 6×9 crossbar switch.

4.5.1.4 Software Interrupts. Eight separate interrupt requests can be generated by writing to eight addresses in Processor Module address space. The write operation itself, to the designated address and with any data pattern, generates the interrupt request under gate array control; there are no registers or control bits associated with this function. The write addresses for generating software interrupts are as follows:

Software Interrupt	Address (hex)
0	0n,FFB,000
1	0n,FFB,001
2	0n,FFB,002
3	0n,FFB,003
4	0n,FFB,004
5	0n,FFB,005
6	0n,FFB,006
7	0n,FFB,007

n = Processor ID in hex
Access at these addresses is supervisor level.

Software interrupts 0 through 3 are routed to the 6×9 crossbar switch; interrupts 4 and 5 are directed to the 10×7 crossbar switch. Software interrupts 6 and 7 generate interrupt requests that can be connected to the global interrupt request lines (refer to Subsection 4.5.4).

4.5.1.5 68901 Interrupt. The 68901 MFP generates a single interrupt request from its internal interrupt controller. The request is initially generated by 1 of the 16 sources monitored by the controller. These sources include those internal to the 68901 and external sources. The internal sources include the following:

- Timer A, B, C, D
- USART (receive buffer full)
- USART (receiver error)
- USART (transmit buffer empty)
- USART (transmitter error)

The external sources are directed to the controller on the eight programmable I/O lines, I0 through I7, and the Timer A external input, TAI. External requests can be received from the following sources:

- Global bus interrupt Y ($\overline{GIRQY}$)
- Global bus interrupt Z ($\overline{GIRQZ}$)
- Software interrupt 0
- Software interrupt 1
- Software interrupt 2
- Software interrupt 3

External requests are initially presented to the input of a programmable 6×9 crossbar switch that is controlled by configuration registers CONFIG12 through CONFIG14 described in the following subsection.

4.5.2 6×9 Crossbar

The 6×9 crossbar, controlled by configuration registers CONFIG12 through CONFIG14, connect a specific source to a specific I/O line based on application requirements. The format of the registers is shown below:

CONFIG12 (6x9 Global Bus Y, Z Input Select)

7	6	5	4	3	2	1	0
IL3	IL2	IL1	IL0	IL3	IL2	IL1	IL0
Global Bus Y				Global Bus Z			

Address: On,FF7,00C hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

CONFIG13 (6x9 Software Interrupt 0, 1 Select)

7	6	5	4	3	2	1	0
IL3	IL2	IL1	IL0	IL3	IL2	IL1	IL0
Software Int. 0				Software Int. 1			

Address: On,FF7,00D hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

CONFIG14 (6x9 Software Interrupt 2, 3 Select)

7	6	5	4	3	2	1	0
IL3	IL2	IL1	IL0	IL3	IL2	IL1	IL0
Software Int. 2				Software Int. 3			

Address: On,FF7,00E hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: FF hex

ILn INPUT LINE - These bits select the 68901 external input line as shown below:

IL3	IL2	IL1	IL0	68901 External Input
0	0	0	0	I0
0	0	0	1	I1
0	0	1	0	I2
0	0	1	1	I3
0	1	0	0	I4
0	1	0	1	I5
0	1	1	0	I6
0	1	1	1	I7
1	0	0	0	TAI
1	0	0	1	Source not selected
1	0	1	0	.
1	0	1	1	.
1	1	0	0	.
1	1	0	1	.
1	1	1	0	.
1	1	1	1	Source not selected

4.5.3 10×7 Crossbar

As shown in Figure 4-7, the following interrupt requests are presented to the 10x7 crossbar switch:

- 512-byte FIFO
- Local expansion bus interrupts W, X, Y, Z
- Global bus interrupts W and X
- Software interrupts 4 and 5
- 68901 MFP

The 68020 interrupt priority level (IPL) for each source is programmed with CONFIG8 through CONFIG11 and CONFIG15. When a request is received, the registers output the programmed priority to an encoder that places the level on the 68020 IPL lines. The format of the registers is shown below:

CONFIG8 (10x7 FIFO/68901 IPL)

7	6	5	4	3	2	1	0
*	PL2	PL1	PL0	*	PL2	PL1	PL0
FIFO				68901			

*Not Used

Address: On,FF7,008 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG9 (10x7 Local Expansion Bus W, X IPL)

7	6	5	4	3	2	1	0
*	PL2	PL1	PL0	*	PL2	PL1	PL0
Local Exp. W				Local Exp. X			

*Not Used

Address: On,FF7,009 hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG10 (10x7 Local Expansion Bus Y, Z IPL)

7	6	5	4	3	2	1	0
*	PL2	PL1	PL0	*	PL2	PL1	P10
Local Exp. Y				Local Exp. Z			

*Not Used

Address: On,FF7,00A hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG11 (10x7 Global Bus W, X IPL)

7	6	5	4	3	2	1	0
*	PL2	PL1	PL0	*	PL2	PL1	PL0
Global Bus W				Global Bus X			

*Not Used

Address: On,FF7,00B hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

CONFIG15 (10x7 Software Interrupts 4, 5 IPL)

7	6	5	4	3	2	1	0
*	PL2	PL1	PL0	*	PL2	PL1	PL0
Software Int. 4				Software Int. 5			

*Not Used

Address: On,FF7,00F hex (n = Processor ID in hex)
Access Level: Supervisor
Initial State: 00 hex

PLn PRIORITY LEVEL - These bits specify the interrupt priority level as shown below:

PL2	PL1	PL0	Interrupt Priority Level
0	0	0	Not Selected
0	0	1	1 (Lowest)
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (Highest)

4.5.4 Processor Module Interrupts

A Processor Module can send interrupt requests to other Processor Modules with the global bus interrupt request lines. The following resources can generate requests:

- Software Interrupt 6
- Software Interrupt 7
- Timer A External Timeout (TAO)
- Timer B External Timeout (TBO)

Any one of the interrupt sources can be connected to any one of the global interrupt request lines with a hardware jumper (refer to Appendix B).

4.6 LOCAL EXPANSION BUS INTERFACE

The local expansion bus interface allows the addition of one or more of the following modules to a Processor Module's local bus:

- Expansion Memory Module (Section 7)
- System I/O Module (Section 8)
- MIL-STD-1553B Module (Section 9)

A maximum of four modules can be attached to one Processor Module. Module types can be combined, but the interface supports only the following quantities:

- 1 System I/O Module
- As many as 4 Expansion Memory Modules
- As many as 4 MIL-STD-1553B Modules

These modules are mapped into Processor Module address space as shown below:

Address (hex)	Assignment
0n,200,000-0n,3FF,FFF	Expansion Memory Module 1
0n,400,000-0n,5FF,FFF	Expansion Memory Module 2
0n,600,000-0n,7FF,FFF	Expansion Memory Module 3
0n,800,000-0n,9FF,FFF	Expansion Memory Module 4
0n,A00,000-0n,BFF,FFF	Expansion Memory Module 5
0n,C00,000-0n,DFF,FFF	Expansion Memory Module 6
0n,FF0,000-0n,FF3,FFF	Expansion I/O (MIL-STD-1553B Module)
0n,FF5,000-0n,FF6,FFF	Unassigned
0n,FFC,000-0n,FFF,FFF	System I/O Module

n = Processor ID in hex

NOTES

5. UTILITY MODULE

5.1 GENERAL DESCRIPTION

A SANDAC V system requires one Utility Module, which provides the following:

- Power
- Clocks
- Global Bus Termination
- Global Serial Bus Interface
- Global Resources:
  - 256K Bytes of EPROM
  - 128K Bytes of RAM
  - 32-bit timer
  - Status Register

A block diagram of the Utility Module is shown in Figure 5-1. A functional description of the module is given in the following subsections.

NOTE

The circuit diagram of the Utility Module is Sandia National Laboratories schematic CK-S64651. All references to component numbers and signals in the following text are from this drawing.

5.2 POWER SYSTEM

The Utility Module power system consists of the following parts:

- Power connector
- Regulator circuit
- Reset/power monitor circuit
- RAM backup power (PRAM) circuit

Descriptions of the major parts are given in the following subsections.

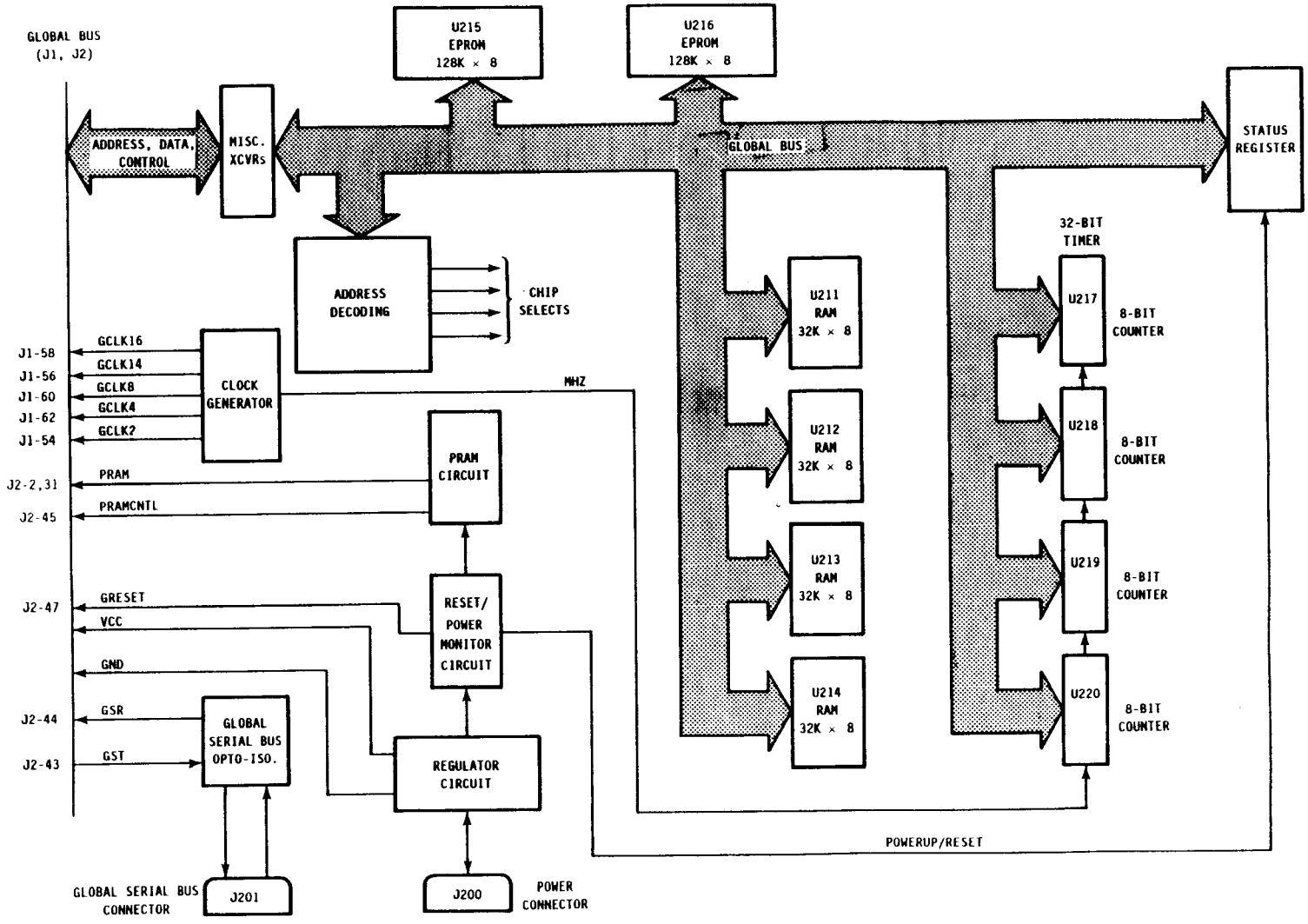


Figure 5-1. Utility Module Block Diagram

5.2.1 Power Connector

The power connector brings primary and secondary power into SANDAC V and also provides pins for other input and output functions. SANDAC V requires a primary power input of 8 to 12 Vdc. A secondary battery power source can be connected to the power connector to provide backup power for RAM and RAM control logic when the primary source is low or off.

The pin-out of the power connector (J200) is shown in Figure 5-2. Pin descriptions are given in Table 5-1.

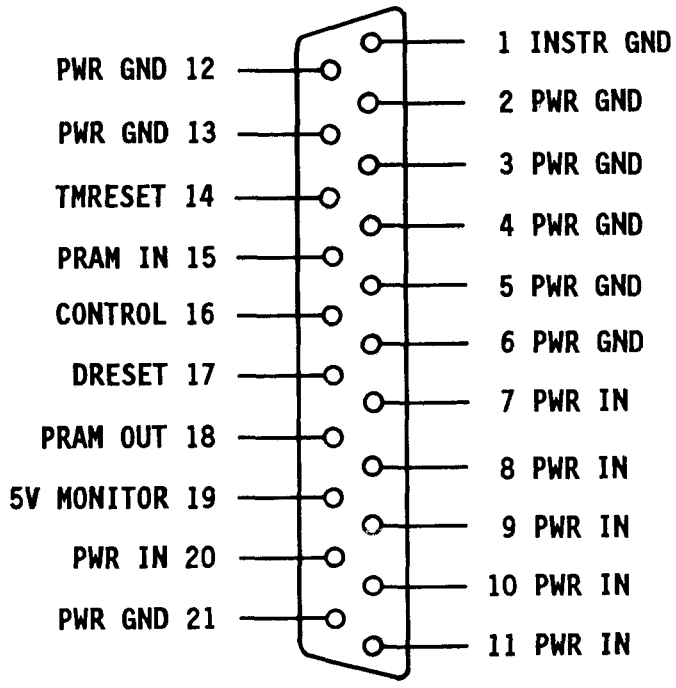


Figure 5-2. Power Connector (J200)

TABLE 5-1. POWER CONNECTOR (J200) PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	INSTR GND	Instrument Ground - Reserved as ground for external test equipment; electrically the same as PWR GND.
2	PWR GND	Power Ground - Ground for external power supplies, e.g., negative rail for PWR IN, PRAM IN, and PRAM OUT.
3	PWR GND	
4	PWR GND	
5	PWR GND	
6	PWR GND	
7	PWR IN	Power In - External power supply, +8 to +12 Vdc.
8	PWR IN	
9	PWR IN	
10	PWR IN	
11	PWR IN	
12	PWR GND	Power Ground - Ground for external power supplies, e.g., negative rail for PWR IN, PRAM IN, and PRAM OUT.
13	PWR GND	
14	$\overline{\text{TMRESET}}$	Telemetry Reset (active low, open collector) - Provides a 500 millisecond (minimum) active-low pulse when Utility Module detects low power or reset condition. (External logic must provide pull-up resistor.)
15	PRAM IN	RAM Primary Backup Power In - Positive rail of nonrechargeable battery (+3.7 to +5.7 Vdc) for RAM backup power.
16	CONTROL	Regulator Output Control - Input to Utility Module voltage regulator adjustment. This input is used during testing and qualification of the module. The function is then disabled by removing the Utility Module CNT jumper.

TABLE 5-1. CONTINUED

Pin	Mnemonic	Description
17	$\overline{\text{DRESET}}$	External Reset (active low) - Input to Utility Module reset/power monitor control circuit. This input is used during testing and qualification of the module. The function is then disabled by removing the Utility Module RST jumper.
18	PRAM OUT	Power Monitor/Secondary Power In - Monitor point for the PRAM voltage. If secondary (rechargeable) battery (+3 to +5 Vdc) is used for backup power, this is the positive rail input and the recharge line.
19	5V MONITOR	Regulator Power Monitor - Monitor point for Utility Module voltage regulator output.
20	PWR IN	Power In - External power supply, +8 to +12 Vdc.
21	PWR GND	Power Ground - Ground for external power supplies, e.g., negative rail for PWR IN, PRAM IN, and PRAM OUT.

5.2.2 Regulator Circuit

The regulator circuit converts external dc power supplied through the power connector (J200) to regulated +5-Volt power (Vcc). The primary component of the regulator is a National Semiconductor LM196K +5-Volt, 10-Amp regulator, VR21. The output of the regulator goes to all components on the Utility Module and is sent out on the global bus to provide power for all modules in the system.

NOTE

The external voltage that supplies the positive rail of the regulator also goes to the global bus as PWRIN (J2-42). None of the currently defined SANDAC V modules use PWRIN, but it is available for possible use on future or custom modules.

5.2.2.1 Adjustment. The output of the regulator circuit is adjustable with trimpot R230 on the Utility Module.

CAUTION

A short across R230 can raise the regulated voltage above 6 Volts. Any adjustment should be performed only by a qualified technician.

5.2.2.2 External Adjustment. The output of the regulator circuit can also be adjusted with a variable dc voltage at J200-16, the CONTROL input. Before external adjustment is possible, the Utility Module CNT hardware jumper must be installed. With the jumper installed, a nominal input voltage of 3.40 to 4.20 Volts varies the regulator output from a minimum of 4.7 to a maximum of 5.4 Volts.

CAUTION

Jumper installation and voltage adjustment should be performed only by a qualified technician.

5.2.3 Reset/Power Monitor Circuit

The reset/power monitor circuit performs the following functions:

- Generates system-wide reset signal at powerup
- Sets the RST bit of the Utility Module status register (5.5.6)
- Resets the Utility Module 32-bit timer (5.5.5)
- Detects low voltage conditions and switches backup power to volatile components

The primary components of the reset/power monitor circuit are U229, a quad op amp, and U223, a dual binary counter. Operational details are given in the following subsections.

5.2.3.1 Powerup Reset. When power is applied to SANDAC V, comparator A in U229 compares the regulator output to the trip-on reference voltage, nominally set at 4.7 Volts. When the regulator voltage goes above 4.7 Volts the following signals are asserted:

- $\overline{\text{GRESET}}$
- RESET
- GRAMPROT
- BDPROT
- $\overline{\text{TMRESET}}$

These signals function as described in Table 5-2.

NOTE

From 4.5 to 4.7 Volts, the above signals are asserted constantly. Below 4.5 Volts, only GRAMPROT and BDPROT are asserted. The other signals are unknown because TTL logic is not guaranteed to function below 4.5 Volts.

TABLE 5-2. POWERUP RESET SIGNALS

Signal	Output	Description
$\overline{\text{GRESET}}$	(U233-10)	Global Reset (active low) - Asserted for 576 ± 4 cycles of the 16 MHz clock. Signal is driven onto the global bus (J2-47) to reset Processor Modules and other system devices.
RESET	(U231-8)	Reset - Asserted for 576 ± 4 cycles of the 16 MHz clock. Supplied to Utility Module Status Register (5.5.6) to signal the reset event.
GRAMPROT	(U230-3)	Global RAM Protect - Asserted until $\overline{\text{GRESET}}$ is negated. Signal is driven onto the global bus (J2-41) to deselect RAM devices during the reset. If backup power is available, this signal is always valid throughout powerup and power down.
BDPROT	(U230-6)	Board Protect - Asserted until $\overline{\text{GRESET}}$ is negated. Deselects Utility Module RAM during the reset event. If backup power is available, this signal is always valid throughout powerup and power down.
$\overline{\text{TMRESET}}$	(U233-4)	Telemetry Reset (active low) - Asserted for 500 milliseconds (minimum) and driven out the power connector (J200-14). Allows external devices to register the reset event. $\overline{\text{TMRESET}}$ is a TTL-level, open-collector signal; the external device must supply the pull-up resistor that is compatible with TTL logic.

5.2.3.2 Low Power Conditions. When the regulator output falls below the low reference voltage of 4.6 Vdc (sensed at U229-A), the reset/power monitor circuit asserts the following signals:

- GRAMPROT and BDPROT
- $\overline{\text{GRESET}}$ and RESET
- $\overline{\text{TMRESET}}$

GRAMPROT and BDPROT deselect system RAM so that the contents of RAM are not disturbed when voltage falls below the operating value. $\overline{\text{GRESET}}$ is driven on the global bus (J2-47) to reset all system modules; RESET is supplied to the Utility Module status register (5.5.6) to indicate that the reset was caused by a low power condition. $\overline{\text{TMRESET}}$ is driven out the power connector (J200-14) so that external devices can register the reset event.

5.2.3.3 External Reset. SANDAC V can be reset externally with a low-active signal through the power connector at J200-17 ($\overline{\text{DRESET}}$). Before external reset is possible, the Utility Module RST hardware jumper must be installed. With the jumper installed, a TTL logic 0 input causes SANDAC V to reset and remain reset until the input goes to a TTL logic 1. When the input transitions from 0 to 1, $\overline{\text{GRESET}}$, RESET, GRAMPROT, BDPROT, and $\overline{\text{TMRESET}}$ are asserted as described in Table 5-2.

5.2.4 PRAM Circuit

The power-for-RAM or PRAM circuit supplies Vcc to RAM and its control logic when the primary 5-Volt supply is functioning. When primary power is low, the PRAM circuit switches in battery backup power provided through the power connector (J200).

The PRAM circuit monitors the BDPROT signal at Q204. When Vcc is available, BDPROT is negated and Q202 shorts Vcc to the PRAM line. During a reset or when power is low, BDPROT is asserted, causing Vcc to disconnect from the PRAM line. PRAM is then supplied with battery backup power through the power connector.

Either nonrechargeable or rechargeable batteries can supply backup power. Nonrechargeable batteries supply 3.7 to 5.7 Vdc through the power connector as PRAM IN (J200-15). At the cathode of CR27, this becomes PRAM. CR27 prevents current flow from Vcc to the nonrechargeable batteries during normal operation.

Rechargeable batteries supply 3.0 to 5.0 Vdc through the power connector as PRAM OUT (J200-18). On the other side of two series resistors, R226 and R249, this becomes PRAM. When rechargeable batteries are used and the system is operating normally with Vcc, PRAM OUT is the recharge path, and trimpot R249 amd resistor R226 are current-limiting resistors. R226 is 4.6Ω.

The value of R249 determines the recharge current as shown in the following example:

Three 1.25-Volt Ni-Cad batteries in series are used for backup power and the recharge current required is 50 milliamps (mA)

$$R249 + R226 = (5V - 3.75V)/50mA$$

or

$$R249 + R226 = 25\Omega$$

R249 must be set at approximately 20Ω.

5.3 CLOCK GENERATOR

The clock generator uses a 32-MHz oscillator (U227) and a 14.7456-MHz oscillator (U226) to produce all system clock signals. The output of the 32-MHz oscillator is divided by a synchronous counter to provide clocks for all processor-related circuits. The 14.7456-MHz oscillator provides the baud rate clock for the System I/O Module 68562 Dual Universal Synchronous Communications Controller (DUSCC) devices and is divided by six to 2.458-MHz to provide clocks for Processor Module and System I/O Module 68901 Multi-Function Peripheral (MFP) devices. Descriptions of the clock generator outputs are in Table 5-3.

The clock generator also provides local 16-MHz, 4-MHz, and 1-MHz clocks all derived from the 32-MHz oscillator. These clocks drive the wait state generator, reset counter, and 32-bit timer, respectively.

TABLE 5-3. CLOCK GENERATOR OUTPUTS

Signal	Output	Description
GCLK14	(U228-12)	Global Clock 14.7456 MHz - Driven on the global bus (J2-62) to provide the baud rate clock for System I/O Module 68562 DUSCC devices.
GCLK2	(U228-10)	Global Clock 2.458 MHz - Derived by dividing the 14.7456 MHz oscillator output by 6. Driven on the global bus (J1-54) to provide clocks for Processor Module and System I/O Module 68901 MFP devices.
GCLK16	(U228-2)	Global Clock 16 MHz - Derived by dividing the 32 MHz oscillator output by 2. Driven on the global bus (J1-58) to provide clocks for processors (MPUs), coprocessors, and associated circuits.
GCLK8	(U228-4)	Global Clock 8 MHz - Derived by dividing the 32 MHz oscillator output by 4. Driven on the global bus (J1-60) to provide clocks for various circuits.
GCLK4	(U228-6)	Global Clock 4 MHz - Derived by dividing the 32 MHz oscillator output by 8. Driven on the global bus (J1-62) to provide clocks for various circuits.

5.4 GLOBAL SERIAL BUS INTERFACE

The global serial bus consists of the global serial transmit line (GST) and the global serial receive line (GSR). GST and GSR run to the 68901 MFPs on all Processor Modules. The serial outputs (SO) of all the 68901s are wire-ORed to the transmit line. All 68901 serial inputs (SI) are directly connected to the receive line. The transmit and receive lines run along the SANDAC V global bus and terminate on the Utility Module at the global serial bus connector J201. The Utility Module provides the pull-up and current limiting resistors for transmit line and optical isolation and buffering for the receive line. The global serial bus interface is shown in Figure 5-3.

Normally, a Gateway terminal is connected to the global serial bus interface. Data sent from the Gateway and received by SANDAC V enter at J201-1 (J201-15 is signal return) and are driven on GSR by opto-isolator U249. When one of the Processor Modules on the bus has data to transmit to the Gateway, the module drives data on GST. These transmit data leave SANDAC V at J201-8 (J201-9 is signal return).

NOTE

Throughout SANDAC V, all received signals require optical isolation and all transmitters must provide a signal return. Thus, all serial channels will have four wires: a "+" and "-" for the receiver optical isolator and "signal" and "signal return" for the transmitter.

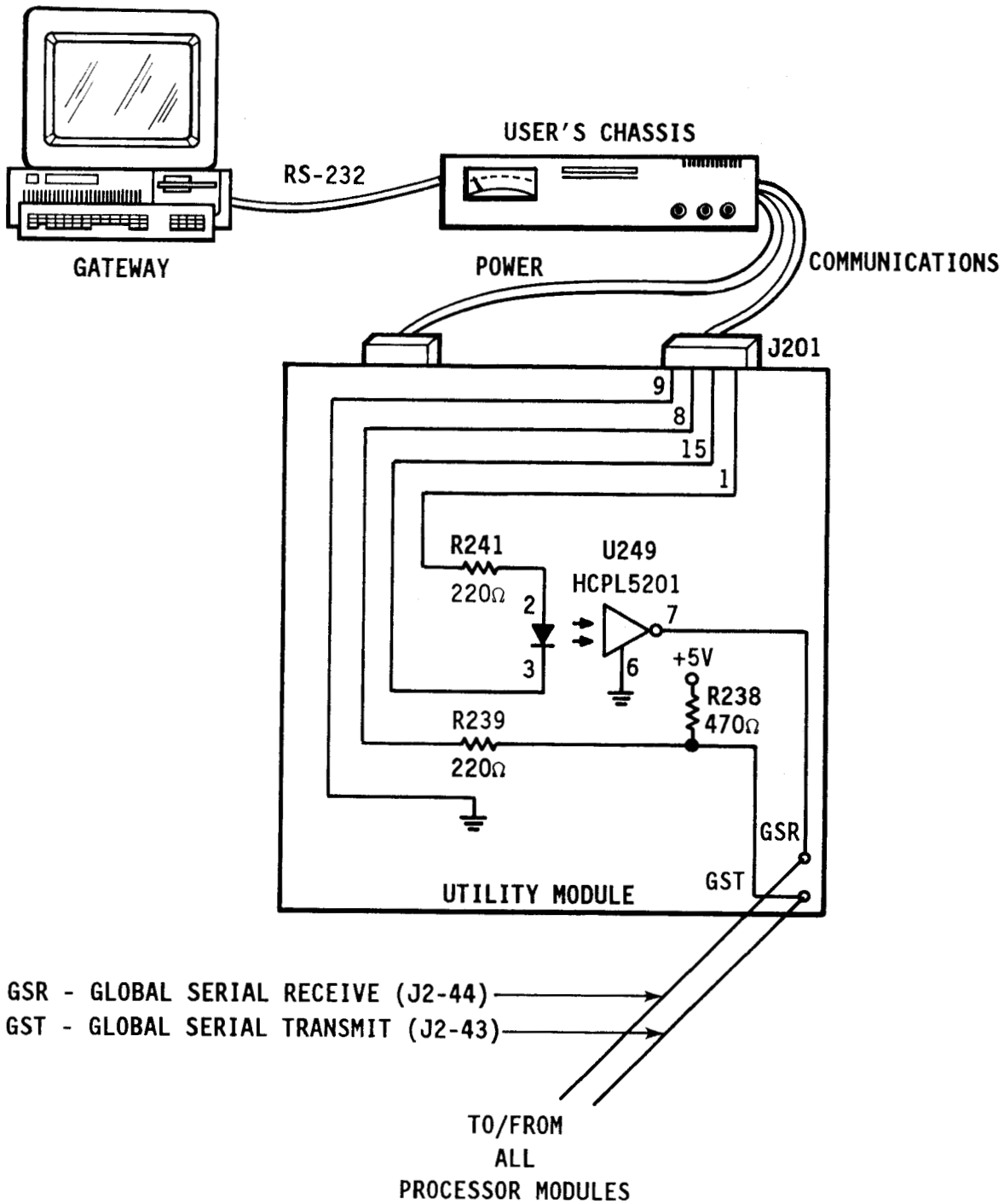


Figure 5-3. Global Serial Bus Interface

5.4.1 Global Serial Bus Connector

In addition to the global serial bus transmit and receive lines, the global serial bus interface connector (J201) provides other outputs that can be used to monitor SANDAC V operation. The pin-out of the connector is shown in Figure 5-4. Connector signals are described in Table 5-4.

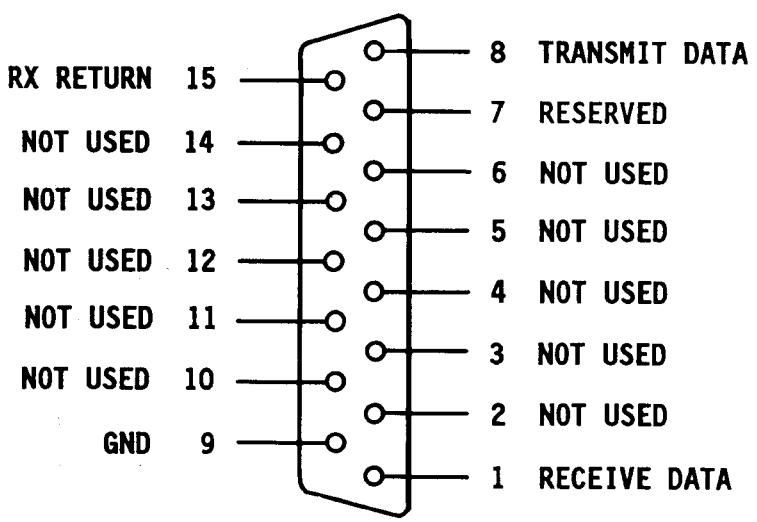


Figure 5-4. Global Serial Bus Connector (J201)

TABLE 5-4. GLOBAL SERIAL BUS CONNECTOR (J201) PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	GSR	Global Serial Bus Receive Data - Serial data from Gateway to SANDAC V. Signal return is J201-15.
2	-	Not Connected.
3	-	
4	-	
5	-	
6	-	
7	Reserved	Do Not Connect.
8	GST	Global Serial Bus Transmit Data - Wire-OR output of all transmitters on the global serial bus. Signal return is J201-9.
9	GND	Dc power return and signal ground
10	-	Not Connected.
11	-	
12	-	
13	-	
14	-	
15	RX RET	Signal Return - Signal return for J201-1 input.

5.5 GLOBAL RESOURCES

The Utility Module provides the following global resources:

- 256K Bytes of EPROM
- 128K Bytes of RAM
- 32-Bit, Microsecond-Resolution Timer
- Status Register

These resources are located in the SANDAC V memory map as shown in Figure 5-5.

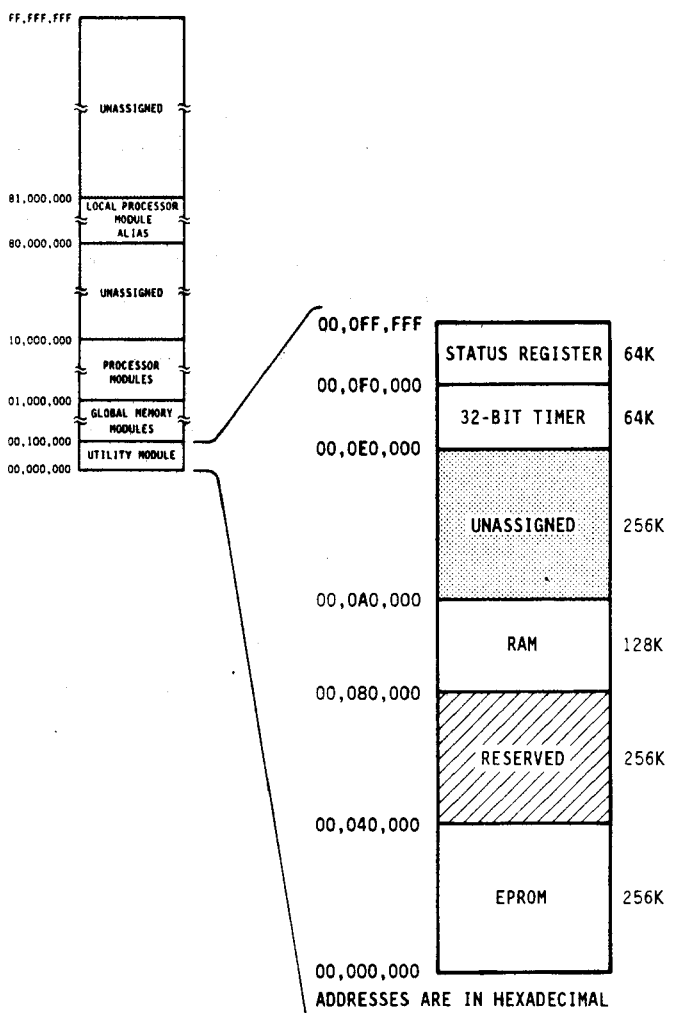


Figure 5-5. Utility Module Memory Map

5.5.1 Address Decoding

Utility Module addressing is summarized in Table 5-5.

TABLE 5-5. UTILITY MODULE ADDRESSES

Assignment (Bytes)	Start Address*	End Address*
EPROM (256K)	00,000,000	00,03F,FFF
Reserved (256K)	00,040,000	00,07F,FFF
RAM (128K)	00,080,000	00,09F,FFF
Unassigned (256K)	00,0A0,000	00,0DF,FFF
32-Bit Timer (64K)	00,0E0,000	00,0EF,FFF
Status Register (64K)	00,0F0,000	00,0FF,FFF

*Addresses are in hexadecimal.

Decoding of addresses issued for Utility Module resources is handled by the following devices:

- U204 - 54ALS679 12-Bit Address Comparator
- U205 - 16L8 Programmable Array Logic (PAL)
- U206 - 54FCT138 3-To-8 Decoder

U204, the address comparator examines the most-significant 12 bits of the global address (GA31-GA20). If all the bits are 0, U204 asserts the Board Select signal, $\overline{\text{BDSEL}}$, indicating the Utility Module is being addressed. Further decoding is done by U205 and U206, which generate select signals for Utility Module resources. The programming of U205, a programmable array logic (PAL) device, is shown in Table 5-6.

5.5.2 Wait States

Utility Module must insert the number of wait states shown below when one of its resources is accessed:

Resource	Wait States
EPROM	4
RAM	2
32-Bit Timer	2
Status Register	2

TABLE 5-6. U205 LOGIC EQUATIONS

OUTPUT	INPUT EQUATIONS
()/BERR	= /A17*/A18*/A19*BRW + /A17*/A18*A19 + A17*A18*A19*FC2*/BRW + A17*A18*A19*BRW
/PORT32	= /A19*/BDSEL + /A18*A17*/BDSEL + A18*/A17*/BDSEL
/MSB	= /A0*/A1*/BDSEL*/A17*/A18*A19
/MUB	= /S0*/A1*/BDSEL*/A17*/A18*A19 + /A1*A0*/BDSEL*/A17*/A18*A19 + S1*/A1*/BDSEL*/A17*/A18*A19
/MLB	= /A0*A1*/BDSEL*/A17*/A18*A19 + /A1*/S0*/S1*/BDSEL*/A17*/A18*A19 + S1*S0*/A1*/BDSEL*/A17*/A18*A19 + /S0*/A1*A0*/BDSEL*/A17*/A18*A19
/LSB	= A0*S0*S1*/BDSEL*/A17*/A18*/A19 + /S0*/S1*/BDSEL*/A17*/A18*A19 + A0*A1*/BDSEL*/A17*/A18*A19 + A1*S1*/BDSEL*/A17*/A18*A19
/EPROMHI	= /A0*BRW*/BDSEL*/A19*/A18*/A17
/EPROMLO	= /S0*/BDSEL*BRW*/A19*/A18*/A17 + A0*/BDSEL*BRW*/A19*/A18*/A17 + S1*/BDSEL*BRW*/A19*/A18*/A17

Wait states are inserted by the wait state generator circuit, which consists of U221, U222, and associated logic. The circuit uses hardware jumpers to generate from one to eight wait states for any Utility Module resource. Default jumpers provide the number of wait states specified above.

The outputs of U221 are labeled 1 through 8 and correspond to a number of wait states. The inputs of U222, labeled P through V and TM, correspond to Utility Module address space (and resources) as shown below:

U222 Input	Address Space	Resource
P	00,000,000 - 00,01F,FFF	EPROM
Q	00,020,000 - 00,03F,FFF	EPROM
R	00,040,000 - 00,05F,FFF	Not Used
S	00,060,000 - 00,07F,FFF	Not Used
T	00,080,000 - 00,09F,FFF	RAM
U	00,0A0,000 - 00,0BF,FFF	Not Used
V	00,0C0,000 - 00,0DF,FFF	Not Used
TM	00,0E0,000 - 00,0FF,FFF	Timer, Status Register

The number of wait states for a resource is configured by connecting a jumper from the jumper pad giving the required number of wait states (1 to 8) to the jumper pad corresponding to the resource (P through V, TM). The 32-bit timer and the status register will have the same number of wait states.

5.5.3 EPROM

On the Utility Module, 256K bytes of space is reserved for EPROM. The Utility Module has two sockets and a strapping pad to accommodate the following EPROM configurations:

EPROM Type	Size	Total EPROM
27256	32K × 8	64K Bytes
27512	64K × 8	128K Bytes
27010	128K × 8	256K Bytes

Hardware jumpers provide the correct addressing for the selected EPROM configuration. Utility Module jumpers A, B, and C are used as follows:

EPROM Type	Jumpers
27256 (32K × 8)	A to B
27512 (64K × 8)	B to C
27010 (128K × 8)	B to C

5.5.4 RAM

The 128K bytes of 32-bit wide CMOS static RAM can be accessed by Processor Modules at either the supervisor or user level. During a write operation, the BRW signal derived from the global bus GRW is low and activates the RAM write enable lines. During a read, BRW, which is high, is inverted and activates the RAM output enable lines.

The RAM supports read-modify-write operations.

5.5.5 32-Bit Timer

The 32-bit timer is implemented with four 8-bit up-counters, U217-U220, clocked at 1 MHz (MHZ signal). At this frequency, the counter value is incremented every microsecond; thus, microsecond resolution is attainable for general-purpose timing.

The timer is cleared by a supervisor-level write operation. No specific data value is required; the write access itself clears the timer. When the timer is read, its value is placed in a holding register, thus allowing the counter to continue running. The entire 32 bits are read with one access. The read can be done at either the supervisor or the user level.

The following is a 32-bit timer programming summary:

Address: 00,0EX,XXX hex (X = don't care)
<u>Access Level</u>
Read: User or Supervisor (Read count)
Write: Supervisor only (Clear timer)
Initial State: 00000000 hex

5.5.6 Status Register

The 32-bit Status Register provides information about the battery backup for SANDAC V RAM and reset conditions. The status register consists of U243 and the associated devices that provide its inputs and control.

The format of the Status Register is shown below:

Utility Module Status Register

31	30	29	28	27 thru 0
*	*	RST	BAK	*

***Not Used**

Address: 00,0FX,XXX hex (X = don't care)
Access Level: User or Supervisor (Read-only)
Initial State: Refer to bit descriptions

RST RESET CONDITION - This bit differentiates between a powerup and a software reset. When the bit is set, it indicates that the reset was the result of a powerup. When cleared, it indicates a software reset. This bit must be read as soon as possible after a reset; it is valid for only 50 milliseconds.

BAK RAM BACKUP - This bit indicates the status of the RAM backup battery. When the bit is set, it indicates that the battery voltage is above 3.1 Vdc and that the contents of RAM will be held intact if the main power source is turned off. When cleared, it indicates a low battery. This bit must be read as soon as possible after a reset; it is valid for only 100 milliseconds.

NOTES

6. GLOBAL MEMORY MODULE

6.1 GENERAL

The Global Memory Module provides 512K bytes of static RAM storage, accessible via the SANDAC V global bus. Within the SANDAC V address map, 30 blocks of 512K bytes each are reserved for Global Memory Modules as shown in Figure 6-1. A Global Memory Module can be placed in any of the 30 blocks. Hardware jumpers on the module are set to provide proper address decoding.

In addition to the 512K bytes of RAM storage, the module also has a programmable access monitor that, when enabled, generates a bus error if an overwrite occurs in a user-selected block (or blocks) of module RAM. The access monitor is implemented with a 4K × 4-bit RAM. Logically, the access monitor occupies the same addresses as the 512K byte block of RAM on the module. The address spaces for the monitor and the RAM are separate because they require different 68020 MPU function codes for access. The access monitor is described in Subsection 6.3.

Both the 512K bytes of RAM and the 4K × 4-bit access monitor RAM are provided with backup power from the Utility Module PRAM circuit (5.2.4).

A block diagram of the Global Memory Module is shown in Figure 6-2. A detailed description of the Global Memory Module is given in the following subsections.

NOTE

The circuit diagram of the Global Memory Module is Sandia National Laboratories schematic CK-S64653. All component and signal references in the following text are from this drawing.

6.2 512K BYTE RAM

The 512K bytes of RAM storage is implemented with 16 32K × 8 bit CMOS static RAMs (U415 through U430). The 512K byte area is divided into four banks of 128K bytes each. The arrangement of the banks on the Global Memory Module is shown in Figure 6-3.

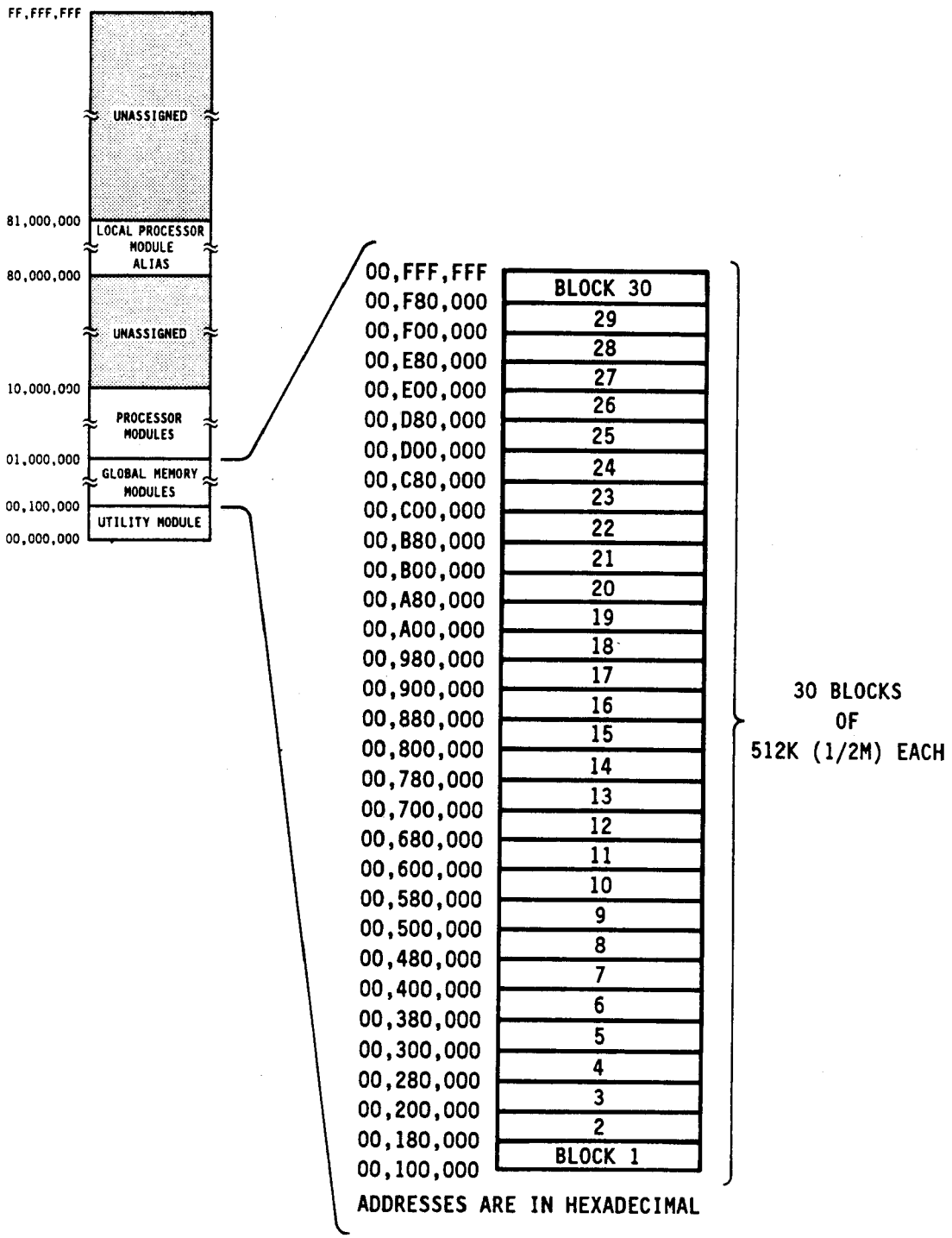


Figure 6-1. Global Memory Module Address Space

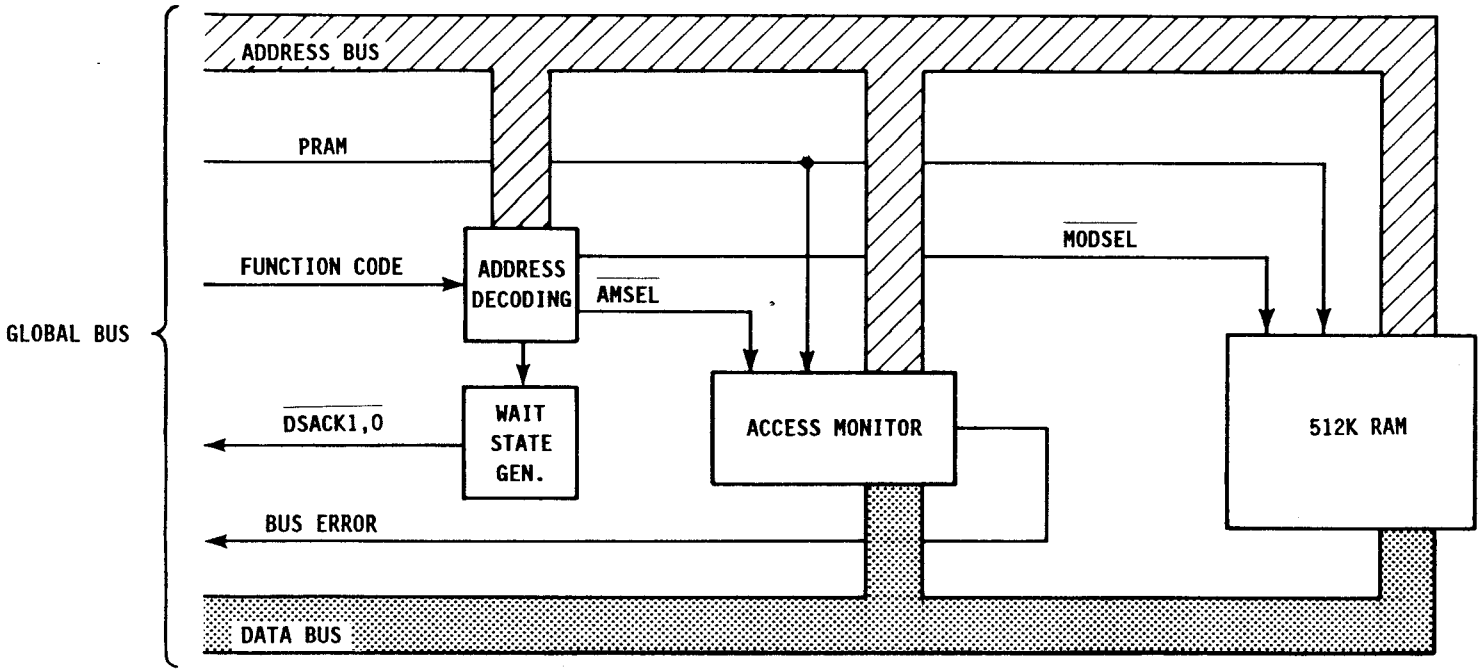


Figure 6-2. Global Memory Module Block Diagram

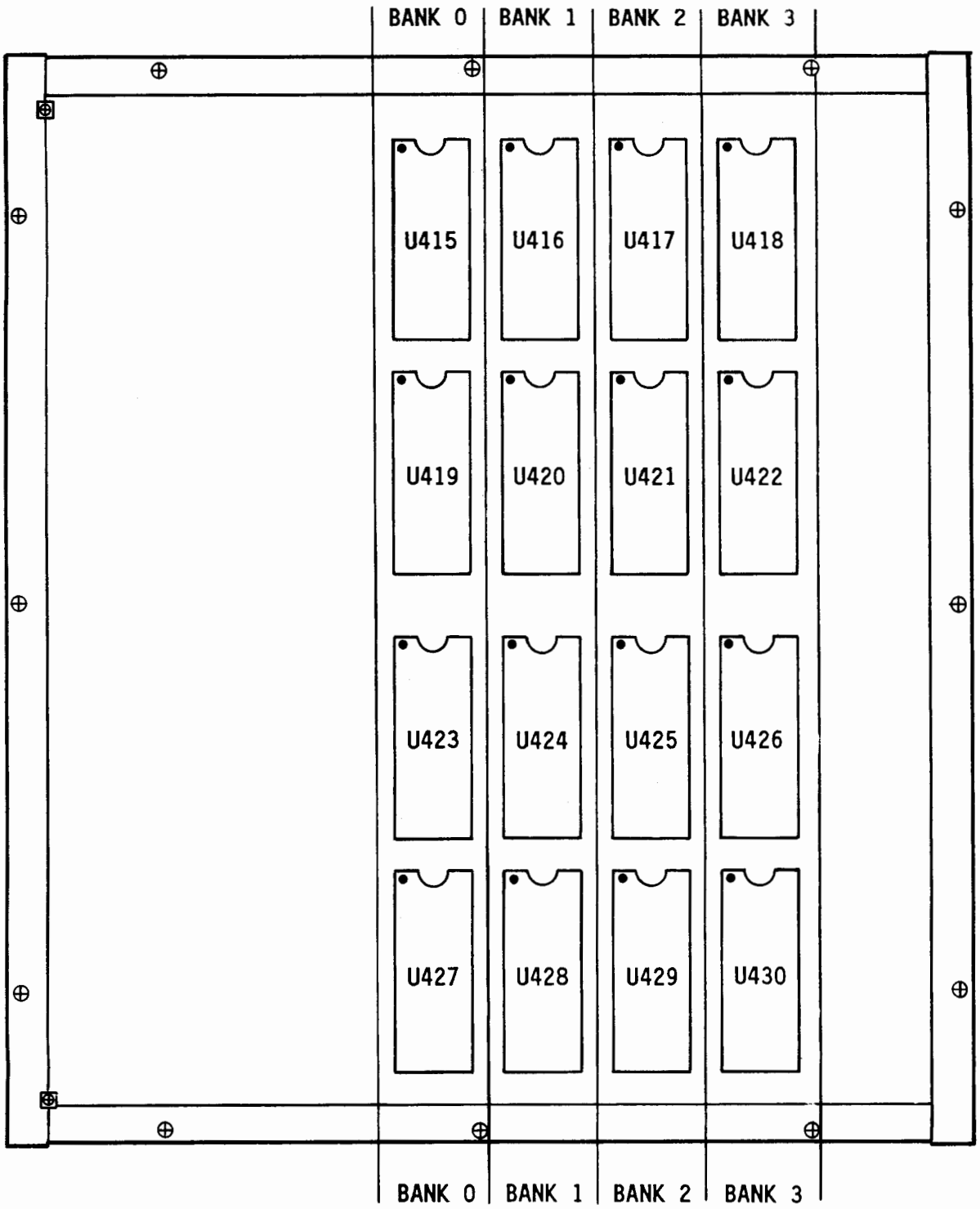


Figure 6-3. Layout of Global Memory Module RAMs

The following is an example of the division of a global memory block into banks:

Global Memory Block 1	00,100,000 - 00,17F,000	(512K Bytes)
Bank 0:	00,100,000 - 00,119,FFF	(128K Bytes)
Bank 1:	00,120,000 - 00,139,FFF	(128K Bytes)
Bank 2:	00,140,000 - 00,159,FFF	(128K Bytes)
Bank 3:	00,160,000 - 00,17F,FFF	(128K Bytes)

The arrangement of four byte-wide RAMs per bank allows byte, word, and long word data operations. The bidirectional buffers U432-U435 provide the data interface with the global data bus (GD31-GD0). The devices U406 through U410 provide chip select and enable signals for the RAMs and the data bus buffers. (The programming of U406, a programmable array logic (PAL) device, is given in Table 6-2.)

6.3 ACCESS MONITOR

The Global Memory Module access monitor, when enabled, generates a bus error if an overwrite occurs in a user-selected block (or blocks) of module RAM.

NOTE

> The access monitor does not inhibit the write operation. An overwrite occurs, and a bus error is indicated.

The access monitor can be enabled and disabled by hardware or software. When the monitor is hardware enabled, software can be used to disable and enable it as required. When the monitor is hardware disabled, any access to its address space causes a bus error. Hardware enable/disable is accomplished via jumper pad X. Appendix B describes the jumper settings.

The access monitor is implemented with a 4K × 4-bit RAM (U431). Only one bit, D1, is used. This bit outputs the indication that an overwrite has occurred. For monitor programming, the bit is connected to data bit 31 on the module data bus.

The 4K locations in the access monitor RAM must provide monitoring for the 512K locations of module RAM; therefore, the access monitor divides module RAM into blocks. The smallest block that can be monitored is 128 bytes (512K/4K). Block sizes from 128 bytes to 256K bytes can be selected with hardware jumpers. As block size increases, the number of blocks required to cover the 512K byte area of module RAM decreases. This relationship is shown below:

Size of Monitored Block (in bytes)	Number of Blocks for 512K Space (decimal)
128	4096
256	2048
512	1024
1K	512
2K	256
4K	128
8K	64
16K	32
32K	16
64K	8
128K	4
256K	2

Selection of monitored block size is made with hardware jumpers that connect address inputs A0-A10 (jumper pad BK, A-K) of the access monitor RAM (U431) to either ground (jumper pad GND, A-K) or address lines BA7-BA17 (jumper pad AD, A-K). The setting of the hardware jumpers for specific block sizes is given in Appendix B.

When the access monitor is hardware enabled and block size has been selected, monitoring for a block of module RAM is enabled by writing all 1s to the starting address of the block *in access monitor space*. Logically, the access monitor RAM occupies a 512K block of address space with the same addresses as the 512K block of RAM on the module. The address spaces for the monitor and the RAM are actually separate because they require different 68020 MPU function codes for access. RAM is accessed with any user-level or supervisor-level function code, which is generated automatically during a normal bus cycle. To write to or read from the access monitor, the 68020 DFC or SFC register must be programmed with function code 011.

The write operation to enable monitoring can be byte, word, or long word in length (FF, FFFF, or FFFFFFFF, respectively) but must be on a long-word boundary. Monitoring is disabled, or not selected, for a block by writing 0s to the starting address of the block in access monitor space.

NOTE

The enabled or disabled status for a block can be determined by reading the block starting address in the access monitor space and examining the most-significant bit of the data returned. The read can be a byte, word, or long-word access but must be on a long-word boundary. A 1 indicates monitoring is enabled; 0 indicates that it is disabled.

Once the access monitor is enabled and initialized, every write access to module RAM is monitored. Address lines BA7-BA18 appear at the input to the access monitor RAM via the block size jumper pads. The access monitor $\overline{WE}$ line (U431-11) is high during a write to module RAM causing the access monitor RAM to be read. The bit stored for the given address (i.e., either 0 or 1) is output on the AM_DATA line (U431-12). If the bit is a 1, U411 asserts ACC_$\overline{ERR}$ (pin 17), causing a bus error to be signaled. If the bit is a 0, there is no action.

At powerup, monitoring is randomly enabled and disabled; therefore, during system initialization, the access monitor should be programmed as required by the application or cleared (monitoring disabled for all blocks). The contents of the access monitor RAM are normally maintained intact at all times by battery backup power. Therefore, the RAM does not have to be reinitialized each time the system is powered on.

6.4 MODULE OPERATION

6.4.1 Address Decoding

Global Memory Module addressing is summarized in Table 6-1. The module decodes the 32-bit address on the global address bus (GA31-GA0) as shown in Figure 6-4.

6.4.1.1 GA31-GA24. Global address bits GA31-GA24 select global address space. On the Global Memory Module, these bits are present on the A side of U403, an 8-bit comparator. The bit pattern on the B side of the comparator is set with hardware jumpers (1A-1H). Since SANDAC V global address space is from 00,000,000 through 00,FFF,FFF hex, which includes Utility Module address space, the B side of U403 must be 00 hex, and jumper points 1A through 1H must be connected to ground ("-" jumper pads). (Appendix B details hardware jumper settings.) Thus, when GA31-GA24 = 00 hex, the global select signal, $\overline{GLBSEL}$, is asserted at U403-19.

6.4.1.2 GA23-GA19. Global address bits GA23-GA19 select a particular Global Memory Module (1 of 30). On the Global Memory Module, the bits are present on the A side of U404 and U405, two 8-bit comparators. The bit pattern on the B side of the comparators is set with hardware jumpers (2A-2E for U404 and 3A-3H for U405). The B-side setting must correspond to address bits GA23-GA19 for the selected module block. A 1 is set by connecting the jumper pad to Vcc (+); a 0 is set by connecting to ground (-). (Appendix B details the hardware jumper settings.)

When GA23-GA19 match the bit pattern set with jumpers 2A-2E, the module select signal, $\overline{MODSEL}$, is asserted at U404-19.

TABLE 6-1. GLOBAL MEMORY ADDRESSES

MEMORY BLOCK	START ADDRESS*	END ADDRESS*
1	00,100,000	00,17F,FFF
2	00,180,000	00,1FF,FFF
3	00,200,000	00,27F,FFF
4	00,280,000	00,2FF,FFF
5	00,300,000	00,37F,FFF
6	00,380,000	00,3FF,FFF
7	00,400,000	00,47F,FFF
8	00,480,000	00,4FF,FFF
9	00,500,000	00,57F,FFF
10	00,580,000	00,5FF,FFF
11	00,600,000	00,67F,FFF
12	00,680,000	00,6FF,FFF
13	00,700,000	00,77F,FFF
14	00,780,000	00,7FF,FFF
15	00,800,000	00,87F,FFF
16	00,880,000	00,8FF,FFF
17	00,900,000	00,97F,FFF
18	00,980,000	00,9FF,FFF
19	00,A00,000	00,A7F,FFF
20	00,A80,000	00,AFF,FFF
21	00,B00,000	00,B7F,FFF
22	00,B80,000	00,BFF,FFF
23	00,C00,000	00,C7F,FFF
24	00,C80,000	00,CFF,FFF
25	00,D00,000	00,D7F,FFF
26	00,D80,000	00,DFF,FFF
27	00,E00,000	00,E7F,FFF
28	00,E80,000	00,EFF,FFF
29	00,F00,000	00,F7F,FFF
30	00,F80,000	00,FFF,FFF

*Addresses are in hexadecimal.

512K BYTE RAM ADDRESS

GA31 - GA24	GA23 - GA19	GA18 - GA2	GA1 - GA0
GLOBAL SELECT	MODULE SELECT	RAM ADDRESS	ACCESS ALIGNMENT

ACCESS MONITOR RAM ADDRESS

GA31 - GA24	GA23 - GA19	GA18 - GA7	GA6 - GA2	GA1 - GA0
GLOBAL SELECT	MODULE SELECT	BLOCK SELECT	NOT USED	LONG WORD ALIGNMENT

Figure 6-4. Global Address Decoding

U405 functions like U404, but it is used to select the module's access monitor. Jumper pads 3A-3E on the B side of U405 must be set with the same configuration as pads 2A-2E on U404. Additionally, as the access monitor is selected with a 68020 MPU function code of 011, jumper pads 3F-3H on U405 must be set to compare with GFC2=0, GFC1=1, and GFC0=1. When a module is addressed and the function code is 011, the access monitor select signal, $\overline{\text{AMSEL}}$, is asserted at U405-19.

6.4.1.3 GA18-GA17. When addressing the 512K bytes of RAM storage, global address bits GA18 and GA17, buffered on the module as BA18 and BA17, are used to select one of the four 128K byte RAM banks. These bits also address the access monitor RAM as A11 (BA18), and A10 if BA17 is connected via the block select jumper pads.

6.4.1.4 GA16-GA2. When addressing the 512K bytes of RAM storage, global address bits GA16-GA2, buffered on the module as BA16-BA2, are used to select locations in the 32K × 8-bit RAM devices (U415-U430). Bits BA16-BA7 also address the access monitor RAM as A9-A0 if they are connected via the block select jumper pads.

6.4.1.5 GA1-GA0. Global address bits GA1 and GA0 determine byte, word, and long word access alignment. These bits along with GSIZ1, GSIZ0, $\overline{\text{GAS}}$, and the select signals $\overline{\text{GLBSEL}}$, $\overline{\text{MODSEL}}$, and $\overline{\text{AMSEL}}$ are decoded by the programmable array logic (PAL) device U406, which generates RAM enable and data strobe signals. The programming of U406 is given in Table 6-2.

TABLE 6-2. U406 LOGIC EQUATIONS

OUTPUT		INPUT EQUATIONS
LLDS	=	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * (GSIZ1)~ * (GSIZ0)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GA1 * GA0]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GSIZ1 * GA1]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GSIZ1 * GSIZ0 * GA0]
LMDS	=	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GA1 * (GA0)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * (GSIZ1)~ * (GSIZ0)~ * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GSIZ1 * GSIZ0 * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GSIZ1 * (GA1)~ * GA0]
UMDS	=	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * (GSIZ0)~ * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * GSIZ1 * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * (GA1)~ * GA0]
UUDS	=	(GLBSEL~)~ * (MODSEL~)~ * AMSEL~ * (GAS~)~ * (BPROT)~ * (GA1)~ * (GA0)~
ENO~	=	{[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * (GSIZ1)~ * (GSIZ0)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GA1 * GA0]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GSIZ1 * GA1]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GSIZ1 * GSIZ0 * GA0]}~
		ENABLE = (BPROT)~

TABLE 6-2. CONTINUED

OUTPUT		INPUT EQUATIONS
EN1~	=	{[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GA1 * (GA0)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * (GSIZ1)~ * (GSIZ0)~ * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GSIZ0 * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GSIZ1 * (GA1)~ * GA0]}~
		ENABLE = (BPROT)~
EN2~	=	{[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * (GSIZ0)~ * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * GSIZ1 * (GA1)~]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * (GA1)~ * (GA0)]}~
		ENABLE = (BPROT)~
EN3~	=	[(GLBSEL~)~ * (MODSEL~)~ * (GAS~)~ * (GA1)~ * (GA0)~]~
		ENABLE = (BPROT)~
RE~	=	[BRW * (BPROT)~]~
WE~	=	[(BRW)~ * (BPROT)~]~

6.4.2 Data Acknowledge/Wait States

The Global Memory Module acknowledges a data transfer (read or write) with the standard 68020 MPU $\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$ signals. The wait state generator implemented with shift register U412 allows sufficient time for an operation to complete before the acknowledge signals are asserted.

The eight outputs of U412 allow from one to eight wait states to be selected for each bank of the 512K bytes of RAM and for the access monitor RAM. The U412 outputs are terminated by jumper pads 5B through 5I. The pads correspond to a number of wait states as shown below:

Pad	Wait States
5B	1
5C	2
5D	3
5E	4
5F	5
5G	6
5H	7
5I	8

The inputs to the programmable array logic (PAL) device U411 supplied by jumper pads 5J through 5N correspond to the four banks of the 512K bytes of RAM and the access monitor RAM as shown below:

Pad	RAM
5J	Bank 3
5K	Bank 2
5L	Bank 1
5M	Bank 0
5N	Access Monitor

Wait states for a bank or the access monitor are configured by connecting a jumper from the pad giving the required number of wait states (5B through 5I) to the pad corresponding to the bank or access monitor (5J through 5N). (Appendix B describes hardware jumper settings.)

When the module is accessed, the wait state generator (U412) is enabled by the $\overline{\text{GLBSEL}}$ signal (U412-9). Once enabled, the shift register asserts successive wait state outputs on each rising edge of GCLK16. Based on the state of BA18 and BA17 or $\overline{\text{AM SEL}}$, U411, a PAL device, waits for one of the bank inputs or the access monitor input to be

asserted. When the required input goes high, $\overline{\text{DSACK}}$ (U411-21) is generated. This signal enables $\overline{\text{GDASCK1}}$ and $\overline{\text{GDASCK0}}$ through U436, the error/acknowledge buffer.

The programming of U411 is given in Table 6-3.

6.4.3 Backup Power

In the event of a Vcc power failure, the backup power circuit (PRAM) from the Utility Module supplies power to the following Global Memory Module components:

- Module RAM (U415-U430)
- Access Monitor RAM (U431)
- PALs (U406, U411)
- Chip Select Decoders (U407-U410)
- Access Monitor Control Buffer (U413)
- Error/Acknowledge Buffer (U436)

On the module, Vcc is supplied directly to module components that are not provided with backup power. For components that are provided with backup power, Vcc is supplied through the field effect transistor (FET) Q401. This voltage at the drain of Q401 is connected to the global bus PRAM line.

At the first indication of a power failure, the Utility Module's reset/power monitor circuit asserts the GRAMPROT signal, which is present on the Global Memory Module as RAMPROT. U413 buffers RAMPROT and asserts it as B PROT to the PAL devices U406 and U411. This action inhibits U406 from generating RAM data strobes (LLDS, LMDS, UMDS, UUDS) and prevents module RAM from being selected. Also, generation of data buffer enable signals (EN0-EN3) is inhibited. B PROT also inhibits U411 from generating $\overline{\text{DSACK}}$.

At the loss of Vcc, PRAMCTL closes Q401's channel, and the module components provided with backup power are supplied by the PRAM input.

TABLE 6-3. U411 LOGIC EQUATIONS

OUTPUT		INPUT EQUATIONS
BDSEL~	=	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * (BPROT)~]~
ACCERR~	=	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * AMSEL~ * (BRW~)~ * AMDATA]~
		ENABLE = (BPROT)~
AMWE~	=	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * (AMSEL~)~ * (BRW~)~ * (BPROT)~]~
DSACK~	=	{[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * (AMSEL~)~ * AMWS]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * AMSEL~ * (BA18)~ * (BA17)~ * BANK0]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * AMSEL~ * (BA18)~ * BA17 * BANK1]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * AMSEL~ * BA18 * (BA17)~ * BANK2]
	+	[(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * AMSEL~ * BA18 * BA17 * BANK3]}
		ENABLE = (BPROT)~
AMDATA	=	(BD31)
		ENABLE = [(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * (AMSEL~)~* (BRW~)~ * (BPROT)~]
BD31	=	(AMDATA)
		ENABLE = [(GLBSEL~)~ * (MODSEL~)~ * (BAS~)~ * (AMSEL~)~* BRW~ * (BPROT)~]

NOTES

7. EXPANSION MEMORY MODULE

7.1 GENERAL

The Expansion Memory Module provides 2 megabytes of battery-backed RAM storage on a Processor Module local expansion bus. Within Processor Module address space, six blocks of 2 megabytes each are reserved for Expansion Memory Modules as shown in Figure 7-1. A module may be placed in any of the blocks; hardware jumpers provide proper address decoding. The address monitor (4.4.2.2) on the host Processor Module can be used for monitoring accesses to this memory space if required. Expansion Memory Modules are provided with backup power from the Utility Module PRAM circuit (5.2.4).

A block diagram of the Expansion Memory Module is shown in Figure 7-2. A detailed description of the module is given in the following subsections.

NOTE

The circuit diagram of the Expansion Memory Module is Sandia National Laboratories schematic CK-S88195. All component and signal references in the following text are from this drawing.

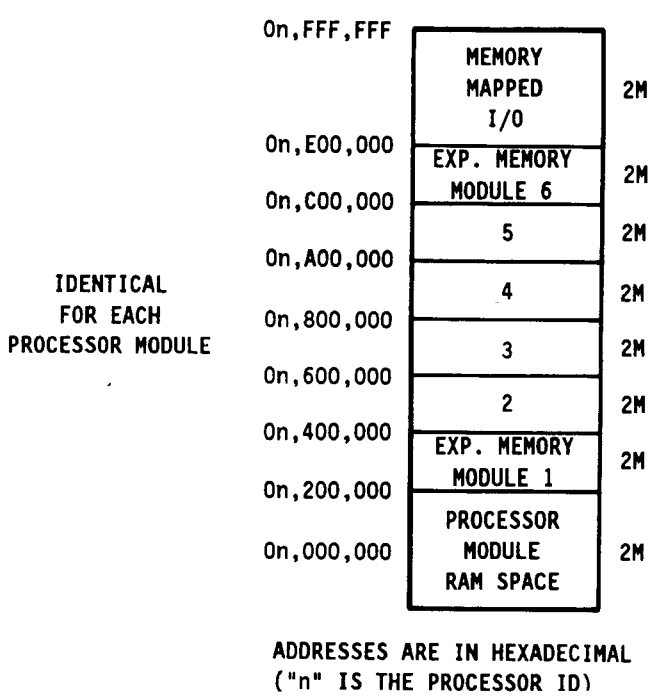


Figure 7-1. Expansion Memory Module Address Space

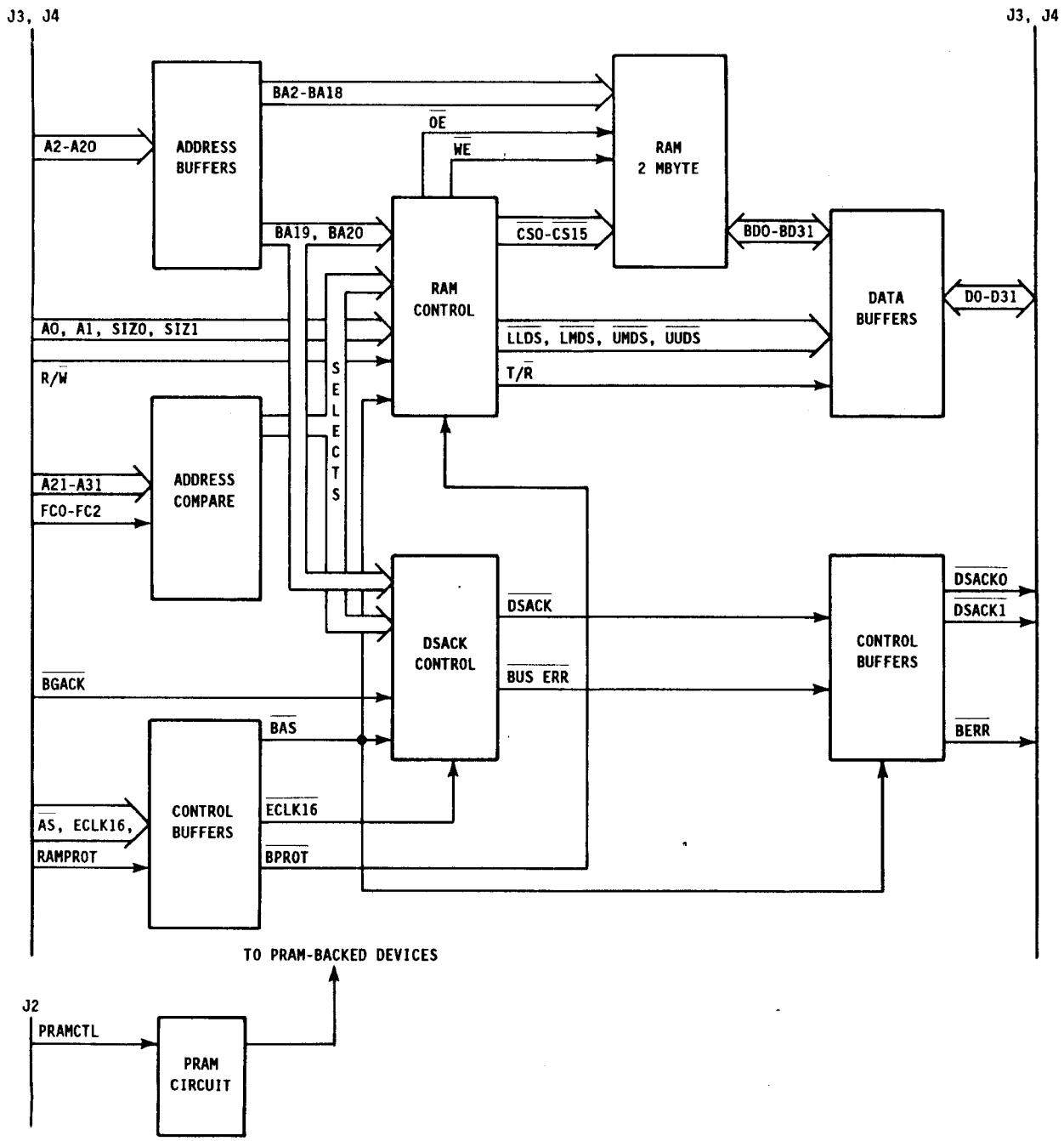


Figure 7-2. Expansion Memory Module Block Diagram

7.2 2 MEGABYTE RAM STORAGE

The 2 megabytes (2 MB) of RAM storage is implemented with 16 128K × 8 bit CMOS static RAMs (U515 - U530). The 2 MB area is divided into four banks of 512K bytes each. The physical arrangement of the banks on the Expansion Memory Module is shown in Figure 7-3. The following is an example of the division of an expansion memory block into banks:

Expansion Memory Block 1	0n,200,000 - 0n,3FF,FFF	(2 Megabytes)
Bank 0	0n,200,000 - 0n,27F,FFF	(512K Bytes)
Bank 1	0n,280,000 - 0n,2FF,FFF	(512K Bytes)
Bank 2	0n,300,000 - 0n,37F,FFF	(512K Bytes)
Bank 3	0n,380,000 - 0n,3FF,FFF	(512K Bytes)

The arrangement of four byte-wide RAMs per bank allows byte, word, and long word data operations. The bidirectional buffers U531 - U534 provide the data interface with the local data bus (D31-D0). The devices U508 through U512 provided chip select and enable signals for the RAMs and the data bus buffers. (The decoding done by U508 is described in Table 7-2.)

Expansion Memory Modules can be built with 1/2, 1, 1 1/2, or 2 MB of RAM. For the various sizes, 128K × 8 bit RAMS are installed in one, two, three, or all four banks. Hardware jumpers are also installed to enable banks that contain RAM and disable banks that are not used. The inputs to the programmable array logic (PAL) device U513 supplied by jumper pads BE0 through BE3, which correspond to the four banks of module RAM as shown below:

Pad	RAM
BE3	Bank 3
BE2	Bank 2
BE1	Bank 1
BE0	Bank 0

A bank of RAM is enabled by connecting its BE jumper pad to an EN jumper pad; a bank is disabled by connecting its BE pad to a DIS pad. (Complete hardware jumper information is given in Appendix B.) If a bank of RAM is disabled and an address to the bank is detected at U513, pins 2 and 3, the bus error signal, $\overline{\text{BUS_ERR}}$, is generated at U513-16. This returns a bus error indication to the host Processor Module through U535 as $\overline{\text{BERR}}$.

The Expansion Memory Module will accommodate 28-pin, 32K × 8-bit RAMs. When these devices are used, module capacity is reduced to a maximum of 1/2 MB. In this configuration, memory addresses are "aliased" four times across the 2 MB space.

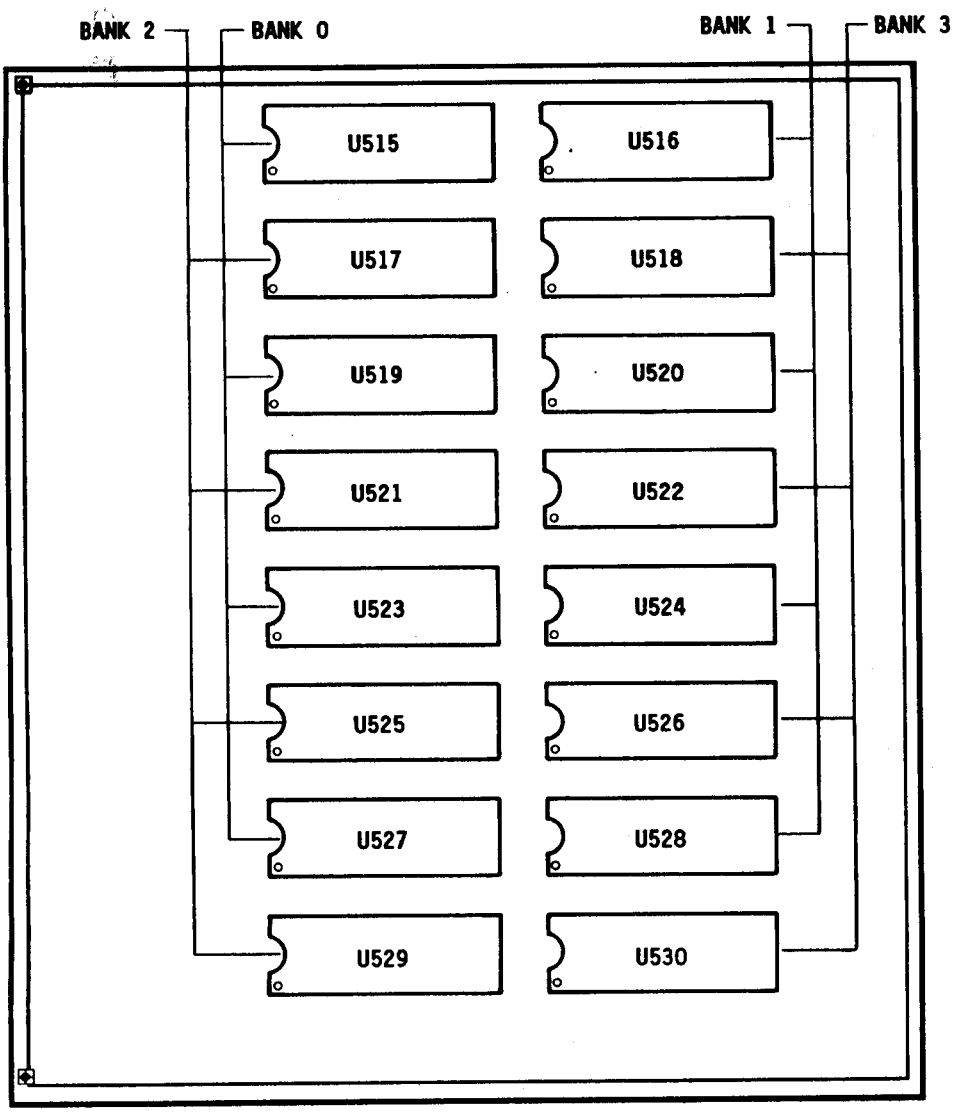


Figure 7-3. Layout of Expansion Memory Module RAMs

7.3 MODULE OPERATION

7.3.1 Address Decoding

Expansion Memory Module addressing is summarized in Table 7-1. The module decodes the 32-bit address on the local address bus (A31-A0) as shown in Figure 7-4.

TABLE 7-1. LOCAL EXPANSION MEMORY ADDRESSES

EXPANSION MODULE	START ADDRESS*	END ADDRESS*
1	0n,200,000	0n,3FF,FFF
2	0n,400,000	0n,5FF,FFF
3	0n,600,000	0n,7FF,FFF
4	0n,800,000	0n,9FF,FFF
5	0n,A00,000	0n,BFF,FFF
6	0n,C00,000	0n,DFF,FFF

*Addresses are in hex; n = Processor ID.

EXPANSION RAM ADDRESS

A31 - A24	A23 - A21	A20 - A19	A18 - GA2	GA1 - GA0
LOCAL SELECT	MODULE SELECT	BLOCK SELECT	RAM ADDRESS	ACCESS ALIGNMENT

Figure 7-4. Expansion RAM Address Decoding

7.3.1.1 A31-A24. Local address bits A31-A24 select local address space. On the Expansion Memory Module, these bits are present at the inputs of U505 and U506. These two devices determine whether A31-A24 equal 80 hex (local Processor Module alias) or 0n hex, where n is the host Processor Module ID. If A31 is a 1, then A30-A24 must be 0 for 80 hex. If A31-A28 are 0 hex, then A27-A24 must match the jumpered Processor Module ID for a match with 0n hex. (The setting of the hardware jumpers is described in Appendix B.) If a match occurs with either 80 or 0n, the local select signal, $\overline{\text{LCLSEL}}$, is asserted at U505-19.

7.3.1.2 A23-A21. Local address bits A23-A21 select a particular Expansion Memory Module. On the module, these bits are present at inputs of U504, a 3-to-8 decoder. Essentially, this device decodes the base address for the module. The base address a module recognizes is determined by jumpering one of the outputs of U504, BA1-BA6, to the BSL jumper pad. (The setting of hardware jumpers is described in Appendix B.) The outputs of U504 correspond to module base addresses as shown below:

U504 Output	Base Address (hex)
BA1	200,000
BA2	400,000
BA3	600,000
BA4	800,000
BA5	A00,000
BA6	C00,000

When A23-A21 are correct for a module's base address and correct output of U504 is jumpered to the BSL pad, the board select signal, $\overline{\text{BDSEL}}$, is asserted.

7.3.1.3 A20-A19. Address bits A20 and A19, buffered on the module as BA20 and BA19, select one of the four 512K byte RAM banks within the 2 MB of RAM storage. These bits are decoded by U509-U512, which generate the appropriate chip select signals ($\overline{\text{CS0}}$-$\overline{\text{CS15}}$).

7.3.1.4 A18-A2. Address bits A18-A2, buffered on the module as BA18-BA2, select locations in the 128K × 8-bit RAM devices (U515-U530).

7.3.1.5 A1-A0. Address bits A1 and A0 determine byte, word, and long word access alignment. These bits along with SIZ1, SIZ0, $\overline{\text{BAS}}$, and the select signals $\overline{\text{LCLSEL}}$ and $\overline{\text{BDSEL}}$ are decoded by the programmable array logic (PAL) device U508, which generates RAM enable and data strobe signals.

Another input to U508 is $\overline{\text{CPU_SPACE}}$. This signal is generated by U507, which has as its inputs 68020 function code line FC2-FC0. U507 prevents access of the Expansion Memory Module when "CPU space" is being accessed. When FC2-FC0 are all 1 (68020 CPU space function code), the $\overline{\text{CPU_SPACE}}$ signal at U507-7 is asserted. This is

decoded at U508 and module access is inhibited. The logic equations for U508 are given in Table 7-2.

7.3.2 Data Acknowledge/Wait States

The Expansion Memory Module acknowledges a data transfer (read or write) with the standard 68020 MPU $\overline{DSACK1}$ and $\overline{DSACK0}$ signals. The wait state generator implemented with shift register U514 allows sufficient time for an operation to complete before the acknowledge signals are asserted.

The seven outputs of U514 allow from two to eight wait states to be selected for each 512K byte bank of the 2 MB RAM area. The U514 outputs, WS2-WS8 are terminated by jumper pads. The outputs correspond to a number of wait states as shown below:

U514 Output	Wait States
WS2	2
WS3	3
WS4	4
WS5	5
WS6	6
WS7	7
WS8	8

The WS1 line (hardwired high) is also terminated with a jumper pad and provides one wait state.

The inputs to the programmable array logic (PAL) device U513, BK0-BK3, correspond to the four 512K byte banks of the 2 MB RAM area as shown below:

U513 Input	RAM Bank
BK3	Bank 3
BK2	Bank 2
BK1	Bank 1
BK0	Bank 0

These inputs are used with the WS outputs of U514. The GLB_WS input of U513 determines the number of wait states inserted when a Processor Module other than the Expansion Memory Module's makes an access (global-to-local access).

TABLE 7-2. U508 LOGIC EQUATIONS

OUTPUT		INPUT EQUATIONS
LLDS~	=	{[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (SIZ1)~ * (SIZ0)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * A1 * A0]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * SIZ1 * A1]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * SIZ1 * SIZ0 * A0]}~
LMDS~	=	{[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * A1 * (A0)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (SIZ1)~ * (SIZ0)~ * (A1)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * SIZ1 * SIZ0 * (A1)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * SIZ1 * (A1)~ * A0]}~
UMDS~	=	{[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (SIZ0)~ * (A1)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * SIZ1 * (A1)~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (A1)~ * A0]}~
UUDS~	=	{(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (A1)~ * (A0)~}~
OE~	=	{(LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * R_W~}~
WE~	=	{(LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (R_W~)~}~
T_R~	=	{(LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (R_W~)~}~

The number of wait states inserted for a particular bank or for a global-to-local access is configured by connecting a jumper from the pad giving the required number of wait states (WS2-WS8 or WS1) to the pad corresponding to the bank or global-to-local access (BK0-BK3, GLB_SEL). (Appendix B describes hardware jumper settings.)

NOTE

If WS1 is selected, $\overline{\text{DSACK}}$ is generated immediately. This is equivalent to one wait state.

When the module is accessed, the wait state generator (U514) is enabled by the $\overline{\text{BAS}}$ signal (U514-9). Once enabled, the shift register asserts successive wait state outputs on each rising edge of ECLK16. Based on the state of BA20 and BA19, U513 waits for one of the bank inputs or the global-to-local input to be asserted. When the required input goes high, $\overline{\text{DSACK}}$ (U513-23) is generated. This signal enables $\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$ through U535, the error/acknowledge buffer. The logic equations for U513 are shown in Table 7-3.

7.3.3 Backup Power

In the event of a Vcc power failure, the backup power circuit (PRAM) from the Utility Module supplies power to the following Expansion Memory Module components:

- Module RAM (U515-U530)
- Chip Select Decoders (U509-U512)
- Control Buffer (U506)

On the module, Vcc is supplied directly to components that are not provided with backup power. For components that are provided with backup power, Vcc is supplied through the field effect transistor (FET) Q501. The voltage at the drain of Q501 is connected to the PRAM line.

At the first indication of a power failure, the Utility Module's reset/power monitor circuit asserts the GRAMPROT signal, which is present on the Expansion Memory Module as RAMPROT. U506 buffers RAMPROT and asserts it as $\overline{\text{BPROT}}$ to the chip select devices U509-U512, which disables them and prevents module RAM from being selected.

At the loss of Vcc, PRAMCTL closes Q501's channel, and the module components provided with backup power are supplied by the PRAM input.

TABLE 7-3. U513 LOGIC EQUATIONS

OUTPUT		INPUT EQUATIONS
DSACK~	=	{[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * BGACK~ * BE0 * BK0 * BA19~ * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * BGACK~ * BE1 * BK1 * BA19 * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * BGACK~ * BE2 * BK2 * BA19~ * BA20]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * BGACK~ * BE3 * BK3 * BA19 * BA20]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BGACK~)~ * BE0 * GLB_WS * BA19~ * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BGACK~)~ * BE1 * GLB_WS * BA19 * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BGACK~)~ * BE2 * GLB_WS * BA19~ * BA20]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BGACK~)~ * BE3 * GLB_WS * BA19 * BA20]}~
		ENABLE = (BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~
		CLOCK = ECLK16~ (DSACK~ IS OUTPUT FROM A D FLIP-FLOP)
BUS_ERR~	=	{[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BE0)~ * BA19~ * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BE1)~ * BA19 * BA20~]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BE2)~ * BA19~ * BA20]
	+	[(BAS~)~ * (LCLSEL~)~ * (BDSEL~)~ * CPU_SPACE~ * (BE3)~ * BA19 * BA20]}~

8. SYSTEM I/O MODULE

The SANDAC V System I/O Module attaches to a Processor Module and provides the following local resources:

- 4 DMA channels
- 1 parallel port
- 5 async/sync serial ports
- 4 16-bit counter/timers
- 4 8-bit counter/timers
- 2 baud-rate generators
- 8 input discretes
- 8 output discretes
- 8 input/output/interrupt discretes
- 4 digital phase-locked loops (DPLLs)
- 4 general-purpose isolated input buffers
- 14 general-purpose nonisolated input/output buffers

Six major circuits support System I/O Module functions as shown in Figure 8-1. The local expansion bus interface provides address decoding and signal conversion from the 68020-compatible signals of the local bus to the 68000-compatible signals required by the devices on the System I/O Module. (The System I/O Module bus is referred to as the "peripheral" bus; all bus signal names are prefixed with "P.") Four channels of direct memory access (DMA) are provided by a Hitachi HD63450 Direct Memory Access Controller (DMAC). The parallel port buffers address, data, and control signals to an external connector. The serial/discrete/timer ports consist of two Signetics SCN68562 Dual Universal Serial Communications Controllers (DUSCC) and one Motorola MC68901 Multi-Function Peripheral (MFP), that provide serial port, discrete, and counter/timer resources. Uncommitted line drivers, opto-couplers, and connector pins can be configured by the user to provide buffered external input or output discrete signals. The interrupt steering logic directs interrupt requests and acknowledges to/from the global and local buses.

System I/O Module resources are memory-mapped within the host Processor Module's address space as shown in Figure 8-2. A detailed description of the System I/O Module is given in the following subsections.

NOTE

The circuit diagram of the System I/O Module is Sandia National Laboratories drawing CK-S64652. In the following text, all component and signal references are from this drawing.

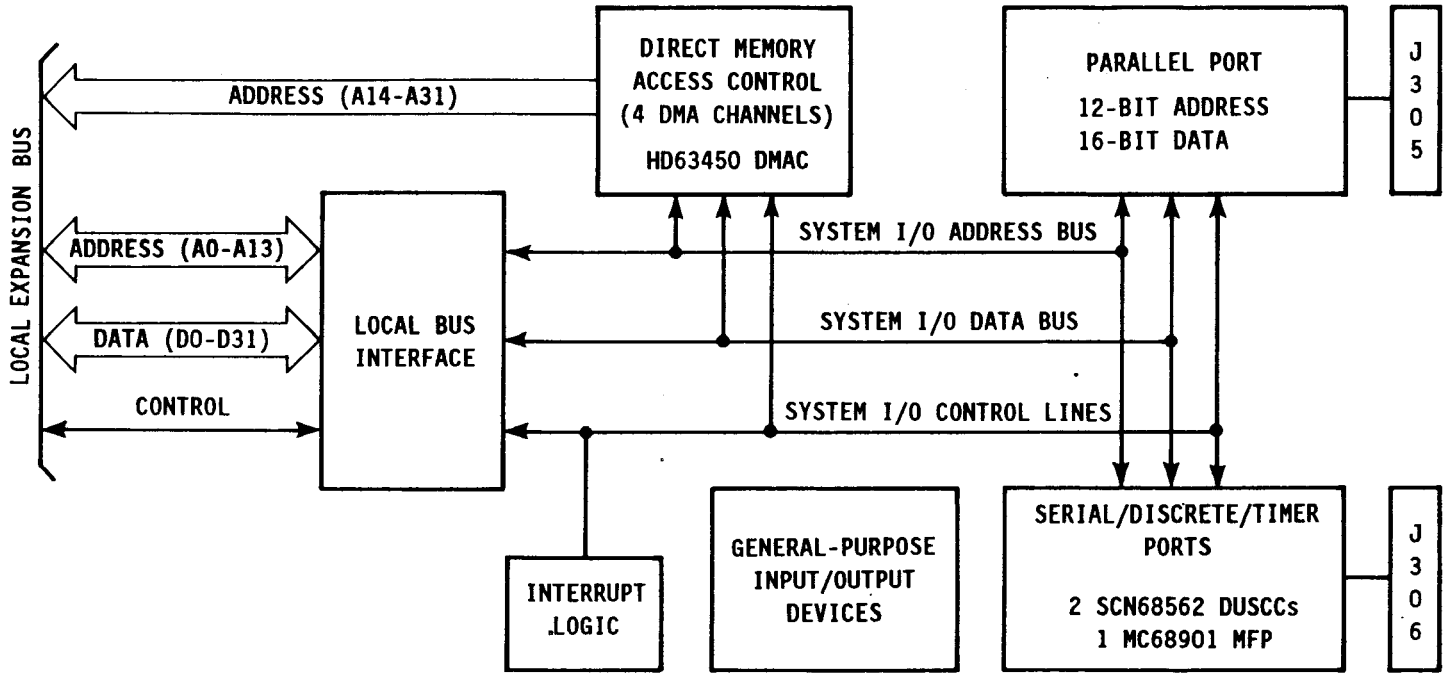


Figure 8-1. System I/O Module Block Diagram

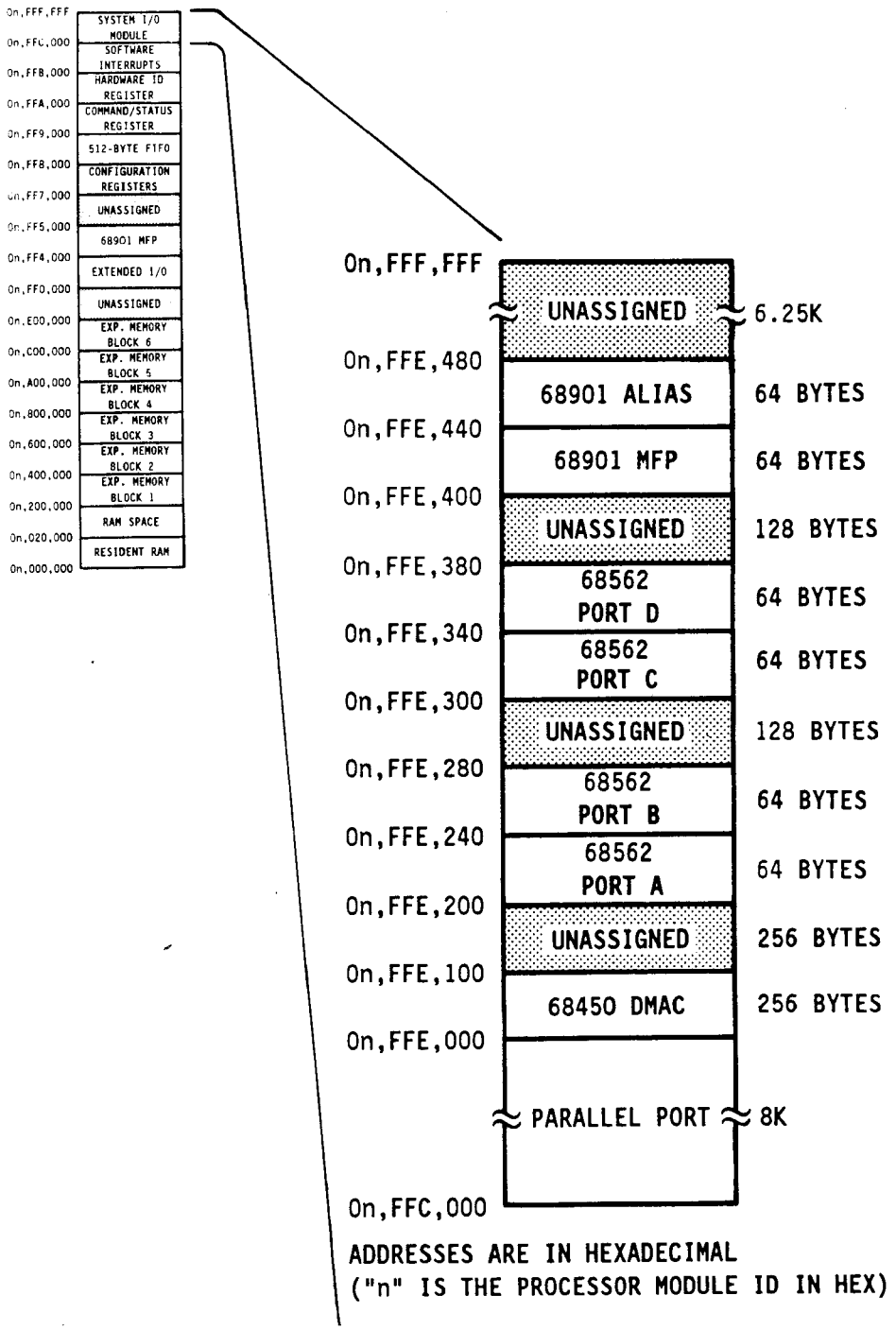


Figure 8-2. System I/O Module Address Space

8.1 LOCAL EXPANSION BUS INTERFACE

System I/O Module resources can be accessed by the local MPU or by the MPU of another Processor Module (remote MPU) that has gained control of the global bus and the host Processor Module's local bus. Conversely, the System I/O Module 63450 DMAC (Subsection 8.2) can become the local bus master. (The DMAC cannot access the global bus.)

When a local or remote MPU controls the local bus, the mode of operation is known as MPU mode. When the 63450 DMAC controls the local bus, the mode is known as DMA mode. The following subsections describe these modes.

8.1.1 MPU Mode

In MPU mode, the local MPU or a remote MPU is the local bus master. System I/O Module resources are addressed by the local bus master at the addresses shown in Table 8-1.

TABLE 8-1. SYSTEM I/O MODULE ADDRESSES

ASSIGNMENT	START ADDRESS[1]	END ADDRESS[1]
Parallel Port	0n,FFC,000	0n,FFD,FFF
63450 DMAC	0n,FFE,000	0n,FFE,0FF
Unassigned	0n,FFE,100	0n,FFE,1FF
68562 Port A	0n,FFE,200	0n,FFE,23F
68562 Port B	0n,FFE,240	0n,FFE,27F
Unassigned	0n,FFE,280	0n,FFE,2FF
68562 Port C	0n,FFE,300	0n,FFE,33F
68562 Port D	0n,FFE,340	0n,FFE,37F
Unassigned	0n,FFE,380	0n,FFE,3FF
68901 MFP	0n,FFE,400	0n,FFE,43F
68901 Alias[2]	0n,FFE,440	0n,FFE,47F
Unassigned	0n,FFE,480	0n,FFF,FFF

1 Addresses are in hexadecimal; "n" is the Processor ID.
2 68901 registers are also selected in this address space.

During an access of the System I/O Module, address bits A31-A14 are decoded by the host Processor Module's gate array, which generates the local bus $\overline{\text{ESIO}}$ signal. On the System I/O Module, individual device addresses are decoded, and the appropriate select signals are generated by the Peripheral Address Decoder, PAD4 (U306). A simplified

schematic of the MPU mode address decoding circuit is shown in Figure 8-3a. The logic equations for PAD4 are shown in Table 8-2.

The System I/O Module is viewed as a 16-bit data port on the local bus, and in MPU mode, data buffers U315 and U316 connect peripheral bus data lines PD0-PD15 to local bus data lines D16-D31. The data buffers are controlled by the Bus Interface Device A (BIFA), U305. A simplified schematic of the MPU mode data interface circuit is shown in Figure 8-3b. The logic equations for BIFA are shown in Table 8-3.

Because the System I/O Module functions as a 16-bit port, it always responds to an access with $\overline{DSACK1}$ = 0 and $\overline{DSACK0}$ = 1. $\overline{DSACK0}$ is not present on the module; it is held in its required high state by the local bus pull-up. $\overline{DSACK1}$ is generated by the $\overline{DTACK}$ signal from the accessed device. On the module, all $\overline{DTACK}$ lines are tied together to form the $\overline{PDTACK}$ signal.

Some devices do not negate $\overline{PTDACK}$ within the required 80 nanoseconds (ns) after $\overline{AS}$ is negated. The lingering $\overline{PDTACK}$ signal is hidden from the Processor Module by using $\overline{PAS}$ as a qualifier at U327-A. The $\overline{ACKEN}$ signal (U306-15) enables the $\overline{DSACK1}$ driver, U326-C. During MPU mode, U326-B steers $\overline{DTACK}$ from the 63450 DMAC. A simplified schematic of the MPU mode data acknowledge circuit is shown in Figure 8-3c.

NOTE

> Subsequent System I/O Module device selects will not be asserted until $\overline{PDTACK}$ has been negated. Additionally, PAD4 imposes a 250 ns delay between successive 68562 DUSCC selects to satisfy timing requirements specific to that device.

8.1.2 DMA Mode

In DMA mode, the System I/O Module 63450 DMAC (U301) is the local bus master, issuing addresses and control signals. During DMA operations, the DMAC asserts the $\overline{OWN}$ signal (U301-4), which controls the direction of address buffers U311 and U312. The BIFA (U305) generates A0, SIZ1, and SIZ0 for correct memory access and asserts AS after these signals are valid. A simplified schematic of the DMA mode address interface circuit is shown in Figure 8-4a. The logic equations for the BIFA are shown in Table 8-3.

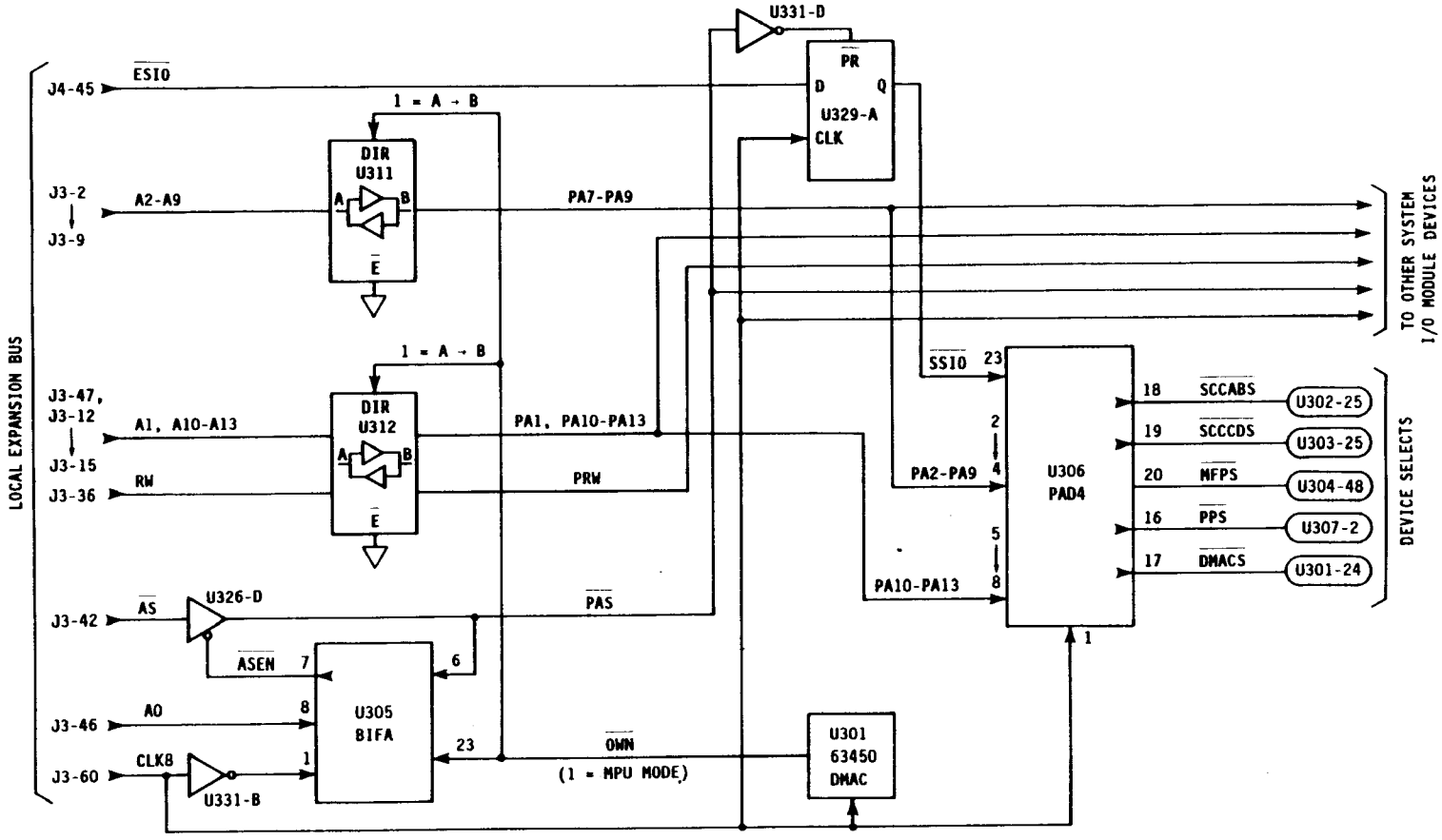


Figure 8-3a. MPU Mode Local Bus Interface - Address Decoding

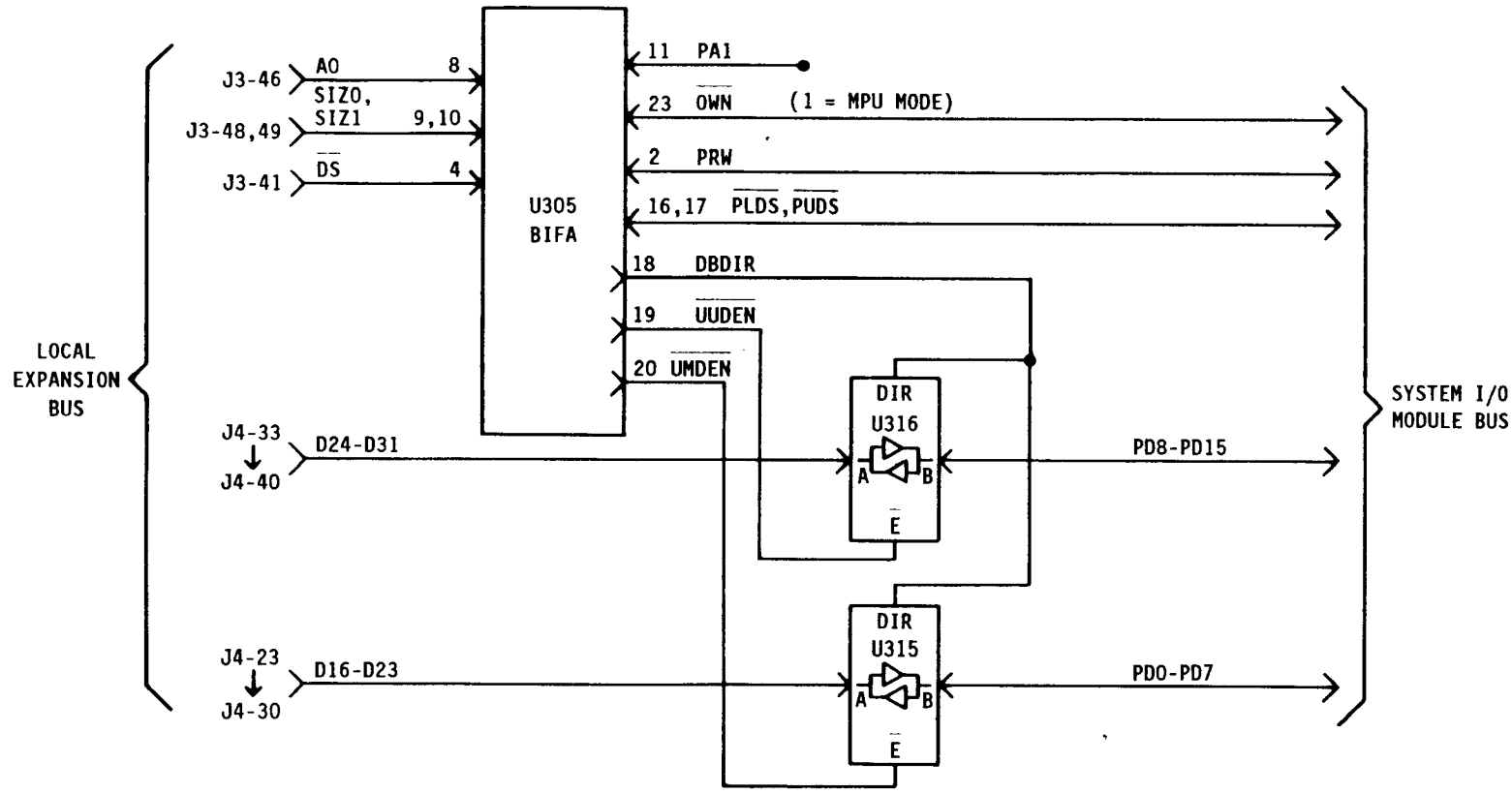


Figure 8-3b. MPU Mode Local Bus Interface - Data Interface

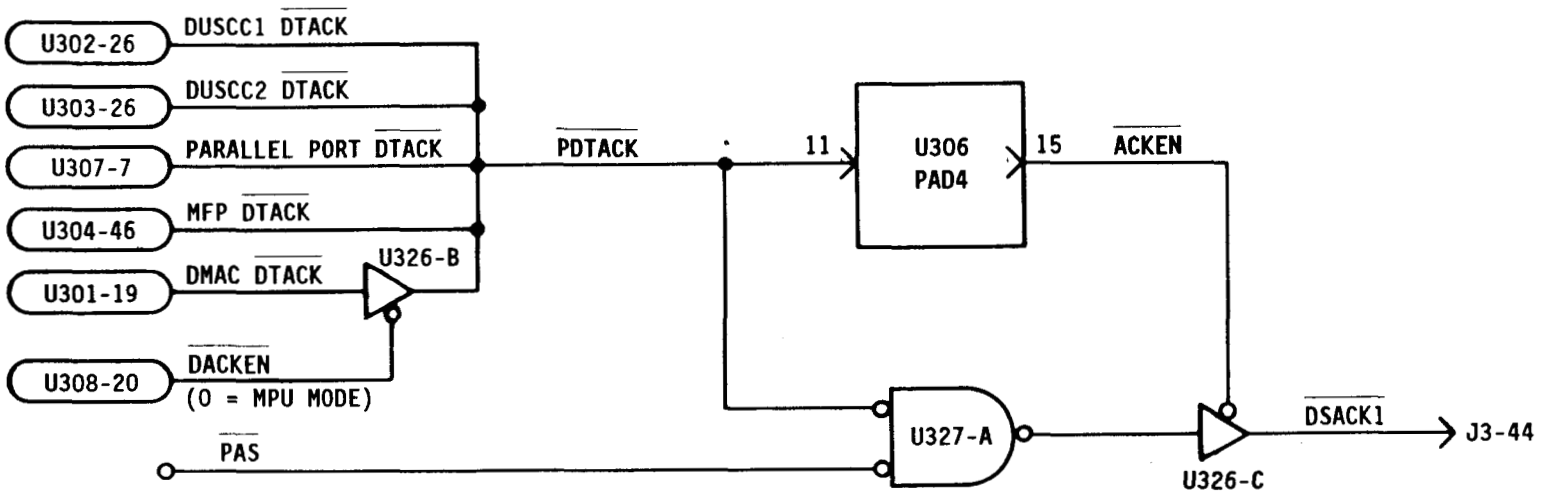


Figure 8-3c. MPU Mode Local Bus Interface - Data Acknowledge

TABLE 8-2. PAD4 (U306) LOGIC EQUATIONS

INPUTS: CLK8@1, SSIO~@23, PLDS~@14, PDTACK~@11, PA13@8, PA12@7, PA11@6, PA10@5, PA9@4, PA8@3, PA7@2, IACK~@21

OUTPUTS: ACKEN~@15, PPS~@16, DMACS~@17, SCCABS~@18, SCCCDS~@19, MFPS~@20, A@9, B@10, INH@22

NETWORK:

```
CLK8 = INP(CLK8)            % 8 MHz clock %
INHclk = CLK8(INHCLK)       % async clock for INH latch %

SSIO = INP(SSIO~)           % synchronized SIO select %
PLDS = INP(PLDS~)           % peripheral bus lower data select
                              %
PDTACK = INP(PDTACK~)       % peripheral bus DTACK~ %
IACK = INP(IACK~)           % SIO IACK cycle in progress %
A13 = INP(PA13)             % local address bits %
A12 = INP(PA12)
A11 = INP(PA11)
A10 = INP(PA10)
A9 = INP(PA9)
A8 = INP(PA8)
A7 = INP(PA7)

ACKEN~ = CONF(ACKENc,VCC)   % DSACK1 buffer enable %
PPS~ = CONF(PPSc,VCC)       % PAR expansion port select %
DMACS~ = CONF(DMACSc,VCC)   % 63450 DMAC select %
SCCABS~ = CONF(SCCASc,VCC)  % 68562 DUSCC 1 (A & B) select %
SCCCDS~ = CONF(SCCDSc,VCC)  % 68562 DUSCC 2 (C & D) select %
MFP~ = CONF(MFPc,VCC)       % 68901 MFP select %

INH, INH = TOTF(INHt,INHclk,INHac,GND,VCC)
                            % Inhibit new access while PDTACK~
                              asserted %

A, A = RORF(Ad,CLK8,GND,GND,VCC)   % state variable lsb %
B, B = RORF(Bd,CLK8,GND,GND,VCC)   % state variable msb %
```

EQUATIONS: See next page

TABLE 8-2. CONTINUED

```
EQUATIONS: INHCLK = SSIO*IACK;          % async clock for INH latch %
           INHac = PDTACK;              % async clear for INH latch %
           INHt = INH'*PDTACK';         % data for INH latch %

           DEVS = SSIO'*INH;
           PPSc = /(DEVS*A13);          % pep address = $0000 - $1FFF %
           DMACSc = /(DEVS*A13*A12'*A11'*A10'*A9'*A8');
                                        % DMAC address = $2000 - $20FF %

           SCCVAD = (two'*three'*A13*A12'*A11'*A10'*A9'*A8');
           SCCASc = /(DEVS*SCCVAD*PLDS'*A8'); % DUSCC 1 (A & B) address
                                                = $2200 - $227F %
           SCCDSc = /(DEVS*SCCVAD*PLDS'*A8);  % DUSCC 2 (C & D) address
                                                = $2300 - $237F %
           MFPSc = /(DEVS*A13*A12'*A11'*A10'*A9'*A8'*A7');
                                              % MFP address = $2400 -
                                                $243F & $2440 - $247F %

           ACKENc =
           /(IACK'*INH'+DEVS*(A13'+A13*A12'*A11'*A10'*A9'*A8'+SCCVAD+A13
           *A12'*A11'*A10*A9'*A8'*A7'));
                                        % enable for DSACK1 buffer %

           zero = B'*A';                % state definitions for DUSCC
                                          holdoff %
           one = B'*A;
           two = B*A';
           three = B*A;

           Ad = zero*DEVS*SCCVAD+zero*IACK'*INH'+one;
           Bd = one*SSIO+three;
```

TABLE 8-3. BIFA (U305) LOGIC EQUATIONS

INPUTS: OWN~@23, PAS~@6, PA1@11, PRW@2, IACK~@15, SSIO~@14, CLK8@1

OUTPUTS: DS~@4, PLDS~@17, PUDS~@16, PA0@8, SIZ0@9, SIZ1@10, AS~@5, ASEN~@7, DBDIR@18, UUDEN~@19, UMDEN~@20, LMDEN~@21, LLDEN~@22, SDLY@3

NETWORK:

```
CLK8 = INP(CLK8~)                % inverted 8 MHz clock %

OWN = INP(OWN~)                  % DMAC owns local bus %
PAS = INP(PAS~)                  % peripheral address strobe %
PA1 = INP(PA1)                   % peripheral address bit 1 %
PRW = INP(PRW)                   % peripheral bus R/W' %
IACK = INP(IACK~)                % SIO IACK cycle in progress %
SSIO = INP(SSIO~)                % I/O select %

UUDEN~ = CONF(UUDENc,VCC)        % upper upper data byte buffer
                                   enable %
UMDEN~ = CONF(UMDENc,VCC)        % upper middle data byte buffer
                                   enable %
LMDEN~ = CONF(LMDENc,VCC)        % lower middle data byte buffer
                                   enable %
LLDEN~ = CONF(LLDENc,VCC)        % lower lower data byte buffer
                                   enable %
DBDIR = CONF(DBDIRc,VCC)         % data bus direction control %
AS~ = CONF(ASc,DMAM)             % AS~ out to local bus %
ASEN~ = CONF(ASENc,VCC)          % external address strobe
                                   buffer enable%

PLDS~, PLDS = COIF(PLDSc,PMM) % SIO lower data strobe %
PUDS~, PUDS = COIF(PUDSc,PMM) % SIO upper data strobe %
DS~, DS = COIF(DSc,DMAM)      % local data strobe
PA0, PA0 = COIF(PA0c,DMAM)    % SIO address bit 0 %
SIZ0, SIZ0 = COIF(SIZ0c,DMAM) % local size inputs %
SIZ1, SIZ1 = COIF(SIZ1c,DMAM)

SDLY, SDLY = RORF(SDLYd,CLK8,SDLYac,GND,VCC)
                                 % strobe delay %
```

TABLE 8-3. CONTINUED

```
EQUATIONS: PMM = OWN;                          % processor module is bus
                                                 master %
           DMAM = OWN';                        % DMAC is bus master %
           UUDENc = /(OWN'*PA1'*PUDS'*SSIO + OWN*PA0'*SSIO');
           UMDENc = /(OWN'*PA1'*PLDS'*SSIO + OWN*SSIO'*(PA0+SIZ0'+SIZ1)
           + IACK');
           LMDENc = /(OWN'*PA1*PUDS'*SSIO);
           LLDENc = /(OWN'*PA1*PLDS'*SSIO);
           DBDIRc = OWN*PRW' + OWN'*PRW;
           ASc = /(PRW*PAS' + PRW'*PAS'*SDLY);
                                           % enable internal buffer with
                                             DMAM %
           ASENc = /PMM;                   % enable internal buffer with
                                             PMM %
           DSc = /(PRW*(PLDS'+PUDS') + PRW'*SDLY*(PLDS'+PUDS'));
           PLDSc = /(DS'*(PA0+SIZ0+SIZ1));
           PUDSc = /(DS'*PA0');
           PA0c = PUDS;
           SIZ0c = PUDS'*PLDS + PUDS*PLDS';
           SIZ1c = PUDS'*PLDS'
           SDLYd = PRW'*(PUDS'+PLDS');
           SDLYac = PAS;                  % async clear for strobe delay %
```

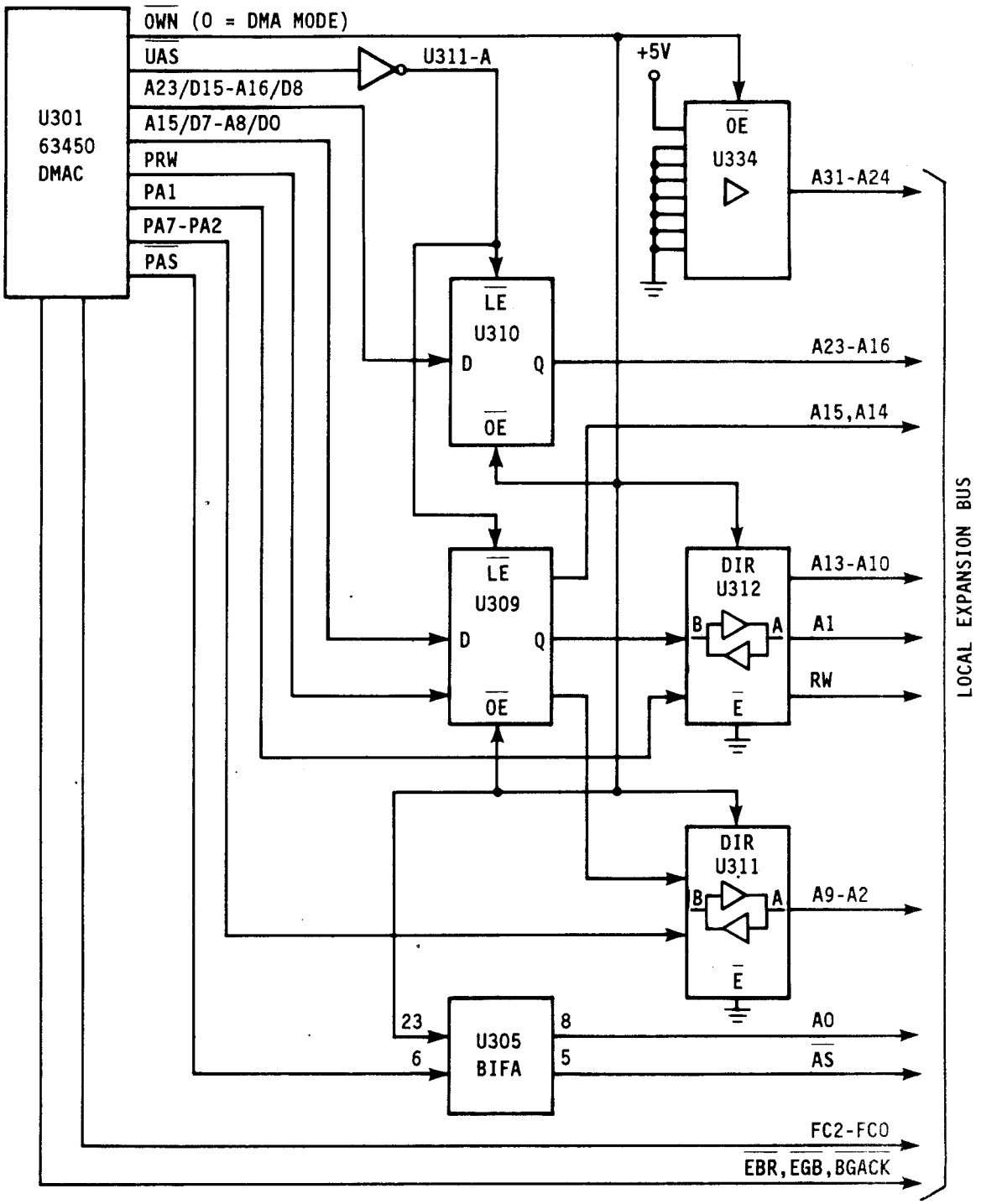


Figure 8-4a. DMA Mode Local Bus Interface - Address Decoding

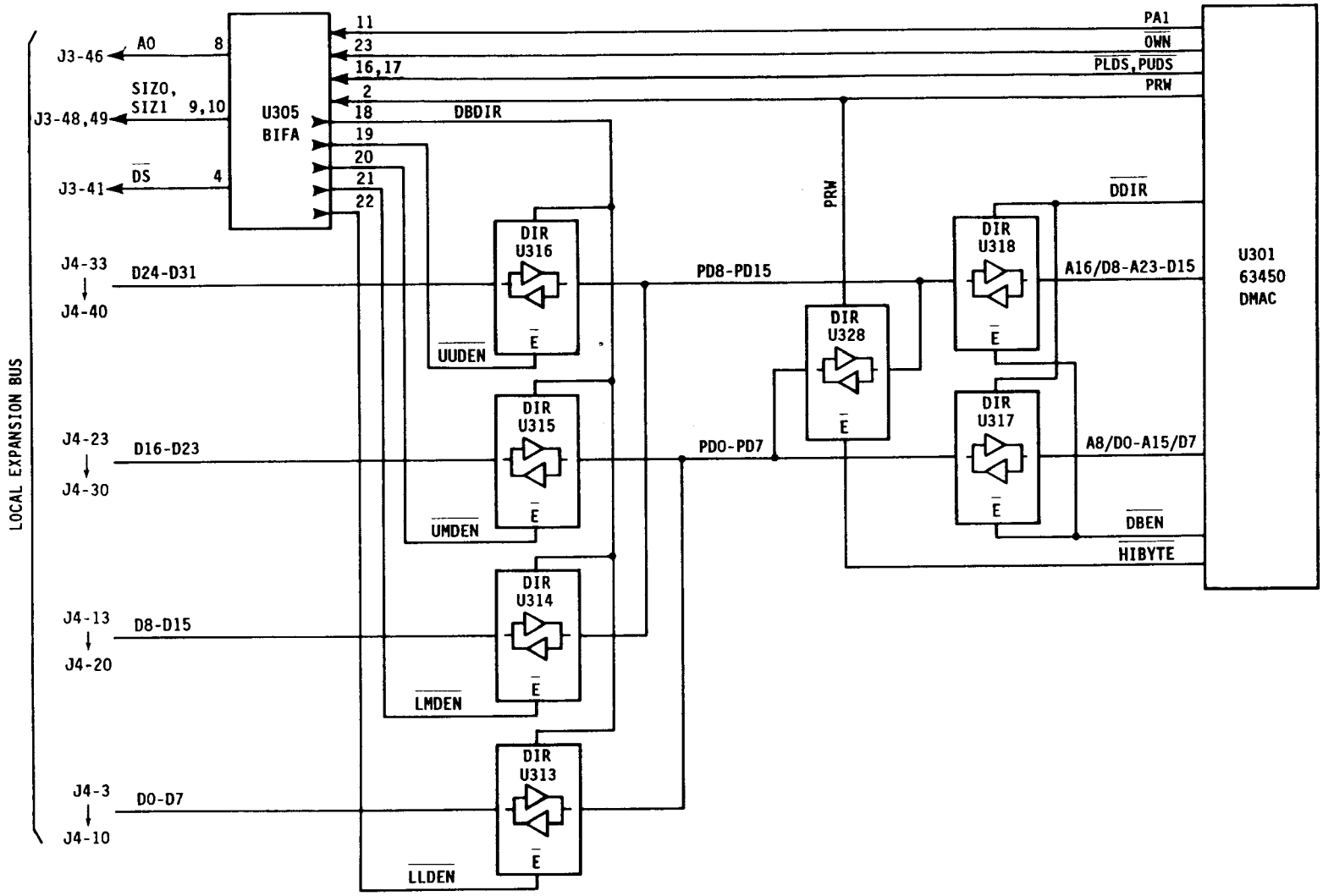


Figure 8-4b. DMA Mode Local Bus Interface - Data Interface

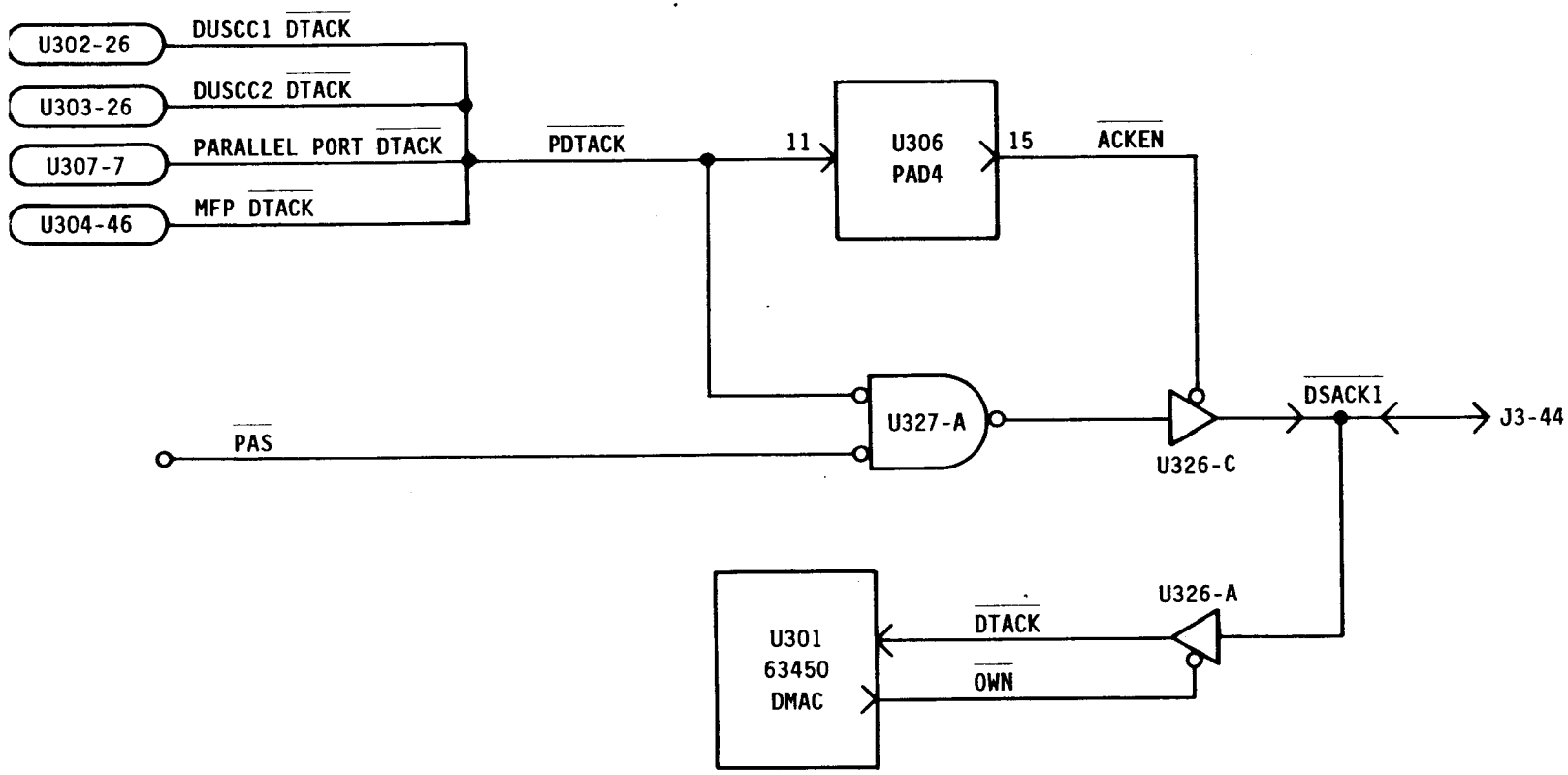


Figure 8-4c. DMA Mode Local Bus Interface - Data Acknowledge

Data buffers U313-U316 steer data between the 16-bit peripheral data bus and the 32-bit local data bus so that the DMAC can access contiguous memory locations. U313 and U314 are enabled for memory accesses at even word addresses (A1=0), and U315 and U316 are enabled for odd word addresses (A1=1). Only one data buffer is enabled for byte transfers. A simplified schematic of the DMA mode data interface circuit is shown in Figure 8-4b.

Devices accessed during a DMA cycle acknowledge a data transfer with $\overline{\text{DSACK1}}$, which is directed to the 63450 DMAC $\overline{\text{DTACK}}$ line (U301-19) with U326-A. A simplified schematic of the DMA mode data acknowledge circuit is shown in Figure 8-4c.

8.2 DIRECT MEMORY ACCESS CONTROLLER

The System I/O Module direct memory access controller (DMAC) provides a means of efficiently servicing I/O devices. Operations controlled by the DMAC are concurrent with and transparent to processes running on the Processor Module. DMAC operations also have shorter service request latency than interrupt-driven operations. Therefore, the DMAC generally allows I/O ports to operate at higher data rates.

The System I/O Module uses the Hitachi HD63450 DMAC device, which is compatible with the Motorola MC68450. Both the HD63450 and the MC68450 have four DMA channels, each of which provides the following types of data transfers:

- Device-to-memory
- Memory-to-device
- Memory-to-memory

NOTE

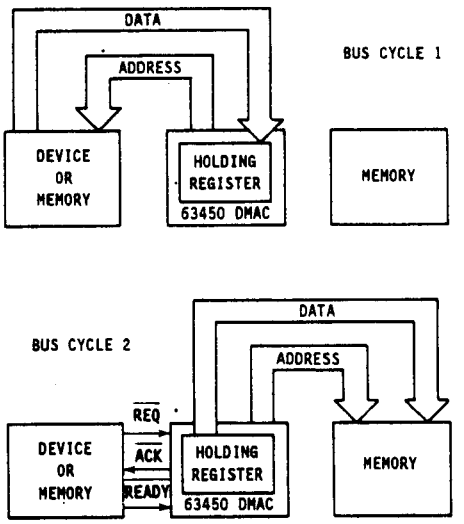
In the SANDAC V, memory-to-memory transfers can be accomplished faster by the Processor Module MPU.

The 63450 DMAC operates in either the dual address (explicit) mode or the single address (implicit) mode. In the dual address mode, both the source and the destination of the transfer are explicitly addressed. The 63450 first addresses the source and transfers the data to an internal 63450 holding register. The 63450 then addresses the destination and transfers the data from the holding register to complete the transfer. Figure 8-5a illustrates the dual address mode of operation. Figure 8-6 details 63450 DMAC operation during a dual address transfer in which data are transferred from an I/O device to memory.

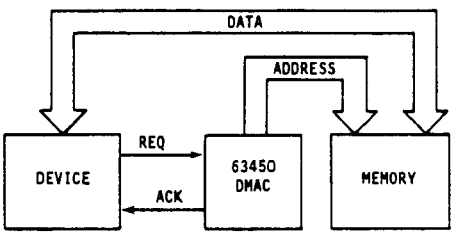
In the single address mode, addressing the I/O device requesting the DMA transfer is not required. Instead, a request/acknowledge protocol between the 63450 and the device

is used. For a transfer, the I/O device asserts a request to the DMAC. The DMAC places the required source or destination address on the bus and acknowledges the request. The data for the transfer is then placed on the bus and transferred directly between the source and the destination. Figure 8-5b illustrates the single address mode of operation.

With the 63450 DMAC, single address operation can use a two-signal protocol ($\overline{REQ}/\overline{ACK}$) or a three-signal protocol ($\overline{REQ}/\overline{ACK}/\overline{READY}$). The System I/O Module supports only the three-signal protocol. Figures 8-7 and 8-8 detail 63450 DMAC operation during a single address transfer using the $\overline{REQ}/\overline{ACK}/\overline{READY}$ protocol.



a. Dual Address (Explicit) DMA Addressing



b. Single Address (Implicit) DMA Addressing

Figure 8-5. DMAC Addressing Modes

I/O DEVICE **63450 DMAC** **MEMORY**

REQUEST DMA TRANSFER

1. Assert request to 63450 via $\overline{REQ}$n.

ADDRESS DEVICE

1. Set R/W to read.
2. Drive A23-A1.
3. Drive FC2-FC0.
4. Assert $\overline{AS}$.
5. Assert data strobes ($\overline{UDS}$ and/or $\overline{LDS}$).
6. Acknowledge request via $\overline{ACK}$.

PRESENT DATA

1. Decode address.
2. Drive data bus.
3. Assert $\overline{DTACK}$.

ACQUIRE DATA

1. Load data into holding register.
2. Assert Data Transfer Complete ($\overline{DTC}$).
3. Negate data strobes.
4. Negate $\overline{AS}$, $\overline{ACK}$, and $\overline{DTC}$.

TERMINATE CYCLE

1. Remove data from data bus.
2. Negate $\overline{DTACK}$.

ADDRESS MEMORY

1. Drive A23-A1.
2. Drive FC2-FC0.
3. Assert $\overline{AS}$.
4. Set R/W to write.
5. Place data on data bus.
6. Assert data strobes ($\overline{UDS}$ and/or $\overline{LDS}$).

Figure 8-6. 63450 DMAC Dual Address Transfer (1 of 2)

I/O DEVICE **63450 DMAC** **MEMORY**

ADDRESS MEMORY

ACCEPT DATA

1. Decode address.
2. Store data.
3. Assert $\overline{DTACK}$.

TERMINATE OUTPUT TRANSFER

1. Assert $\overline{DTC}$.
2. Negate data strobes.
3. Negate $\overline{AS}$, $\overline{ACK}$, $\overline{DTC}$.
4. Remove data from data bus.
5. Set R/W to read (negate write).

TERMINATE CYCLE

1. Negate $\overline{DTACK}$.

Figure 8-6. 63450 DMAC Dual Address Transfer (2 of 2)

I/O DEVICE **63450 DMAC** **MEMORY**

REQUEST DMA TRANSFER

1. Request DMA transfer via $\overline{REQ}$n to 63450.

ADDRESS MEMORY

1. Drive A23-A1.
2. Drive FC2-FC0.
3. Assert $\overline{AS}$.
4. Set R/W to write.
5. Acknowledge request via $\overline{ACK}$n.

PRESENT DATA

1. Place data on data bus.
2. Assert $\overline{READY}$.

ENABLE DATA

1. Assert data strobes ($\overline{UDS}$ and/or $\overline{LDS}$).

ACCEPT DATA

1. Decode address.
2. Load data.
3. Assert $\overline{DTACK}$.

TERMINATE TRANSFER

1. Assert Data Transfer Complete ($\overline{DTC}$).
2. Negate data strobes.
3. Negate $\overline{AS}$, $\overline{ACK}$, $\overline{DTC}$.

TERMINATE CYCLE

1. Negate $\overline{DTACK}$.

Figure 8-7. 63450 Single Address Transfer - I/O to Memory

I/O DEVICE **63450 DMAC** **MEMORY**

REQUEST DMA TRANSFER

1. Request DMA transfer via $\overline{REQ}$n to 63450.

ADDRESS MEMORY

1. Set R/W to read.
2. Drive A23-A1.
3. Drive FC2-FC0.
4. Assert $\overline{AS}$.
5. Assert data strobes ($\overline{UDS}$ and/or $\overline{LDS}$).
6. Acknowledge request via $\overline{ACK}$n.

PRESENT DATA

1. Decode address.
2. Place data on data bus.
3. Assert $\overline{DTACK}$.

ACQUIRE DATA

1. Load data.
2. Assert $\overline{READY}$.

TERMINATE TRANSFER

1. Assert Data Transfer Complete ($\overline{DTC}$).
2. Negate data strobes.
3. Negate $\overline{AS}$, $\overline{ACK}$, $\overline{DTC}$.

TERMINATE CYCLE

1. Negate $\overline{DTACK}$.

Figure 8-8. 63450 Single Address Transfer - Memory to I/O

An address map of the 63450 DMAC showing the location and sizes of its internal registers is shown in Figure 8-9. Complete information on the 63450 DMAC is in the Hitachi publication, *HD63450, HD63450Y Direct Memory Access Controller (DMAC).*

An addressing summary for the System I/O Module DMAC is given in Table 8-4. In MPU mode, DMAC registers are accessed like any other peripheral device. Details of DMAC implementation on the System I/O Module are given in the following subsections.

8.2.1 63450 DMAC Implementation

A block diagram of the System I/O Module DMAC circuit is shown in Figure 8-10. The 63450 DMAC has a multiplexed address and data bus. Latches U309 and U310 and buffers U317 and U318 provide the demultiplexing required for compatibility with the rest of the system. Since the DMAC has only 24 address bits, the upper byte of the 32-bit local bus address is generated by U334 as a fixed 80 hex (local Processor Module alias, see subsection 2.1.4). This restricts the DMAC to accessing the local address space. U328 is used during single address transfers to steer data between 8-bit peripherals and the upper and lower byte positions of the peripheral data bus. This is necessary for access to contiguous memory locations.

The 63450 DMAC can generate service requests internally or respond to external requests. Since the Processor Module MPU is more efficient for the types of transfers possible with internal requests, the DMAC should be used exclusively with external requests. This requires that the DMAC external request inputs, $\overline{REQ0}$-$\overline{REQ3}$ (T139-T136), be wired to the service request outputs of the devices selected for service. When operating with external requests, the DMAC supports both dual address and single address transfers. The System I/O Module parallel port (8.3), 68562 DUSCCs (8.4.1), and 68901 MFP (8.4.2) can all perform DMA transfers in the dual address mode. Only the 68562 DUSCCs support the faster single address transfers with a $\overline{REQ}$/$\overline{ACK}$/$\overline{READY}$ protocol.

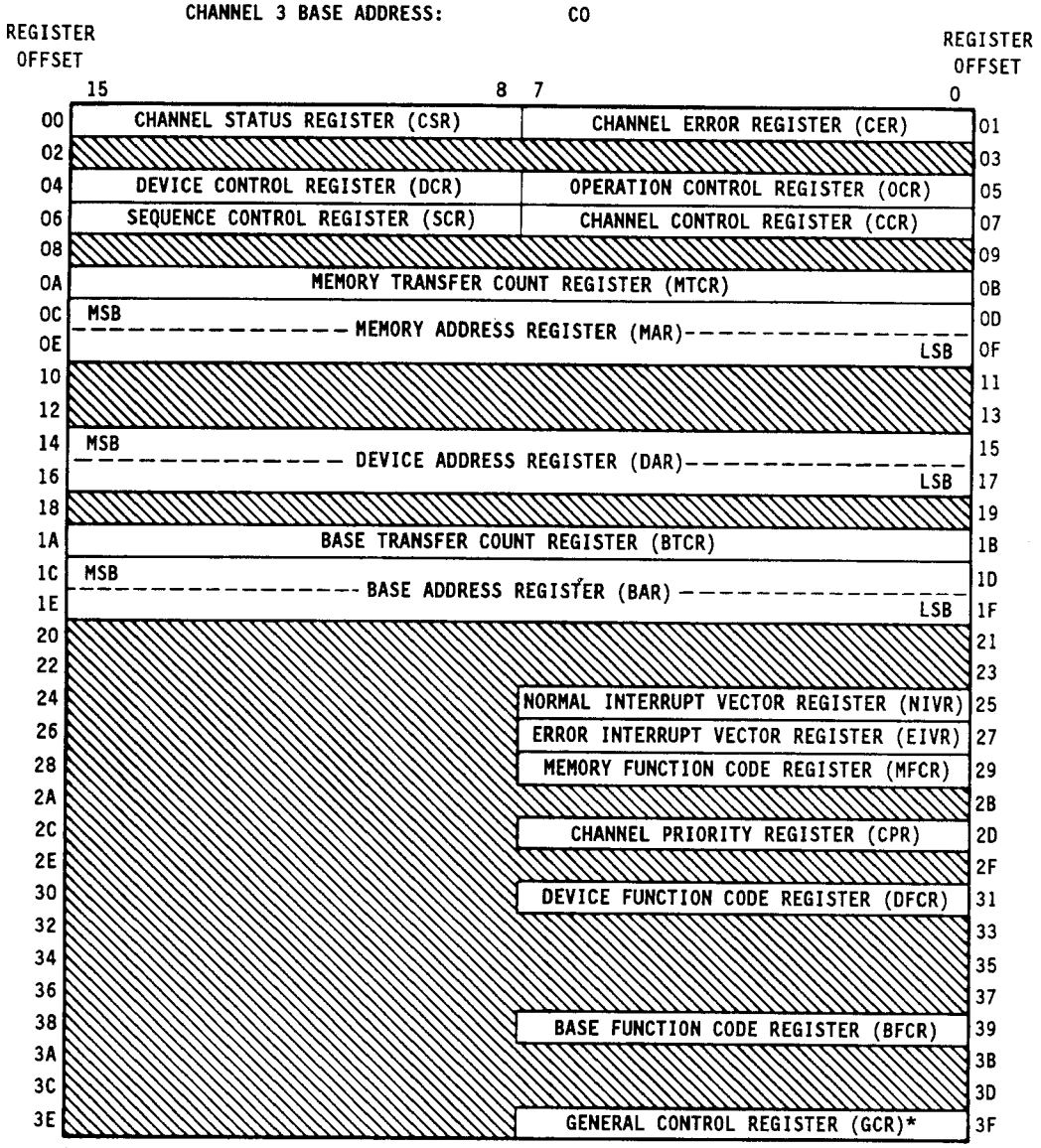
In the single address mode, a DUSCC requests a DMA transfer by asserting the one of the DMAC request inputs ($\overline{REQ3}$-$\overline{REQ0}$). The DMAC obtains the bus and responds with one of the $\overline{ACK3}$-$\overline{ACK0}$ outputs. The DMAC then waits for a $\overline{READY}$ response from the DUSCC. $\overline{READY}$ is sensed on the DMAC Peripheral Control Line ($\overline{PCL}$) pins.

NOTE

The $\overline{PCL}$ pins can function as inputs or outputs. On the System I/O Module, the PCL pins should always be programmed as inputs.

63450 DMAC BASE ADDRESS: On,FFE,000 HEX (n = PROCESSOR ID)
(80,FFE,000)

CHANNEL 0 BASE ADDRESS: 00
CHANNEL 1 BASE ADDRESS: 40
CHANNEL 2 BASE ADDRESS: 80
CHANNEL 3 BASE ADDRESS: C0



*GCR IS LOCATED AT FF ONLY.

Figure 8-9. 63450 DMAC Address Map

TABLE 8-4. 63450 DMAC REGISTER ADDRESSING

63450 DMAC Register	Size in Bits	Address (hex) by DMAC Channel			
		Channel 0	Channel 1	Channel 2	Channel 3
CSR	8	0n,FFE,000	0n,FFE,040	0n,FFE,080	0n,FFE,0C0
CER	8	0n,FFE,001	0n,FFE,041	0n,FFE,081	0n,FFE,0C1
DCR	8	0n,FFE,004	0n,FFE,044	0n,FFE,084	0n,FFE,0C4
OCR	8	0n,FFE,005	0n,FFE,045	0n,FFE,085	0n,FFE,0C5
SCR	8	0n,FFE,006	0n,FFE,046	0n,FFE,086	0n,FFE,0C6
CCR	8	0n,FFE,007	0n,FFE,047	0n,FFE,087	0n,FFE,0C7
MTCR	16	0n,FFE,00A	0n,FFE,04A	0n,FFE,08A	0n,FFE,0CA
MAR	32	0n,FFE,00C	0n,FFE,04C	0n,FFE,08C	0n,FFE,0CC
DAR	32	0n,FFE,014	0n,FFE,054	0n,FFE,094	0n,FFE,0D4
BTCR	16	0n,FFE,01A	0n,FFE,05A	0n,FFE,09A	0n,FFE,0DA
BAR	32	0n,FFE,01C	0n,FFE,05C	0n,FFE,09C	0n,FFE,0DC
NIVR	8	0n,FFE,025	0n,FFE,065	0n,FFE,0A5	0n,FFE,0E5
EIVR	8	0n,FFE,027	0n,FFE,067	0n,FFE,0A7	0n,FFE,0E7
MFCR	8	0n,FFE,029	0n,FFE,069	0n,FFE,0A9	0n,FFE,0E9
CPR	8	0n,FFE,02D	0n,FFE,06D	0n,FFE,0AD	0n,FFE,0ED
DFCR	8	0n,FFE,031	0n,FFE,071	0n,FFE,0B1	0n,FFE,0F1
BFCR	8	0n,FFE,039	0n,FFE,079	0n,FFE,0B9	0n,FFE,0F9
GCR	8	0n,FFE,0FF	0n,FFE,0FF	0n,FFE,0FF	0n,FFE,0FF

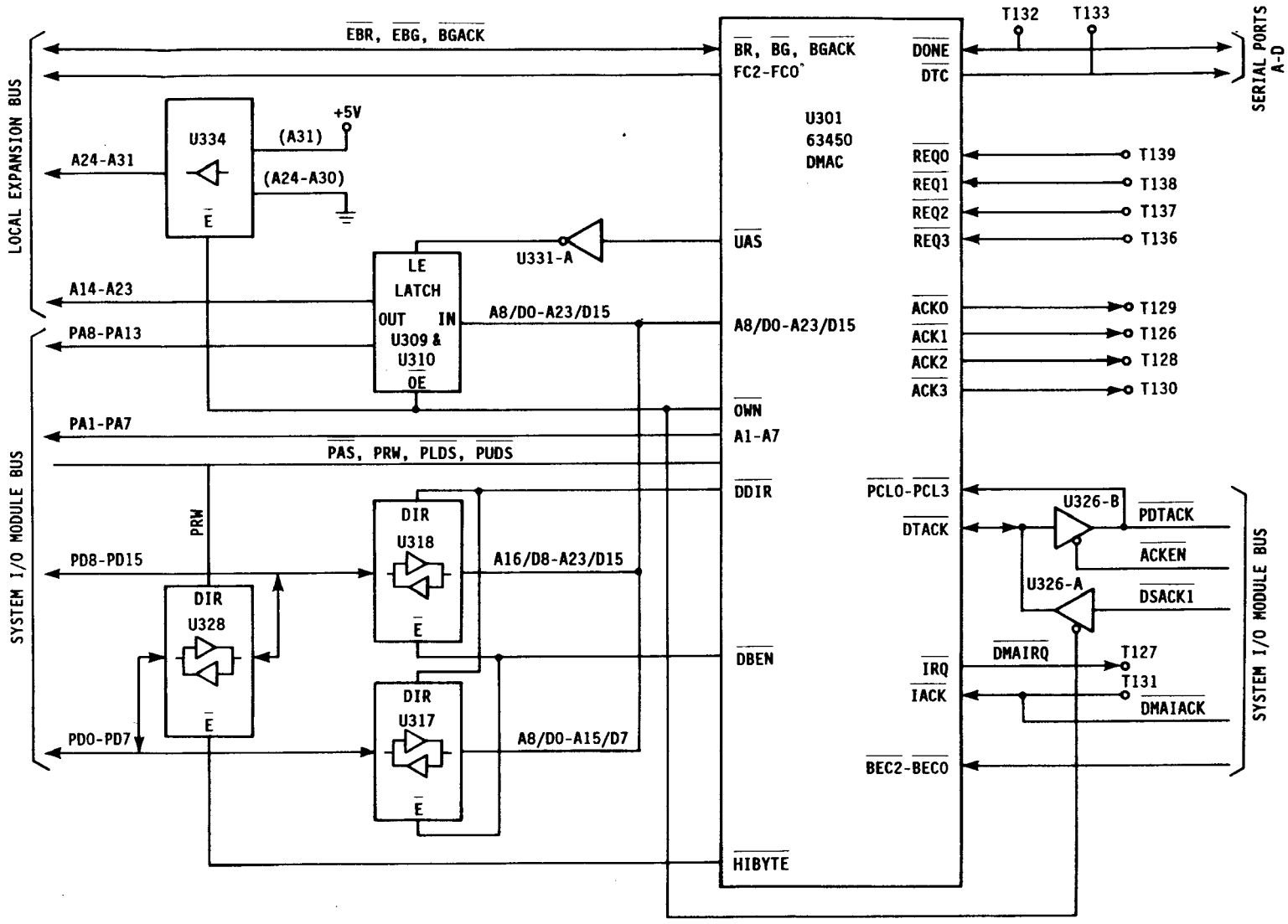


Figure 8-10. DMAC Circuit Block Diagram

8.2.2 Restrictions

DMAC usage on the System I/O Module is subject to the following restrictions:

1. The DMAC should be programmed to operate in burst mode when used with 68562 DUSCC devices that have no revision level (no Rev). These devices may generate a spurious pulse on the $\overline{REQ}$n line at the end of a transfer. If the DMAC is in cycle steal mode, this may be recognized as a valid request because the request input is edge sensitive. In burst mode, the input is level sensitive and the pulse will not be recognized because it is negated before the DMAC can arbitrate for the bus. This anomaly has been fixed in Rev A 68562 devices, which became available in 1987.

2. Array-chained and linked-array chained transfers are not available in single address (implicit) mode. This is because no provision has been made to provide a $\overline{READY}$ input when reading the chaining information from memory.

8.2.3 Bus Exceptions

The 63450 DMAC uses three bus exception control signals, BEC0-BEC2, to detect abnormal conditions. These are encoded by the BIFB device (U308) from local bus signals $\overline{BERR}$, $\overline{HALT}$, $\overline{RESET}$, and $\overline{BR}$ as shown below:

BIFB Input				BIFB Output			Condition
$\overline{BERR}$	$\overline{HALT}$	$\overline{BR}$	$\overline{RESET}$	BEC2	BEC1	BEC0	
1	1	1	1	1	1	1	No Exception
0	1	X	1	1	0	1	Bus Error
0	0	1	1	0	1	1	Relinquish & Retry
1	0	1	1	1	1	0	Halt
1	X	0	1	1	1	0	Halt
X	X	X	0	0	0	0	Reset

(X = don't care.)

Logic equations for the BIFB are given in Table 8-5.

The $\overline{BR}$ signal is the bus request asserted to the local MPU when a remote MPU is requesting the local bus. A jumper installed from T145 to T151 allows this signal to halt the DMAC when it is bus master. When the global access is completed, the DMAC will rearbitrate for the local bus and finish its transfer.

NOTE

It is recommended that this jumper not be installed with Hitachi HD68450 devices because abnormal behavior has been observed at some temperatures. The problem has not been seen with the 63450 CMOS DMAC, which is being installed in all new System I/O Modules.

8.2.4 Hardware Jumpers

The hardware jumpers associated with the DMAC circuit are described in Appendix B.

TABLE 8-5. BIFB (U308) LOGIC EQUATIONS

INPUTS: RESET~@15, HALT~@16, BERR~@11, BR~@14, PAS~@2, SCCIACK~@3, DMAIACK~@4, DMACS~@5, PPIACK~@23, MFPIACK~@22, OWN~@7

OUTPUTS: BEC0~@8, BEC1~@9, BEC2~@10, RSTP~@17, IACK~@21, DACKEN~@20

NETWORK:

```
RESET = INP(RESET~)            % local reset %
HALT = INP(HALT~)              % local halt %
BERR = INP(BERR~)              % local bus error %
BR = INP(BR~)                  % 68020 BR, used to DMAC on
                                 global BR %
OWN = INP(OWN~)                % DMAC is bus master %
PAS = INP(PAS~)                % peripheral address strobe %
SCCIACK = INP(SCCIACK~)        % IACK to DUSCCs %
DMAIACK = INP(DMAIACK~)        % IACK to DMAC %
DMACS = INP(DMACS~)            % DMA CS %
PPIACK = INP(PPIACK~)          %IACK to parallel port %
MFPIACK = INP(MFPIACK~)        % IACK to MFP %

BEC0~ = CONF(BEC0c,VCC)        % bus exception code to DMAC %
BEC1~ = CONF(BEC1c,VCC)
BEC2~ = CONF(BEC2c,VCC)
RSTP~ = CONF(RSTPc,VCC)        % peripheral reset %
IACK~ = CONF(IACKc,VCC)        % SIO IACK cycle %
DACKEN~ = CONF(DACKENc,VCC)    % enable to DMAC DTACK buffer %
```

EQUATIONS:

```
BEC0c = /(OWN'*PAS'*RESET*BERR*(HALT'*BR+BR') + RESET');
BEC1c = /(OWN'*PAS'*RESET*BERR'*HALT+RESET');
BEC2c = /(OWN'*PAS'*RESET*BERR'*HALT'*BR+RESET');
RSTPc = RESET;
IACKc = /(PAS'*(SCCIACK'+MFPIACK'+DMACIACK'+PPIACK'));
DACKENc = /(DMACS'+DMAIACK');
```

8.3 PARALLEL PORT

The System I/O Module parallel port extends the peripheral address, data, and control buses to connector J305 for high-speed communication with external devices connected to SANDAC V. Devices connected to the parallel port reside in the 8K bytes of local memory space from 0n,FFC,000 to 0n,FFD,FFF hex, where "n" is the host Processor ID. A block diagram of the parallel port circuit is shown in Figure 8-11.

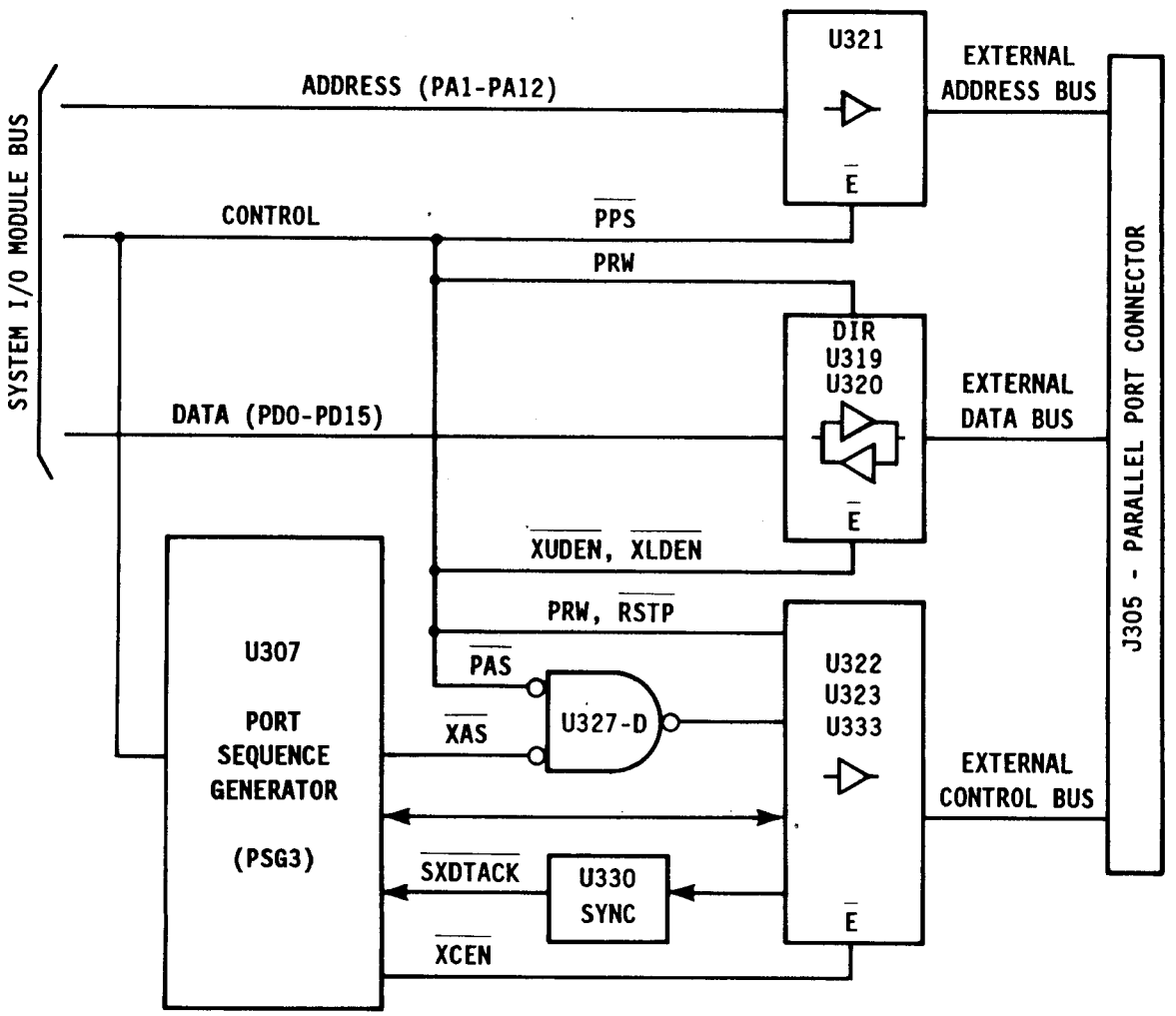


Figure 8-11. Parallel Port Block Diagram

8.3.1 Parallel Port Connector

The parallel port connector, J305, is shown in Figure 8-12. Descriptions of the connector pins are given in Table 8-6.

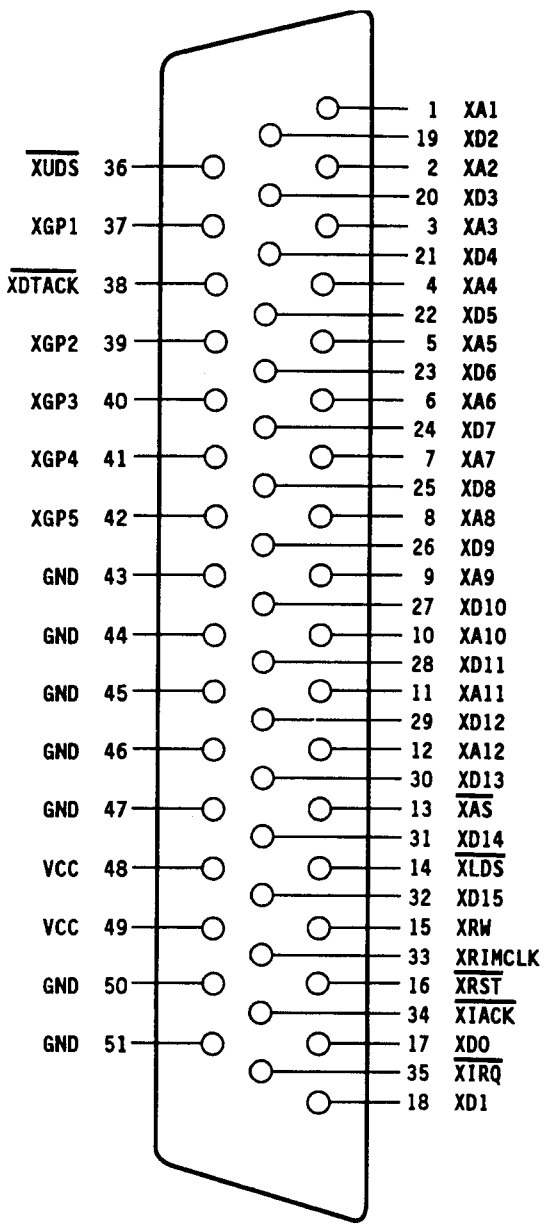


Figure 8-12. Parallel Port Connector (J305)

TABLE 8-6. PARALLEL PORT CONNECTOR (J305) PIN DESCRIPTIONS

Pin	Mnemonic	I/O*	Description
1	XA1	O	External Address Bit 1 - External address bus (XA12-XA1) provides 8K addressing for external devices.
2	XA2	O	External Address Bit 2
3	XA3	O	External Address Bit 3
4	XA4	O	External Address Bit 4
5	XA5	O	External Address Bit 5
6	XA6	O	External Address Bit 6
7	XA7	O	External Address Bit 7
8	XA8	O	External Address Bit 8
9	XA9	O	External Address Bit 9
10	XA10	O	External Address Bit 10
11	XA11	O	External Address Bit 11
12	XA12	O	External Address Bit 12
13	$\overline{XAS}$	O	External Address Strobe - Indicates valid address and read/write information is on the port.
14	$\overline{XLDS}$	O	External Lower Data Strobe - Indicates data are to be transferred on the lower 8 bits of data bus (XD0-XD7). For a read, indicates slave device should drive the data bus. For a write, indicates data is valid.
15	XRW	O	External Read Write - Defines direction of data transfer. A high level indicates a read; a low level indicates a write.
16	$\overline{XRST}$	O	External Reset - Asserted at powerup and when MPU executes a RESET instruction.
17	XD0	I/O	External Data Bit 0 - External data bus (XD15-XD0) provides 16-bit bidirectional data path between the port and external devices.
18	XD1	I/O	External Data Bit 1
19	XD2	I/O	External Data Bit 2
20	XD3	I/O	External Data Bit 3
21	XD4	I/O	External Data Bit 4

TABLE 8-6. CONTINUED

Pin	Mnemonic	I/O*	Description
22	XD5	I/O	External Data Bit 5 - External data bus (XD15-XD0) provides 16-bit bidirectional data path between the port and external devices.
23	XD6	I/O	External Data Bit 6
24	XD7	I/O	External Data Bit 7
25	XD8	I/O	External Data Bit 8
26	XD9	I/O	External Data Bit 9
27	XD10	I/O	External Data Bit 10
28	XD11	I/O	External Data Bit 11
29	XD12	I/O	External Data Bit 12
30	XD13	I/O	External Data Bit 13
31	XD14	I/O	External Data Bit 14
32	XD15	I/O	External Data Bit 15
33	XRIMCLK	I	External RIMS Clock - General-purpose input for a synchronizing clock from an external system, such as a roll-stabilized intertial measurement system (RIMS).
34	$\overline{\text{XIACK}}$	O	External Interrupt Acknowledge - MPU response to an interrupt request from an external device (XIRQ, J305-35). Slave device should respond with interrupt vector on XD0-XD7.
35	$\overline{\text{XIRQ}}$	I	External Interrupt Request - Devices asserting this signal must respond to $\overline{\text{XIACK}}$ with an interrupt vector.
36	$\overline{\text{XUDS}}$	O	External Upper Data Strobe - Indicates data are to be transferred on upper 8 bits of the data bus (XD8-XD15). For a read, indicates that the slave device should drive the data bus. For a write, indicates data are valid.
37	XGP1	I/O	External General-Purpose Pin 1 - Uncommitted connector pin available for user-defined input or output.

TABLE 8-6. CONTINUED

Pin	Mnemonic	I/O*	Description
38	$\overline{\text{XDTACK}}$	I	External Data Transfer Acknowledge - Asserted by slave device to indicate data transfer complete.
39	XGP2	I/O	External General-Purpose Pin 2 - Uncommitted connector pin available for user-defined input or output.
40	XGP3	I/O	External General-Purpose Pin 3
41	XGP4	I/O	External General-Purpose Pin 4
42	XGP5	I/O	External General-Purpose Pin 5
43	GND	I/O	Signal and power ground.
44	GND	I/O	
45	GND	I/O	
46	GND	I/O	
47	GND	I/O	
48	VCC	O	Nominal 5-Volt power for external devices. Recommended maximum current drain is 200 milliamps.
49	VCC	O	
50	GND	I/O	Signal and power ground.
51	GND	I/O	

*I/O: I = Input; O = Output

8.3.2 Parallel Port Operation

The Port Sequence Generator (PSG3), U307, generates all port control signals. Descriptions of the parallel port signals are given in Table 8-7. Figures 8-13 through 8-15 are flow diagrams that illustrate parallel port read, write, and interrupt acknowledge operations, respectively. A detailed timing diagram of parallel port operation is shown in Figure 8-16. The state diagram for PSG3 is shown in Figure 8-17; logic equations for the device (U307) are given in Table 8-8.

TABLE 8-7. PARALLEL PORT SIGNAL DESCRIPTIONS

Signal	Source	Dest.	Description
A, B, C	U307-4,5,6		PSG3 States - Indicate the state of PSG3 state machine.
CLK8	J3-60	U307-1	Clock, 8 MHz.
ESIO	J4-45	U329-2	Expansion Bus System I/O Select - From host Processor Module indicating access in System I/O Module address space.
$\overline{PAS}$	U326-3	U327-2	Peripheral Address Strobe - Indicates valid address and read/write information is on the System I/O Module.
$\overline{PDTACK}$	U307-7	U327-13	Peripheral Data Transfer Acknowledge. Indicates data transfer complete (converted to $\overline{DSACK1}$).
$\overline{PLDS}$	U305-17	U307-10	Peripheral Lower Data Strobe - Indicates data to be transferred on lower 8 bits of peripheral data bus (PD0-PD7).
$\overline{PPIDC}$	U307-15	T107	Parallel Port Interrupt Daisy Chain - When no interrupt is pending from a device on the parallel port, this signal is asserted in response to $\overline{SPIACK}$ to propagate the interrupt acknowledge cycle to the next device in the daisy chain.

TABLE 8-7. CONTINUED

Signal	Source	Dest.	Description
$\overline{PPS}$	U306-16	U307-2	Parallel Port Select - From PAD4 indicating access in parallel port address space. (Also goes to U321-1, U321-19, and U322-1.)
PRW	U312-14	U307-3	Peripheral Read/Write - Defines direction of data transfer. A high level indicates a read; a low level indicates a write.
$\overline{PUDS}$	U305-16	U307-11	Peripheral Upper Data Strobe - Indicates data to be transferred on upper 8 bits of peripheral data bus (PD8-PD15).
$\overline{SPIACK}$	U329-9	U307-8	Synchronized Port Interrupt Acknowledge - Indicates MPU cycle to read interrupt vector. Synchronized to rising edge of CLK8.
$\overline{SXDTACK}$	U330-9	U307-14	Synchronized External Data Transfer Acknowledge - $\overline{XDTACK}$ delayed until the next rising edge of CLK8.
$\overline{XCEN}$	U307-16	U322-19	External Control Enable - Switches buffers for $\overline{XAS}$, $\overline{XLDS}$, $\overline{XUDS}$, and XRW from high impedance to active state when port is accessed.
$\overline{XLDEN}$	U307-17	U319-19	External Lower Data Enable - Switches buffers for XD0-XD7 from high impedance to active state when lower byte is transferred.
$\overline{XUDEN}$	U307-18	U320-19	External Upper Data Enable - Switches buffers for XD8-XD15 from high impedance to active state when the upper byte is transferred.

LOCAL BUS MASTER **PARALLEL PORT** **EXTERNAL DEVICE**

ADDRESS PARALLEL PORT

1. Set PRW to read.
2. Drive PA1-PA12.
3. Assert $\overline{PAS}$.
4. Assert data strobes:
   $\overline{PUDS}$ for upper byte read.
   $\overline{PLDS}$ for lower byte read.
   $\overline{PUDS}$ and $\overline{PLDS}$ for word read.
5. Assert $\overline{PPS}$.

ADDRESS EXTERNAL DEVICE

1. Enable external address buffers (assert $\overline{PPS}$); drive XA1-XA12.
2. Assert $\overline{XCEN}$.
3. Set XRW to read.
4. Enable external data buffers:
   $\overline{XUDEN}$ for upper byte read.
   $\overline{XLDEN}$ for lower byte read.
   $\overline{XUDEN}$ and $\overline{XLDEN}$ for word read.
5. Wait until $\overline{XDTACK}$ is negated.
6. Assert $\overline{XAS}$.
7. Assert external data strobes:
   $\overline{XUDS}$ for upper byte read.
   $\overline{XLDS}$ for lower byte read.
   $\overline{XUDS}$ and $\overline{PLDS}$ for word read.

PRESENT DATA

1. Decode address.
2. Drive data:
   XD8-XD15 for upper byte read.
   XD0-XD7 for lower byte read.
   XD0-XD15 for word read.
3. Assert $\overline{XDTACK}$.

CONDITION DATA TRANSFER ACKNOWLEDGE

1. Synchronize $\overline{XDTACK}$ to CLK8 ($\overline{SXDTACK}$).
2. Delay 125 ns (data settling time).
3. Assert $\overline{PDTACK}$.

Figure 8-13. Parallel Port Read (1 of 2)

LOCAL BUS MASTER **PARALLEL PORT** **EXTERNAL DEVICE**

CONDITION DATA TRANSFER ACKNOWLEDGE

ACQUIRE DATA

1. Latch data.
2. Negate $\overline{PAS}$.
3. Negate $\overline{PUDS}$, $\overline{PLDS}$.
4. Negate $\overline{PPS}$.

NEGATE STROBES

1. Negate $\overline{XAS}$.
2. Negate $\overline{PDTACK}$.
3. Negate $\overline{XUDS}$, $\overline{XLDS}$.

TERMINATE CYCLE

1. Remove data from XD0-XD15.
2. Negate $\overline{XDTACK}$.

4. Negate external address buffer enable ($\overline{PPS}$).
5. Negate $\overline{XUDEN}$, $\overline{XLDEN}$.
6. Delay 125 ns.
7. Negate $\overline{XCEN}$.

START NEXT CYCLE

Figure 8-13. Parallel Port Read (2 of 2)

LOCAL BUS MASTER **PARALLEL PORT** **EXTERNAL DEVICE**

ADDRESS PARALLEL PORT

1. Set PRW to write.
2. Drive PA1-PA12.
3. Assert $\overline{PAS}$.
4. Assert $\overline{PPS}$.
5. Place data on PD0-PD15.
6. Assert data strobes:
   $\overline{PUDS}$ for upper byte write.
   $\overline{PLDS}$ for lower byte write.
   $\overline{PUDS}$ and PLDS for word write.

ADDRESS EXTERNAL DEVICE

1. Enable external address buffers with $\overline{PPS}$ and drive XA1-XA12.
2. Assert $\overline{XCEN}$.
3. Set XRW to write.
4. Assert external data buffer enables and drive external data lines:
   $\overline{XUDEN}$ to drive XD8-XD15 for upper byte write.
   $\overline{XLDEN}$ to drive XD0-XD7 for lower byte write.
   $\overline{XUDEN}$ and $\overline{XLDEN}$ to drive XD0-XD15 for word write.
5. Wait until $\overline{XDTACK}$ is negated.
6. Assert $\overline{XAS}$.
7. Wait 125 ns (data settling time).
8. Assert external data strobes:
   $\overline{XUDS}$ for upper byte write.
   $\overline{XLDS}$ for lower byte write.
   $\overline{XUDS}$ and $\overline{PLDS}$ for word write.

ACCEPT DATA

1. Decode address.
2. Latch data.
3. Assert $\overline{XDTACK}$.

CONDITION DATA TRANSFER ACKNOWLEDGE

1. Synchronize $\overline{XDTACK}$ to CLK8 ($\overline{SXDTACK}$).
2. Assert $\overline{PDTACK}$.

Figure 8-14. Parallel Port Write (1 of 2)

LOCAL BUS MASTER **PARALLEL PORT** **EXTERNAL DEVICE**

CONDITION DATA TRANSFER ACKNOWLEDGE

TERMINATE OUTPUT TRANSFER

1. Negate $\overline{PAS}$.
2. Negate $\overline{PUDS}$, $\overline{PLDS}$.
3. Remove data from PD0-PD15.
4. Negate $\overline{PPS}$.

NENGATE STROBES

1. Negate $\overline{XAS}$.
2. Negate $\overline{PDTACK}$.
3. Negate $\overline{XUDS}$, $\overline{XLDS}$.

TERMINATE CYCLE

1. Negate $\overline{XDTACK}$.

4. Negate external address buffer enable.
5. Negate $\overline{XUDEN}$, $\overline{XLDEN}$.
6. Delay 125 ns.
7. Negate $\overline{XCEN}$.

START NEXT CYCLE

Figure 8-14 Parallel Port Write (2 of 2)

LOCAL BUS MASTER **PARALLEL PORT** **EXTERNAL DEVICE**

REQUEST INTERRUPT

1. Assert $\overline{XIRQ}$.

ACKNOWLEDGE INTERRUPT REQUEST

1. Set PRW to read.
2. Assert $\overline{SPIACK}$.
3. Assert $\overline{PAS}$.
4. Assert $\overline{PLDS}$.

ACKNOWLEDGE INTERRUPT

1. Assert $\overline{XCEN}$.
2. Set XRW to read.
3. Assert $\overline{XLDEN}$.
4. Wait until $\overline{XDTACK}$ negated.
5. Assert $\overline{XIACK}$.
6. Assert $\overline{XAS}$.
   (NOTE: System I/O Module Rev A01 has a wiring error that results in $\overline{XAS}$ not being asserted. This has been corrected on Rev A02.)
7. Assert $\overline{XLDS}$.

PROVIDE VECTOR

1. Place vector on XD0-XD7.
2. Assert $\overline{XDTACK}$.
3. Negate $\overline{XIRQ}$.

CONDITION DATA TRANSFER ACKNOWLEDGE

1. Synchronize $\overline{XDTACK}$ to CLK8 ($\overline{SXDTACK}$).
2. Delay 125 ns (data settling time).
3. Assert $\overline{PDTACK}$.

ACQUIRE VECTOR

1. Latch vector.
2. Negate $\overline{PAS}$.
3. Negate $\overline{PLDS}$.
4. Negate $\overline{SPIACK}$.

Figure 8-15. Parallel Port Interrupt Acknowledge (1 of 2)

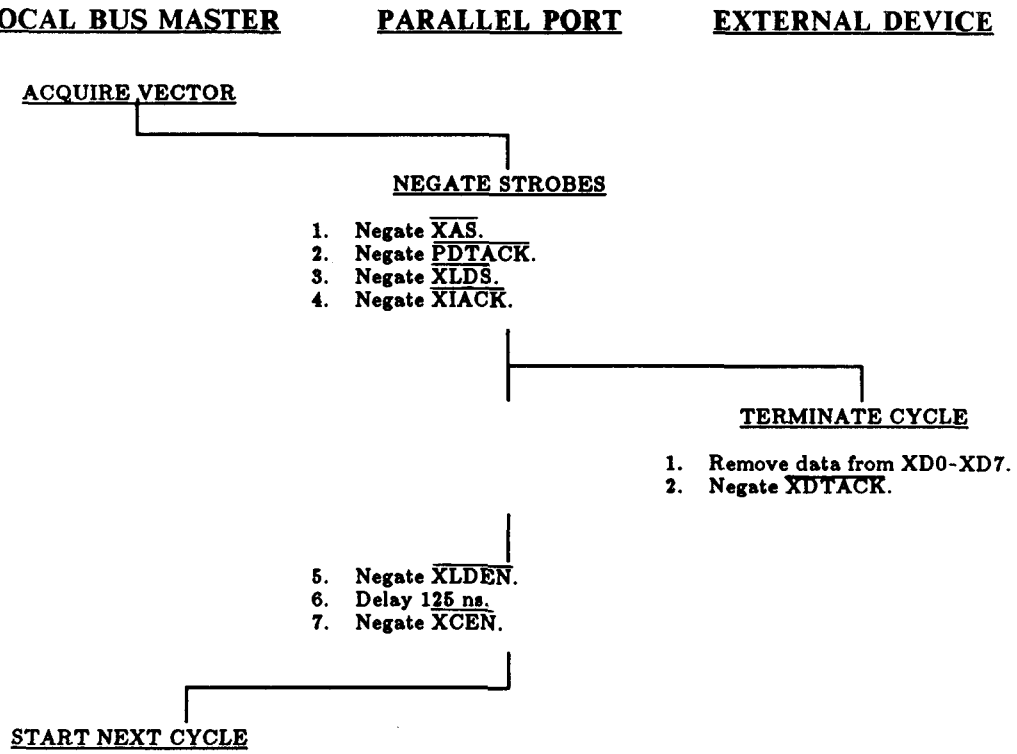


Figure 8-15. Parallel Port Interrupt Acknowledge (2 of 2)

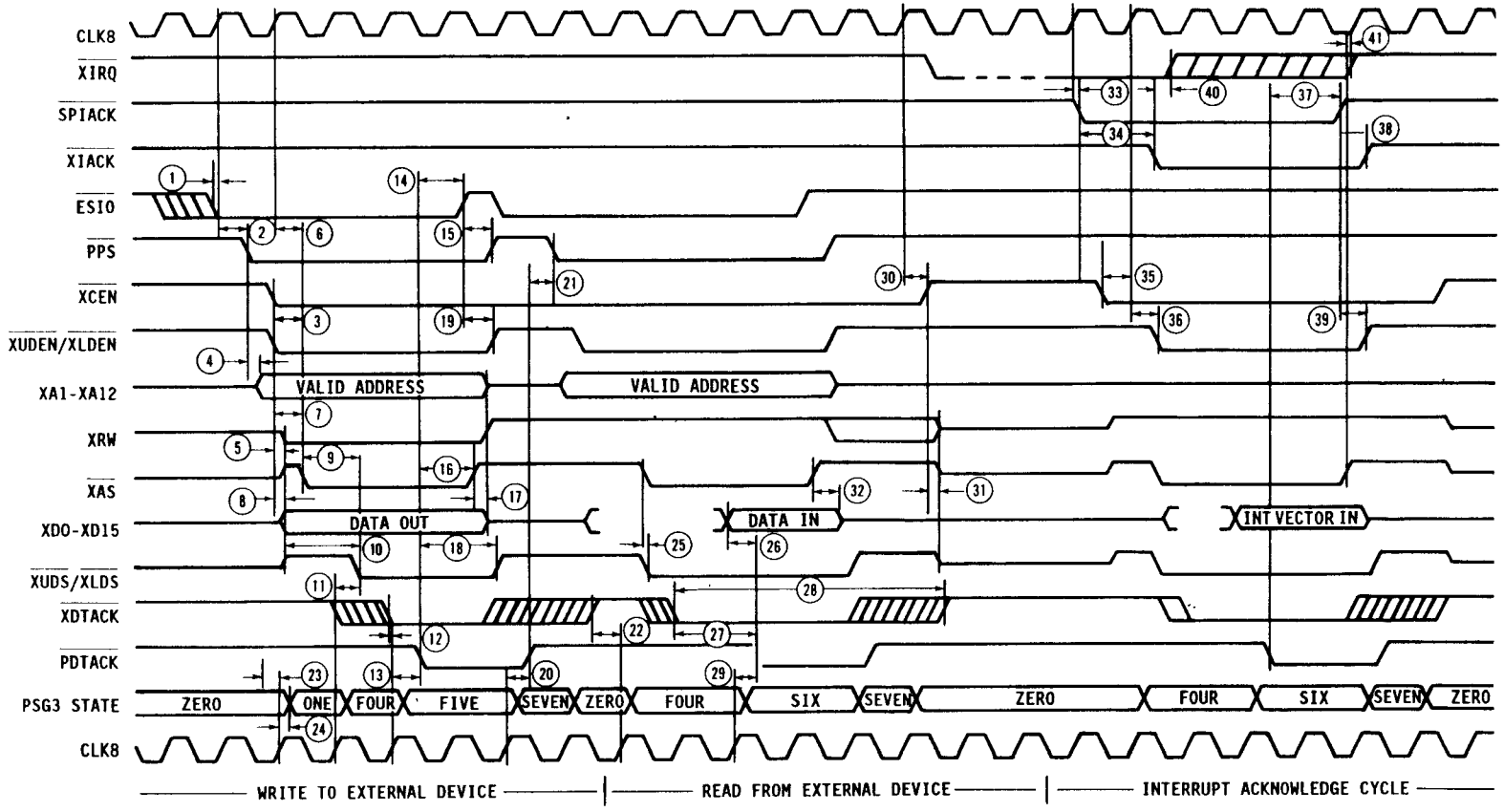


Figure 8-16. Parallel Port Timing Diagram

Parallel Port Timing Diagram References

Ref Num	Description	Min	Typ	Max	Unit	Notes
1	$\overline{ESIO}$ asserted before CLK8 to start cycle	5	30	125	ns	1,2
2	CLK8 to $\overline{PPS}$ asserted		40	65	ns	1,2
3	PPS asserted to $\overline{XCEN}$, $\overline{XUDEN}$/$\overline{XLDEN}$ asserted		35	55	ns	1,2,4
4	$\overline{PPS}$ asserted to XA1-XA12 asserted	1	10	20	ns	1,2
5	$\overline{XCEN}$ asserted to XRW, $\overline{XAS}$, $\overline{XUDS}$, $\overline{XLDS}$ enabled	1	10	20	ns	1,2,3
6	CLK8 to $\overline{XAS}$ asserted		55	70	ns	1,2,3
7	XA1-XA12 asserted to $\overline{XAS}$ asserted (settling time)	120			ns	1,2
8	$\overline{XUDEN}$/$\overline{XLDEN}$ asserted to XD8-XD15/XD0-XD7 asserted	1	10	15	ns	1,4
9	$\overline{XAS}$ assert. to $\overline{XUDS}$/$\overline{XLDS}$ asserted		125		ns	1,4
10	XD8-XD15/XD0-XD7 asserted to $\overline{XUDS}$/$\overline{XLDS}$ asserted (data settling time, write)	125	170		ns	1,4
11	CLK8 to $\overline{XUDS}$/$\overline{XLDS}$ asserted		55	70	ns	1,2,3,4
12	$\overline{XDTACK}$ asserted to CLK8 (setup time for synchronizing flip flop)	6	12	19	ns	1,2,3
13	CLK8 to $\overline{PDTACK}$ asserted		45	65	ns	1
14	$\overline{PDTACK}$ asserted to $\overline{ESIO}$ neg.		170	210	ns	1,2,5
15	$\overline{ESIO}$ negated to $\overline{PPS}$ negated		45	70	ns	1,2

Timing Diagram References, Continued

Ref Num	Description	Min	Typ	Max	Unit	Notes
16	$\overline{PDTACK}$ asserted to $\overline{XAS}$ negated		185	250	ns	1,2,3
17	$\overline{XAS}$ neg. to XA1-XA12 invalid	0	15		ns	1,2,5
	$\overline{XAS}$ negated to XRW invalid	0	15		ns	1,2,3,5
	$\overline{XAS}$ neg. to XD0-XD15 invalid	0	15		ns	1,5
18	$\overline{PDTACK}$ asserted to $\overline{XUDS}$/$\overline{XLDS}$ negated		190	280	ns	1,2,3,4
19	$\overline{ESIO}$ negated to $\overline{XUDEN}$/$\overline{XLDEN}$ negated			100	ns	1,2,4
20	CLK8 to $\overline{PDTACK}$ negated		35	55	ns	1,2,3
21	$\overline{PDTACK}$ negated to $\overline{PPS}$ asserted for next cycle if all other $\overline{PPS}$ terms are true		35	55	ns	1,2
22	$\overline{XDTACK}$ negated before CLK8 for next cycle to (set up time)		40	66	ns	1,2,3
23	State change conditions valid to CLK8 (setup time)			35	ns	1,2,3
24	CLK8 to $\overline{PSG3}$ state change		15	30	ns	1,2,3
25	$\overline{XAS}$ assert. to $\overline{XUDS/XLDS}$ asserted		0		ns	2,3
26	Data valid to $\overline{PDTACK}$ asserted (data setup time)	0			ns	2,3
27	$\overline{XDTACK}$ asserted to $\overline{PDTACK}$ asserted	125		310	ns	2,3
28	$\overline{XDTACK}$ asserted pulse width			15	us	1,2,3
29	CLK8 to $\overline{PDTACK}$ asserted		35	55	ns	2,3

Timing Diagram References, Continued

Ref Num	Description	Min	Typ	Max	Unit	Notes
30	CLK8 to $\overline{XCEN}$ negated		35	55	ns	1,2,3
31	$\overline{XCEN}$ negated to XRW, $\overline{XAS}$, $\overline{XUDS}$, $\overline{XLDS}$ disabled (high impedance)		9	16	ns	1,2,3,4
32	$\overline{XAS}$ negated to data invalid (data hold time)	0			ns	2,3
33	CLK8 to $\overline{SPIACK}$ asserted	5		11	ns	3
34	$\overline{SPIACK}$ asserted to $\overline{XIACK}$ asserted		155	185	ns	3
35	$\overline{SPIACK}$ assert. to $\overline{XCEN}$ assert.		35	55	ns	3
36	CLK8 to $\overline{XLDEN}$ asserted		35	55	ns	3
37	$\overline{PDTACK}$ asserted to $\overline{SPIACK}$ negated		112	172	ns	3
38	$\overline{SPIACK}$ negated to $\overline{XIACK}$ neg.		40	65	ns	3
39	$\overline{SPIACK}$ negated to $\overline{XLDEN}$ neg.			100	ns	3
40	$\overline{XIACK}$ asserted to $\overline{XIRQ}$ negated (hold time)	0			ns	3
41	$\overline{XAS}$ negated to $\overline{XIRQ}$ negated			0	ns	3

1 Write cycle.
2 Read cycle.
3 Interrupt Acknowledge cycle.
4 $\overline{XUDS}$, $\overline{XLDS}$, $\overline{XUDEN}$, and $\overline{XLDEN}$ are asserted as follows:

Access	$\overline{XUDEN}$	$\overline{XUDS}$	$\overline{XLDEN}$	$\overline{XLDS}$
Even Byte	assert	assert	negate	negate
Odd Byte	negate	negate	negate	negate
Word	assert	assert	assert	assert

5 68020 MPU controlling bus. May be slower with DMAC as bus master.

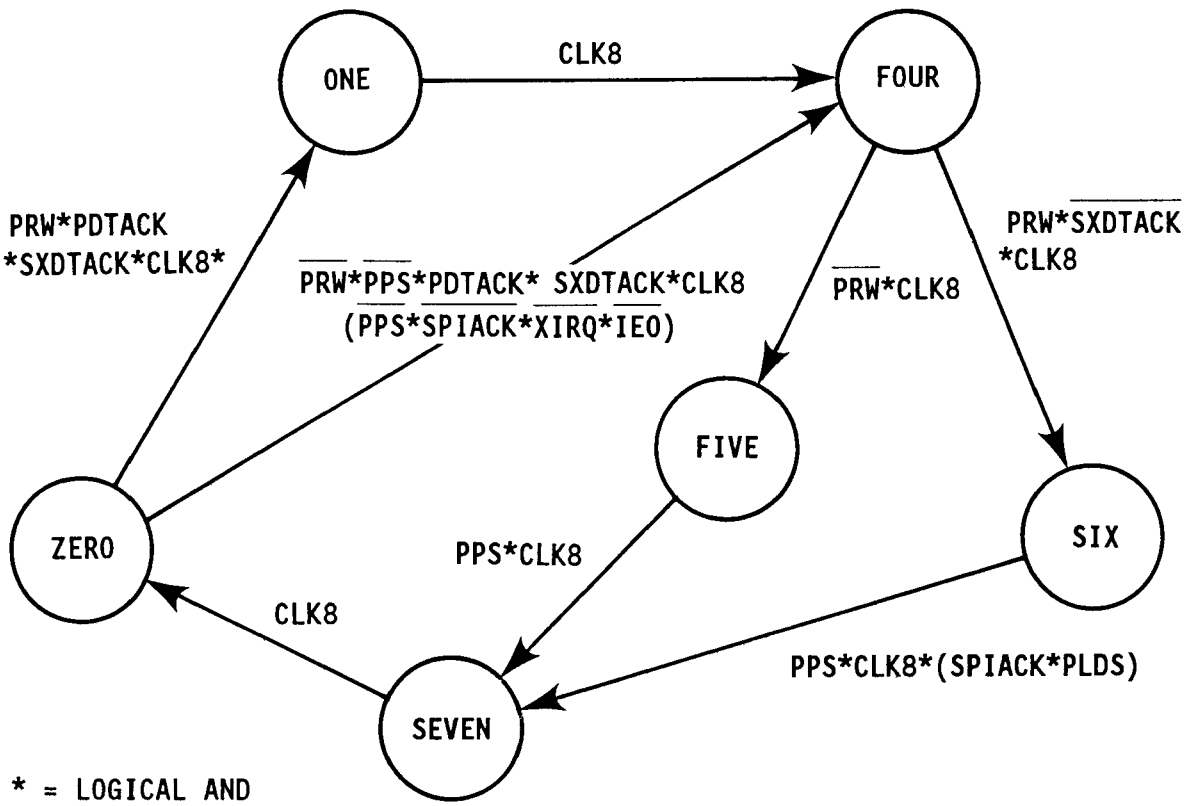


Figure 8-17. Parallel Port State Diagram

TABLE 8-8. PSG3 (U307) LOGIC EQUATIONS

INPUTS: CLK8@1, PPS~@2, PLDS~@10, PUDSC~@11, PRW@3, SPOACK~@8, XIRQ~@23, SXDTACK~@14

OUTPUTS: PDTACK~@7, PPIDC~@16, XIACK~@22, XCEN~@16, XLDEN~@17, XUDEN~@18, XAS~@19, XLDS~@20, XUDS~@21, A@6, B@5, C@4, IEO@9

NETWORK:

```
CLK8 = INP(CLK8)            % 8 MHz clock %
PPS = INP(PPS~)             % pep select %
PLDS = INP(PLDS~)           % SIO lower data strobe %
PUDS = INP(PUDS~)           % SIO upper data strobe %
PRW = INP(PRW)              % SIO R/W~ %
SPIACK = INP(SPIACK~)       % synchronized parallel port IACK %
XIRQ = INP(XIRQ~)           % external interrupt request %
SXDTACK = INP(SXDTACK~)     % synchronized external DTACK %

PDTACK~, PDTACK = COIF(PDTACKc,AKEN) % SIO DTACK %

PPIDC~ = CONF(PPIDCc,VCC) % interrupt daisy chain out %
XIACK~ = CONF(XIACKc,VCC) % external interrupt acknowledge
                            out %
XCEN~ = CONF(XCENc,VCC)   % external control buffer enable %
XLDEN~ = CONF(XLDENc,VCC) % ext. lower data buffer enable %
XUDEN~ = CONF(XUDENc,VCC) % ext. upper data buffer enable %
XAS~ = CONF(XASc,VCC)     % external address strobe %
XLDS~ = CONF(XLDSc,VCC)   % external lower data strobe %
XUDS~ = CONF(XUDSc,VCC)   % external upper data strobe %

A, A = RORF(Ad,CLK8,GND,GND,VCC)   % state variable lsb %
B, B = RORF(Bd,CLK8,GND,GND,VCC)
C, C = RORF(Cd,CLK8,GND,GND,VCC)   % state variable msb %

IEO, IEO = SOSF(IEOs,CLK8,IEOr,IEOac,GND,VCC)
                                   % interrupt daisy chain
                                     out %
```

EQUATIONS: See next page

TABLE 8-8. CONTINUED

```
EQUATIONS: zero = C'*B'*A';          % state variable definitions %
           one = C'*B'*A;
           four = C*B'*A';
           five = C*B'*A;
           six = C*B*A';

           Ad =
           zero*PPS'*PRW'*PDTACK*SXDTACK+four*PRW'+five+six*PPS*(SPIACK+
           PLDS);
           Bd = four*PRW*SXDTACK'+five*PPS+six;
           Cd =
           zero*PRW*(PPS'+SPIACK'*XIRQ'*IEO')*PDTACK*SXDTACK+one+four
           +five+six;

           XCENc = /(zero*(SPIACK'*XIRQ'*IEO'+PPS')+zero);
           XLDENC = /(SPIACK'*zero'+PPS')*PLDS');
           XUDENc = /(PPS'*PUDS');
           XASc = /(one+four+(five+six)*(PPS'+SPIACK'*PLDS'));
           XLDSc = /((four+five+six)*(PPS'+SPIACK')*PLDS');
           XUDSc = /(PPS'*PUDS'*(four+five+six));
           XIACKc = /(SPIACK'*(four+six)*PLDS');
           PDTACKc = /((four*PRW'+five+six)*SXDTACK');
           AKEN = C;
           IEOs = SPIACK'*XIRQ*zero;
           IEOr = SPIACK;
           IEOac = SPIACK;
           PPIDCc = /(SPIACK'*IEO);
```

8.3.3 External Device Interface

Within the parallel port circuit, U319-U323 and U333 and the associated resistor networks provide the electrical interface to external devices. The 54ACT244 buffer/line drivers and 54ACT245 transceivers have balanced 24 milliamp (mA) source and sink output currents with equal rise and fall times and will drive 75Ω transmission lines over the military temperature range. The 100Ω series resistors approximate port transmission line impedance and provide back-matching termination for the line driver. Additionally, the resistors provide current limiting to prevent latch-up in the drivers or receivers when an external device is powered up and SANDAC V is off. The 22KΩ pull-up resistors pull the port lines to the high signal level when the line drivers are disabled.

Three of the parallel port inputs are configured differently than described above. $\overline{\text{XDTACK}}$ has a 2.2KΩ pull-up resistor and is on the other side of the 100Ω series resistor to allow multiple external devices to drive this line with open collector drivers in a wired-OR configuration. $\overline{\text{XIRQ}}$ and XRIMCLK use 54ALS1035 open collector buffers. These two receivers do not have series resistors but do have 22KΩ pull-up resistors.

Five buffers within U323 have their inputs and outputs tied to jumper pads. These buffers are available for user configuration.

Regulated 5-Volt power from SANDAC V is available to external devices on J305-48, 49. Current drain should be limited to a maximum of 200 mA. Signal and power grounds are on J305-43 through 47, 50 and 51.

8.3.4 DMA Considerations

The parallel port supports only dual address DMA transfers.

8.3.5 Hardware Jumpers

Parallel port hardware jumpers are described in Appendix B.

8.4 SERIAL/DISCRETE/TIMER PORTS

Two Signetics SCN68562 Dual Universal Serial Communication Controller (DUSCC) devices and one Motorola MC68901 Multi-Function Peripheral (MFP) device and their associated circuitry comprise the serial/discrete/timer ports. The primary resources provided by these devices are five serial communications channels, System I/O Module serial ports A through E. The various discrete I/O lines and timers included in the DUSCC and MFP devices support serial port operation or can be used for other functions. Serial/discrete/timer resources are summarized below:

DUSCC 1:	2 Receiver/Transmitters
(U302)	(Serial Ports A, B)
	2 16-bit Counter/Timers
	4 General-Purpose Input Lines
	4 General-Purpose Output Lines
	2 Digital Phase-Locked Loops
DUSCC 2:	2 Receiver/Transmitters
(U303)	(Serial Ports C, D)
	2 16-bit Counter/Timers
	4 General-Purpose Input Lines
	4 General-Purpose Output Lines
	2 Digital Phase-Locked Loops
MFP:	1 USART
(U304)	(Serial Port E)
	4 8-bit Counter/Timers
	8 General-Purpose Input/Output/Interrupt Lines
	1 16-Channel Interrupt Controller

A block diagram of the serial/discrete/timer ports is shown in Figure 8-18. Descriptions of the DUSCC and MFP devices are given in the following subsections.

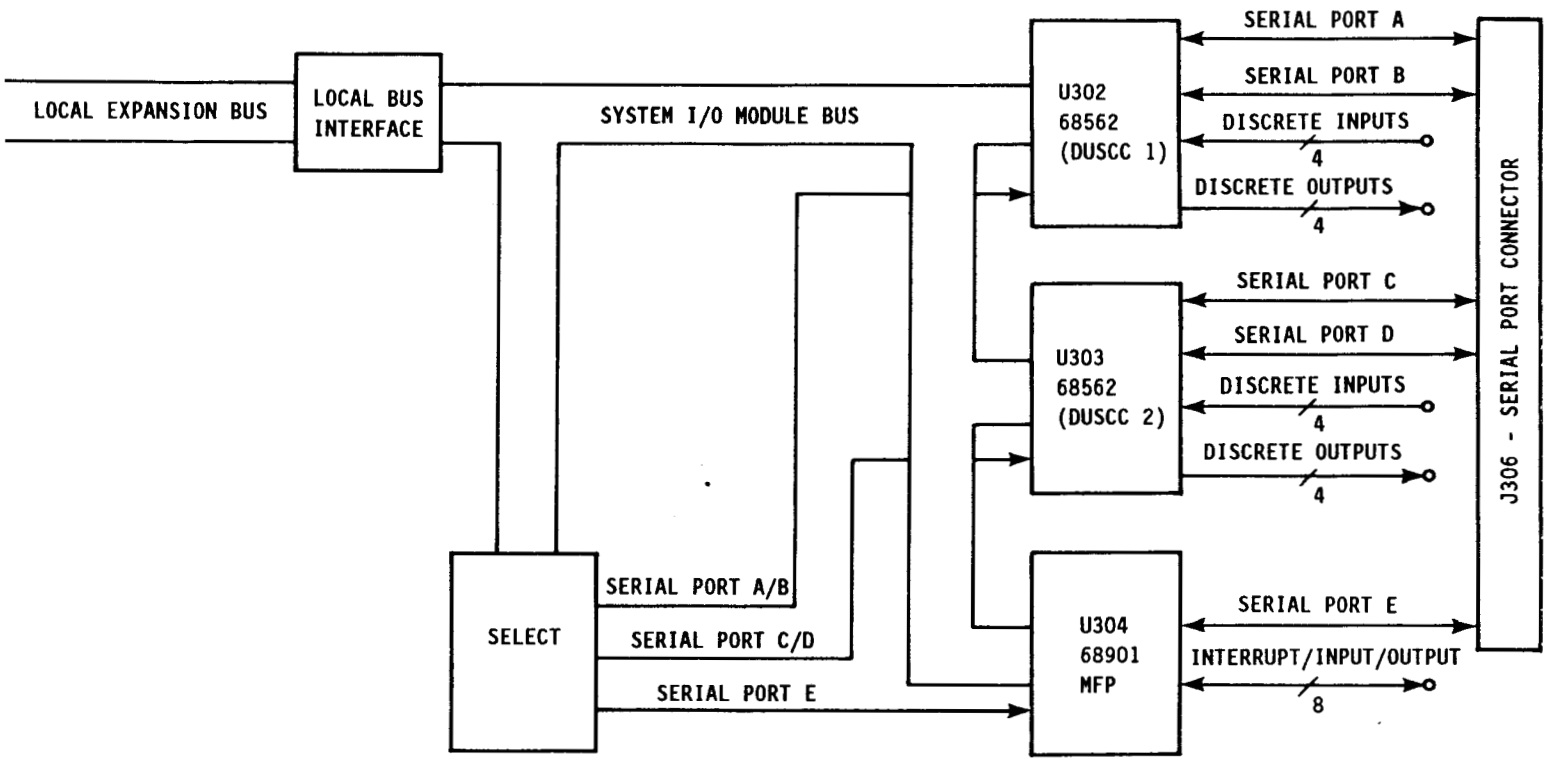


Figure 8-18. Serial/Discrete/Timer Ports

8.4.1 68562 DUSCC

The System I/O Module contains two Signetics SCN68562 Dual Universal Synchronous Communications Controllers (DUSCCs), U302 and U303. A single 68562 has two independent receiver/transmitter channels (A and B) that support bit-oriented and character-oriented synchronous protocols, and asynchronous protocols. Each channel contains the following:

- Receiver
- Transmitter
- 16-bit counter/timer
- Digital phase-locked loop (DPLL)
- Parity/CRC generator-checker

The two channels share a bit rate generator that operates from an external clock. On the System I/O Module, this is the 14.7456 MHz clock GCLK14.

Complete information on the 68562 is in the Signetics publication, *SCN68562 Dual Universal Serial Communications Controller (DUSCC).*

A DUSCC address map is shown in Table 8-9; all registers are 8 bits wide. On the System I/O Module, serial ports A and B, which are supported by DUSCC 1 (U302), are located at local address 0n,FFE,201+ hex (n = Processor ID). Serial ports C and D, which are supported by DUSCC 2 (U303), are located at local address 0n,FFE,301+ hex. A complete addressing summary of the System I/O Module DUSCCs is given in Table 8-10. Details of DUSCC implementation are given in the following subsections.

TABLE 8-9. 68562 DUSCC ADDRESS MAP

Register	Acronym	Offset[1]	Mode[2]
Channel Mode Reg. 1	CMR1	01	R/W
Channel Mode Reg. 2	CMR2	03	R/W
SYN 1/Secondary Addr. 1 Reg.	S1R	05	R/W
SYN 2/Secondary Addr. 2 Reg.	S2R	07	R/W
Transmitter Parameter Reg.	TPR	09	R/W
Transmitter Timing Reg.	TTR	0B	R/W
Receiver Parameter Reg.	RPR	0D	R/W
Receiver Timing Reg.	RTR	0F	R/W
Counter/Timer Preset Reg. High	CTPRH	11	R/W
Counter/Timer Preset Reg. Low	CTPRL	13	R/W
Counter/Timer Control Reg.	CTCR	15	R/W
Output/ Misc. Reg.	OMR	17	R/W
Counter/Timer High	CTH	19	R/W
Counter/Timer Low	CTL	1B	R/W
Pin Configuration Reg.	PCR	1D	R/W
Channel Command Reg.	CCR	1F	R/W
Transmitter FIFO	TXFIFO	21-27	W
Receiver FIFO	RXFIFO	29-2F	R
Receiver Status Reg.	RSR	31	R/W[3]
Transmitter/Receiver Stat. Reg.	TRSR	33	R/W[3]
Input/Counter/Timer Stat. Reg.	ICTSR	35	R/W[3]
General Status Reg.	GSR[4]	37	R/W[3]
Interrupt Enable Reg.	IER	39	R/W
Not Used	-	3B	
Interrupt Vect. Reg. (Unmodified)	IVR	3D[5]	R/W
Interrupt Vect. Reg. (Modified)	IVRM	7D[5]	R
Interrupt Control Reg.	ICR	3F[5]	R/W

1 Offset in hex from serial port (channel) base address:
Port A: 0n,FFE,200 hex (n is the Processor ID)
Port B: 0n,FFE,240
Port C: 0n,FFE,300
Port D: 0n,FFE,340

2 Read (R), Write (W)

3 A write to this register may reset status.

4 The GSR may be accessed as either DUSCC channel.

5 Offset is from device base address (0n,FFE,200 for Ch. A, B; 0n,FFE,300 for Ch. C, D)

TABLE 8-10. 68562 DUSCC REGISTER ADDRESSING

68562 DUSCC Register	Address[1] by System I/O Module Serial Port (DUSCC # & Ch.) Port A (#1, Ch. A)	Port B (#1, Ch. B)	Port C (#2, Ch. A)	Port D (#2, Ch. B)
CMR1	0n,FFE,201	0n,FFE,241	0n,FFE,301	0n,FFE,341
CMR2	0n,FFE,203	0n,FFE,243	0n,FFE,303	0n,FFE,343
S1R	0n,FFE,205	0n,FFE,245	0n,FFE,305	0n,FFE,345
S2R	0n,FFE,207	0n,FFE,247	0n,FFE,307	0n,FFE,347
TPR	0n,FFE,209	0n,FFE,249	0n,FFE,309	0n,FFE,349
TTR	0n,FFE,20B	0n,FFE,24B	0n,FFE,30B	0n,FFE,34B
RPR	0n,FFE,20D	0n,FFE,24D	0n,FFE,30D	0n,FFE,34D
RTR	0n,FFE,20F	0n,FFE,24F	0n,FFE,30F	0n,FFE,34F
CTPRH	0n,FFE,211	0n,FFE,251	0n,FFE,311	0n,FFE,351
CTPRL	0n,FFE,213	0n,FFE,253	0n,FFE,313	0n,FFE,353
CTCR	0n,FFE,215	0n,FFE,255	0n,FFE,315	0n,FFE,355
OMR	0n,FFE,217	0n,FFE,257	0n,FFE,317	0n,FFE,357
CTH	0n,FFE,219	0n,FFE,259	0n,FFE,319	0n,FFE,359
CTL	0n,FFE,21B	0n,FFE,25B	0n,FFE,31B	0n,FFE,35B
PCR	0n,FFE,21D	0n,FFE,25D	0n,FFE,31D	0n,FFE,35D
CCR	0n,FFE,21F	0n,FFE,25F	0n,FFE,31F	0n,FFE,35F
TXFIFO	0n,FFE,221[2]	0n,FFE,261[2]	0n,FFE,321[2]	0n,FFE,361[2]
RXFIFO	0n,FFE,229[2]	0n,FFE,269[2]	0n,FFE,329[2]	0n,FFE,369[2]
RSR	0n,FFE,231	0n,FFE,271	0n,FFE,331	0n,FFE,371
TRSR	0n,FFE,233	0n,FFE,273	0n,FFE,333	0n,FFE,373
ICTSR	0n,FFE,235	0n,FFE,275	0n,FFE,335	0n,FFE,375
GSR	0n,FFE,237	0n,FFE,277	0n,FFE,337	0n,FFE,377
IER	0n,FFE,239	0n,FFE,279	0n,FFE,339	0n,FFE,379
IVR	0n,FFE,23D	0n,FFE,23D	0n,FFE,33D	0n,FFE,33D
IVRM	0n,FFE,27D	0n,FFE,27D	0n,FFE,37D	0n,FFE,37D
ICR	0n,FFE,23F	0n,FFE,23F	0n,FFE,33F	0n,FFE,33F

1 Addresses are in hexadecimal; n is the Processor ID.
2 FIFOs are four consecutive odd address locations.

8.4.1.1 Serial Communications Channels. A channel's transmit and receive clocks are independent and may be provided by the same or different sources. Available sources are on-chip bit rate generators, digital phase-locked loops, counter/timers, or an external source. The maximum data rate using internally generated transmit and receive clocks is 921.6 Kbaud with a 1X clock (typical for synchronous) and 57.6 Kbaud with a 16X clock (typical for asynchronous). The maximum external receiver/transmitter clock frequency is 4 MHz.

Four pins associated with DUSCC serial channels, RTXCA, RTXCB, TRXCA, and TRXCB can be programmed via the 68562's PCR for various clocking functions.

The RTXCA and RTXCB pins can be programmed as inputs to supply clocks for the following:

- Receiver
- Transmitter
- Counter/Timer
- DPLL

As outputs, the RTXCA and RTXCB pins can be programmed to supply the following signals:

- Counter/Timer Output
- Transmitter Shift Clock (1X)
- Receiver Sampling Clock (1X)

The TRXCA and TRXCB pins can be programmed as inputs to supply clocks for the following:

- Receiver
- Transmitter
- Counter/Timer
- DPLL

As outputs, the TRXCA and TRXCB pins can be programmed to supply the following signals:

- Counter/Timer Ouput
- Transmitter Shift Clock (1X)
- Receiver Sampling Clock (1X)
- Transmitter BRG Clock (16X)
- Receiver BRG Clock (16X)
- Internal System Clock (X1/2)

These pins are connected to jumper pads so that they may be wired to external counter/timer or clock signals via general-purpose buffers. Figure 8-19 illustrates the jumpers for a typical synchronous link where these pins supply the external transmitter clock and input the external receiver clock. In this arrangement, the clocks and data should follow similar paths to eliminate skew.

These pins need not be used for serial channels that use clocks derived on the DUSCC and have no external clock requirements, for example, asynchronous mode with 16X clocks or synchronous mode with clock recovered from data by the DPLL.

A DUSCC also includes a set of Request-to-Send/Clear-to-Send pins for each channel (RTSNA, CTSNA, RTSNB, and CTSNB). On the System I/O Module, these lines are buffered through inverters (U331 and U332) and terminated with jumper pads. This allows the lines to be configured for modem control or for hardware handshake.

8.4.1.2 Counter/Timers. A DUSCC contains two 16-bit counter/timers. A counter/timer can supply the transmit and/or receive clocks for the serial channels or for external devices. The counter/timer can also be used in any of the following capacities:

- Event counting
- Character counting
- Delay generation
- Pulse width measurement

8.4.1.3 Discretes. Each channel of a DUSCC has four two general-purpose input pins and two general-purpose output pins. If a DUSCC channel uses direct memory access (DMA) transfers, the general-purpose pins can be programmed for handshaking with the DMA controller (DMAC). If a channel does not use DMA transfers, the general-purpose pins can be programmed to sense and control discrete signals. In this mode, the input signals are read as two bits in the DUSCC's ICTSRx, where "x" is the DUSCC channel (A or B). The outputs are controlled by two bits in the DUSCC's OMRx.

The general-purpose input and outputs on both of the System I/O Module DUSCCs are brought out to jumper pads for user configuration. The general-purpose inputs and outputs are summarized in Table 8-11.

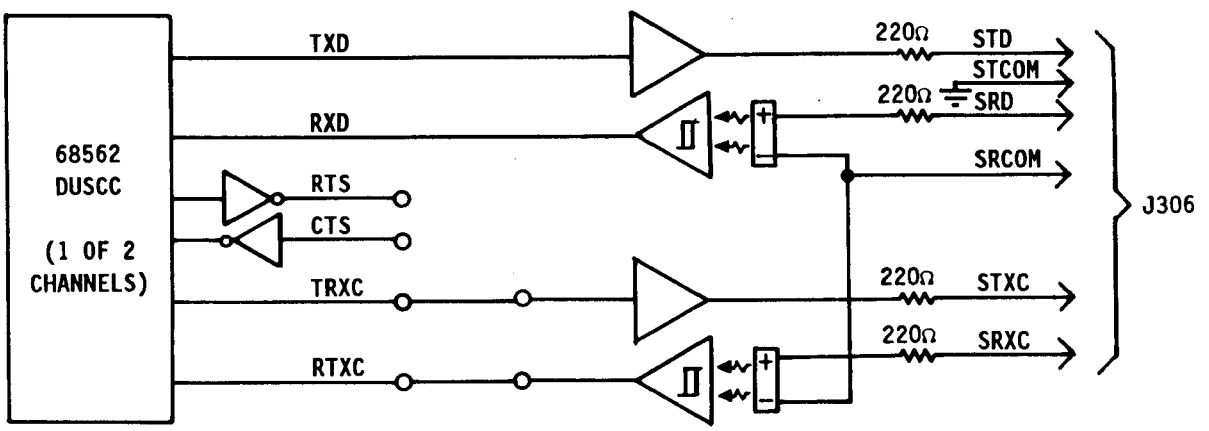


Figure 8-19. Typical 68562 Synchronous Data Link

TABLE 8-11. DUSCC GENERAL-PURPOSE I/O PINS

DUSCC/ Channel/ Serial Port	Mnemonic	Pin	I/O	Jumper Pad
DUSCC 1 (U302)	GPI1A/$\overline{\text{RTADAK}}$	U302-44	I	T79
Channel A	GPI2A/$\overline{\text{TXADAK}}$	U302-35	I	T87
Serial Port A	GPO1A/$\overline{\text{RTADRQ}}$	U302-34	O	T88
	GPO2A/$\overline{\text{TXADRQ}}$	U302-33	O	T90
DUSCC 1 (U302)	GPI1B/$\overline{\text{RTBDAK}}$	U302-5	I	T78
Channel B	GPI2B/$\overline{\text{TXBDAK}}$	U302-14	I	T86
Serial Port B	GPO1B/$\overline{\text{RTBDRQ}}$	U302-15	O	T89
	GPO2B/$\overline{\text{TXBDRQ}}$	U302-16	O	T91
DUSCC 2 (U303)	GPI1C/$\overline{\text{RTCDAK}}$	U303-44	I	T93
Channel A	GPI2C/$\overline{\text{TXCDAK}}$	U303-35	I	T102
Serial Port C	GPO1C/$\overline{\text{RTCDRQ}}$	U303-34	O	T103
	GPO2C/$\overline{\text{TXCDRQ}}$	U303-33	O	T105
DUSCC 2 (U303)	GPI1D/$\overline{\text{RTDDAK}}$	U303-5	I	T92
Channel B	GPI2D/$\overline{\text{TXDDAK}}$	U303-14	I	T101
Serial Port D	GPO1D/$\overline{\text{RTDDRQ}}$	U303-15	O	T104
	GPO2D/$\overline{\text{TXDDRQ}}$	U303-16	O	T106

8.4.1.4 DMA Operations. The System I/O Module DUSCCs can function with the 63450 DMAC for either single-address or dual-address transfers. The operation of a DUSCC during a DMA transfer depends on whether the DUSCC channel is operating in the half duplex or the full duplex mode and the DMAC addressing mode (single address or dual address). For DMA operation, the general-purpose input and output lines must be hardware jumpered to the appropriate 63450 DMAC request/acknowledge lines ($\overline{\text{REQ0}}$-$\overline{\text{REQ3}}$/$\overline{\text{ACK0}}$-$\overline{\text{ACK3}}$) to perform handshaking. Table 8-12 summarizes 68562 DMA configurations and modes.

TABLE 8-12. 68562 DMA OPERATION

Mode	Description
Half Duplex/Dual Address	Handshake Connection: 68562 GPO1x/$\overline{\text{RTxDRQ}}$ output to 63450 DMAC $\overline{\text{REQ}}$y, where "x" is the serial port (A-D), and "y" is the DMAC channel (0-3). Description: The single handshake connection provides both DMA read and write requests to the DMAC. Requests are acknowledged via normal bus read and write cycles. Data transfer requires two bus cycles. The DMAC acquires the data from the source on the first cycle and deposits it at the destination on the second cycle. This mode allows a single 63450 DMAC channel to service both the DUSCC receiver and transmitter. DUSCC pins GPI1x, GPI2x, and GPO2x remain available for general-purpose use.
Half Duplex/Single Address	Handshake Connection: 68562 GPO1x/$\overline{\text{RTxDRQ}}$ to 63450 DMAC $\overline{\text{REQ}}$y; 63450 DMAC $\overline{\text{ACK}}$y to 68562 GPI1x/$\overline{\text{RTxDAK}}$, where "x" is the serial port (A-D), and "y" is the DMAC channel (0-3). Description: The first handshake connection listed above provides both DMA read and write requests to the DMAC. Requests are acknowledged via the second handshake connection. Data transfer is accomplished in one bus cycle. The DMAC addresses the source or destination and then issues the acknowledge signal. This causes the 68562 to either input the data on the data bus to its transmit FIFO (DMA write) or output data from its receive FIFO to the data bus (DMA read). This mode allows a single 63450 DMAC channel to service both the DUSCC receiver and transmitter. DUSCC pins GPI2x and GPO2x remain available for general-purpose use.
Full Duplex/Dual Address	Handshake Connection: 68562 GPO1x/$\overline{\text{RTxDRQ}}$ to 63450 DMAC $\overline{\text{REQ}}y_1$; 68562 GPO2x/$\overline{\text{TXxDRQ}}$ to 63450 DMAC $\overline{\text{REQ}}y_2$, where "x" is the serial port (A-D), and "y_1" and "y_2" are two separate 63450 DMAC channels (0-3). (Continued on next page.)

TABLE 8-12. CONTINUED

Mode	Description
Full Duplex/Dual Address	Description: The first handshake connection listed above provides DMA read requests to the DMAC from the DUSCC receiver. The second handshake connection provides DMA write requests from the DUSCC transmitter. Requests are acknowledged via normal bus read and write cycles. Data transfer requires two bus cycles. The DMAC acquires the data from the source on the first cycle and deposits it at the destination on the second cycle. This mode requires that two 63450 DMAC channels be used to service the DUSCC, one for the receiver and one for the transmitter. DUSCC pins GPI1x and GPI2x remain available for general-purpose use.
Full Duplex/Single Address	Handshake Connection: 68562 GPO1x/$\overline{\text{RTxDRQ}}$ to 63450 DMAC $\overline{\text{REQ}}y_1$; 68562 GPO2x/$\overline{\text{TXxDRQ}}$ to 63450 DMAC $\overline{\text{REQ}}y_2$; 63450 DMAC $\overline{\text{ACK}}y_1$ to 68562 GPI1x/$\overline{\text{RTxDAK}}$; 63450 DMAC $\overline{\text{ACK}}y_2$ to 68562 GPI2x/$\overline{\text{RXxDAK}}$, where "x" is the serial port (A-D), and "y_1" and "y_2" are two separate 63450 DMAC channels (0-3). Description: The first handshake connection listed above provides DMA read requests to the DMAC from the DUSCC receiver. The second handshake connection provides DMA write requests from the DUSCC transmitter. Receiver requests are acknowledged via the third handshake connection; transmitter requests are acknowledged via the fourth handshake connection. Data transfer is accomplished in one bus cycle. The DMAC addresses the source or destination and then issues the acknowledge signal. This causes the 68562 to either input the data on the data bus to its transmit FIFO (DMA write) or output data from its receive FIFO to the data bus (DMA read). This mode requires that two 63450 DMAC channels be used to service the DUSCC, one for the receiver and one for the transmitter.

8.4.2 68901 MFP

The System I/O Module contains a Motorola MC68901 Multi-Function Peripheral (MFP), U304, that provides the following resources:

- 4 timers (Timers A, B, C, D)
- 1 Universal Synchronous/Asynchronous Receiver-Transmitter (USART)
- 8 programmable I/O lines with interrupt capability
- 1 16-source interrupt controller

Complete information on the 68901 is in the Motorola publication, *MC68901 Multi-Function Peripheral.*

A 68901 MFP address map is shown in Table 8-13; all registers are 8 bits wide. On the System I/O Module, Serial Port E, which is supported by the MFP, is located at local address 0n,FFE,401+ hex (n = Processor ID). Details of MFP implementation are given in the following paragraphs.

8.4.2.1 USART. The 68901 USART supports System I/O Module Serial Port E. The USART is a full-duplex receiver and transmitter that supports asynchronous and limited synchronous protocols.

USART transmit and receive clocks can be provided by one or two of the 68901 counter/timers or an external source. The 2.4576 MHz input clock (GCLK2) allows the counter/timers to generate clocks for standard baud rates. The maximum data rates using internally generated clocks are 307.2 Kbaud with 1X and 19.2 Kbaud with 16X clock. The external clock lines, TCE (U304-7) and RCE (U304-10), are terminated with jumper pads (T109 and T108, respectively) for connection to external clock sources.

For asynchronous operation, hardware handshake control can be established by using one of the general-purpose inputs as the Clear-to-Send (CTS) input and the Receiver Ready ($\overline{RR}$) DMA control signal as the Request-to-Send (RTS) output. All of the general-purpose I/O lines and the $\overline{RR}$ output (U304-31) are terminated with jumper pads for user configuration. A typical hardware handshake configuration is shown in Figure 8-20.

TABLE 8-13. SYSTEM I/O MODULE 68901 MFP ADDRESS MAP

Register	Acronym	Offset*	Module Address
General-Purpose Input/Output	GPIP	01	0n,FFE,401
Active Edge	AER	03	0n,FFE,403
Data Direction	DDR	05	0n,FFE,405
Interrupt Enable A	IERA	07	0n,FFE,407
Interrupt Enable B	IERB	09	0n,FFE,409
Interrupt Pending A	IPRA	0B	0n,FFE,40B
Interrupt Pending B	IPRB	0D	0n,FFE,40D
Interrupt In-Service A	ISRA	0F	0n,FFE,40F
Interrupt In-Service B	ISRB	11	0n,FFE,411
Interrupt Mask A	IMRA	13	0n,FFE,413
Interrupt Mask B	IMRB	15	0n,FFE,415
Vector	VR	17	0n,FFE,417
Timer A Control	TACR	19	0n,FFE,419
Timer B Control	TBCR	1B	0n,FFE,41B
Timer C and D Control	TCDCR	1D	0n,FFE,41D
Timer A Data	TADR	1F	0n,FFE,41F
Timer B Data	TBDR	21	0n,FFE,421
Timer C Data	TCDR	23	0n,FFE,423
Timer D Data	TDDR	25	0n,FFE,425
Synchronous Character	SCR	27	0n,FFE,427
USART Control	UCR	29	0n,FFE,429
Receiver Status	RSR	2B	0n,FFE,42B
Transmitter Status	TSR	2D	0n,FFE,42D
USART Data	UDR	2F	0n,FFE,42F

*Offset in hex from Serial Port E base address 0n,FFE,400

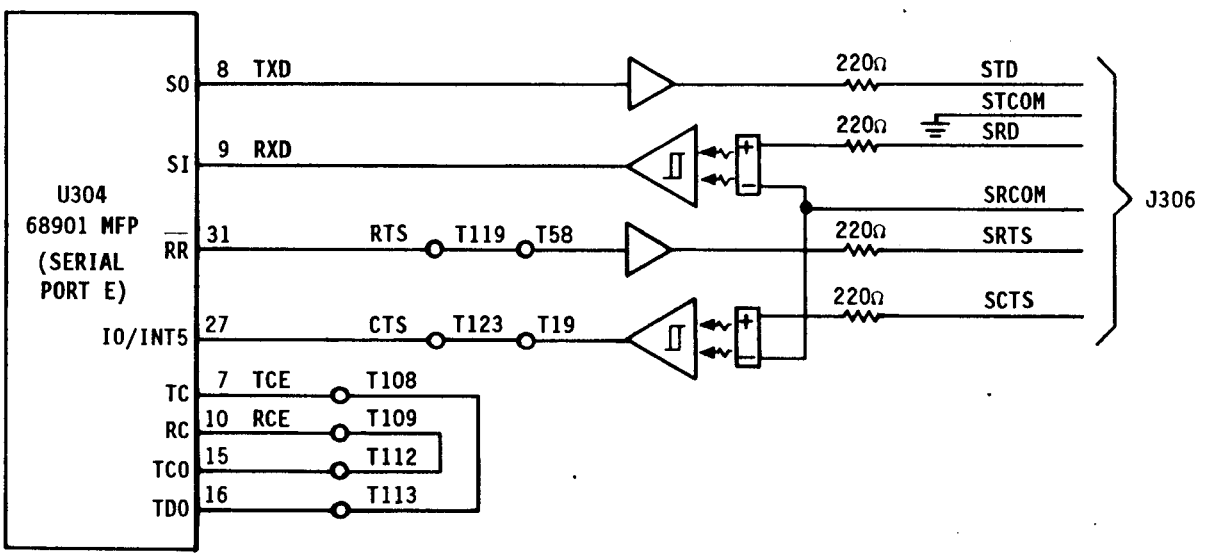


Figure 8-20. 68901 MFP Hardware Handshake Configuration

8.4.2.2 Timers. Each of the four 68901 timers is an 8-bit counter with a programmable prescaler, which can be used for general-purpose functions or can supply the transmit and/or receive clocks for the 68901 USART. Timers A and B can be programmed to operate in any of the following modes:

- Delay
- Pulse width measurement
- Event count

Timers C and D operate only in the delay mode. (Refer to the 68901 manual for a description of these modes.)

MFP timers A and B have both their inputs and outputs connected to jumper pads and are available for user configuration. The outputs of Timers C and D are connected to jumper pads for user configuration.

8.4.2.3 Programmable I/O Lines. The programmable I/O lines are eight individually programmable I/O lines with interrupt capability. This allows for the configuration of an 8-bit I/O port or eight discrete input/output/interrupt signals. All of the I/O lines are terminated with jumper pads for user configuration.

8.4.2.4 Interrupt Controller. The 68901 interrupt controller has 16 prioritized channels for handling interrupt requests. The requests presented to the controller are generated by sources internal to the 68901 and by external sources. The internal sources include the 68901 timers and USART. The external sources are routed to the controller on the eight programmable I/O lines and the Timer A (TAI, U304-19) and Timer B (TBI, U304-20) external inputs.

The 16 interrupt controller channels are prioritized. Concurrent requests are handled highest priority first. The channel assignments for the interrupt controller and their priorities are as follows:

Channel	Interrupt Request	Priority
1111	Input 7 (IO/INT7)	Highest
1110	Input 6 (IO/INT6)	.
1101	Timer A	.
1100	USART (receive buffer full)	.
1011	USART (receiver error)	.
1010	USART (transmit buffer empty)	.
1001	USART (transmitter error)	.
1000	Timer B	.
0111	Input 5 (IO/INT5)	.
0110	Input 4 (IO/INT4)	.
0101	Timer C	.
0100	Timer D	.
0011	Input 3 (IO/INT3)	.
0010	Input 2 (IO/INT2)	.
0001	Input 1 (IO/INT1)	.
0000	Input 0 (IO/INT0)	Lowest

When interrupt requests are presented to the interrupt controller, the controller responds to the highest priority source and causes the 68901 to generate a single vectored interrupt request. During the 68020 interrupt acknowledge cycle, the 68901 furnishes an interrupt vector with the following format:

68901 Interrupt Vector Format

7	6	5	4	3	2	1	0
V3	V2	V1	V0	CH3	CH2	CH1	CH0

Vn VECTOR - The four bits in this field are copied from the 68901 Vector Register (VR) (refer to the programming model). The bits are loaded into the VR when the 68901 is initialized to designate the interrupt vector the device will use.

CHn CHANNEL - The four bits in this field designate the interrupt controller channel that made the interrupt request.

8.4.2.5 DMA Operation. The MFP can only operate in the dual address DMA mode. For dual address DMA operation, the receiver service request signal is $\overline{\text{RXEDRQ}}$ (U304-31), jumper pad T119; the transmitter service request signal is $\overline{\text{TXEDRQ}}$ (U304-30), jumper pad T120. These must be jumpered to the appropriate DMAC request inputs, $\overline{\text{REQ0}}$-$\overline{\text{REQ3}}$. $\overline{\text{RXEDRQ}}$ also functions as RTSE for hardware handshaking. These two functions are compatible and may be used simultaneously.

8.4.3 Hardware Jumpers

Hardware jumpers associated with the serial/discrete/timer ports are described in Appendix B.

8.4.4 Serial Port Interfacing

Each of the five serial ports has two line drivers and two opto-couplers for external interfacing. The particular devices associated with each port are summarized below.

Serial Port	Line Drivers	Opto-Couplers
A	U324-A U324-B	U335
B	U324-C U324-D	U336
C	U324-E U324-F	U337
D	U324-G U324-H	U338
E	U325-A U325-B	U339

These devices isolate SANDAC V electrically from equipment connected to its serial ports. The convention is to have an opto-coupler at the receiving end of each signal line. One line driver and one opto-coupler are dedicated to the serial transmit (Tx) and receive (Rx) signals respectively. The other line driver and opto-coupler may be jumpered to provide clock, hardware handshake, counter/timer, or discrete signals as required for particular applications.

Recommended input current, I_F, to the HCPL-5231 opto-couplers is 4 to 8 mA. Specified input forward voltage at I_F=8 mA is 1.0 V min, 1.3 V typ, and 1.8 V max. There are 220Ω current-limiting resistors in series with each of the signal lines. Typically, additional resistance will be required in external devices. The value depends on the types of line drivers and opto-couplers used, cable length, and data rate. 270Ω is appropriate for similar interface devices, short cables, and modest data rates.

A typical connection between a SANDAC V serial port and an external device is shown in Figure 8-21.

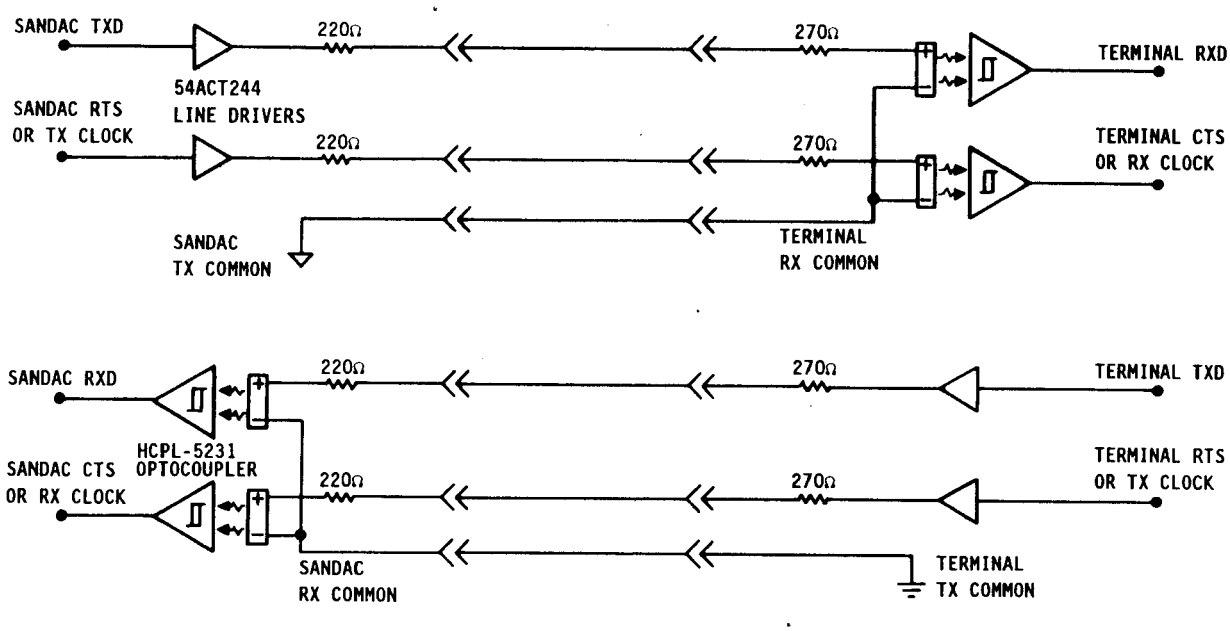


Figure 8-21. Typical Serial Port Interface

8.4.5 Serial Port Connector

The serial port connector, J306, is shown in Figure 8-22. Descriptions of the connector pins are given in Table 8-15.

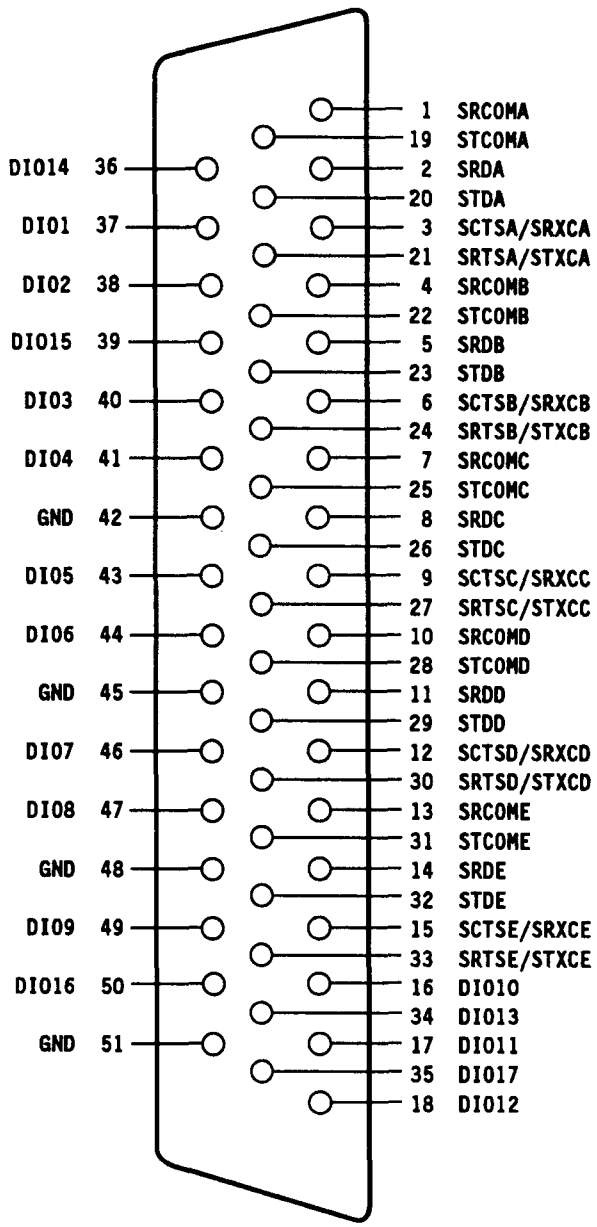


Figure 8-22. Serial Port Connector (J306)

TABLE 8-14. SERIAL PORT CONNECTOR (J306) PIN DESCRIPTIONS

Pin	Mnemonic	I/O*	Description
1	SRCOMA	I	Serial Port A Receiver Common.
2	SRDA	I	Serial Port A Receive Data.
3	SCTSA/SRXCA	I	Serial Port A Clear-To-Send/Receiver Clock.
4	SRCOMB	I	Serial Port B Receiver Common.
5	SRDB	I	Serial Port B Receive Data.
6	SCTSB/SRXCB	I	Serial Port B Clear-To-Send/Receiver Clock.
7	SRCOMC	I	Serial Port C Receiver Common.
8	SRDC	I	Serial Port C Receive Data.
9	SCTSC/SRXCC	O	Serial Port C Clear-To-Send/Receiver Clock.
10	SRCOMD	I	Serial Port D Receiver Common.
11	SRDD	I	Serial Port D Receive Data.
12	SCTSD/SRXCD	I	Serial Port D Clear-To-Send/Receiver Clock.
13	SRCOME	I	Serial Port E Receiver Common.
14	SRDE	I	Serial Port E Receive Data.
15	SCTSE/SRXCE	I	Serial Port E Clear-To-Send/Receiver Clock.
16	DIO10	I	Discrete Input/Output 10.
17	DIO11	I/O	Discrete Input/Output 11.
18	DIO12	I	Discrete Input/Output 12.
19	STCOMA	O	Serial Port A Transmitter Common.
20	STDA	O	Serial Port A Transmit Data.

TABLE 8-14. CONTINUED

Pin	Mnemonic	I/O*	Description
21	SRTSA/STXCA	O	Serial Port A Request-To-Send/Transmitter Clock.
22	STCOMB	O	Serial Port B Transmitter Common.
23	STDB	O	Serial Port B Transmit Data.
24	SRTSB/STXCB	O	Serial Port B Request-To-Send/Transmitter Clock.
25	STCOMC	O	Serial Port C Transmitter Common.
26	STDC	O	Serial Port C Transmit Data.
27	SRTSC/STXCC	O	Serial Port C Request-To-Send/Transmitter Clock.
28	STCOMD	O	Serial Port D Transmitter Common.
29	STDD	O	Serial Port D Transmit Data.
30	SRTSD/STXCD	O	Serial Port D Request-To-Send/Transmitter Clock.
31	STCOME	O	Serial Port E Transmitter Common.
32	STDE	O	Serial Port E Transmit Data.
33	SRTSE/STXCE	O	Serial Port E Request-To-Send/Transmitter Clock.
34	DIO13	I/O	Discrete Input/Output 13.
35	DIO17	I/O	Discrete Input/Output 17.

TABLE 8-14. CONTINUED

Pin	Mnemonic	I/O*	Description
36	DIO14	I	Discrete Input/Output 14.
37	DIO1	I/O	Discrete Input/Output 1.
38	DIO2	I/O	Discrete Input/Output 2.
39	DIO15	I/O	Discrete Input/Output 15.
40	DIO3	I/O	Discrete Input/Output 3.
41	DIO4	I/O	Discrete Input/Output 4.
42	GND	I/O	Signal and power ground.
43	DIO5	I/O	Discrete Input/Output 5.
44	DIO6	I/O	Discrete Input/Output 6.
45	GND	I/O	Signal and power ground.
46	DIO7	I/O	Discrete Input/Output 7.
47	DIO8	I/O	Discrete Input/Output 8.
48	GND	I/O	Signal and power ground.
49	DIO9	I/O	Discrete Input/Output 9.
50	DIO16	I	Discrete Input/Output 16.
51	GND	I/O	Signal and power ground.

*I/O: I = Input; O = Output

8.5 GENERAL-PURPOSE DEVICES

Uncommitted buffers, opto-couplers and connector pins wired to jumper pads allow the System I/O Module to be configured for the particular needs of an application. Figure 8-23 shows the general-purpose devices available on the module.

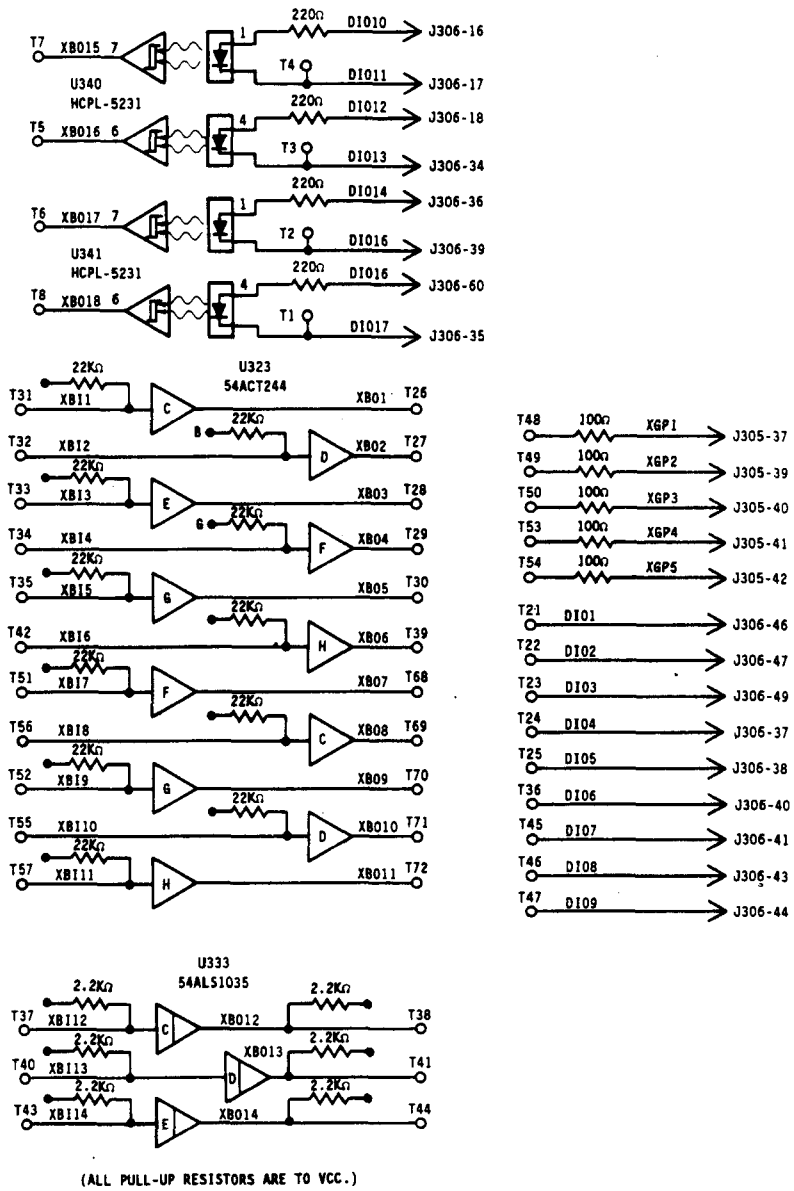


Figure 8-23. System I/O Module General-Purpose Devices

8.6 INTERRUPTS TO THE PROCESSOR MODULE

The System I/O Module interrupt system is shown in Figure 8-24. Both of the 68562 DUSCCs are hardwired to local expansion bus interrupt request W ($\overline{EIRQW}$). Requests from additional devices can be wire-ORed to this line with hardware jumpers. The interrupt acknowledge for this request is returned on the local expansion bus interrupt acknowledge W ($\overline{EIACKW}$). The acknowledge is first brought to DUSCC 1 (U302), which supports serial ports A and B. If no interrupts are pending, DUSCC 1 propagates the acknowledge to DUSCC 2 (U303), which supports serial ports C and D. The acknowledge for additional devices using $\overline{EIRQW}$/$\overline{EIACKW}$ is propagated by DUSCC 2 via hardware jumper T95.

The 68901 MFP (U304) is hardwired to local expansion bus interrupt request X ($\overline{EIRQX}$). Requests from additional devices can be wire-ORed to this line with hardware jumpers. The interrupt acknowledge for this request is returned on the local expansion bus interrupt acknowledge X ($\overline{EIACKX}$). The acknowledge for additional devices using $\overline{EIRQX}$/$\overline{EIACKX}$ is propagated by the MFP through OR gate U327-C and hardware jumper T135.

The paths for interrupt requests from the 63450 DMAC (U301) and the parallel port are selectable with hardware jumpers.

The interrupt acknowledge daisy chain line ($\overline{EIACKDC}$) connects all modules on the local expansion bus. This allows devices on other modules to be included in an interrupt acknowledge daisy chain. For example, the acknowledge signal out of a propagating device on the System I/O Module can be connected to $\overline{EIACKDC}$; on another expansion bus module, $\overline{EIACKDC}$ is connected to the acknowledge line into another device in the daisy chain. (The BFIF device, U308, is part of the interrupt acknowledge circuit. The logic equations for the device were previously given in Table 8-5.)

NOTE

> The 63450 cannot propagate an acknowledge; therefore it must always be last if it is placed in a daisy chain configuration.

Global bus interrupt requests $\overline{GIRQW}$, $\overline{GIRQX}$, $\overline{GIRQY}$, and $\overline{GIRQZ}$ are each available for one interrupt request. Requests using these lines must be autovectored because no mechanism exists for returning an acknowledge.

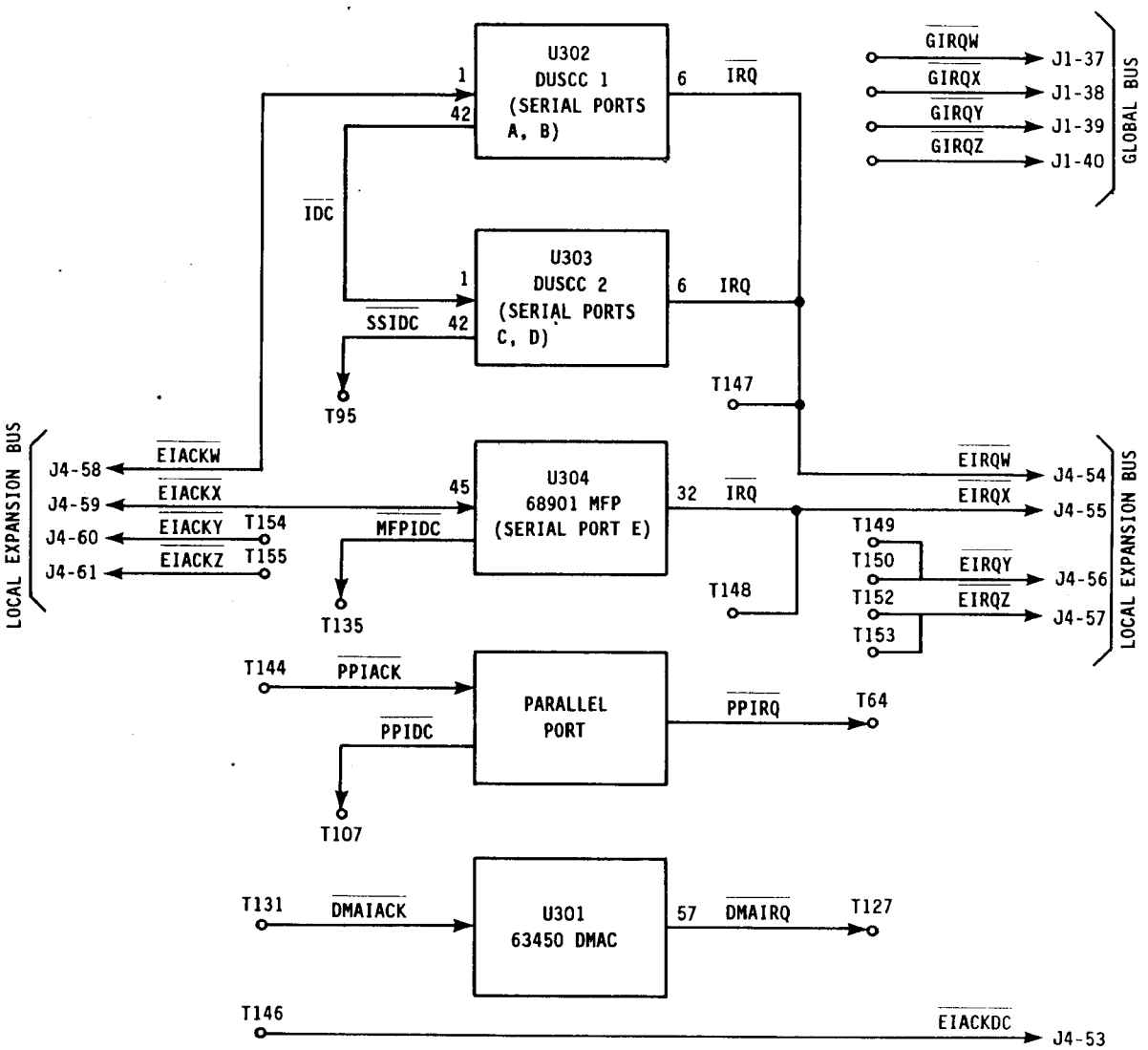


Figure 8-24. System I/O Module Interrupt System

9. MIL-STD-1553B MODULE

9.1 GENERAL

The MIL-STD-1553B Module attaches to a Processor Module and provides a dual-redundant MIL-STD-1553B interface. The interface is memory mapped within the host module's address space. The 1553 module can function as a 1553 bus controller (BC), remote terminal unit (RTU), or a bus monitor (MT).

The MIL-STD-1553B Module contains the following major circuits:

- Local Bus Interface
- 4K × 16-bit RAM
- BUS-66300 II MIL-STD-1553-to-Microprocessor Interface Unit
- Remote Terminal Address Connector
- BUS-66300 II External Registers
  - Remote Terminal Address Register
  - Tag Register/Counter
  - Prescale/Count Enable Register
  - Interrupt Vector Register
- BUS-65600 MIL-STD-1553 BC, RTU, and MT
- 1553 Bus Interface
- Interrupt Request/Acknowledge Logic

The architecture of the MIL-STD-1553B Module is shown in Figure 9-1; the major circuits are described in the following paragraphs. The module's operation as a bus controller, a remote terminal unit, and a bus monitor is also described.

NOTE

The circuit diagram of the MIL-STD-1553B Module is Sandia National Laboratories schematic CK-88144. In the following text, all references to component numbers and signals are from this drawing.

9.2 LOCAL BUS INTERFACE

On the local expansion bus, the MIL-STD-1553B Module is implemented as a 32-bit data port for accesses of the 4K × 16-bit RAM and as a 16-bit data port for accesses of registers. The module is mapped into a 16K area of the host Processor Module's 16M address space. Table 9-1 summarizes MIL-STD-1553B Module addressing.

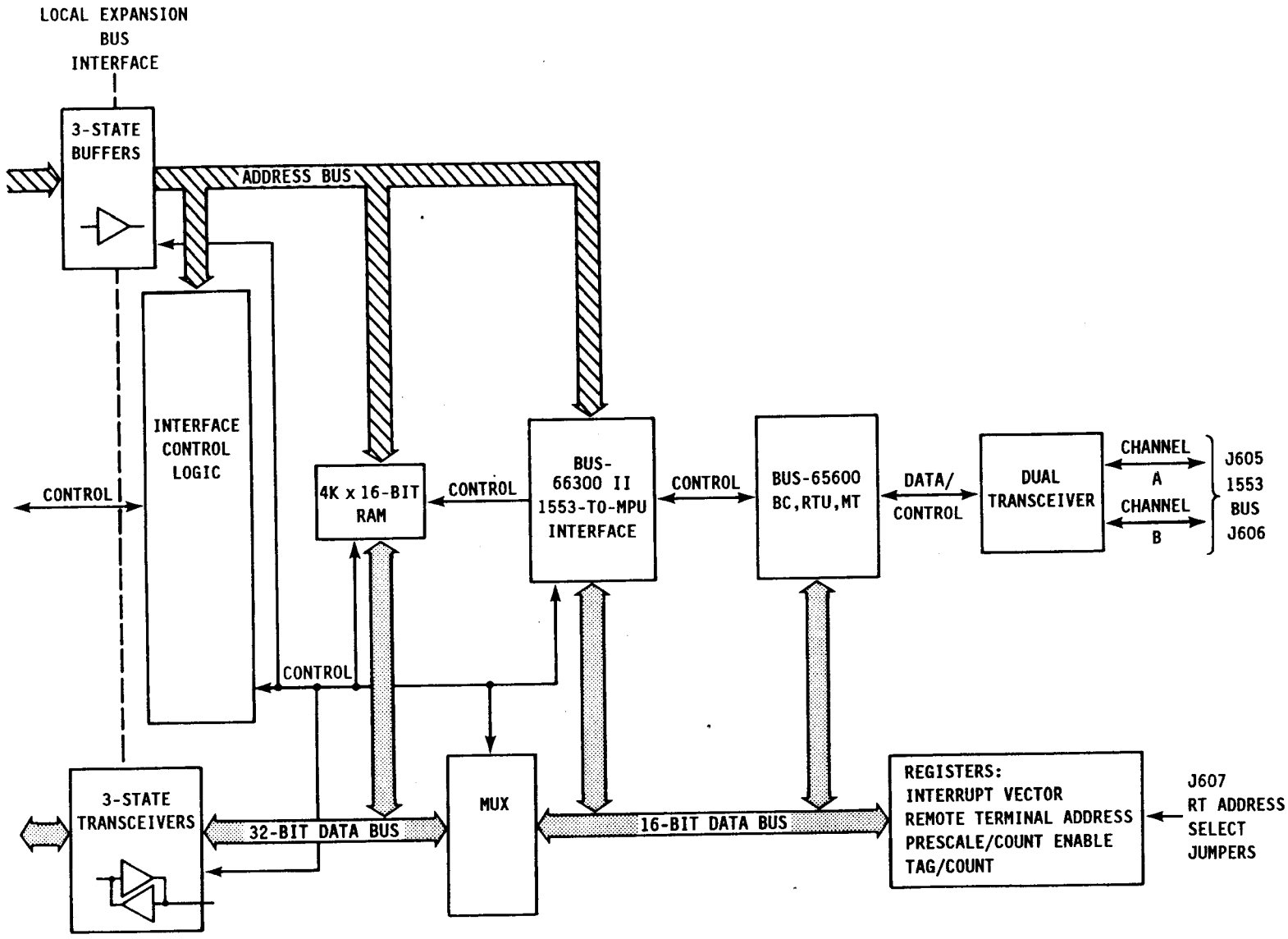


Figure 9-1. MIL-STD-1553B Module Architecture

TABLE 9-1. MIL-STD-1553B MODULE ADDRESSES

Assignment	Address*
4K × 16-bit RAM	0n,FF0,000-0n,FF1,FFF
BUS-66300 II Int. Mask Reg.	0n,FF2,000
BUS-66300 II Config. Reg.	0n,FF2,002
Not Used	0n,FF2,004
BUS-66300 II Start/Reset Reg.	0n,FF2,006
Interrupt Vector Reg.	0n,FF2,008
Remote Term. Addr. Reg.	0n,FF2,00A
Prescale/Count Enable Reg.	0n,FF2,00C
Tag Register/Counter	0n,FF2,00E

*Addresses are in hexadecimal; "n" is the Processor ID.

(The register addresses in the block from 0n,FF2,000 through 0n,FF2,00F are replicated throughout the space 0n,FF2,010 through 0n,FF3,FFF.)

9.3 4K × 16-BIT RAM

The 4K × 16-bit RAM (U612-U615) is accessible by both the local bus master and the BUS-66300 II (U601). All 1553 transfers are accomplished through this shared buffer. Data to be transmitted over the 1553 bus are written to the RAM by an MPU (local or remote). The 66300 II then reads the RAM and passes the data to the BUS-65600 (U602). The 65600 formats and passes the data to the 1553 interface circuit, which transmits them out on the 1553 bus. Data received on the 1553 bus are passed to the 66300 II via the bus interface circuit and the 65600. 66300 II then writes the data to RAM. An MPU (local or remote) then reads the RAM to get the received data.

An MPU views the 4K × 16-bit RAM as a byte-addressable data port at addresses 0n,FF0,000 through 0n,FF1,FFF hex, where "n" is the Processor ID. The BUS-66300 II views the RAM as a word-addressable data port addressed from 0000 through 0FFF hex. Understanding the difference in viewpoints is crucial because the MPU must establish pointers for the 66300 II at addresses in the RAM where the 66300 II expects to find them. Also, the pointers must be in the set of 66300 II addresses (0000-FFFF) and must direct the 66300 II to the correct RAM locations. Conversely, the MPU must issue the correct addresses to read data that was written by the 66300 II using its set of addresses and pointers.

In software, the 4K × 16-bit RAM can be divided into two areas to support a double buffering scheme. The two areas, designated A and B, are alternately used as "current" and "noncurrent" areas. Under MPU control, the 66300 II is directed to the current area.

While the 66300 II is processing 1553 messages using the current area, the MPU can be can be working with the noncurrent area.

9.4 BUS-66300 II

The BUS-66300 II MIL-STD-1553-to-Microprocessor Interface Unit (Unnn) functions as the intermediary between the 4K × 16-bit RAM and the BUS-65600 MIL-STD-1553 BC, RTU, and MT (Unnn). The 66300 II has three internal registers:

- Interrupt Mask Register (IMR)
- Configuration Register (CR)
- Start/Reset Register (S/RR)

Using these registers, the MPU establishes 66300 II operating features. Descriptions of the registers are given in the following subsections. Complete information on the BUS-66300 II is in the ILC Data Device Corporation publication, *BUS-66300 II MIL-STD-1553 to Microprocessor Interface Unit.*

9.4.1 Configuration Register

The Configuration Register (CR) establishes the 1553 operating mode (BC, RTU, MT) and also sets additional operating parameters. In RTU mode, the register controls four bits in the 1553 status word. The format of the CR is shown below:

Configuration Register (CR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE		$\overline{A}$/B	SOE	$\overline{DBA}$	$\overline{BSY}$	$\overline{SRQ}$	$\overline{SSF}$	Not Used (= 1)							

Address: On,FF2,002 hex (n = Processor ID)
Access Level: Supervisor
Initial State: 00FF hex

MODE 1553 Operating Mode - These two bits establish the 1553 operating mode as shown below:

Bit 15	Bit 14	Operating Mode
0	0	Bus Controller (BC)
0	1	Bus Monitor (MT)
1	0	Remote Terminal Unit (RTU)
1	1	Illegal

$\overline{A}$/B RAM Buffer A or B - The 1553 interface can be implemented with the 4K × 16-bit RAM divided into two buffer areas, current and noncurrent. The designations A and B are given to these two areas, and either may be the current area. The area that the 66300 II accesses is determined by the state of the A/B bit: 0 - A, 1 - B.

SOE Stop On Error - When this bit is set, the 66300 II stops at the end of the current data block transfer if an error is detected. When the bit is cleared, the 66300 II continues if there are more messages to send after the current block is transferred.

$\overline{DBA}$ Dynamic Bus Control Acceptance - This bit corresponds to the bit in the 1553 status word that occurs at bit time 18. The function of this bit as stated in MIL-STD-1553B (page 13) is as follows:

> This bit shall be used if the RT implements the optional dynamic bus control function. This bit, when used, shall indicate the acceptance or rejection of a dynamic bus control offer. . . . A logic one shall indicate acceptance of control, and a logic zero shall indicate rejection of control. If this function is not used, this bit [in the 1553 status word] shall be set to logic zero.

A zero in bit position 11 of the CR asserts this bit in the 1553 status word. A one negates it.

$\overline{BSY}$ Busy - This bit corresponds to the bit in the 1553 status word that occurs at bit time 16. The function of this bit as stated in MIL-STD-1553B (page 13) is as follows:

> This bit, when used, shall indicate that the RT or subsystem is unable to move data to or from the subsystem in compliance with the bus controller's command. A logic one shall indicate the presence of a busy condition, and a logic zero its absence. In the event the busy bit is set in response to a transmit command, then the RT shall transmit its status word only. If this function is not implemented, the bit [in the 1553 status word] shall be set to logic zero.

A zero in bit position 10 of the CR asserts this bit in the 1553 status word. A one negates it.

$\overline{\text{SRQ}}$ Service Request - This bit corresponds to the bit in the 1553 status word that occurs at bit time 11. The function of this bit as stated in MIL-STD-1553B (page 12) is as follows:

> This bit, when used, shall indicate the need for the bus controller to take specific predefined actions relative to either the RT or associated subsystem. Multiple subsystems, interfaced to a single RT, which individually require a service request signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific requesting subsystem. The service request bit is intended to be used only to trigger data transfer operations which take place on an exception rather than a periodic basis. A logic one shall indicate the presence of a service request, and a logic zero its absence. If this function is not implemented, the bit [in the 1553 status word] shall be set to zero.

A zero in bit position 9 of the CR asserts this bit in the 1553 status word. A one negates it.

$\overline{\text{SSF}}$ Subsystem Flag - This bit corresponds to the bit in the 1553 status word that occurs at bit time 17. The function of this bit in MIL-STD-1553B (page 13) is as follows:

> This bit, when used, shall flag a subsystem fault condition, and alert the bus controller to potentially invalid data. Multiple subsystems, interfaced to a single RT, which individually require a subsystem flag bit signal shall logically OR their individual signals into the single status word bit. In the event

this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific reporting subsystem. A logic one shall indicate the presence of the flag, and a logic zero its absence. If not used, this bit [in the 1553 status word] shall be set to logic zero.

A zero in bit position 8 of the CR asserts this bit in the 1553 status word. A one negates it.

9.4.2 Start/Reset Register

The Start/Reset Register (S/RR) is a write-only register that contains two bits for initiating data transfers and resetting all 66300 II registers. The format of the S/RR is shown below:

Start/Reset Register (S/RR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														CS	RST

Address: On,FF2,006 hex (n = Processor ID)
Access Level: Supervisor (Write only)
Initial State: Write Only

CS Controller Start - In BC mode, setting this bit causes the 66300 II to start message transmission. In MT mode, setting this bit enables monitor operation.

RST Reset - Setting this bit clears all 66300 II registers.

9.4.3 Interrupt Mask Register

The Interrupt Mask Register (IMR) enables and disables interrupt requests on certain data transfer conditions. The format of the IMR is shown below:

Interrupt Mask Register (IMR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used (= 1)								Not Used				BEM	F/S	*	EOM

*Not Used

Address: On,FF2,000 hex (n = Processor ID)
Access Level: Supervisor
Initial State: FF00 hex

BEM Bus Controller End of Message - When this bit is set, the 66300 II generates an interrupt request after all BC messages have been transferred. When cleared, no interrupt is generated for this condition.

F/S Format Error/Status Set - When this bit is set, the 66300 II generates an interrupt request under the following conditions:

Loop Test Failure: Received loopback word did not match the transmitted word.

Message Error: Received message contained an address error, a status word with one of the eight 1553 status bits set, or a 1553 specification violation such as a parity error or a Manchester encoding error.

Time Out: Transmission was not received within the allotted time.

Status Set: Received status word contained status bits set or an address error.

When the bit is cleared, no interrupt is generated for these conditions.

EOM End of Message - When this bit is set, the 66300 generates an interrupt request after every message transfer. When cleared, no interrupt is generated for this condition.

9.5 REMOTE TERMINAL ADDRESS CONNECTOR

The remote terminal address connector, J607, accommodates a hardwired plug that specifies the module's 1553 remote terminal address. The pinout of J607 is shown in Figure 9-2. Pin descriptions are given in Table 9-2.

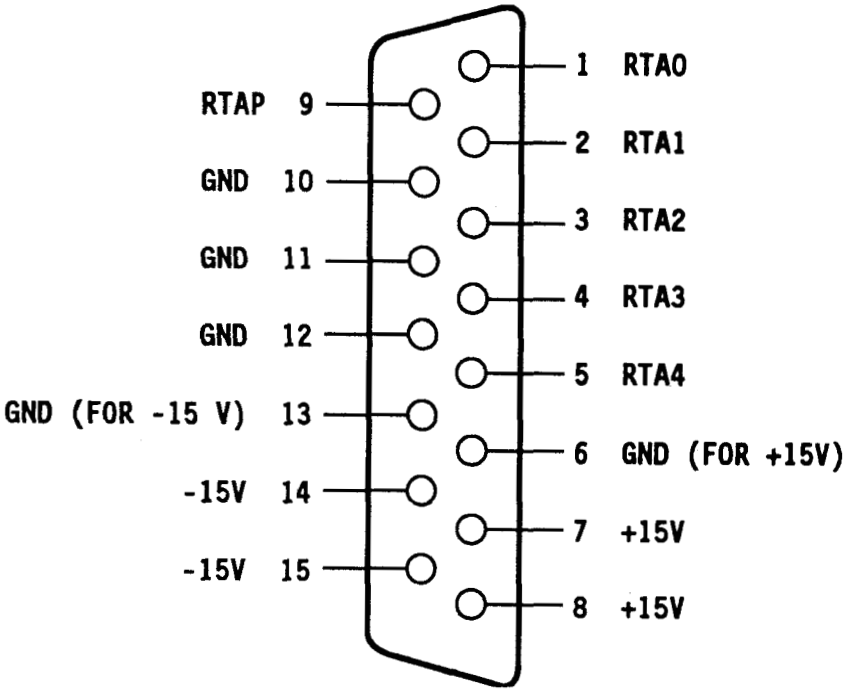


Figure 9-2. Remote Terminal Address Connector (J607)

TABLE 9-2. REMOTE TERMINAL ADDRESS CONNECTOR (J607) PIN DESCRIPTIONS

Pin	Mnemonic	Description
1	RTA0	Remote Terminal Address Bit 0 (LSB).
2	RTA1	Remote Terminal Address Bit 1.
3	RTA2	Remote Terminal Address Bit 2.
4	RTA3	Remote Terminal Address Bit 3.
5	RTA4	Remote Terminal Address Bit 4 (MSB).
6	GND	Ground for +15 V pins (7, 8).
7	+15 V	+15 V power input to 1553 transceiver device (U603). (These inputs are only used if the transceiver device requires +15 V. Normally, the device only requires +5 V from the 1553 module.)
8	+15 V	
9	RTAP	Remote Terminal Address Parity Bit.
10	GND	Logic ground from the 1553 module. These pins can be used to set any of the RTA0-RTA4 and RTAP bits to logic 0.
11	GND	
12	GND	
13	GND	Ground for the -15 V pins (14, 15).
14	-15 V	-15 V power input to 1553 transceiver device (U603). (These inputs are only used if the transceiver device requires -15 V. Normally, the device only requires +5 V from the 1553 module.)
15	-15 V	

Notes:

1. The BUS-65600 has internal pull-up resistors for RTA0-RTA4 and RTAP. These lines will default to a logic 1 if left unconnected.

2. The ±15 V inputs are only required if the 1553 transceiver device uses ±15 V power. The standard transceiver used on the SANDAC V MIL-STD-1553B Module does not require power from these inputs.

9.6 66300 II EXTERNAL REGISTERS

In addition to its three internal registers, the 66300 II uses the following external registers:

- Remote Terminal Address Register (RTAR)
- Prescale/Count Enable Register (P/CER)
- Tag Register/Counter (TR/C)
- Interrupt Vector Register (IVR)

These registers are described in the following subsections.

9.6.1 Remote Terminal Address Register

The Remote Terminal Address Register (RTAR), U616, is a read-only register that reflects the RTU address at the remote terminal address connector (J607). The format of the RTAR is shown below:

Remote Terminal Address Register (RTAR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used = 1								0	0	P	RTU Address				

Address: 0n,FF2,00A hex (n = Processor ID)
Access Level: Supervisor
Initial State: Determined by address on J607

RTU Address - 5-bit RTU address.

P - Parity: Odd parity for the 5 bits in positions 4 through 0.

9.6.2 Prescale/Counter Enable Register

The Prescaler/Counter Enable Register (P/CER), U608, contains eight bits of prescale count value and one bit that enables the Tag Register/Counter (TR/C). The function of the P/CER is directly related to the TR/C (9.6.3). Writing any value to the P/CER clears the TR/C. The format of the P/CER is shown below:

Prescale/Count Enable Register (P/CER)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used							TCE	Prescale Count							

Address: On,FF2,00C hex (n = Processor ID)
Access Level: Supervisor
Initial State: Indeterminate (all except TCE are write only)

TCE Tag Register Count Enable - When this bit is set, the tag counter is enabled, and the value in the Tag Register/Counter is incremented by one each time the prescale counter rolls over. When this bit is cleared, the tag counter is disabled. This bit is both readable and writable.

Prescale Count - Bits 7 through 0 are write-only and form a prescale value for the tag counter. The prescaler divides a 2 MHz input clock by the divisor value established by these bits. The required divisor is loaded into the register in 2's complement form. A divisor of 1 (FF in 2's complement) is illegal; a value of 00 gives a divisor of 256.

9.6.3 Tag Register/Counter

The Tag Register/Counter (TR/C), U609 and U610, stores a fixed value or accumulates a count of the prescaler output as described in 9.6.2. The TR/C is cleared by writing to the P/CER. The value in the TR/C is written to the 4K × 16-bit RAM at the beginning and the end of every message transfer. The format of the TR/C is shown below:

Tag/Count Register (T/CR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tag Value															

Address: On,FF2,00E hex (n = Processor ID)
Access Level: Supervisor
Initial State: 0000 hex

9.6.4 Interrupt Vector Register

The Interrupt Vector Register (IVR) stores the 8-bit interrupt vector to be returned to the MPU during an interrupt acknowledge cycle. A user-selected vector is written to the register by the MPU. The register is also readable. The format of the IVR is shown below:

Interrupt Vector Register (IVR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used = 1								Interrupt Vector							

Address: On,FF2,008 hex (n = Processor ID)
Access Level: Supervisor
Initial State: Indeterminate

9.7 BUS-65600

The BUS-65600 BC, RTU, and MT (U602) interfaces the BUS-66300 II (U601) with the BUS-63125 Dual Transceiver. The 65600 is controlled by handshaking from the 66300 II and has no user-accessible locations. Complete information on the BUS-65600 is in the ILC Data Device Corporation publication, *BUS-65600 MIL-STD-1553 Bus Controller, Remote Terminal, and Bus Monitor.*

In RTU mode, the 65600 is supported by U605, an erasable programmable logic device (EPLD), that reports illegal 1553 "mode codes." This device is described in the following subsection.

9.7.1 Illegal Mode Code EPLD

When the MIL-STD-1553B Module is operating as an RTU, a 1553 command containing a mode code may be received. (Refer to document *MIL-STD-1553B* for a description of mode codes.) The MIL-STD-1553B Module allows selected mode codes to be deemed illegal via the EPLD, U605. The EPLD has as its inputs the word count (WC4-WC0), mode code (LMC), transmit/receive (T/R), and broadcast (BCST) outputs of the BUS-65600. All mode codes received are presented to the EPLD via these lines. When a received mode code matches one of the preprogrammed illegal mode codes, the EPLD asserts the 65600 ILLCMD line, causing the ERR (error) bit to be set in the 1553 status word.

With standard SANDAC V hardware, all mode codes assigned in the document *MIL-STD-1553B* are allowed; all others are illegal. The EPLD may be reprogrammed to make any mode codes illegal. The logic equations for the standard EPLD are given in Table 9-3.

TABLE 9-3. STANDARD EPLD (U605) LOGIC EQUATIONS

```
INPUTS:    WC0@2, WC1@3, WC2@4, WC3@5, WC4@6, TR@7, LMC@8, BCSTRCV~@9

OUTPUTS:   ILCMD~@12, DUMMY1@13, DUMMY2@14, DUMMY3@15, DUMMY4@16,
           DUMMY5@17, DUMMY6@18, DUMMY7@19

NETWORK:   WC0 = INP(WC0)              % Word count bits from 65600 %
           WC1 = INP(WC1)
           WC2 = INP(WC2)
           WC3 = INP(WC3)
           WC4 = INP(WC4)
           TR = INP(TR)                % Transmit/receive~ bit %
           LMC = INP(LMC)              % Latched mode code %
           BCSTRCV = INP(BCSTRCV~)     % Broadcast receive bit %

           ILLCMD~ = CONF(ILLCMNDc,VCC) %Illegal command output to 65600
                                        %
           DUMMY1 = CONF(DUMMY1c,VCC) % Make Macrocells available %
           DUMMY2 = CONF(DUMMY2c,VCC) % Make Macrocells available %
           DUMMY3 = CONF(DUMMY3c,VCC) % Make Macrocells available %
           DUMMY4 = CONF(DUMMY4c,VCC) % Make Macrocells available %
           DUMMY5 = CONF(DUMMY5c,VCC) % Make Macrocells available %
           DUMMY6 = CONF(DUMMY6c,VCC) % Make Macrocells available %
           DUMMY7 = CONF(DUMMY7c,VCC) % Make Macrocells available %

EQUATIONS: See Next Page
```

TABLE 9-3. CONTINUED

```
EQUATIONS: ILLCMD- = LMC'
                   + LMC * TR * WC4' * (WC3' + WC3 * WC2' * WC1' * WC0')
                   + LMC * TR * WC4 * WC3' * WC2' *
                     (WC1' * WC0' + WC1 * WC0' * WC1 * WC0)
                   + LMC * TR' * WC4 * WC3' * WC1' *
                     (WC2' * WC0 + WC2 * WC0' * WC2 * WC0);

           DUMMY1c = BCSTRCV;
           DUMMY2c = BCSTRCV;
           DUMMY3c = BCSTRCV;
           DUMMY4c = BCSTRCV;
           DUMMY5c = BCSTRCV;
           DUMMY6c = BCSTRCV;
           DUMMY7c = BCSTRCV;
```

9.8 1553 BUS INTERFACE

The 1553 bus interface supports two 1553 channels, Channel A and Channel B. The bus interface circuit consists of the following components:

1 STC FC1593921 (5V) Dual Transceiver (U603)
2 STC FC1553TI (5V) Transformers (T601, T602)
2 Triaxial Connectors (J605, J606)

Each channel of the dual transceiver has a data and control interface with the BUS-65600 (U602). The transceiver also interfaces with the primaries of the two coupling transformers. The secondaries of the transformers can be jumpered to the triaxial connectors to provide either direct bus coupling or transformer coupling. Complete information on jumper configurations for bus coupling is provided in Appendix B.

9.9 INTERRUPT LOGIC

The MIL-STD-1553B Module can use local expansion bus interrupt request lines $\overline{IRQW}$, $\overline{IRQX}$, $\overline{IRQY}$, or $\overline{IRQZ}$. A hardware jumper connects the module $\overline{IRQ}$ output (U607-13) to the selected request line. The corresponding local expansion bus interrupt acknowledge line, $\overline{IACKW}$, $\overline{IACKX}$, $\overline{IACKY}$, or $\overline{IACKZ}$, must be connected to the

module $\overline{IACK}$ input (U607-19). The default jumper setting uses request and acknowledge Y ($\overline{IRQY}$/$\overline{IACKY}$). The module also provides an $\overline{IACK}$ daisy chain output that can be jumpered to the local bus through J4-53 ($\overline{EIACKDC}$). (Detailed hardware jumper information is given in Appendix B.)

In response to a 68020 MPU interrupt acknowledge cycle, the module's Interrupt Vector Register (IVR), U611, supplies a user-selected interrupt vector. (The IVR is described in 9.6.4.)

9.10 OPERATION AS A BUS CONTROLLER

For the MIL-STD-1553B Module to function as a bus controller (BC), the following steps are required:

1. The 4K × 16-bit RAM is partitioned for BC operation.

2. The RAM is initialized with the required data values.

3. The BUS-66300 II is reset and programmed for BC mode. Other desired 66300 II operational features, e.g., interrupt conditions, are also established.

4. A Controller Start command is issued to the BUS-66300 II.

Once the 66300 II has been started, it works autonomously with the RAM and the BUS-65600 to complete the 1553 transfer. Detailed descriptions of the steps listed above are given in the following paragraphs.

9.10.1 BC Mode RAM Partitioning

For BC operation, the 4K × 16-bit RAM is partitioned as shown in Table 9-4. To support double buffering, locations are specified for both A and B area stack pointers, message counters, internal pointers, descriptor stacks, and messages. An overview of how these components are used for BC mode memory management is shown in Figure 9-3.

TABLE 9-4. 4K × 16-BIT RAM PARTITIONING FOR BC MODE

Processor Module Address*	BUS-66300 II Address*	Function
0n,FF0,000-0n,FF0,1FF	0000-00FF	User Defined**
0n,FF0,200-0n,FF0,201	0100	Stack Pointer A
0n,FF0,202-0n,FF0,203	0101	Message Counter A
0n,FF0,204-0n,FF0,207	0102-0103	Internal Pointer A
0n,FF0,208-0n,FF0,209	0104	Stack Pointer B
0n,FF0,20A-0n,FF0,20B	0105	Message Counter B
0n,FF0,20C-0n,FF0,20F	0106-0107	Internal Pointer B
0n,FF0,210-0n,FF1,FFF	0108-0FFF	User Defined**

*Addresses are in hex; "n" is the Processor ID.
**User-defined areas include Descriptor Stacks A and B and message blocks.

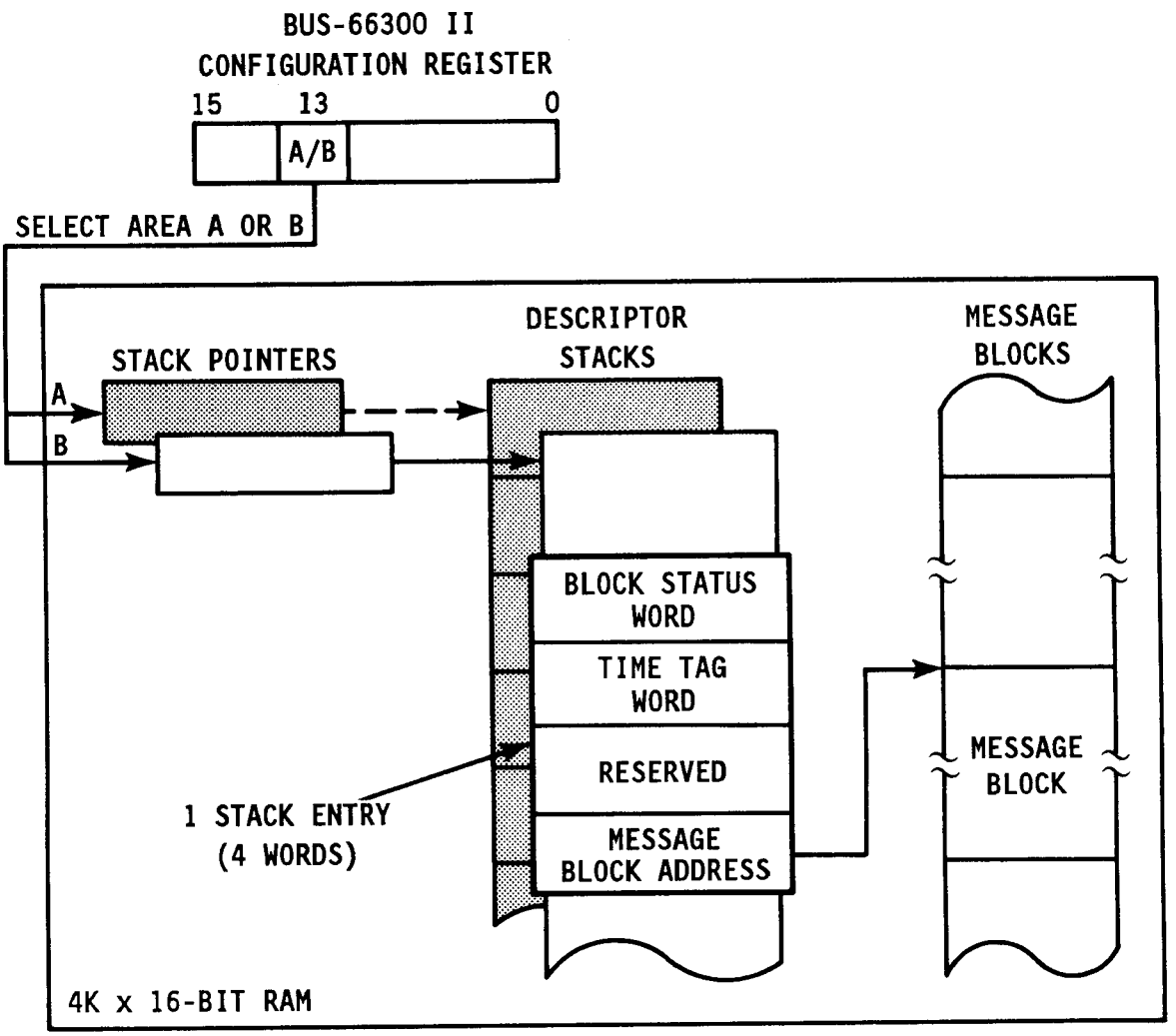


Figure 9-3. BC Mode Memory Management

9.10.2 BC Mode RAM Initialization

The following steps are required to initialize the 4K × 16-bit RAM for BC mode operation:

1. Initialize stack pointers.
2. Load message counter.
3. Initialize descriptor stack with message block addresses.
4. Load message blocks.

Descriptions of the components loaded into RAM are given in the following paragraphs.

9.10.2.1 Stack Pointers A, B. The stack pointers specify the 16-bit address of a descriptor stack. Stack Pointer A has the address of Descriptor Stack A; Stack Pointer B has the address of Descriptor Stack B. A Descriptor Stack contains 64 four-word entries and automatically wraps around (last entry is followed by the first). The current area stack pointer determines the Descriptor Stack entry that applies to the current message. The BUS-66300 II automatically increments the current area stack pointer by four upon completion of each message even if an error is detected.

9.10.2.2 Message Counters A, B. The message counters specify the 16-bit count of the number of messages that will be included in the 1553 transfer. The count (number of messages) must be in 1's complement form.

9.10.2.3 Descriptor Stacks A, B. The descriptor stack contains one four-word entry for each message in the 1553 transfer. The format of a stack entry is shown below:

WORD 1	BLOCK STATUS
WORD 2	TIME TAG
WORD 3	RESERVED
WORD 4	MESSAGE BLOCK ADDRESS

9.10.2.3.1 Block Status. The Block Status word is initialized by the BUS-66300 II when it starts a message transfer and is updated at the conclusion of a transfer. The format of the Block Status word is shown below:

BLOCK STATUS WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOM	SOM	$\overline{A}$/B	ERR	SS	FE	RTO	LTF	Not Used							

EOM End of Message - Set to indicate a message transfer is complete.

SOM Start of Message - Set to indicate that a message transfer has been started and is in progress. When the transfer is complete, this bit is cleared and EOM is set.

$\overline{A}$/B In BC mode, this bit is always 0. In RTU mode, this bit is 0 if 1553 channel A is used; it is 1 if channel B is used.

ERR Error - Set to indicate that an error was detected during a message transfer.

SS Status Set - Set to indicate that the status word received for the 1553 transfer contained one or more status bits set or an address error (BC mode only).

FE Format Error - Set to indicate that a transfer violated a 1553 specification (parity error, Manchester encoding error, etc.).

RTO Response Timeout - Set to indicate the expected transmission was not received in the allotted time (BC mode only).

LTF Loop Test Fail - Set to indicate that the word received on loop back did not match the transmitted word.

9.10.2.3.2 Time Tag. The Time Tag stores the value provided by the Tag Register/Counter (TR/C). This location is initialized with the value from the TR/C at the start of a message transfer and is updated at the end of the transfer.

9.10.2.3.3 Message Block Address. The Message Block Address is the 16-bit address of the message for the 1553 transfer.

9.10.2.4 Message Blocks. The message blocks in the 4K × 16-bit RAM consist of a group of consecutive words that are loaded with the control, command, data, and status words for a 1553 message. The formats of the different 1553 message types used in BC mode are shown in Figure 9-4.

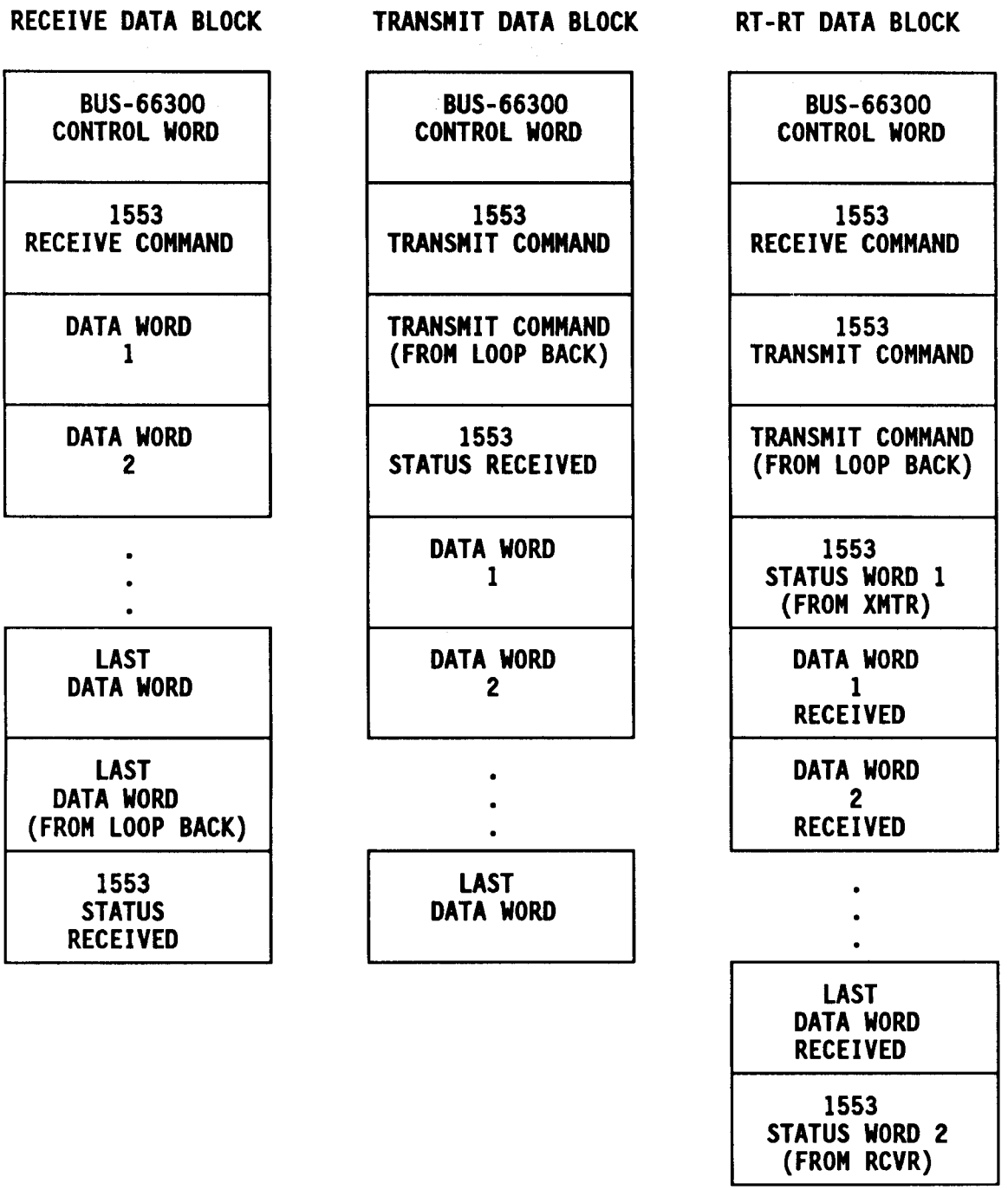


Figure 9-4 (1 of 3). BC Mode Message Block Formats

MODE CODE WITHOUT DATA	MODE CODE WITH DATA RECEIVE DATA	MODE CODE WITH DATA TRANSMIT DATA
BUS-66300 CONTROL WORD	BUS-66300 CONTROL WORD	BUS-66300 CONTROL WORD
1553 MODE COMMAND	1553 MODE COMMAND	1553 MODE COMMAND
MODE COMMAND (FROM LOOP BACK)	DATA WORD	MODE COMMAND (FROM LOOP BACK)
1553 STATUS WORD	DATA WORD (FROM LOOP BACK)	1553 STATUS WORD
	1553 STATUS WORD	DATA WORD RECEIVED

Figure 9-4 (2 of 3). BC Mode Message Block Formats

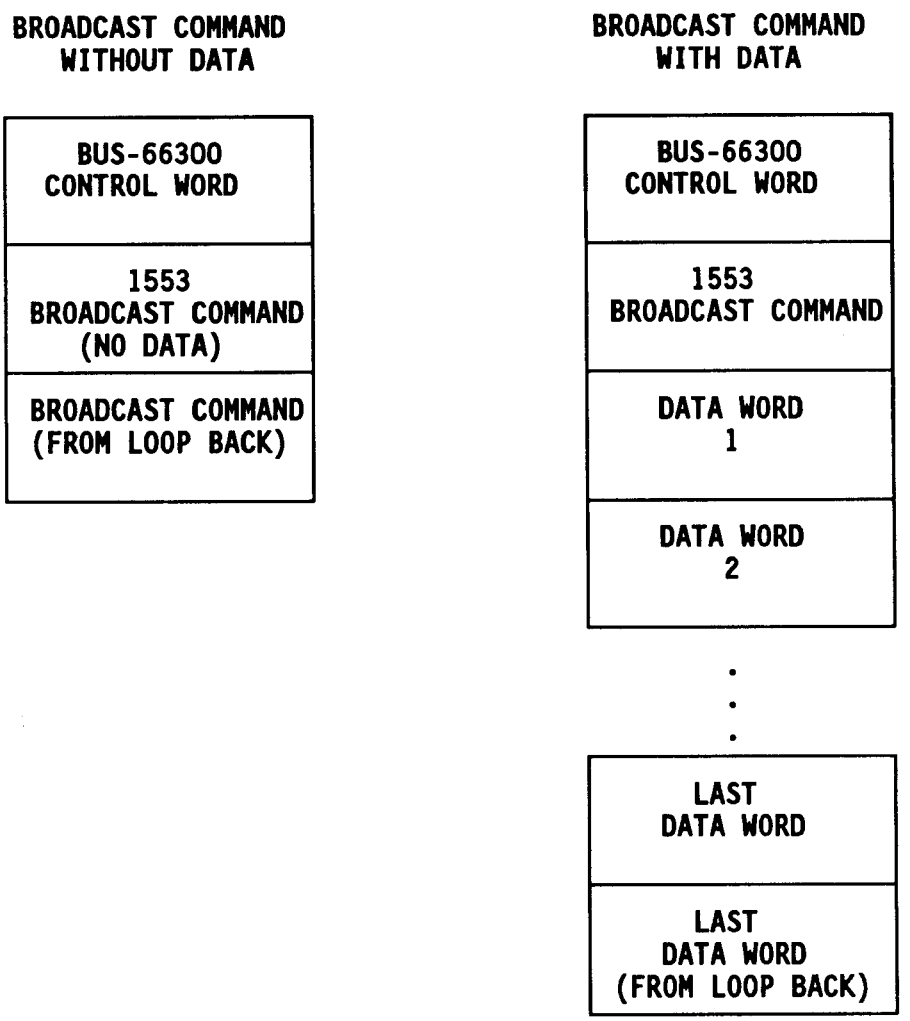


Figure 9-4 (3 of 3). BC Mode Message Block Formats

For a description of the 1553 command, data, and status words included in the message blocks, refer to *MIL-STD-1553B*. The format of the BUS-66300 II control word included in the message blocks is shown below:

BUS-66300 II CONTROL WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								A/$\overline{B}$	*	MBB	*		MC	B	R-R

*Not Used

A/$\overline{B}$ Bus Channel A/B - Setting this bit causes transmission over 1553 bus A. Clearing the bit causes transmission over 1553 bus B.

MBB Mask Broadcast Bit - Setting this bit prevents the Broadcast RCVD bit of the status word response from signaling a status error during a Broadcast command.

MC Mode Code - When this bit is set, it signifies that the 1553 command word count field signifies a mode code type. When cleared, the field contains a count.

B Broadcast - When this bit is set, it indicates a Broadcast command (multiple RTUs addressed, no status word expected).

R-R RTU-to-RTU - When this bit is set, the BC initiates an RTU-to-RTU transfer.

9.10.3 BC Mode BUS-66300 II Initialization

After the 4K × 16-bit RAM has been initialized, the BUS-66300 II is initialized as follows:

1. A Reset command is issued to the 66300 II.
2. The BC mode of operation is set in the 66300 II Configuration Register.
3. The required interrupt masks are set via the 66300 II Interrupt Mask Register.

Once the device is initialized, a Controller Start command is issued. The BUS-66300 II then works autonomously with the BUS-65600 and the 4K × 16-bit RAM to complete the 1553 transfer. One or more of the interrupts described in 9.4.3 may be used to notify the MPU of completion or errors.

9.11 OPERATION AS A REMOTE TERMINAL UNIT

For the MIL-STD-1553B Module to function as a remote terminal unit (RTU), the following steps are required:

1. The 4K × 16-bit RAM is partitioned for RTU operation.

2. The RAM is initialized with the required data values.

3. The BUS-66300 II is reset and programmed for RTU mode. Other desired 66300 II operational features, for example, interrupt conditions, are also established.

4. The 66300 II waits for a 1553 command.

Once the 66300 II receives a 1553 command, it works autonomously with the 4K × 16-bit RAM and the BUS-65600 to complete the 1553 transfer. Detailed descriptions of the steps listed above are given in the following subsections.

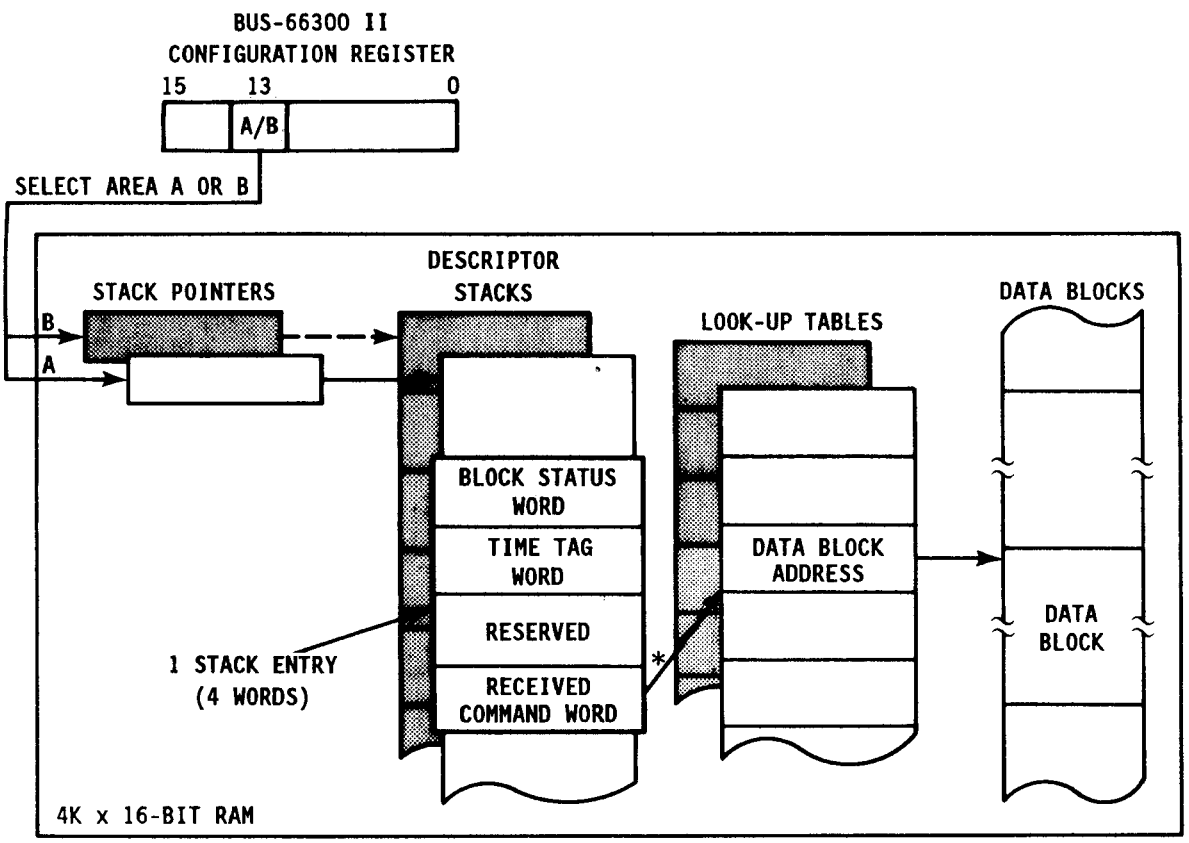
9.11.1 RTU Mode RAM Partitioning

For RTU operation, the 4K × 16-bit RAM is partitioned as shown in Table 9-5. To support double buffering, locations are specified for both A and B area stack pointers, internal pointers, look-up tables, descriptor stacks, and data blocks. An overview of how these components are used for RTU mode memory management is shown in Figure 9-5.

TABLE 9-5. 4K × 16-BIT RAM PARTITIONING FOR RTU MODE

Processor Module Address*	BUS-66300 II Address*	Function
0n,FF0,000-0n,FF0,1FF	0000-00FF	User Defined**
0n,FF0,200-0n,FF0,201	0100	Stack Pointer A
0n,FF0,202-0n,FF0,203	0101	Reserved
0n,FF0,204-0n,FF0,207	0102-0103	Internal Pointer A
0n,FF0,208-0n,FF0,209	0104	Stack Pointer B
0n,FF0,20A-0n,FF0,20B	0105	Reserved
0n,FF0,20C-0n,FF0,20F	0106-0107	Internal Pointer B
0n,FF0,210-0n,FF0,27F	0108-013F	User Defined**
0n,FF0,280-0n,FF0,2FF	0140-017F	Look-up Table A
0n,FF0,300-0n,FF0,37F	0180-01BF	User Defined**
0n,FF0,380-0n,FF0,3FF	01C0-01FF	Look-up Table B
0n,FF0,400-0n,FF1,FFF	0200-0FFF	User Defined**

*Addresses are in hex; "n" is the Processor ID.
**User-defined areas include Descriptor Stacks A and B and data blocks.



*POINTER IS FORMED WITH T/$\bar{R}$ BIT AND SUBADDRESS FIELD OF COMMAND WORD AND BIT 13 OF CR.

Figure 9-5. RTU Mode Memory Management

9.11.2 RTU Mode RAM Initialization

The following steps are required to initialize the 4K × 16-bit RAM for RTU mode operation:

1. Initialize stack pointers.
2. Load look-up table with data block addresses.
3. Load data into transmit data blocks.

The stack pointers function the same as those used in BC mode; refer to 9.10.2.1 for a description. The look-up tables and descriptor stacks are described in the following paragraphs.

9.11.2.1 Look-Up Tables. The first 32 words of the look-up table contain the addresses of the data blocks to be used when receiving data from 1553 subaddresses 0 through 31, respectively. The next 32 words of the table contain the addresses of the data blocks to be used when the RTU transmits data to 1553 subaddresses 0 through 31, respectively.

9.11.2.2 Descriptor Stacks A, B. The descriptor stack contains one four-word entry for each message in the 1553 transfer. The format of a stack entry is shown below:

WORD 1	BLOCK STATUS
WORD 2	TIME TAG
WORD 3	RESERVED
WORD 4	RECEIVED COMMAND WORD

The Block Status and Time Tag words are the same as those used for BC mode; refer to 9.10.2.3.1 and 9.10.2.3.2 for a description. The Received Command word is described below.

9.11.2.2.1 Received Command Word. The format of the descriptor stack Received Command word is shown below:

RECEIVED COMMAND WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTU Address					T/R	RTU Subaddress					Word Cnt/Mode Code				

This word is an exact copy of the 1553 command that was sent to the RTU. For a description of the fields refer to *MIL-STD-1553B*.

The BUS-66300 II uses the T/R and the RTU Subaddress fields of the command word and the A/B bit in the Configuration Register to formulate a look-up table address. This step is illustrated in Figure 9-6. The format of the address is shown below:

LOOK-UP TABLE ADDRESS CALCULATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	$\bar{A}$/B	1	T/R	RTU Subaddress				

9.11.2.3 Data Blocks. Data blocks are reserved in 4K × 16-bit RAM for storing data received from 1553 subaddresses 0 through 31 and for holding data to be transmitted to 1553 subaddresses 0 through 31. A data block may be any length sufficient to contain the particular message as long as it does not cross a 256-word boundary. Data blocks may be shared by the Look-up Tables A and B.

9.11.3 RTU Mode BUS-66300 II Initialization

After the 4K × 16-bit RAM has been initialized for RTU mode, the BUS-66300 II is initialized as follows:

1. A Reset command is issued to the 66300 II.
2. The RTU mode of operation is set in the 66300 II Configuration Register.
3. The required interrupt masks are set via the 66300 II Interrupt Mask Register.

Once the 66300 II is initialized, it waits for a 1553 command. When a command is received, the 66300 II works autonomously with the BUS-65600 and the 4K × 16-bit RAM to complete the transfer. One or more of the interrupts described in 9.4.3 may be used to notify the MPU of completion or errors.

9.12 OPERATION AS A BUS MONITOR

For the MIL-STD-1553B Module to function as a bus monitor (MT), the following steps are required:

1. The 4K × 16-bit RAM is partitioned for MT operation.

2. The RAM is cleared and the stack pointers are loaded.

3. The BUS-66300 II is reset and programmed for MT mode. Other desired 66300 II operational features, for example, interrupt conditions, are also established.

4. A Controller Start command is issued to the 66300 II.

Once the 66300 II has been started, it works autonomously with the BUS-65600 and the 4K × 16-bit RAM. Detailed descriptions of the steps listed above are given in the following subsections.

9.12.1 MT Mode RAM Partitioning

For MT operation, the 4K × 16-bit RAM is partitioned as shown in Table 9-6. To support double buffering, locations are specified for both A and B area stack pointers.

9.12.2 MT Mode RAM Initialization

The following steps initialize the 4K × 16-bit RAM for MT mode operation:

1. Clear entire RAM.
2. Initialize stack pointers.

In MT mode, the entire 4K × 16-bit RAM is used as a stack to store valid 1553 words and their corresponding identification words. The stack pointers contain the address where the first received word will be stored. This value is loaded into an internal register in the BUS-66300 II. Once MT operation begins, the stack pointer locations are overwritten.

TABLE 9-6. 4K × 16-BIT RAM PARTITIONING FOR MT MODE

Processor Module Address*	BUS-66300 II Address*	Function
0n,FF0,000-0n,FF0,001	0000	1553 Word
0n,FF0,002-0n,FF0,003	0001	Identification (ID) Word for preceding 1553 word
0n,FF0,004-0n,FF0,1FF	0002-0FFF	1553 word/ID word pairs
0n,FF0,200-0n,FF0,201	0100	Stack Pointer A**
0n,FF0,208-0n,FF0,209	0104	Stack Pointer B**

*Addresses are in hex; "n" is the Processor ID.
**These areas are overwritten once data collection begins.

The format of the identification word stored with each 1553 word is shown below:

MT IDENTIFICATION WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Gap Time								1	1	1	ERR	CS	$\overline{A}$/B	CD	0

Gap Time - This field contains eight bits that are used as a counter. The field is reset for each new transmission and incremented every 0.5 μs. If the field reaches a count of FF hex (128 μs), it remains static.

Bits 7,6,5 Word Transfer - These bits are set to 1. They may be used to indicate that a word was successfully transferred from the 1553 bus. The bits may be cleared in memory by the MPU at the time it reads the corresponding data word; this provides a method of keeping track of words that have been processed.

ERR Error - When this bit is cleared, it indicates that the associated 1553 word was valid. When set, it indicates the word had a Manchester error, parity error, low bit count, or status/sync field.

CS Command Sync - When this bit is set, it indicates a command or status sync field. When cleared, it indicates a data sync field.

$\overline{A}$/B Channel $\overline{A}$/B - When this bit is set, it indicates that the transmission was received on channel B. When cleared, it indicates channel A.

CD Contiguous Data - This bit is set if the current word was received at least 2 μs after receipt of the previous word (mid-parity to mid-sync).

9.12.3 MT Mode BUS-66300 II Initialization

After RAM has been initialized for MT mode, the BUS-66300 II is initialized as follows:

1. A Reset command is issued to the 66300 II.
2. The MT mode of operation is set in the 66300 II Configuration Register.
3. Initialize the stack pointer.

Once the device is initialized, a Controller Start command is issued to the 66300 II to start MT operation. The 66300 II then works autonomously with the BUS-65600 and the 4K $\times$ 16-bit RAM logging 1553 transfers into memory.

NOTES

APPENDIX A: MODULE IDENTIFICATION

CONTENTS

PROCESSOR MODULE A-2
UTILITY MODULE A-2
GLOBAL MEMORY MODULE A-3
EXPANSION MEMORY MODULE A-3
SYSTEM I/O MODULE A-4
MIL-STD-1553B MODULE A-4

Processor Module

PM - 'M' XXX 'T' - n000000 - nFFFFFF (PMn)

- Address Space
- Type
  - Q - Mission Qualified
  - X - Socketed Unit
- Serial Number
- Manufacturer
  - H - Honeywell
  - S - Sandia Labs
- Processor Module

Utility Module

UM - 'M' XXX 'T' - 00000000 - 000FFFFF

- Address Space
- Type
  - Q - Mission Qualified
  - X - Socketed Unit
- Serial Number
- Manufacturer
  - H - Honeywell
  - S - Sandia Labs
- Utility Module

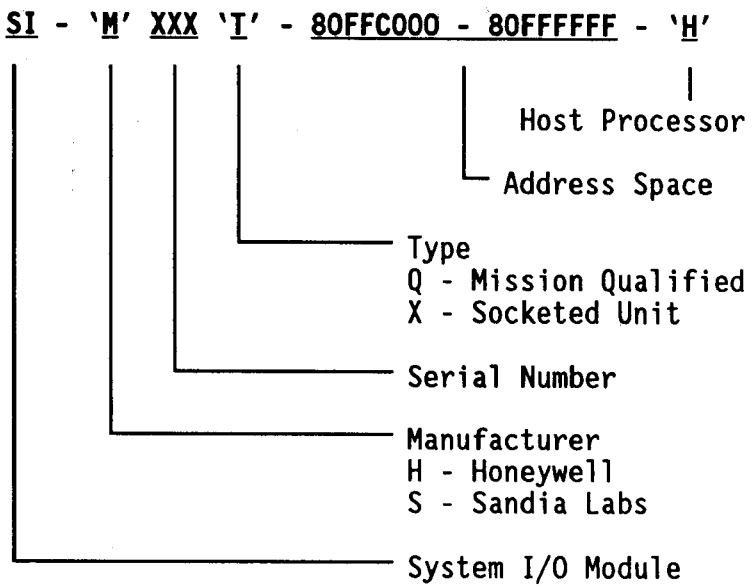
Global Memory Module GM - 'M' XXX 'T' - 'W' - nn0000 - nnFFFF

- nn0000 - nnFFFF: Address Space
- 'W': Wait States
- 'T': Type
  - Q - Mission Qualified
  - X - Socketed Unit
- XXX: Serial Number
- 'M': Manufacturer
  - H - Honeywell
  - S - Sandia Labs
- GM: Global Memory Module

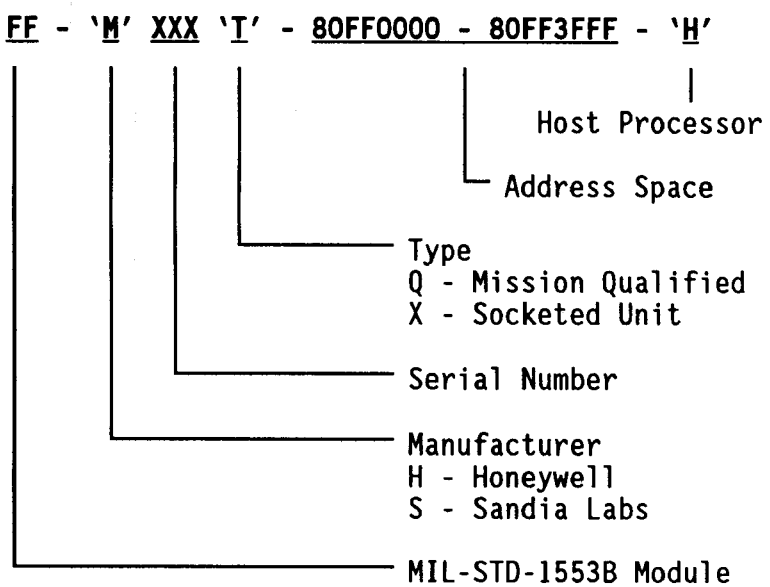
Expansion Memory Module EM - 'M' XXX 'T' - n00000 - nFFFFF - 'H'

- 'H': Host Processor
- n00000 - nFFFFF: Address Space
- 'T': Type
  - Q - Mission Qualified
  - X - Socketed Unit
- XXX: Serial Number
- 'M': Manufacturer
  - H - Honeywell
  - S - Sandia Labs
- EM: Expansion Memory Module

System I/O Module



MIL-STD-1553B Module



APPENDIX B: HARDWARE JUMPERS

CONTENTS

PROCESSOR MODULE B-3
UTILITY MODULE B-7
GLOBAL MEMORY MODULE B-13
EXPANSION MEMORY MODULE B-21
SYSTEM I/O MODULE B-27
MIL-STD-1553B MODULE B-69

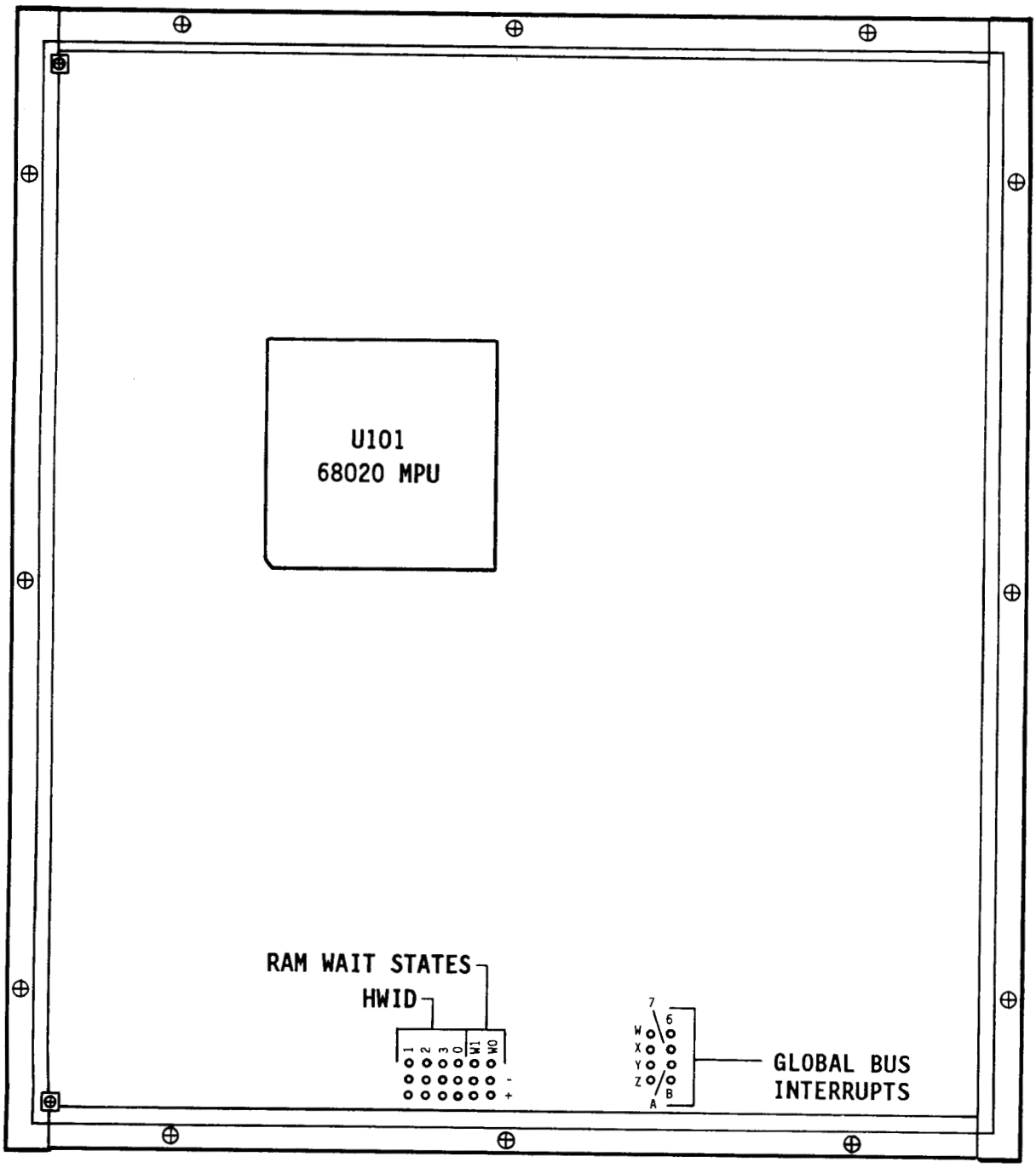


Figure B-1. Processor Module Jumper Locations

B.1 PROCESSOR MODULE

The Processor Module has three groups of hardware jumpers that configure the following:

- Hardware ID (HWID)
- RAM Wait States
- Global Bus Interrupt Requests

The location of the jumper groups is shown in Figure B-1 (facing page). Jumper settings are described in the following subsections.

B.1.1 HWID

The Processor Module HWID is set by connecting the four jumper pads labeled 3, 2, 1, and 0 to an adjacent "+" or "-" pad. Connecting to a + pad ties the HWID bit to Vcc; connecting to a - pad ties the HWID bit to GND.

HWIDs 1 to 15 are set by connecting jumper pads 3 through 0 to + or - pads as shown below.

HWID	3	2	1	0
1	-	-	-	+
2	-	-	+	-
3	-	-	+	+
4	-	+	-	-
5	-	+	-	+
6	-	+	+	-
7	-	+	+	+
8	+	-	-	-
9	+	-	-	+
10	+	-	+	-
11	+	-	+	+
12	+	+	-	-
13	+	+	-	+
14	+	+	+	-
15	+	+	+	+

B.1.2 RAM Wait States

The number of wait states inserted when Processor Module RAM is accessed is set by connecting the jumper pads W1 and W0 to an adjacent "+" or "-" pad. Connecting to a + pad ties the Wn pad to Vcc; connecting to a - pad ties the Wn pad to GND.

From 0 to 3 wait states are set by connecting jumper pads W1 and W0 to + or - pads as shown below.

Wait States	W1	W0
0	-	-
1	-	+
2	+	-
3	+	+

The default setting is for zero wait states.

B.1.3 Global Bus Interrupt Requests

Figure B-2 shows the Processor Module global interrupt request drivers, configuration jumper pads, and the global bus interrupt request lines.

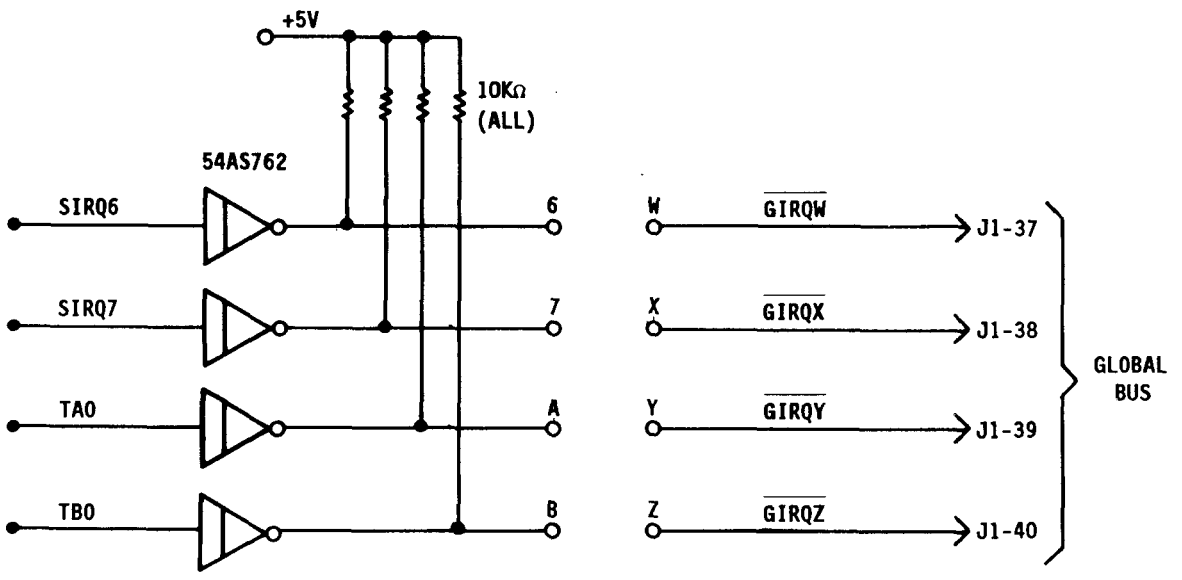


Figure B-2. Processor Module Global Interrupt Jumpers

The output of any one interrupt request driver can be connected to any one interrupt request line with a hardware jumper. Jumper settings are summarized in Table B-1.

TABLE B-1. PROCESSOR MODULE GLOBAL INTERRUPT JUMPERS

Interrupt Request	Global Request Line	Jumper
SIRQ6 (Software Interrupt 6)	$\overline{GIRQW}$	6 to W
	$\overline{GIRQX}$	6 to X
	$\overline{GIRQY}$	6 to Y
	$\overline{GIRQZ}$	6 to Z
SIRQ7 (Software Interrupt 7)	$\overline{GIRQW}$	7 to W
	$\overline{GIRQX}$	7 to X
	$\overline{GIRQY}$	7 to Y
	$\overline{GIRQZ}$	7 to Z
TAO (68901 Timer A Output)	$\overline{GIRQW}$	A to W
	$\overline{GIRQX}$	A to X
	$\overline{GIRQY}$	A to Y
	$\overline{GIRQZ}$	A to Z
TBO (68901 Timer B Output)	$\overline{GIRQW}$	B to W
	$\overline{GIRQX}$	B to X
	$\overline{GIRQY}$	B to Y
	$\overline{GIRQZ}$	B to Z

The default condition is as follows:

- SIRQ6 to $\overline{GIRQW}$ (6 to W)
- SIRQ7 to $\overline{GIRQX}$ (7 to X)
- TAO to $\overline{GIRQY}$ (A to Y)
- TBO to $\overline{GIRQZ}$ (B to Z)

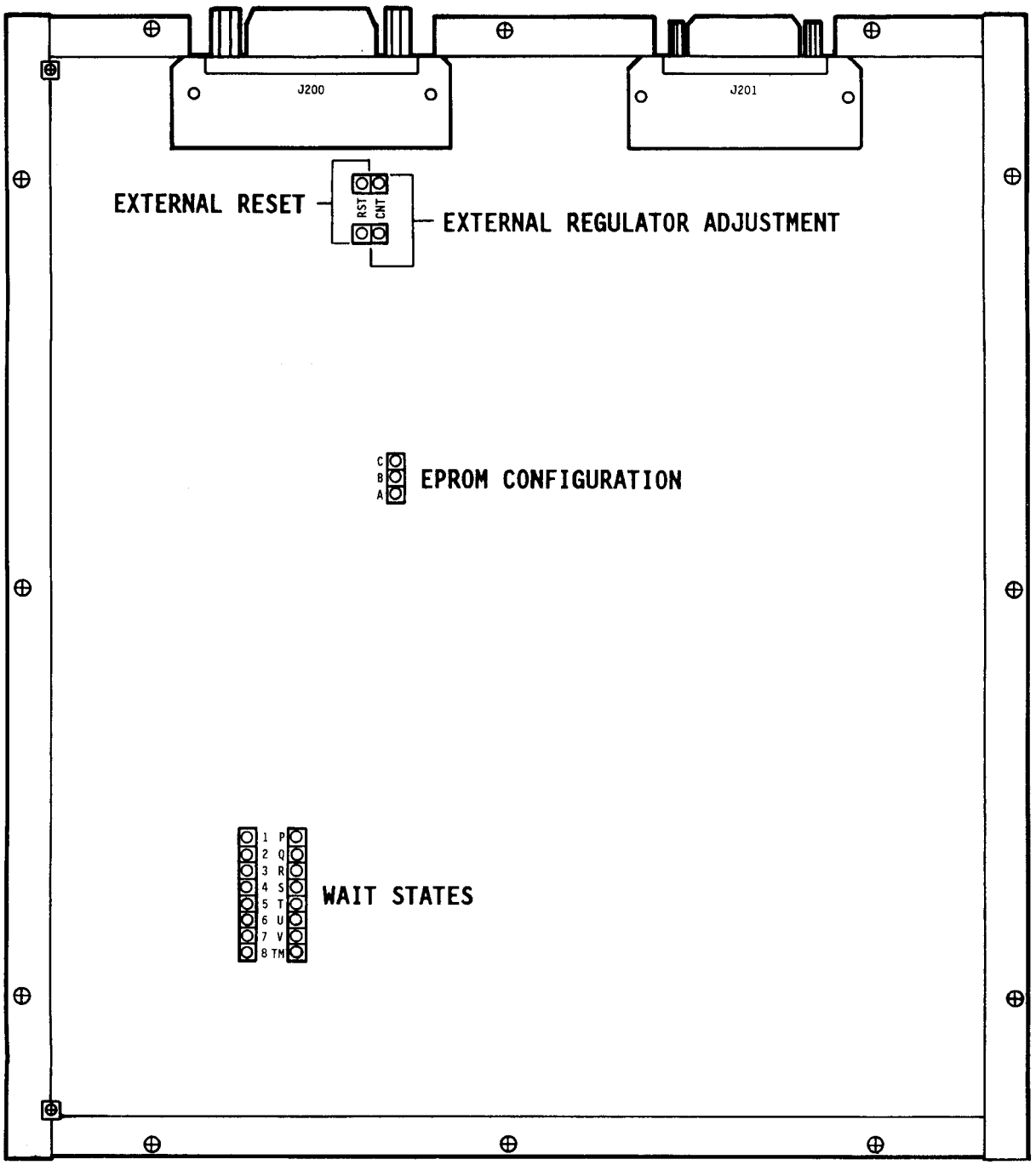


Figure B-3. Utility Module Jumper Locations

B.2 UTILITY MODULE

The Utility Module has four groups of hardware jumpers that function as follows:

- Enable/disable external regulator adjustment
- Enable/disable external hardware reset
- Select number of wait states
- Select addressing for EPROM configuration

The location of the jumper groups is shown in Figure B-3 (facing page). Jumper settings are described in the following subsections.

B.2.1 External Regulator Adjustment

The CNT jumper enables or disables external adjustment of the Utility Module voltage regulator as follows:

- External adjustment is ENABLED when the CNT jumper is INSTALLED.

- External adjustment is DISABLED when the CNT jumper is REMOVED.

The default setting is the CNT jumper removed (external adjustment disabled).

B.2.2 External Hardware Reset

The RST jumper enables or disables external hardware reset of the Utility Module as follows:

- External reset is ENABLED when the RST jumper is INSTALLED.

- External reset is DISABLED when the RST jumper is REMOVED.

The default setting is the RST jumper removed (external reset disabled).

B.2.3 Wait States

Figure B-4 illustrates the Utility Module wait state generator.

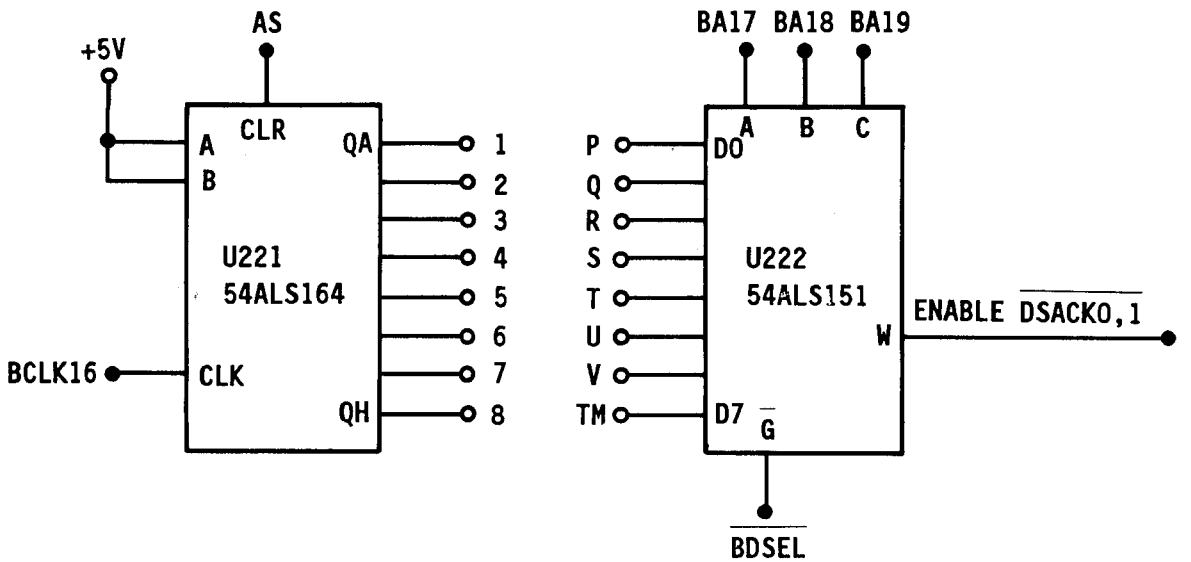


Figure B-4. Utility Module Wait State Jumpers

Each output of U221 provides a different number of wait states (1 to 8, as marked). The inputs of U222 correspond to Utility Module address space (and resources) as shown below.

U222 Input	Address Space	Resource
P	00,000,000 - 00,01F,FFF	EPROM
Q	00,020,000 - 00,03F,FFF	EPROM
R	00,040,000 - 00,05F,FFF	Not Used
S	00,060,000 - 00,07F,FFF	Not Used
T	00,080,000 - 00,09F,FFF	RAM
U	00,0A0,000 - 00,0BF,FFF	Not Used
V	00,0C0,000 - 00,0DF,FFF	Not Used
TM	00,0E0,000 - 00,0FF,FFF	Timer/Status Register

The number of wait states for a resource is configured by connecting a jumper from the jumper pad corresponding to the desired number of wait states (1 through 8) to the jumper pad corresponding to the resource (P through V, TM). The Utility Module's 32-bit timer and status register will always have the same number of wait states. The default settings are as follows:

- EPROM - 4 wait states (pad 4 to pad P and pad 4 to pad Q)
- RAM - 2 wait states (2 to T)
- Timer/Status Register - 2 wait states (2 to TM)

Complete wait state jumper information is summarized in Table B-2.

TABLE B-2. UTILITY MODULE WAIT STATE JUMPERS

Resource	# Wait States	Jumper
EPROM	1	1 to P, 1 to Q
.	2	2 to P, 2 to Q
.	3	3 to P, 3 to Q
.	4	4 to P, 4 to Q
.	5	5 to P, 5 to Q
.	6	6 to P, 6 to Q
.	7	7 to P, 7 to Q
EPROM	8	8 to P, 8 to Q
RAM	1	1 to T
.	2	2 to T
.	3	3 to T
.	4	4 to T
.	5	5 to T
.	6	6 to T
.	7	7 to T
RAM	8	8 to T
Timer/Status Register	1	1 to TM
.	2	2 to TM
.	3	3 to TM
.	4	4 to TM
.	5	5 to TM
.	6	6 to TM
.	7	7 to TM
Timer/Status Register	8	8 to TM

B.2.4 EPROM Addressing

The Utility Module has two sockets (U215 and U216) and a jumper pad (ABC) to accommodate the following EPROM configurations:

Total EPROM	Type	Size
64K Bytes	27256	32K × 8
128K Bytes	27512	64K × 8
256K Bytes	27010	128K × 8

Correct addressing per EPROM type is provided as follows:

Type	Jumper
27256	A to B
27512	B to C
27010	B to C

The default Utility Module configuration has two 27512 devices and a jumper from B to C.

NOTES

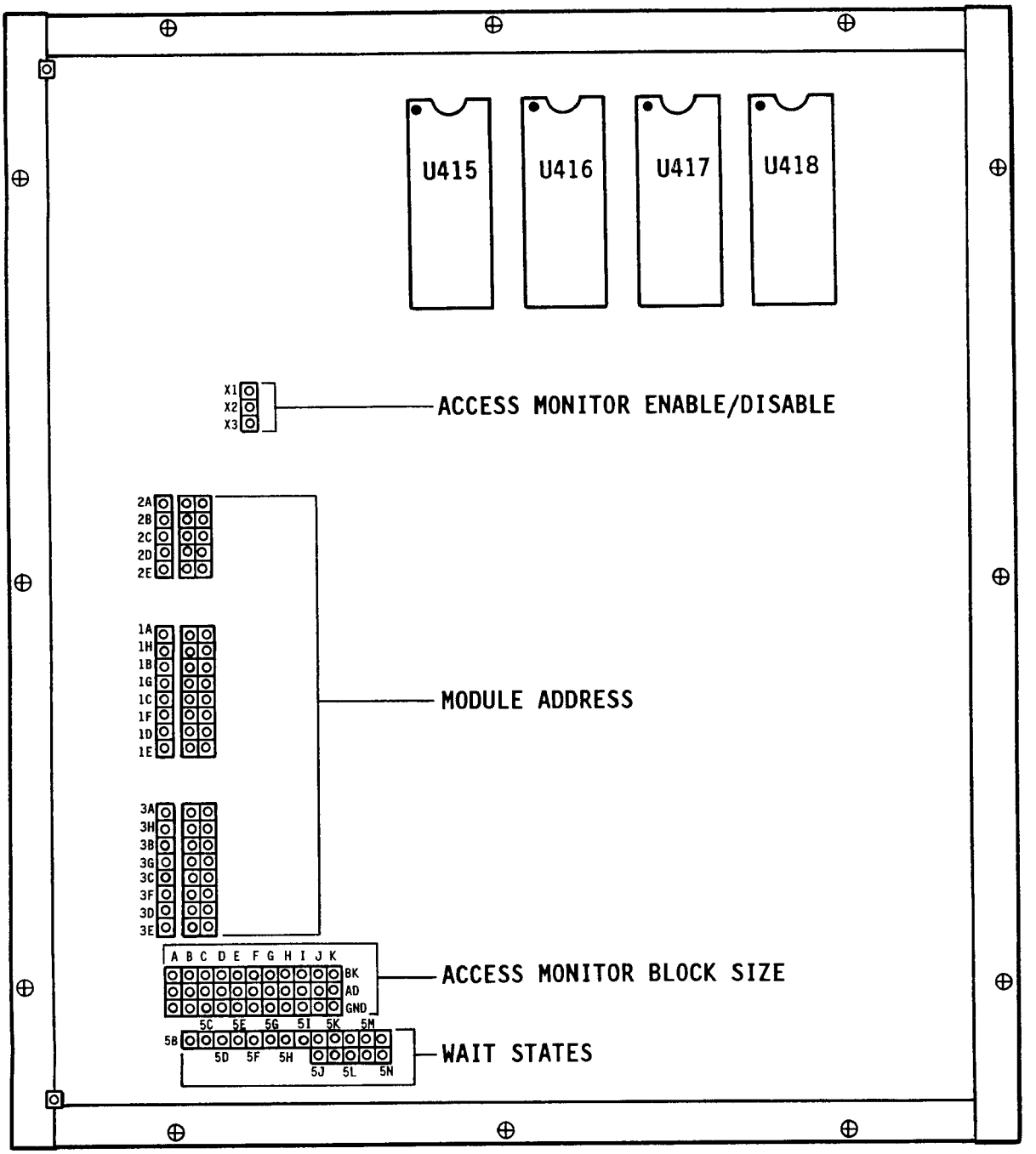


Figure B-5. Global Memory Module Jumper Locations

B.3 GLOBAL MEMORY MODULE

The Global Memory Module has four sets of hardware jumpers for the following:

- Module Address
- RAM Wait States
- Access Monitor Enable/Disable
- Access Monitor Block Size

The locations of the jumper groups are shown in Figure B-5 (facing page). Jumper settings are described in the following subsections.

B.3.1 Module Address

The block of addresses a Global Memory Module responds to is configured by connecting each of the jumper pads in the groups 1A-1H, 2A-2E, and 3A-3H to an adjacent "+" or "-" pad. Connecting to a + pad ties the point to Vcc; connecting to - ties the point to GND. Jumper settings for the 30 possible module starting addresses are shown in Table B-3. The default setting is for module starting address 00,100,000 hex.

B.3.2 RAM Wait States

Figure B-6 illustrates the Global Memory Module wait state generator.

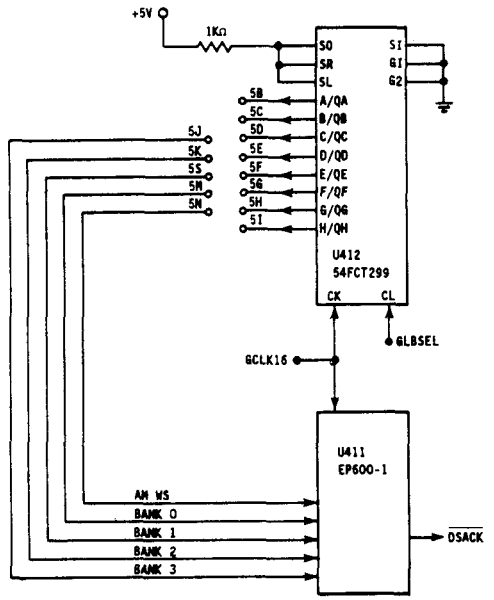


Figure B-6. Global Memory Module Wait State Jumpers

TABLE B-3. GLOBAL MEMORY MODULE ADDRESS JUMPERS

Module Start Address	1A	1B	1C	1D	1E	1F	1G	1H	2A	2B	2C	2D	2E	3A	3B	3C	3D	3E	3F	3G	3H
00,100,000	-	-	-	-	-	-	-	-	-	+	-	-	-	-	+	-	-	-	+	+	-
00,180,000	-	-	-	-	-	-	-	-	+	+	-	-	-	+	+	-	-	-	+	+	-
00,200,000	-	-	-	-	-	-	-	-	-	-	+	-	-	-	-	+	-	-	+	+	-
00,280,000	-	-	-	-	-	-	-	-	+	-	+	-	-	+	-	+	-	-	+	+	-
00,300,000	-	-	-	-	-	-	-	-	-	+	+	-	-	-	+	+	-	-	+	+	-
00,380,000	-	-	-	-	-	-	-	-	+	+	+	-	-	+	+	+	-	-	+	+	-
00,400,000	-	-	-	-	-	-	-	-	-	-	-	+	-	-	-	-	+	-	+	+	-
00,480,000	-	-	-	-	-	-	-	-	+	-	-	+	-	+	-	-	+	-	+	+	-
00,500,000	-	-	-	-	-	-	-	-	-	+	-	+	-	-	+	-	+	-	+	+	-
00,580,000	-	-	-	-	-	-	-	-	+	+	-	+	-	+	+	-	+	-	+	+	-
00,600,000	-	-	-	-	-	-	-	-	-	-	+	+	-	-	-	+	+	-	+	+	-
00,680,000	-	-	-	-	-	-	-	-	+	-	+	+	-	+	-	+	+	-	+	+	-
00,700,000	-	-	-	-	-	-	-	-	-	+	+	+	-	-	+	+	+	-	+	+	-
00,780,000	-	-	-	-	-	-	-	-	+	+	+	+	-	+	+	+	+	-	+	+	-
00,800,000	-	-	-	-	-	-	-	-	-	-	-	-	+	-	-	-	-	+	+	+	-
00,880,000	-	-	-	-	-	-	-	-	+	-	-	-	+	+	-	-	-	+	+	+	-
00,900,000	-	-	-	-	-	-	-	-	-	+	-	-	+	-	+	-	-	+	+	+	-
00,980,000	-	-	-	-	-	-	-	-	+	+	-	-	+	+	+	-	-	+	+	+	-
00,A00,000	-	-	-	-	-	-	-	-	-	-	+	-	+	-	-	+	-	+	+	+	-

TABLE B-3. CONTINUED

Module Start Address	1A	1B	1C	1D	1E	1F	1G	1H	2A	2B	2C	2D	2E	3A	3B	3C	3D	3E	3F	3G	3H
00,A80,000	-	-	-	-	-	-	-	-	+	-	+	-	+	+	-	+	-	+	+	+	-
00,B00,000	-	-	-	-	-	-	-	-	-	+	+	-	+	-	+	+	-	+	+	+	-
00,B80,000	-	-	-	-	-	-	-	-	+	+	+	-	+	+	+	+	-	+	+	+	-
00,C00,000	-	-	-	-	-	-	-	-	-	-	-	+	+	-		-	+	+	+	+	-
00,C80,000	-	-	-	-	-	-	-	-	+	-	-	+	+	+	-	-	+	+	+	+	-
00,D00,000	-	-	-	-	-	-	-	-	-	+	-	+	+	-	+	-	+	+	+	+	-
00,D80,000	-	-	-	-	-	-	-	-	+	+	-	+	+	+	+	-	+	+	+	+	-
00,E00,000	-	-	-	-	-	-	-	-	-	-	+	+	+	-	-	+	+	+	+	+	-
00,E80,000	-	-	-	-	-	-	-	-	+	-	+	+	+	+	-	+	+	+	+	+	-
00,F00,000	-	-	-	-	-	-	-	-	-	+	+	+	+	-	+	+	+	+	+	+	-
00,F80,000	-	-	-	-	-	-	-	-	+	+	+	+	+	+	+	+	+	+	+	+	-

Jumper pads 5B through 5I correspond to a number of wait states as shown below.

Pad	Wait States
5B	1
5C	2
5D	3
5E	4
5F	5
5G	6
5H	7
5I	8

Jumper pads 5J through 5N correspond to the four banks of 512K bytes of RAM and the access monitor RAM as shown below.

Pad	RAM
5J	Bank 3
5K	Bank 2
5L	Bank 1
5M	Bank 0
5N	Access Monitor

Wait states for a bank of RAM or the access monitor are configured by connecting a jumper from the pad giving the required number of wait states (5B-5I) to the pad corresponding to the bank or the access monitor (5J-5N). The default setting is for 1 wait state for all the RAM banks and 1 wait state for the access monitor.

All jumper settings are summarized in Table B-4.

TABLE B-4. GLOBAL MEMORY MODULE WAIT STATE JUMPERS

RAM Area	# Wait States	Jumper
Bank 3	1	5J to 5B
.	2	5J to 5C
.	3	5J to 5D
.	4	5J to 5E
.	5	5J to 5F
.	6	5J to 5G
.	7	5J to 5H
Bank 3	8	5J to 5I

TABLE B-4. CONTINUED

RAM Area	# Wait States	Jumper
Bank 2	1	5K to 5B
.	2	5K to 5C
.	3	5K to 5D
.	4	5K to 5E
.	5	5K to 5F
.	6	5K to 5G
.	7	5K to 5H
Bank 2	8	5K to 5I
Bank 1	1	5L to 5B
.	2	5L to 5C
.	3	5L to 5D
.	4	5L to 5E
.	5	5L to 5F
.	6	5L to 5G
.	7	5L to 5H
Bank 1	8	5L to 5I
Bank 0	1	5M to 5B
.	2	5M to 5C
.	3	5M to 5D
.	4	5M to 5E
.	5	5M to 5F
.	6	5M to 5G
.	7	5M to 5H
Bank 0	8	5M to 5I
Access Monitor	1	5N to 5B
.	2	5N to 5C
.	3	5N to 5D
.	4	5N to 5E
.	5	5N to 5F
.	6	5N to 5G
.	7	5N to 5H
Access Monitor	8	5N to 5I

B.3.3 Enable/Disable Access Monitor

The X jumpers enable and disable the access monitor as follows:

- The access monitor is ENABLED when a jumper is installed from X2 TO X3.
- The access monitor is DISABLED when a jumper is installed from X1 TO X3.

The default setting is the access monitor enabled (X2 to X3).

B.3.4 Access Monitor Block Size

Access monitor block size is configured by connecting the group of BK jumper pads (BK, A-K) to either a corresponding GND jumper pad (GND, A-K) or a corresponding AD jumper pad (AD, A-K). The connections required for specific block sizes are given in Table B-5. The default setting is for a block size of 128 bytes.

TABLE B-5. ACCESS MONITOR BLOCK SIZE JUMPERS

Block Size	BK-A	BK-B	BK-C	BK-D	BK-E	BK-F	BK-G	BK-H	BK-I	BK-J	BK-K
128 Bytes	AD-A	AD-B	AD-C	AD-D	AD-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
256 Bytes	GND-A	AD-B	AD-C	AD-D	AD-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
512 Bytes	GND-A	GND-B	AD-C	AD-D	AD-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
1K Bytes	GND-A	GND-B	GND-C	AD-D	AD-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
2K Bytes	GND-A	GND-B	GND-C	GND-D	AD-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
4K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	AD-F	AD-G	AD-H	AD-I	AD-J	AD-K
8K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	AD-G	AD-H	AD-I	AD-J	AD-K
16K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	GND-G	AD-H	AD-I	AD-J	AD-K
32K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	GND-G	GND-H	AD-I	AD-J	AD-K
64K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	GND-G	GND-H	GND-I	AD-J	AD-K
128K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	GND-G	GND-H	GND-I	GND-J	AD-K
256K Bytes	GND-A	GND-B	GND-C	GND-D	GND-E	GND-F	GND-G	GND-H	GND-I	GND-J	GND-K

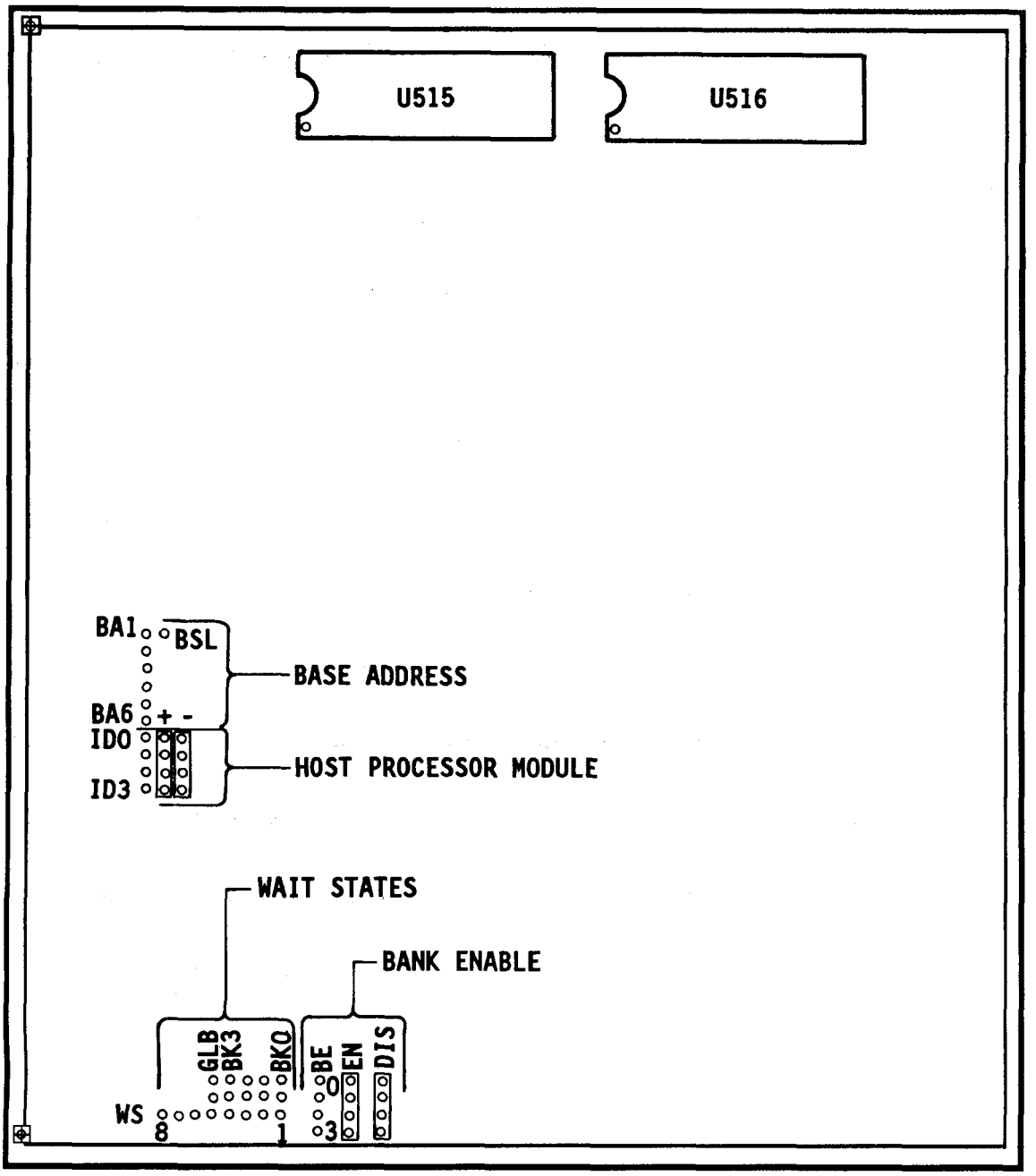


Figure B-7. Expansion Memory Module Jumper Locations

B.4 EXPANSION MEMORY MODULE

The Expansion Memory Module has four sets of hardware jumpers that configure the following:

- Host Processor Module ID
- Module Base Address
- Bank Enable/Disable
- Wait States

The locations of the jumper groups are shown in Figure B-7 (facing page). Jumper settings are described in the following subsections.

B.4.1 Host Processor Module ID

The ID of the host Processor Module (its HWID) is set by connecting the four jumper pads labeled ID3-ID0 to an adjacent "+" or "-" pad. HWIDs of 1 to 15, corresponding to the host Processor Module, are set by connecting jumper pads ID3-ID0 as shown below.

Host Module	ID3	ID2	ID1	ID0
1	-	-	-	+
2	-	-	+	-
3	-	-	+	+
4	-	+	-	-
5	-	+	-	+
6	-	+	+	-
7	-	+	+	+
8	+	-	-	-
9	+	-	-	+
10	+	-	+	-
11	+	-	+	+
12	+	+	-	-
13	+	+	-	+
14	+	+	+	-
15	+	+	+	+

B.4.2 Module Base Address

The base address an Expansion Memory Module responds to is configured by connecting the appropriate output of U504 (BA1-BA6) to the BSL jumper pad. The jumper connections for a particular base address are summarized below.

Base Address (hex)	Jumper
200,000	BA1 to BSL
400,000	BA2 to BSL
600,000	BA3 to BSL
800,000	BA4 to BSL
A00,000	BA5 to BSL
C00,000	BA6 to BSL

The default setting is for base address 200,000 hex (BA1 to BSL). This setting is hardwired on the circuit board.

B.4.3 Bank Enable/Disable

The four 512K byte banks (banks 3 through 0) of the 2 megabyte RAM area are enabled or disabled individually by connecting the BE inputs (BE3-BE0) of U513 to a corresponding EN (enable) jumper pad or a DIS (disable) jumper pad. Jumpering to enable or disable the banks is summarized below.

Bank	Enable	Disable
3	EN to BE3	DIS to BE3
2	EN to BE2	DIS to BE2
1	EN to BE1	DIS to BE1
0	EN to BE0	DIS to BE0

The default setting is all banks enabled. This setting is hardwired on the circuit board.

B.4.4 RAM Wait States

The Expansion Memory Module wait state generator is provided by the shift register U514 and the programmable array logic device U513. U514 outputs WS2 through WS8 and the WS1 line correspond to a number of wait states as shown below.

Output	Wait States
WS1	1
WS2	2
WS3	3
WS4	4
WS5	5
WS6	6
WS7	7
WS8	8

U513 inputs BK0 through BK3 correspond to the four 512K byte banks of the 2 megabyte RAM area.

Input	RAM
BK3	Bank 3
BK2	Bank 2
BK1	Bank 1
BK0	Bank 0

The GLB_WS corresponds to a global-to-local access of the module. Wait states for a bank of RAM or for a global-to-local access are configured by connecting a jumper from the pad giving the required number of wait states (WS1-WS8) to the pad corresponding to the bank or the global-to-local access (BK3-BK0, GLB_WS). The default setting is for 1 wait state for all the RAM banks and 2 wait states for a global-to-local access. This setting is hardwired on the circuit board. All jumper configurations are summarized in Table B-6.

TABLE B-6. EXPANSION MEMORY MODULE WAIT STATE JUMPERS

Bank or Access	# Wait States	Jumper
Bank 3	1	WS1 to BK3
.	2	WS2 to BK3
.	3	WS3 to BK3
.	4	WS4 to BK3
.	5	WS5 to BK3
.	6	WS6 to BK3
.	7	WS7 to BK3
Bank 3	8	WS8 to BK3
Bank 2	1	WS1 to BK2
.	2	WS2 to BK2
.	3	WS3 to BK2
.	4	WS4 to BK2
.	5	WS5 to BK2
.	6	WS6 to BK2
.	7	WS7 to BK2
Bank 2	8	WS8 to BK2
Bank 1	1	WS1 to BK1
.	2	WS2 to BK1
.	3	WS3 to BK1
.	4	WS4 to BK1
.	5	WS5 to BK1
.	6	WS6 to BK1
.	7	WS7 to BK1
Bank 1	8	WS8 to BK1
Bank 0	1	WS1 to BK0
.	2	WS2 to BK0
.	3	WS3 to BK0
.	4	WS4 to BK0
.	5	WS5 to BK0
.	6	WS6 to BK0
.	7	WS7 to BK0
Bank 0	8	WS8 to BK0
Global-to-Local		See next page

TABLE B-6. CONTINUED

Bank or Access	# Wait States	Jumper
Global-to-Local	1	WS1 to GLB_WS
.	2	WS2 to GLB_WS
.	3	WS3 to GLB_WS
.	4	WS4 to GLB_WS
.	5	WS5 to GLB_WS
.	6	WS6 to GLB_WS
.	7	WS7 to GLB_WS
Global-to-Local	8	WS8 to GLB_WS

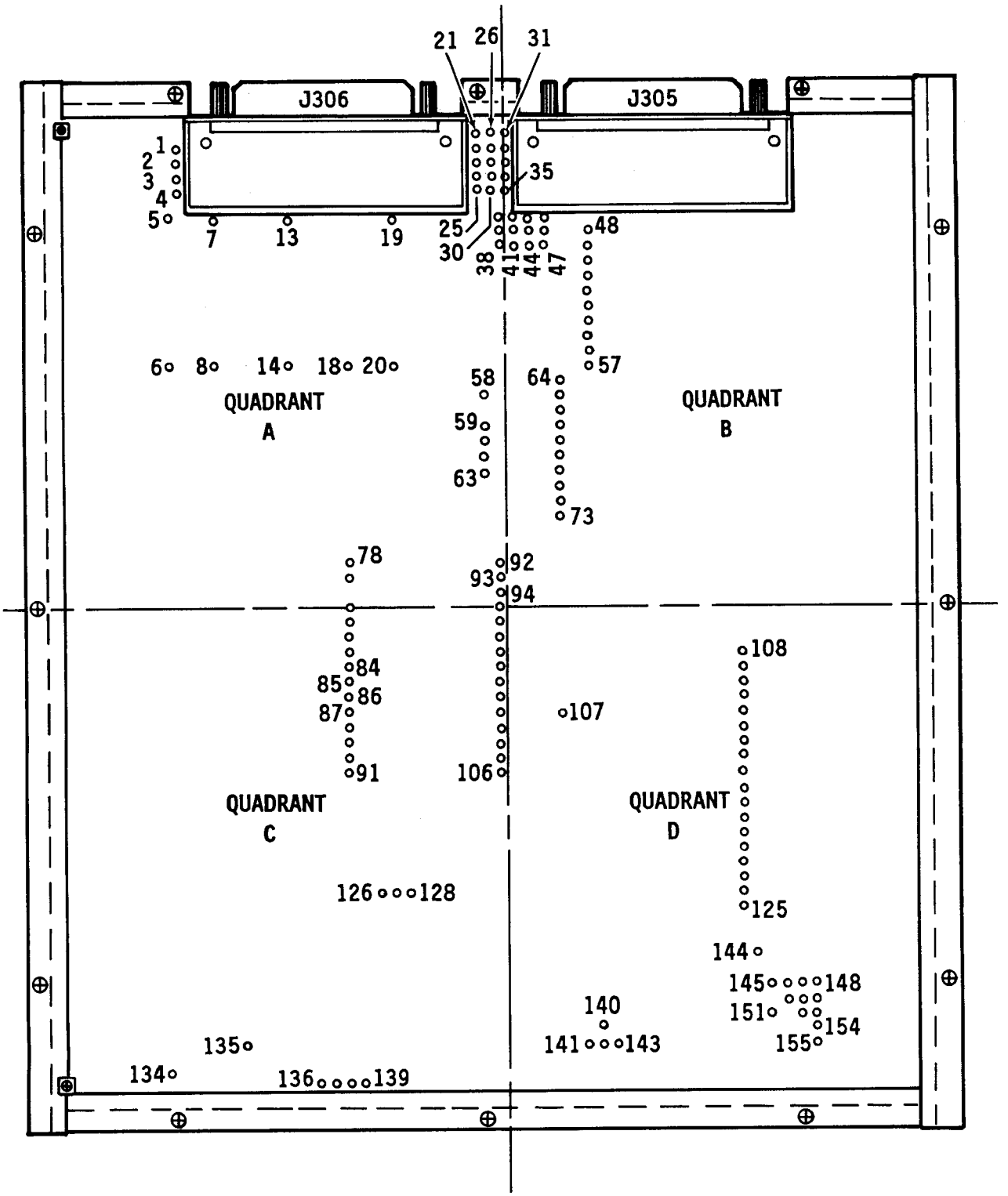


Figure B-8. System I/O Module Jumper Locations

B.5 SYSTEM I/O MODULE

The System I/O Module has numerous jumper pads for module configurations. Groups of jumper pads are associated with the following module circuits:

- General-Purpose Devices
- DMA Controller
- Parallel Port
- Serial/Discrete/Timer Ports
- Interrupt System
- Clocks/Power

The functions of the System I/O Module jumper pads within their respective circuits are given in the following subsections.

NOTE

Figure B-8 (preceding page) shows the location of jumper pads on the module. Table B-7 is designed to aid in finding the location of a particular jumper pad on the module (referenced to Figure B-8), the location on the Sandia National Laboratories schematic (CK-S64652), or the description of a pad's function in the following subsections.

TABLE B-7. SYSTEM I/O MODULE JUMPER PAD LOCATOR

Jumper Pad	On Module (Figure B-8 Quadrant)	On Schematic (CK-S64652 Sheet/Grid)	Description (Appendix B Page Number)
T1	A	2/H4	B-33, B-39
T2	A	2/H4	B-33, B-39
T3	A	2/H5	B-33, B-39
T4	A	2/H5	B-33, B-39
T5	A	2/G5	B-33, B-39
T6	A	2/H4	B-33, B-39
T7	A	2/G5	B-33, B-39
T8	A	2/H4	B-33, B-39
T9	A	2/G6	B-53
T10	A	2/G5	B-53

TABLE B-7. CONTINUED

Jumper Pad	On Module (Figure B-8 Quadrant)	On Schematic (CK-S64652 Sheet/Grid)	Description (Appendix B Page Number)
T11	A	2/G3	B-53
T12	A	2/G3	B-53
T13	A	2/G6	B-53
T14	A	2/G6	B-53
T15	A	2/C1	B-66
T16	A	2/B1	B-66
T17	A	2/B1	B-66
T18	A	2/G3	B-53
T19	A	2/D2	B-53
T20	A	2/G3	B-53
T21	A	2/D1	B-33, B-39
T22	A	2/D1	B-33, B-39
T23	A	2/D1	B-33, B-39
T24	A	2/D1	B-34, B-39
T25	A	2/D1	B-34, B-39
T26	B	2/D1	B-34, B-39
T27	B	2/D1	B-34, B-39
T28	B	2/D1	B-34, B-39
T29	B	2/D1	B-34, B-39
T30	B	2/D1	B-34, B-39
T31	B	2/D2	B-34, B-40
T32	B	2/D2	B-34, B-40
T33	B	2/D2	B-34, B-40
T34	B	2/D2	B-34, B-40
T35	B	2/D2	B-35, B-40
T36	B	2/D1	B-35, B-40
T37	B	2/C2	B-35, B-40
T38	B	2/C1	B-35, B-40
T39	B	2/D1	B-35, B-40
T40	B	2/C2	B-35, B-40
T41	B	2/C1	B-35, B-40
T42	B	2/D2	B-35, B-40
T43	B	2/C3	B-35, B-40
T44	B	2/C1	B-35, B-40
T45	B	2/C1	B-35, B-40
T46	B	2/C1	B-36, B-41
T47	B	2/C1	B-36, B-41

TABLE B-7. CONTINUED

Jumper Pad	On Module (Figure B-8 Quadrant)	On Schematic (CK-S64652 Sheet/Grid)	Description (Appendix B Page Number)
T48	B	2/B4	B-36, B-41
T49	B	2/B4	B-36, B-41
T50	B	2/B3	B-36, B-41
T51	B	2/B4	B-36, B-41
T52	B	2/B3	B-36, B-41
T53	B	2/B3	B-36, B-41
T54	B	2/B3	B-36, B-41
T55	B	2/B3	B-36, B-41
T56	B	2/B4	B-36, B-41
T57	B	2/B3	B-37, B-41
T58	A	2/E2	B-53
T59	A	2/G6	B-53
T60	A	2/G6	B-53
T61	A	2/G6	B-53
T62	A	2/G5	B-54
T63	A	2/G3	B-54
T64	B	2/C3	B-47, B-65
T65	B	2/C3	B-47
T66	B	2/G3	B-54
T67	B	2/G3	B-54
T68	B	2/C4	B-37, B-41
T69	B	2/C4	B-37, B-41
T70	B	2/C3	B-37, B-41
T71	B	2/C3	B-37, B-41
T72	B	2/C3	B-37, B-41
T73	B	2/G3	B-54
T74	D	1/D4	B-65
T75	D	1/D4	B-65
T76	D	1/C4	B-65
T77	D	1/C4	B-65
T78	A	2/G5	B-54
T79	A	2/G5	B-54
T80	D	2/G5	B-54
T81	D	2/G5	B-54
T82	D	2/G6	B-54
T83	D	2/G6	B-54
T84	D	2/G5	B-54

TABLE B-7. CONTINUED

Jumper Pad	On Module (Figure B-8 Quadrant)	On Schematic (CK-S64652 Sheet/Grid)	Description (Appendix B Page Number)
T85	D	2/G5	B-54
T86	D	2/G5	B-54
T87	D	2/G5	B-54
T88	D	2/F7	B-54
T89	D	2/F7	B-55
T90	D	2/F7	B-55
T91	D	2/F7	B-55
T92	B	2/G3	B-55
T93	B	2/G3	B-55
T94	B	2/G3	B-55
T95	C	2/E3	B-55, B-65
T96	C	2/G3	B-55
T97	C	2/G3	B-55
T98	C	2/G3	B-55
T99	C	2/G3	B-55
T100	C	2/G3	B-55
T101	C	2/G3	B-55
T102	C	2/G3	B-55
T103	C	2/F4	B-55
T104	C	2/F4	B-55
T105	C	2/F4	B-56
T106	C	2/F4	B-56
T107	C	2/D7	B-47, B-65
T108	C	2/E3	B-56
T109	C	2/D3	B-56
T110	C	2/D3	B-56
T111	C	2/D3	B-56
T112	C	2/D3	B-56
T113	C	2/D3	B-56
T114	C	2/D3	B-56
T115	C	2/D3	B-56
T116	C	2/D3	B-56
T117	C	2/D3	B-56
T118	C	2/D3	B-56
T119	C	2/E3	B-56
T120	C	2/E3	B-56
T121	C	2/D3	B-56

TABLE B-7. CONTINUED

Jumper Pad	On Module (Figure B-8 Quadrant)	On Schematic (CK-S64652 Sheet/Grid)	Description (Appendix B Page Number)
T122	C	2/D3	B-56
T123	C	2/D3	B-56
T124	C	2/D3	B-56
T125	C	2/D3	B-57
T126	D	1/F3	B-43
T127	D	1/F3	B-43, B-65
T128	D	1/F3	B-43
T129	D	1/F3	B-43
T130	D	1/F3	B-43
T131	D	1/F3	B-43, B-65
T132	D	1/H3	B-43
T133	D	1/H3	B-43
T134	D	2/E4	B-66
T135	D	2/E6	B-57, B-65
T136	D	1/G3	B-43
T137	D	1/G3	B-43
T138	D	1/G3	B-43
T139	D	1/G3	B-43
T140	C	2/A4	B-66
T141	C	2/A3	B-66
T142	C	2/A3	B-66
T143	C	2/A2	B-66
T144	C	1/B4	B-47, B-65
T145	C	1/B4	B-44
T146	C	1/B4	B-65
T147	C	1/C4	B-65
T148	C	1/C4	B-65
T149	C	1/C4	B-65
T150	C	1/C4	B-65
T151	C	1/B4	B-44
T152	C	1/C4	B-66
T153	C	1/C4	B-66
T154	C	1/B4	B-66
T155	C	1/B4	B-66

B.5.1 General-Purpose Devices

The System I/O Module contains several opto-couplers, buffers, and connector pins available for use in any of its circuits. These devices are accessed via jumper pads connected to their inputs and/or outputs. Figure B-9 illustrates the available general-purpose devices. Table B-8 describes the general-purpose device jumper pads.

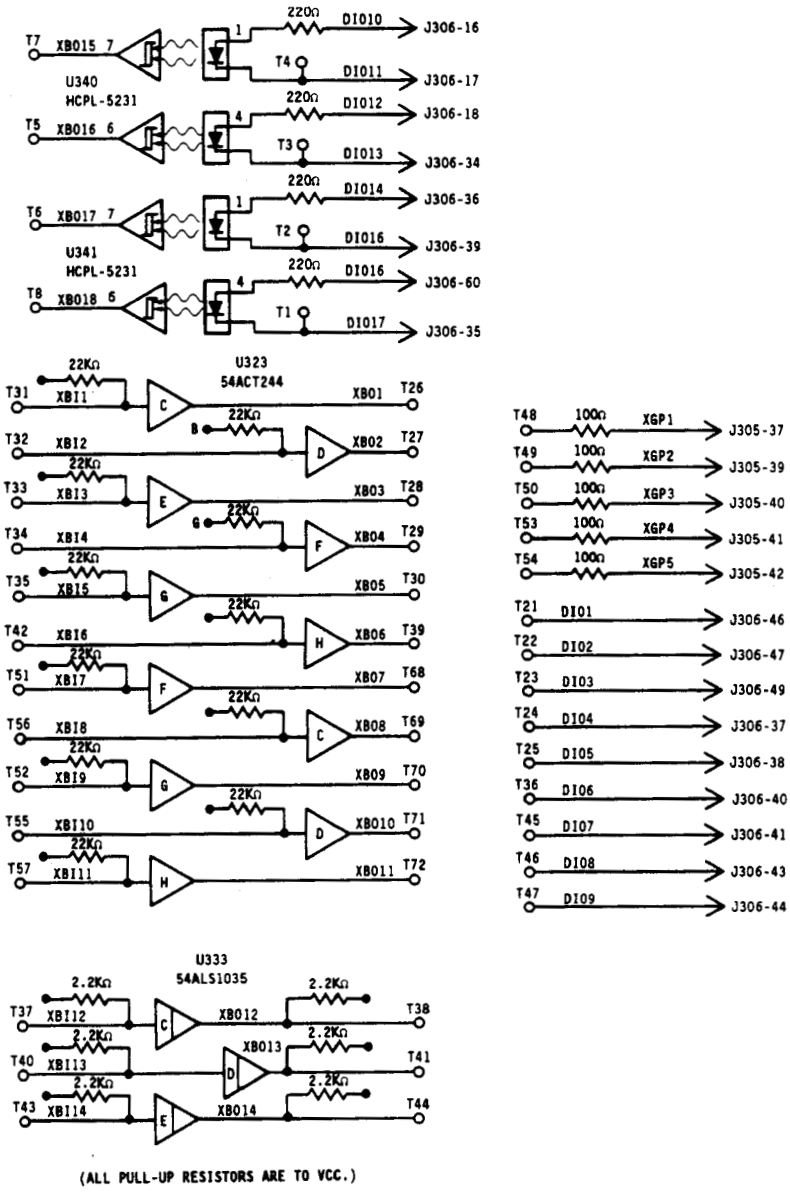


Figure B-9. System I/O General-Purpose Devices

TABLE B-8. SYSTEM I/O GENERAL-PURPOSE DEVICE JUMPERS

Jumper	Signal	Function
T1	DIO17	Discrete I/O Pin 17 - Connects jumper pad T1 to external connector pin J306-35.
T2	DIO15	Discrete I/O Pin 15 - Connects jumper pad T2 to external connector pin J306-39.
T3	DIO13	Discrete I/O Pin 13 - Connects jumper pad T3 to external connector pin J306-34.
T4	DIO11	Discrete I/O Pin 11 - Connects jumper pad T4 to external connector pin J306-17.
T5	XBO16	External Buffer Output 16 - Output from uncommitted HCPL-5231 opto-coupler (1/2 of U340, pin 6). Inputs are DIO12 (J306-18, +) and DIO13 (J306-34, -).
T6	XBO17	External Buffer Output 17 - Output from uncommitted HCPL-5231 opto-coupler (1/2 of U341, pin 7). Inputs are DIO14 (J306-36, +) and DIO15 (J306-39, -).
T7	XBO15	External Buffer Output 15 - Output from uncommitted HCPL-5231 opto-coupler (1/2 of U340, pin 7). Inputs are DIO10 (J306-16, +) and DIO11 (J306-17, -).
T8	XBO18	External Buffer Output 18 - Output from uncommitted HCPL-5231 opto-coupler (1/2 of U341, pin 6). Inputs are DIO16 (J306-50, +) and DIO17 (J306-35, -).
T21	DIO1	Discrete I/O Pin 1 - Connects jumper pad T21 to external connector pin J306-37.
T22	DIO2	Discrete I/O Pin 2 - Connects jumper pad T22 to external connector pin J306-38.
T23	DIO3	Discrete I/O Pin 3 - Connects jumper pad T23 to external connector pin J306-40.

TABLE B-8. CONTINUED

Jumper	Signal	Function
T24	DIO4	Discrete I/O Pin 4 - Connects jumper pad T24 to external connector pin J306-41.
T25	DIO5	Discrete I/O Pin 5 - Connects jumper pad T25 to external connector pin J306-43.
T26	XBO1	External Buffer Output 1 - Output from uncommitted 54ACT244 buffer (U325-C, pin 18). Buffer input is XBI1 (T31).
T27	XBO2	External Buffer Output 2 - Output from uncommitted 54ACT244 buffer (U325-D, pin 16). Buffer input is XBI2 (T32).
T28	XBO3	External Buffer Output 3 - Output from uncommitted 54ACT244 buffer (U325-E, pin 3). Buffer input is XBI3 (T33).
T29	XBO4	External Buffer Output 4 - Output from uncommitted 54ACT244 buffer (U325-F, pin 12). Buffer input is XBI4 (T34).
T30	XBO5	External Buffer Output 5 - Output from uncommitted 54ACT244 buffer (U325-G, pin 14). Buffer input is XBI5 (T35).
T31	XBI1	External Buffer Input 1 - Input to uncommitted 54ACT244 buffer (U325-C, pin 2). Buffer output is XBO1 (T26).
T32	XBI2	External Buffer Input 2 - Input to uncommitted 54ACT244 buffer (U325-D, pin 4). Buffer output is XBO2 (T27).
T33	XBI3	External Buffer Input 3 - Input to uncommitted 54ACT244 buffer (U325-E, pin 17). Buffer output is XBO3 (T28).
T34	XBI4	External Buffer Input 4 - Input to uncommitted 54ACT244 buffer (U325-F, pin 8). Buffer output is XBO4 (T29).

TABLE B-8. CONTINUED

Jumper	Signal	Function
T35	XBI5	External Buffer Input 1 - Input to uncommitted 54ACT244 buffer (U325-G, pin 6). Buffer output is XBO5 (T30).
T36	DIO6	Discrete I/O Pin 6 - Connects jumper pad T36 to external connector pin J306-44.
T37	XBI12	External Buffer Input 12 - Input to uncommitted 54ALS1035 open collector buffer (U333-C, pin 1). Buffer output is XBO12 (T38).
T38	XBO12	External Buffer Output 12 - Output from uncommitted 54ALS1035 open collector buffer (U333-C, pin 2). Buffer input is XBI12 (T37).
T39	XBO6	External Buffer Output 6 - Output from uncommitted 54ACT244 buffer (U325-H, pin 5). Buffer input is XBI6 (T42).
T40	XBI13	External Buffer Input 13 - Input to uncommitted 54ALS1035 open collector buffer (U333-D, pin 3). Buffer output is XBO13 (T41).
T41	XBO13	External Buffer Output 13 - Output from uncommitted 54ALS1035 open collector buffer (U333-D, pin 4). Buffer input is XBI13 (T40).
T42	XBI6	External Buffer Input 6 - Input to uncommitted 54ACT244 buffer (U325-H, pin 15). Buffer output is XBO6 (T39).
T43	XBI14	External Buffer Input 14 - Input to uncommitted 54ALS1035 open collector buffer (U333-E, pin 5). Buffer output is XBO14 (T44).
T44	XBO14	External Buffer Output 14 - Output from uncommitted 54ALS1035 open collector buffer (U333-E, pin 6). Buffer input is XBI14 (T43).
T45	DIO7	Discrete I/O Pin 7 - Connects jumper pad T45 to external connector pin J306-46.

TABLE B-8. CONTINUED

Jumper	Signal	Function
T46	DIO8	Discrete I/O Pin 8 - Connects jumper pad T46 to external connector pin J306-47.
T47	DIO9	Discrete I/O Pin 9 - Connects jumper pad T47 to external connector pin J306-49.
T48	XGP1	External General-Purpose Pin 1 - Connects jumper pad T48 to external connector pin J305-37 through a 100Ω series resistor.
T49	XGP2	External General-Purpose Pin 2 - Connects jumper pad T49 to external connector pin J305-39 through a 100Ω series resistor.
T50	XGP3	External General-Purpose Pin 3 - Connects jumper pad T50 to external connector pin J305-40 through a 100Ω series resistor.
T51	XBI7	External Buffer Input 7 - Input to uncommitted 54ACT244 buffer (U323-F, pin 2). Buffer output is XBO7 (T68).
T52	XBI9	External Buffer Input 9 - Input to uncommitted 54ACT244 buffer (U323-G, pin 6). Buffer output is XBO9 (T70).
T53	XGP4	External General-Purpose Pin 4 - Connects jumper pad T53 to external connector pin J305-41 through a 100Ω series resistor.
T54	XGP5	External General-Purpose Pin 5 - Connects jumper pad T54 to external connector pin J305-42 through a 100Ω series resistor.
T55	XBI10	External Buffer Input 10 - Input to uncommitted 54ACT244 buffer (U323-D, pin 8). Buffer output is XBO10 (T71).
T56	XBI8	External Buffer Input 8 - Input to uncommitted 54ACT244 buffer (U323-C, pin 4). Buffer output is XBO8 (T69).

TABLE B-8. CONTINUED

Jumper	Signal	Function
T57	XBI11	External Buffer Input 11 - Input to uncommitted 54ACT244 buffer (U323-H, pin 15). Buffer output is XBO11 (T72).
T68	XBO7	External Buffer Output 7 - Output from uncommitted 54ACT244 buffer (U323-F, pin 18). Buffer input is XBI7 (T51).
T69	XBO8	External Buffer Output 8 - Output from uncommitted 54ACT244 buffer (U323-C, pin 16). Buffer input is XBI8 (T56).
T70	XBO9	External Buffer Output 9 - Output from uncommitted 54ACT244 buffer (U323-G, pin 14). Buffer input is XBI9 (T52).
T71	XBO10	External Buffer Output 10 - Output from uncommitted 54ACT244 buffer (U323-D, pin 12). Buffer input is XBI10 (T55).
T72	XBO11	External Buffer Output 11 - Output from uncommitted 54ACT244 buffer (U323-H, pin 5). Buffer input is XBI11 (T57).

The default connections of the general-purpose devices are shown in Figure B-10. Table B-9 describes the default connections.

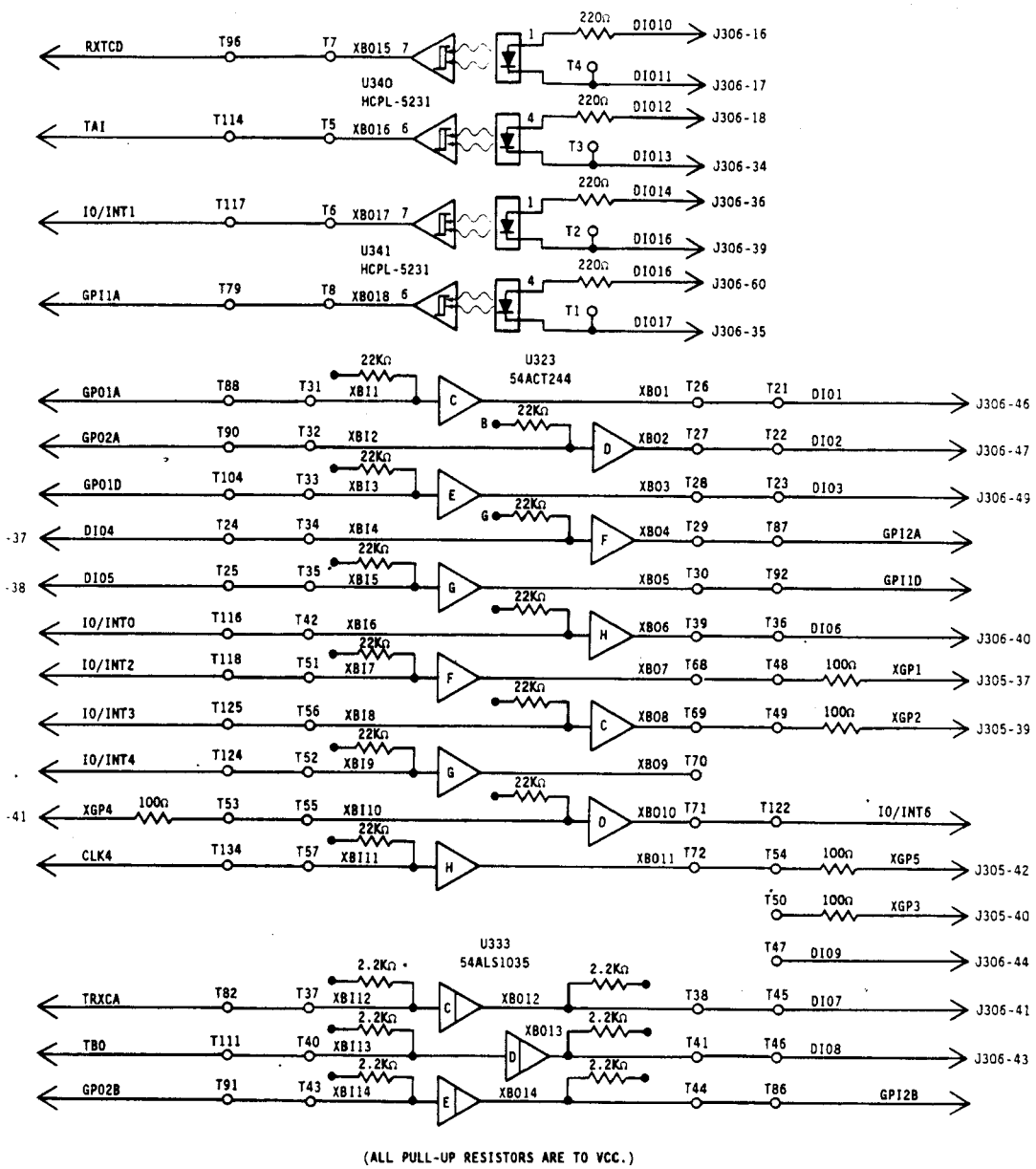


Figure B-10. System I/O General-Purpose Device Defaults

TABLE B-9. SYSTEM I/O GENERAL-PURPOSE DEVICE DEFAULTS

Jumper	Connection	Function
T1	Not connected	
T2	Not connected	
T3	Not connected	
T4	Not connected	
T5	T5 to T114	External buffer 16 output (XBO16) to MFP timer A input (TAI).
T6	T6 to T117	External buffer 17 output (XBO17) to MFP IO/INT1.
T7	T7 to T96	External buffer 15 output (XBO15) to DUSCC timer D input (RTXCD).
T8	T8 to T79	External buffer 18 output (XBO18) to serial port A general-purpose input 1 (GPI1A).
T21	T26 to T21	External buffer 1 output (XBO1) to J306-37 (DIO1).
T22	T27 to T22	External buffer 2 output (XBO2) to J306-38 (DIO2).
T23	T28 to T23	External buffer 3 output (XBO3) to J306-40 (DIO3).
T24	T24 to T34	J306-41 (DIO4) to external buffer 4 input (XBI4).
T25	T25 to T35	J306-43 (DIO5) to external buffer 5 input (XBI5).
T26	T26 to T21	External buffer 1 output (XBO1) to J306-37 (DIO1).
T27	T27 to T22	External buffer 2 output (XBO2) to J306-38 (DIO2).
T28	T28 to T23	External buffer 3 output (XBO3) to J306-40 (DIO3).
T29	T29 to T87	External buffer 4 output (XBO4) to serial port A general-purpose input 2 (GPI2A).
T30	T30 to T92	External buffer 5 output (XBO5) to serial port D general-purpose input 1 (GPI1D).

TABLE B-9. CONTINUED

Jumper	Connection	Function
T31	T88 to T31	Serial port A general-purpose output 1 (GPO1A) to external buffer 1 input (XBI1).
T32	T90 to T32	Serial port A general-purpose output 2 (GPO2A) to external buffer 2 input (XBI2).
T33	T104 to T33	Serial port D general-purpose output 1 (GPO1D) to external buffer 3 input (XBI3).
T34	T24 to T34	J306-41 (DIO4) to external buffer 4 input (XBI4).
T35	T25 to T35	J306-43 (DIO5) to external buffer 5 input (XBI5).
T36	T39 to T36	External buffer 6 output (XBO6) to J306-44 (DIO6).
T37	T82 to T37	DUSCC 1 (U302) timer A output (TRXCA) to external buffer 12 input (XBI12).
T38	T38 to T45	External buffer 12 output (XBO12) to J306-46 (DIO7).
T39	T39 to T36	External buffer 6 output (XBO6) to J306-44 (DIO6).
T40	T111 to T40	MFP timer B output (TBO) to external buffer 13 input (XBI13).
T41	T41 to T46	External buffer 13 output (XBO13) to J306-47 (DIO8).
T42	T116 to T42	MFP IO/INT0 output to J306-44 (XBI6).
T43	T91 to T43	Serial port B general-purpose output 2 (GPO2B) to external buffer 14 input (XBI14) for factory test.
T44	T44 to T86	External buffer 14 output (XBO14) to serial port B general-purpose input 2 (GPI2B) for factory test.
T45	T38 to T45	External buffer 12 output (XBO12) to J306-46 (DIO7).

TABLE B-9. CONTINUED

Jumper	Connection	Function
T46	T41 to T46	External buffer 13 output (XBO13) to J306-47 (DIO8).
T47	Not connected	
T48	T68 to T48	External buffer 7 output (XBO7) to J305-37 (XGP1).
T49	T69 to T49	External buffer 8 output (XBO7) to J305-39 (XGP2).
T50	Not connected	
T51	T118 to T51	MFP IO/INT2 output to external buffer 7 input (XBI7).
T52	T124 to T52	MFP IO/INT4 output to external buffer 9 input (XBI9).
T53	T53 to T55	J305-41 (XGP4) to external buffer 10 input (XBI10).
T54	T72 to T54	External buffer 11 output (XBO11) to J305-42 (XGP5).
T55	T53 to T55	J305-41 (XGP4) to external buffer 10 input (XBI10).
T56	T125 to T56	MFP IO/INT3 output to external buffer 8 input (XBI8).
T57	T134 to T57	4 MHz clock (CLK4) to external buffer 11 input (XBI11).
T68	T68 to T48	External buffer 7 output (XBO7) to J305-37 (XGP1).
T69	T69 to T49	External buffer 8 output (XBO7) to J305-39 (XGP2).
T70	Not connected	
T71	T71 to T122	External buffer 10 output (XBO10) to MFP IO/INT6.
T72	T72 to T54	External buffer 11 output (XBO11) to J305-42 (XGP5).

B.5.2 DMA Controller

Figure B-11 illustrates the hardware jumpers associated with the DMA Controller (DMAC). Table B-10 describes the jumpers.

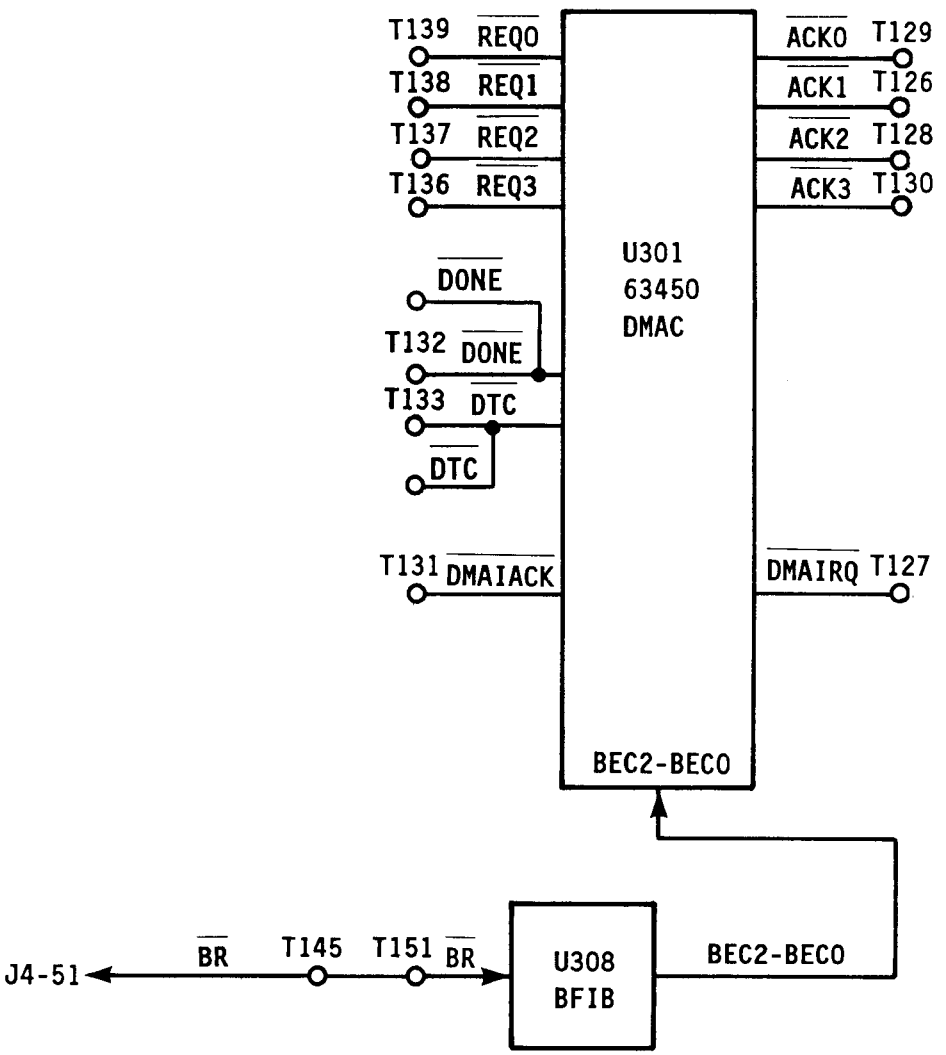


Figure B-11. System I/O DMAC Hardware Jumpers

TABLE B-10. SYSTEM I/O DMAC CONTROLLER JUMPERS

Jumper	Signal	Function
T126	$\overline{ACK1}$	DMAC Channel 1 Acknowledge - Acknowledge to device requesting DMA transfer via DMAC channel 1.
T127	$\overline{DMAIRQ}$	DMAC Interrupt Request - 63450 DMAC interrupt request output.
T128	$\overline{ACK2}$	DMAC Channel 2 Acknowledge - Acknowledge to device requesting DMA transfer via DMAC channel 2.
T129	$\overline{ACK0}$	DMAC Channel 0 Acknowledge - Acknowledge to device requesting DMA transfer via DMAC channel 0.
T130	$\overline{ACK3}$	DMAC Channel 3 Acknowledge - Acknowledge to device requesting DMA transfer via DMAC channel 3.
T131	$\overline{DMAIACK}$	DMAC Interrupt Acknowledge - 63450 DMAC interrupt acknowledge input.
T132	$\overline{DONE}$	Asserted by DMAC or peripheral device to indicate the last transfer in a block.
T133	$\overline{DTC}$	Data Transfer Complete - Asserted by DMAC to indicate successful data transfer.
T136	$\overline{REQ3}$	DMA Request, Channel 3 - Request for DMA transfer via 63450 DMAC channel 3.
T137	$\overline{REQ2}$	DMA Request, Channel 2 - Request for DMA transfer via 63450 DMAC channel 2.
T138	$\overline{REQ1}$	DMA Request, Channel 1 - Request for DMA transfer via 63450 DMAC channel 1.
T139	$\overline{REQ0}$	DMA Request, Channel 0 - Request for DMA transfer via 63450 DMAC channel 0.

TABLE B-10. CONTINUED

Jumper	Signal	Function
T145	$\overline{BR}$	Bus Request - Bus request signal from host Processor Module indicating another Processor Module is requesting the local bus (global-to-local request).
T151	U308-14	Bus request input to DMAC exception logic. When a jumper is installed from T145 to T151, a global-to-local bus request halts the DMAC if it is performing a DMA transfer.

The default jumper connections for the DMAC are shown in Figure B-12.

The default jumpers provide external request/acknowledge signals between the System I/O Module serial ports and the DMA Controller for operation in single address DMA mode as follows:

- DMAC Channel 0 - Port B Receiver and Transmitter (half duplex only)
- DMAC Channel 1 - Port D Transmitter
- DMAC Channel 2 - Port C Receiver and Transmitter (half duplex only)
- DMAC Channel 3 - Port C Transmitter

The default jumpers also connect the DMAC to local bus interrupt request Y ($\overline{EIRQY}$) and make the DMAC second in the interrupt acknowledge Y ($\overline{EIACKY}$) daisy chain, following the parallel port. A complete description of the System I/O Module interrupt system jumpers is given in B.5.5.

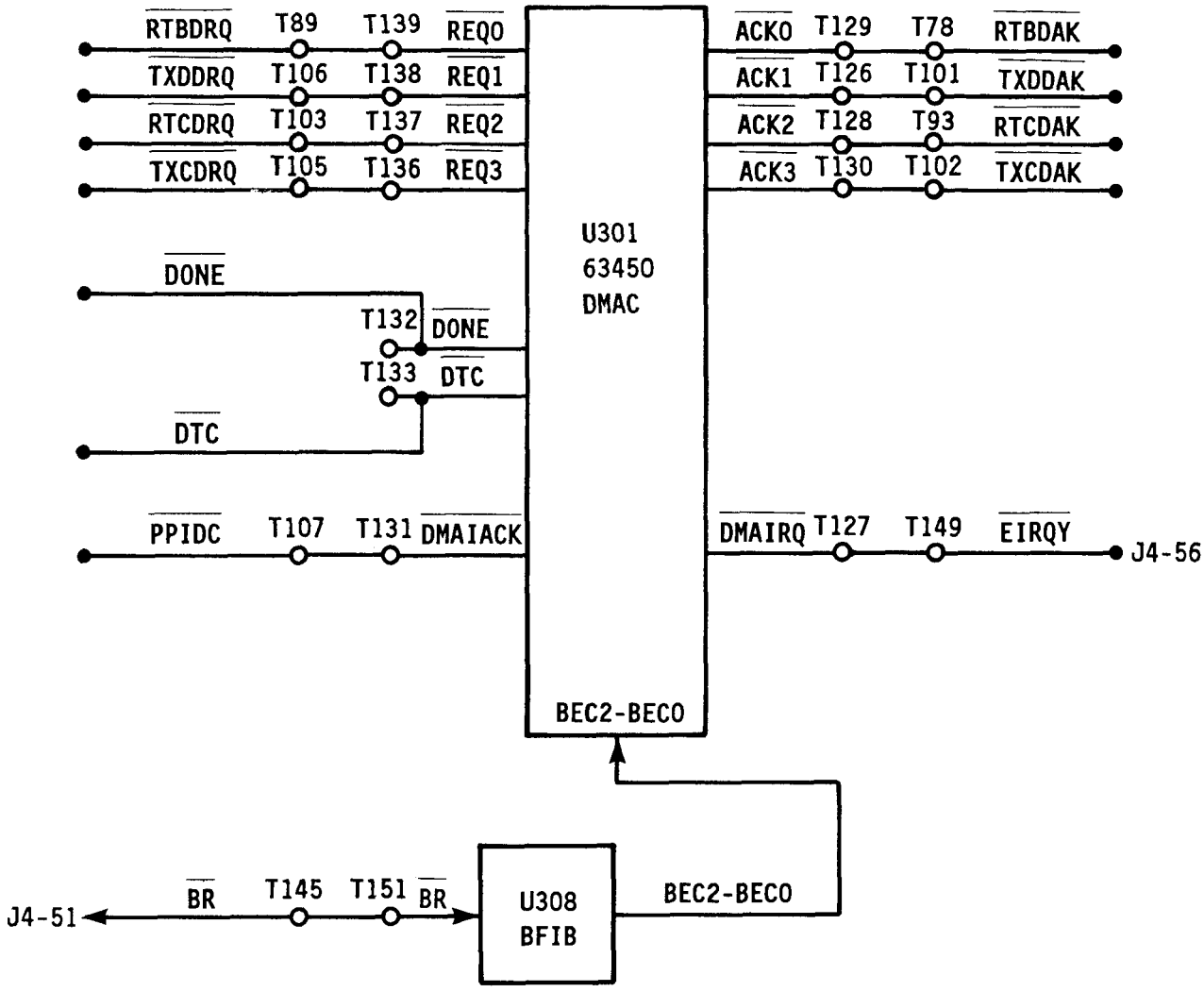


Figure B-12. System I/O DMAC Default Jumpers

B.5.3 Parallel Port

Figure B-13 illustrates the hardware jumpers associated with the parallel port. Table B-11 describes the jumpers.

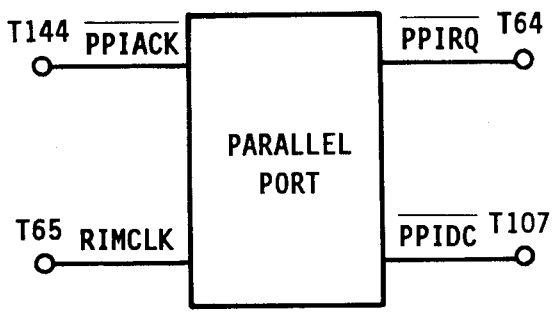


Figure B-13. System I/O Parallel Port Jumpers

NOTE

In configuring the parallel port, some of the general-purpose inputs from connector J305 and some general-purpose buffers may be required. These devices and the jumpers required to use them are listed in B.5.1.

TABLE B-11. SYSTEM I/O PARALLEL PORT JUMPERS

Jumper	Signal	Function
T64	$\overline{\text{PPIRQ}}$	Parallel Port Interrupt Request - Parallel port interrupt request output.
T65	RIMCLK	Remote Inertial Measurement Clock - Clock input from external device connected to parallel port.
T107	$\overline{\text{PPIDC}}$	Parallel Port Interrupt Daisy Chain - Interrupt acknowledge signal propagated by parallel port.
T144	$\overline{\text{PPIACK}}$	Parallel Port Interrupt Acknowledge - Parallel port interrupt acknowledge input.

The default jumper connections for the parallel port connect the port to local bus interrupt request Y ($\overline{\text{EIRQY}}$) and make the the port first in the interrupt acknowledge Y ($\overline{\text{EIACKY}}$) daisy chain. The port propagates the acknowledge to the DMAC. A complete description of the System I/O Module interrupt system jumpers is given in B.5.5.

B.5.4 Serial/Discrete/Timer Ports

Figures B-14 through B-18 show the serial/discrete/timer ports (A through E, respectively) and the associated hardware jumpers. Table B-12 describes the jumpers.

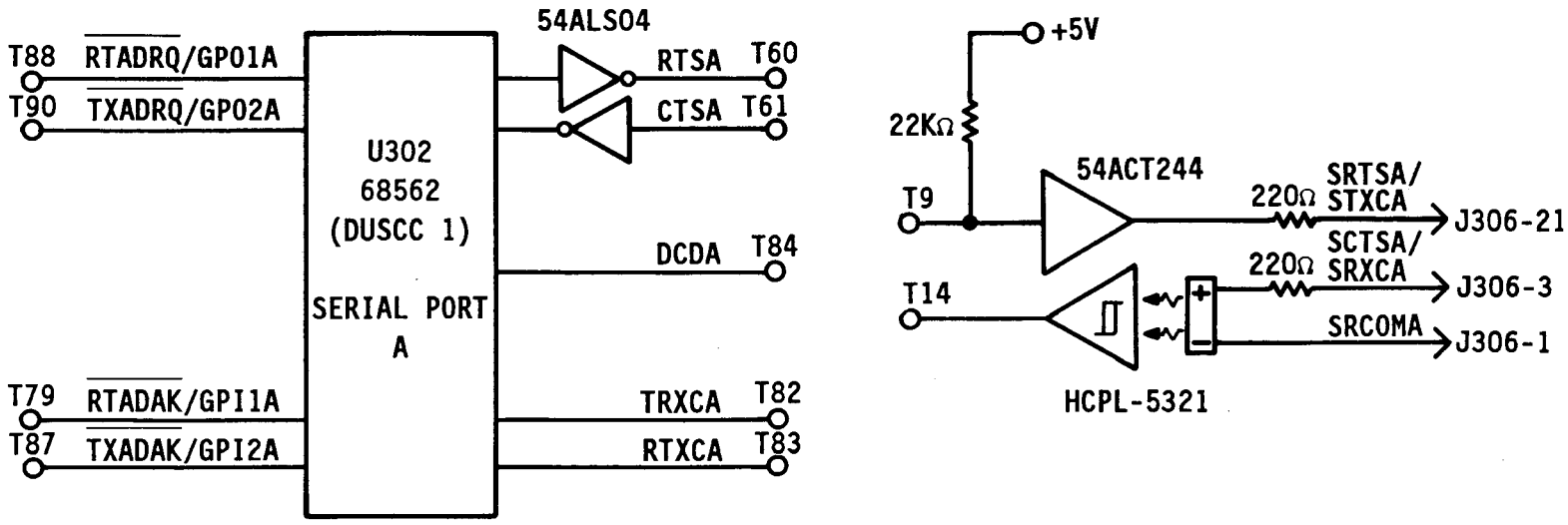


Figure B-14. System I/O Serial Port A Jumpers

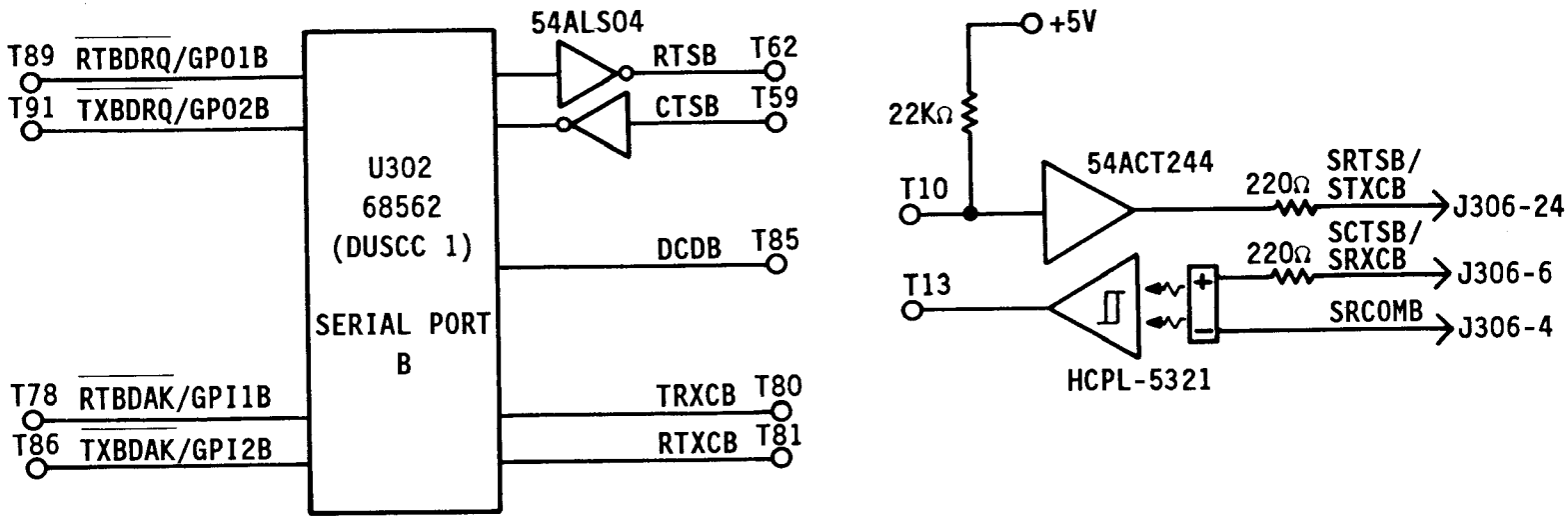


Figure B-15. System I/O Serial Port B Jumpers

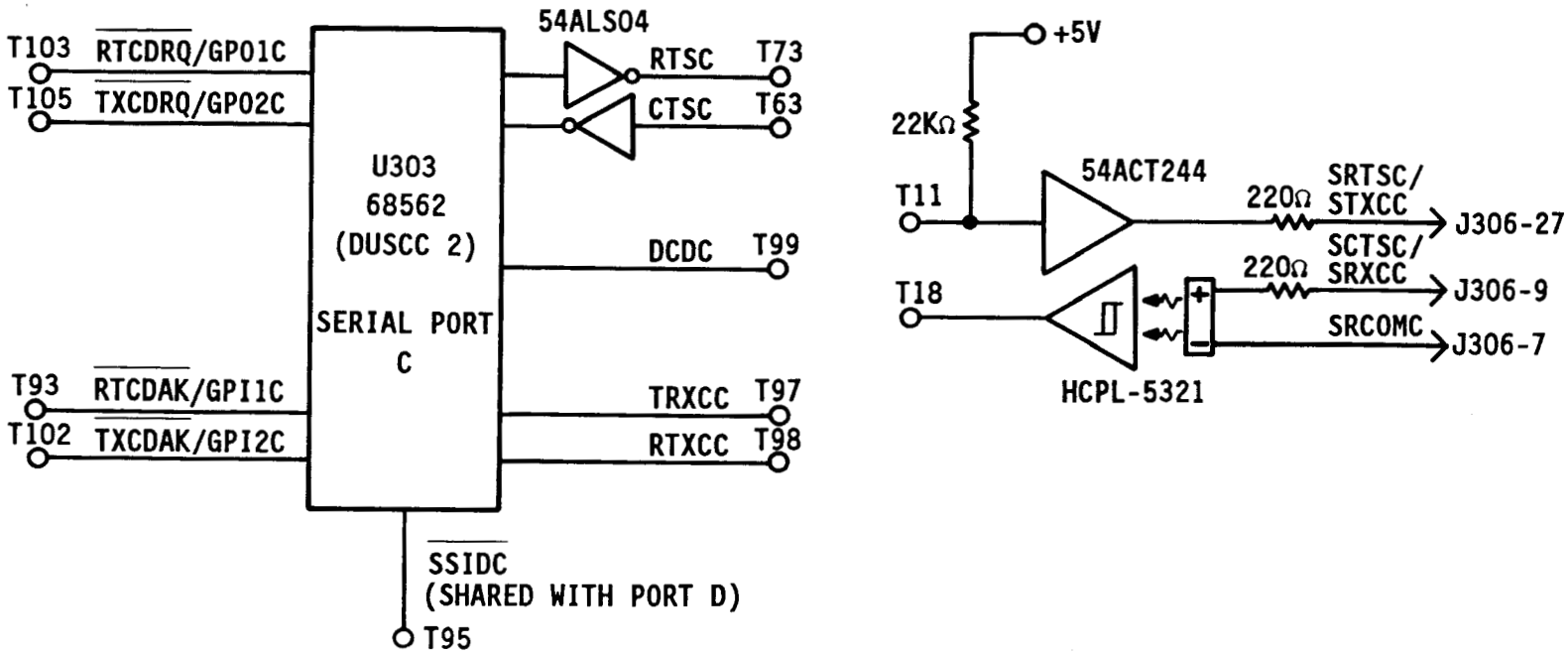


Figure B-16. System I/O Serial Port C Jumpers

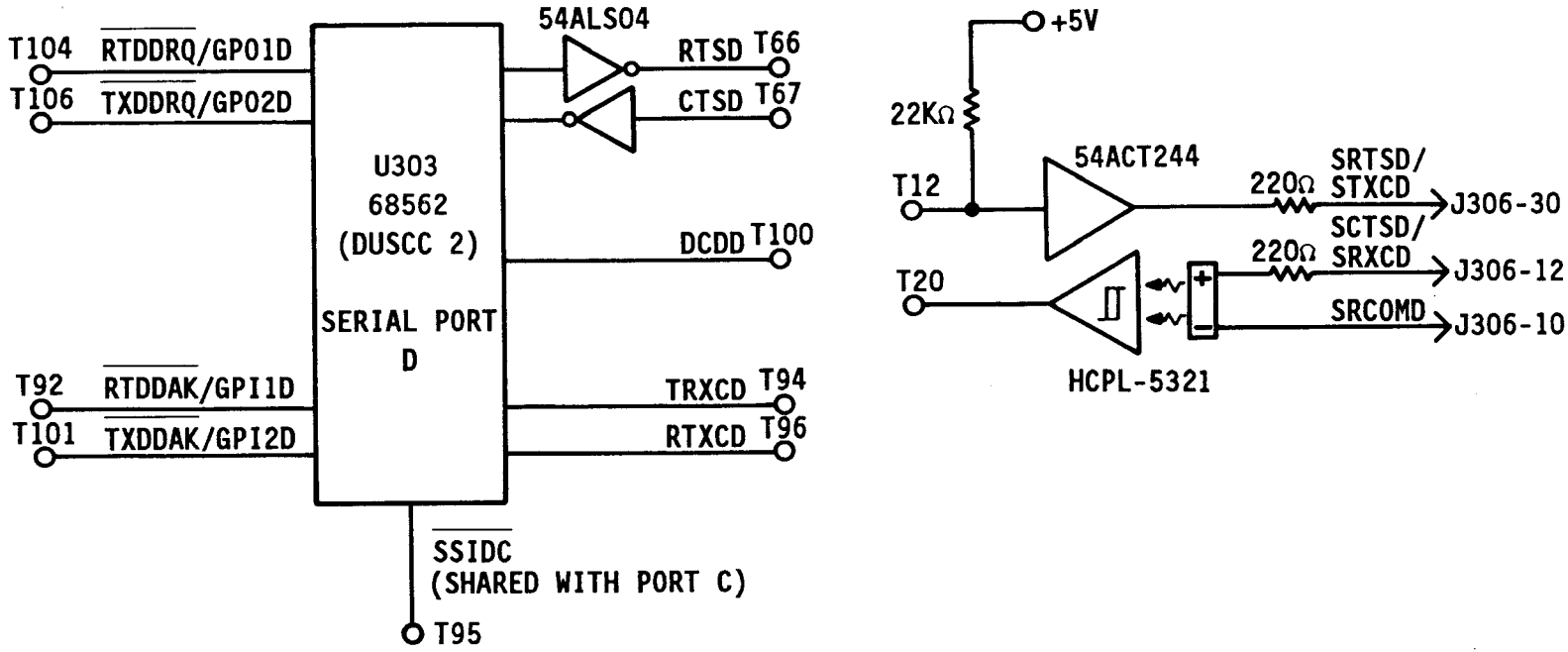


Figure B-17. System I/O Serial Port D Jumpers

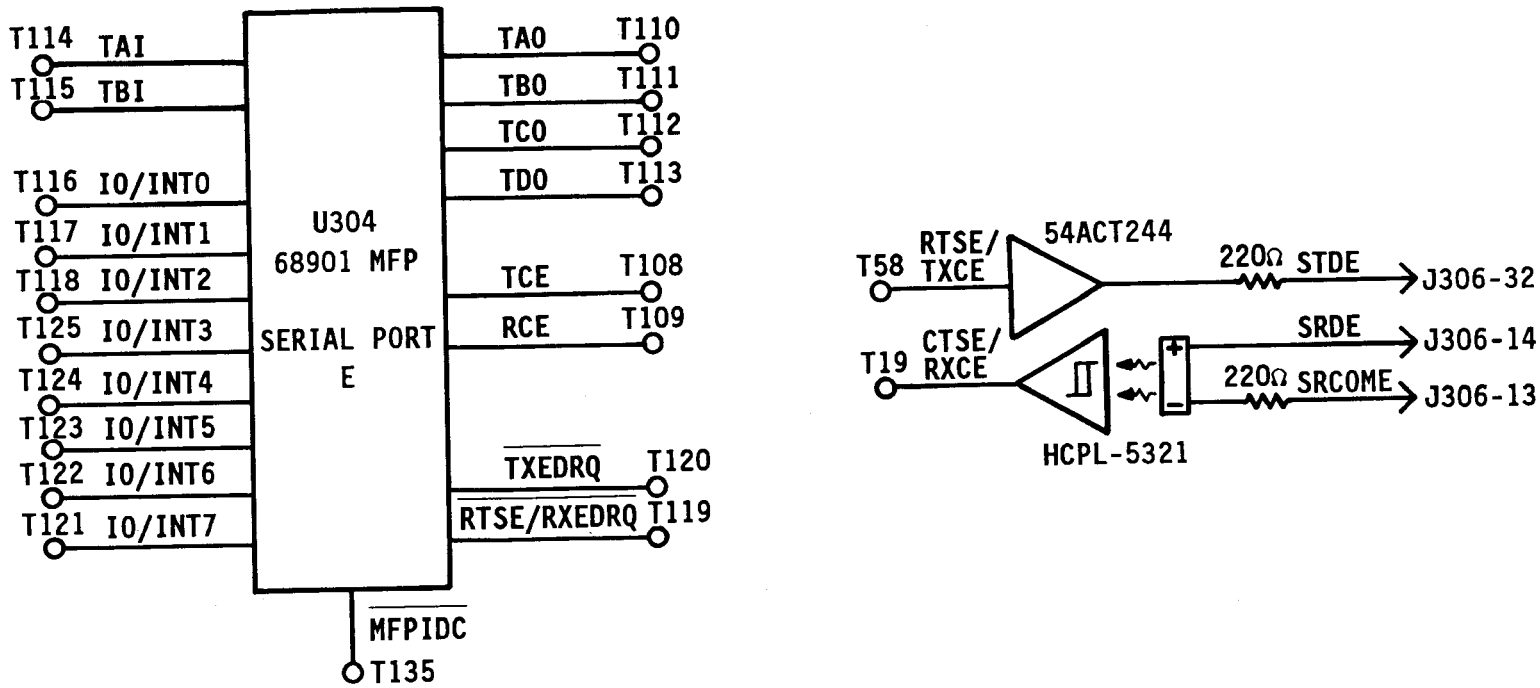


Figure B-18. System I/O Serial Port E Jumpers

TABLE B-12. SYSTEM I/O SERIAL/DISCRETE/TIMER JUMPERS

Jumper	Signal	Function
T9	U324-2	Input to buffer that supplies Request-to-Send or Transmit Clock to serial port A.
T10	U324-4	Input to buffer that supplies Request-to-Send or Transmit Clock to serial port B.
T11	U324-17	Input to buffer that supplies Request-to-Send or Transmit Clock to serial port C.
T12	U324-15	Input to buffer that supplies Request-to-Send or Transmit Clock to serial port D.
T13	U336-6	Output from opto-coupler that supplies Clear-to-Send or Receive Clock for serial port B.
T14	U335-6	Output from opto-coupler that supplies Clear-to-Send or Receive Clock for serial port B.
T18	U337-6	Output from opto-coupler that supplies Clear-to-Send or Receive Clock for serial port B.
T19	U339-6	Output from opto-coupler that supplies Clear-to-Send or Receive Clock for serial port E.
T20	U338-6	Output from opto-coupler that supplies Clear-to-Send or Receive Clock for serial port B.
T58	U325-11	Input to buffer that supplies Request-to-Send or Transmit Clock to serial port E.
T59	U332-1	Input to inverter that supplies Clear-to-Send to serial port B.
T60	U331-13	Output from inverter that drives Request-to-Send from serial port A.
T61	U331-3	Input to inverter that supplies Clear-to-Send to serial port A.

TABLE B-12. CONTINUED

Jumper	Signal	Function
T62	U332-3	Output from inverter that drives Request-to-Send from serial port B.
T63	U332-5	Input to inverter that supplies Clear-to-Send to serial port C.
T66	U332-13	Output from inverter that drives Request-to-Send from serial port D.
T67	U332-11	Input to inverter that supplies Clear-to-Send to serial port D.
T73	U332-9	Output from inverter that drives Request-to-Send from serial port C.
T78	GPI1B/$\overline{\text{RTBDAK}}$	Serial port B General-Purpose Input 1 or Receiver/Transmitter (B) DMA Acknowledge.
T79	GPI1A/$\overline{\text{RTADAK}}$	Serial port A General-Purpose Input 1 or Receiver/Transmitter (A) DMA Acknowledge.
T80	TRXCB	Serial port B Transmitter/Receiver Clock.
T81	RTXCB	Serial port B Receiver/Transmitter Clock.
T82	TRXCA	Serial port A Transmitter/Receiver Clock.
T83	RTXCA	Serial port A Receiver/Transmitter Clock.
T84	DCDA	Serial port A Data Carrier Detect.
T85	DCDB	Serial port B Data Carrier Detect.
T86	GPI2A/$\overline{\text{TXADAK}}$	Serial port A General-Purpose Input 2 or Transmitter (A) DMA Acknowledge.
T87	GPI2B/$\overline{\text{TXBDAK}}$	Serial port B General-Purpose Input 2 or Transmitter (B) DMA Acknowledge.
T88	$\overline{\text{RTADRQ}}$/GPO1A	Serial Port A Receiver/Transmitter DMA Request or General-Purpose Output 1.

TABLE B-12. CONTINUED

Jumper	Signal	Function
T89	$\overline{\text{RTBDRQ}}$/GPO1B	Serial Port B Receiver/Transmitter DMA Request or General-Purpose Output 1.
T90	$\overline{\text{TXADRQ}}$/GPO2A	Serial Port A Transmitter DMA Request or General-Purpose Output 2.
T91	$\overline{\text{TXBDRQ}}$/GPO2B	Serial Port B Transmitter DMA Request or General-Purpose Output 2.
T92	GPI1D/$\overline{\text{RTDDAK}}$	Serial Port D General-Purpose Input 1 or Receiver/Transmitter (D) DMA Acknowledge.
T93	GPI1C/$\overline{\text{RTCDAK}}$	Serial Port C General-Purpose Input 1 or Receiver/Transmitter (C) DMA Acknowledge.
T94	TRXCD	Serial Port D Transmitter/Receiver Clock.
T95	$\overline{\text{SSIDC}}$	Interrupt acknowledge daisy chain output from DUSCC 2 (serial ports C and D).
T96	RTXCD	Serial Port D Receiver/Transmitter Clock.
T97	TRXCC	Serial Port C Transmitter/Receiver Clock.
T98	RTXCC	Serial Port C Receiver/Transmitter Clock.
T99	DCDC	Serial Port C Data Carrier Detect.
T100	DCDD	Serial Port D Data Carrier Detect.
T101	GPI2C/$\overline{\text{TXCDAK}}$	Serial Port C General-Purpose Input 2 or Transmitter (C) DMA Acknowledge.
T102	GPI2D/$\overline{\text{TXDDAK}}$	Serial Port D General-Purpose Input 2 or Transmitter (D) DMA Acknowledge.
T103	$\overline{\text{RTCDRQ}}$/GPO1C	Serial Port C Receiver/Transmitter DMA Request or General-Purpose Output 1.
T104	$\overline{\text{RTDDRQ}}$/GPO1D	Serial Port D Receiver/Transmitter DMA Request or General-Purpose Output 1.

TABLE B-12. CONTINUED

Jumper	Signal	Function
T105	$\overline{\text{TXCDRQ}}$/GPO2C	Serial Port C Transmitter DMA Request or General-Purpose Output 2.
T106	$\overline{\text{TXDDRQ}}$/GPO2D	Serial Port D Transmitter DMA Request or General-Purpose Output 2.
T108	TCE	Serial Port E Transmitter Clock.
T109	RCE	Serial Port E Receive Clock.
T110	TAO	68901 MFP Timer A Output.
T111	TBO	68901 MFP Timer B Output.
T112	TCO	68901 MFP Timer C Output.
T113	TDO	68901 MFP Timer D Output.
T114	TAI	68901 MFP Timer A External Input.
T115	TBI	68901 MFP Timer B External Input.
T116	IO/INT0	68901 MFP General-Purpose I/O/Interrupt 0.
T117	IO/INT1	68901 MFP General-Purpose I/O/Interrupt 1.
T118	IO/INT2	68901 MFP General-Purpose I/O/Interrupt 2.
T119	RTSE/$\overline{\text{RXEDRQ}}$	Serial Port E Request-to-Send or DMA Request.
T120	$\overline{\text{TXEDRQ}}$	Serial Port E Transmitter DMA Request.
T121	IO/INT7	68901 MFP General-Purpose I/O/Interrupt 7.
T122	IO/INT6	68901 MFP General-Purpose I/O/Interrupt 6.
T123	IO/INT5	68901 MFP General-Purpose I/O/Interrupt 5.
T124	IO/INT4	68901 MFP General-Purpose I/O/Interrupt 4.

TABLE B-12. CONTINUED

Jumper	Signal	Function
T125	IO/INT3	68901 MFP General-Purpose I/O/Interrupt 3.
T135	$\overline{\text{MFPIDC}}$	Interrupt acknowledge daisy chain output from 68901 MFP (serial port E).

The default connections for the serial/discrete/timer jumpers are shown in Figures B-19 through B-23. The connections are described in the subsections that follow.

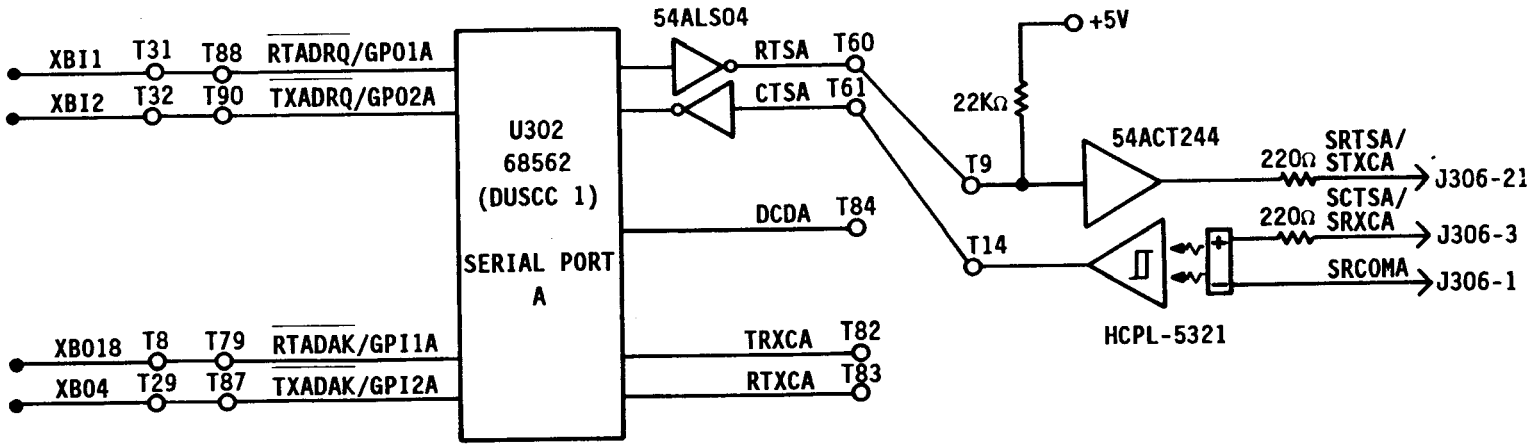


Figure B-19. System I/O Serial Port A Default Jumpers

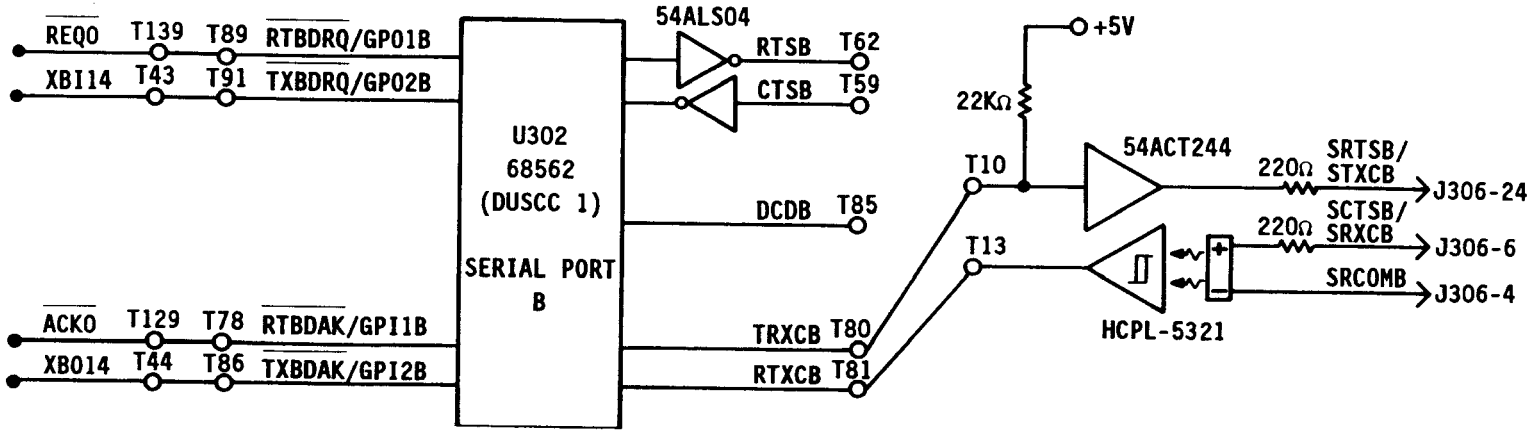


Figure B-20. System I/O Serial Port B Default Jumpers

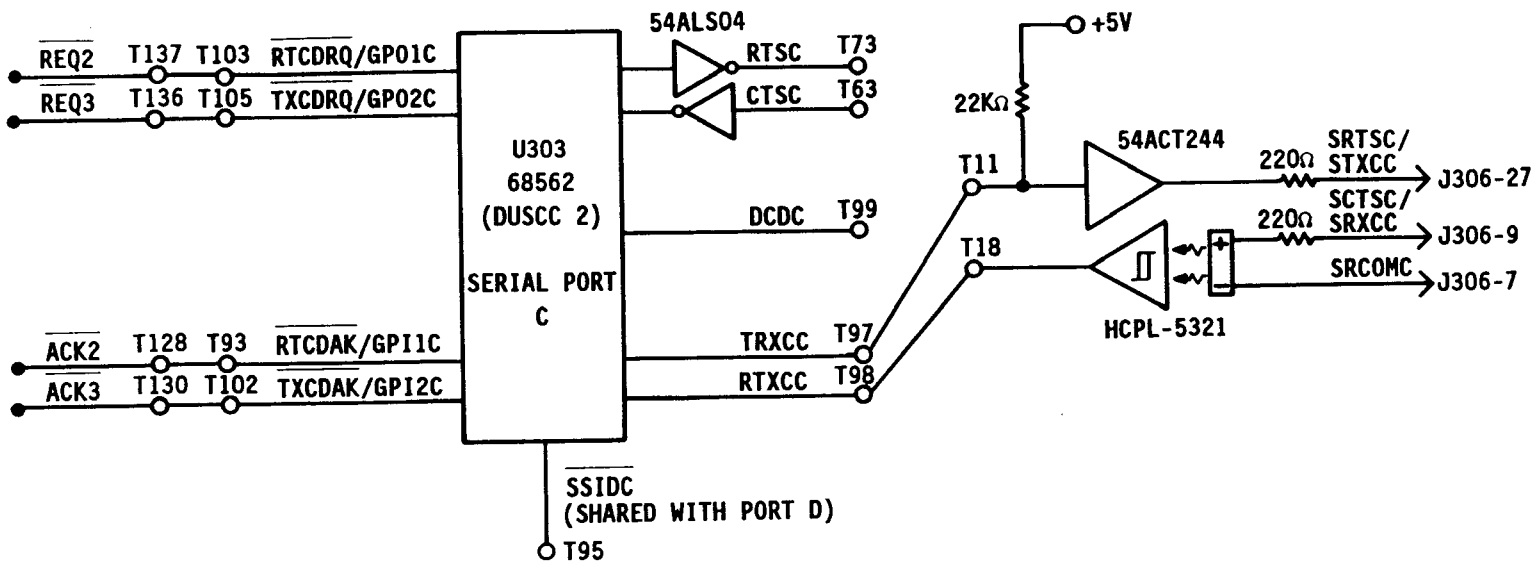


Figure B-21. System I/O Serial Port C Default Jumpers

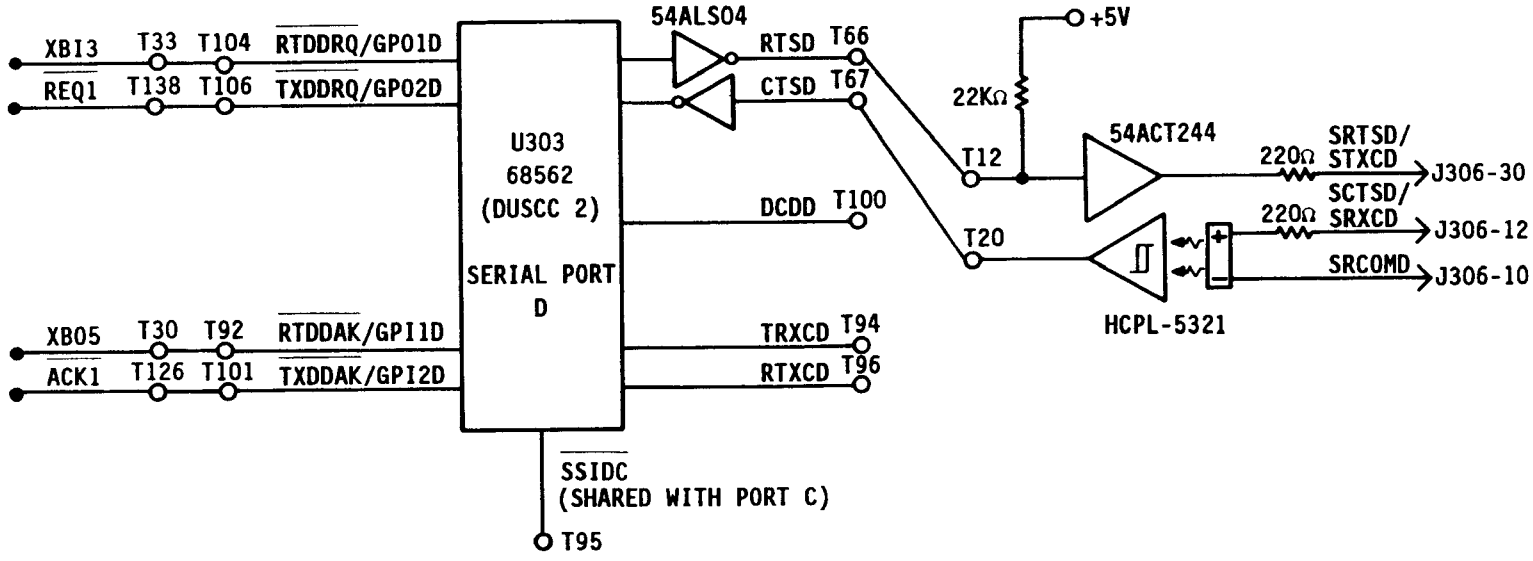


Figure B-22. System I/O Serial Port D Default Jumpers

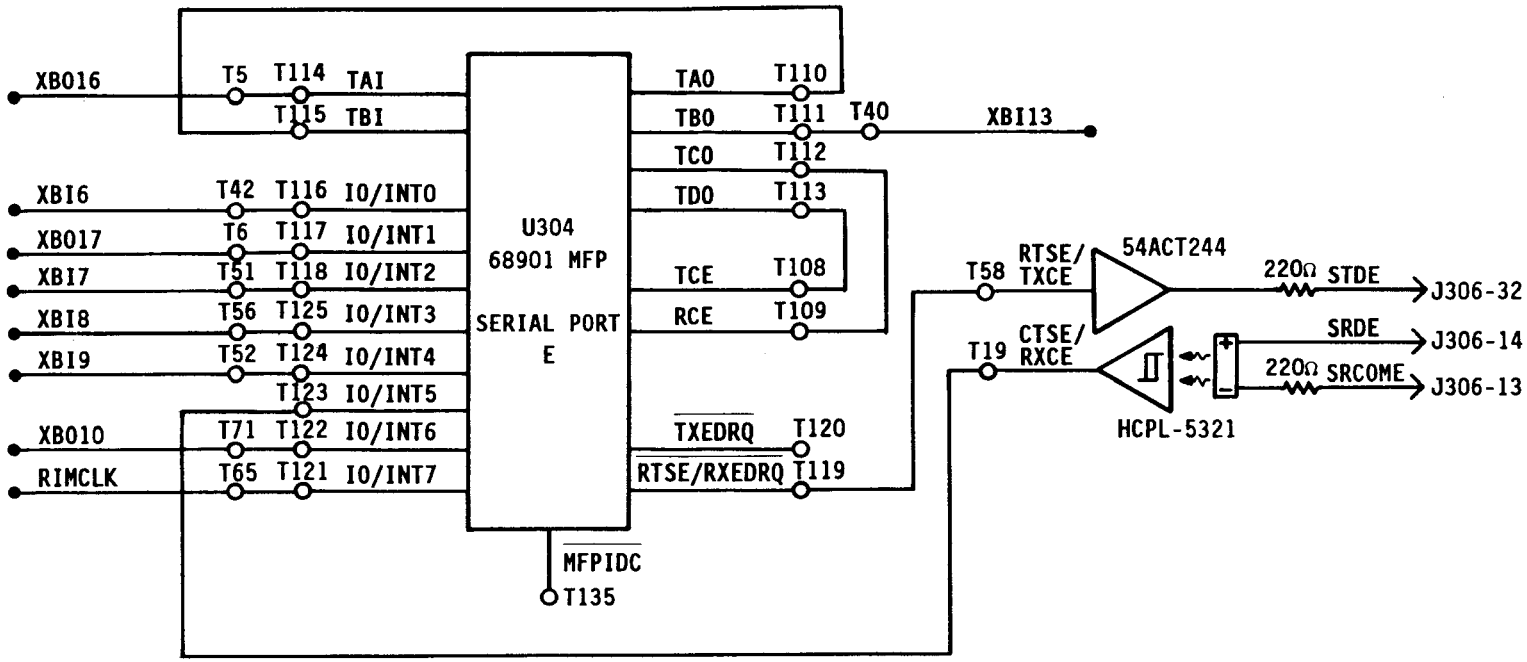


Figure B-23. System I/O Serial Port E Default Jumpers

B.5.4.1 Serial Ports. The System I/O Module serial ports are configured for hardware handshake with the RTS/CTS signals or for supplying a transmit (Tx) clock to and inputting a receive (Rx) clock from an external device as follows:

- Port A - Hardware handshake
- Port B - External clocks
- Port C - External clocks
- Port D - Hardware handshake
- Port E - Hardware handshake

Port E uses the 68901 MFP's Timer C for the Rx clock and Timer D for the Tx clock. A summary of the default jumpers is given in Table B-14.

TABLE B-14. SYSTEM I/O SERIAL PORT CLOCK/HANDSHAKE DEFAULTS

Serial	Jumpers		Signals		
Port	From	To	From	To	Description
A	T14	T61	SCTSA	CTSA	Hardware handshake in.
	T60	T9	RTSA	SRTSA	Hardware handshake out.
B	T13	T81	SRXCB	RTXCB	Rx clock in.
	T80	T10	TRXCB	STXCB	Tx clock out.
C	T18	T98	SRXCC	RTXCC	Rx clock in.
	T97	T11	TRXCC	STXCC	Tx clock out.
D	T20	T67	SCTSD	CTSD	Hardware handshake in.
	T66	T12	RTSD	SRTSD	Hardware handshake out.
E	T19	T123	CTSE	IO/INT5	Hardware handshake in.
	T119	T58	RTSE	SRTSE	Hardware handshake out.
	T112	T109	TCO	RCE	MFP Timer C out to Rx clock in.
	T113	T108	TDO	TCE	MFP Timer D out to Tx clock in.

B.5.5 Interrupt Logic

Figure B-24 illustrates the System I/O Module interrupt logic and associated hardware jumpers. Table B-14 describes the jumpers.

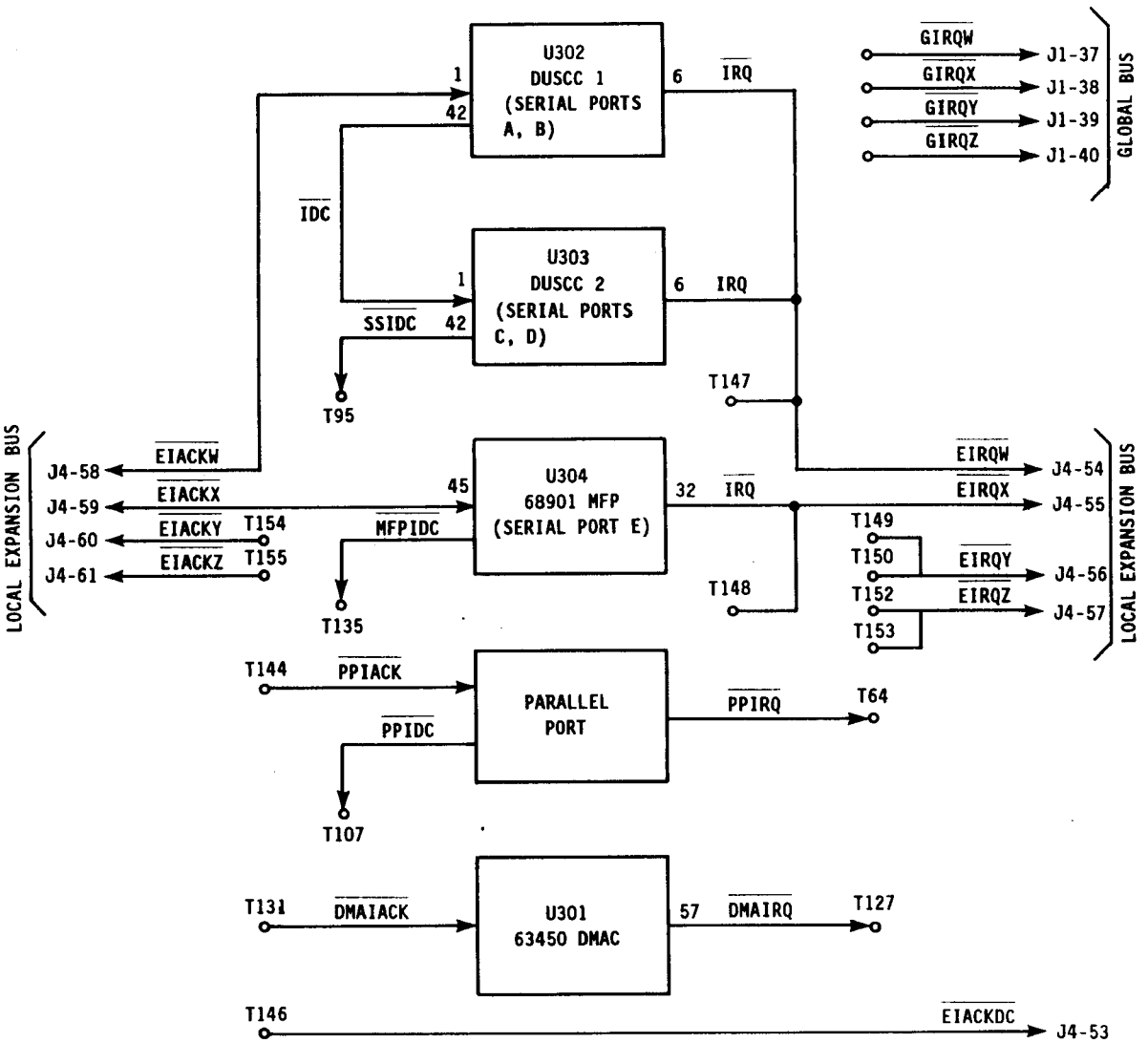


Figure B-24. System I/O Interrupt Jumpers

TABLE B-14. SYSTEM I/O INTERRUPT JUMPERS

Jumper	Signal	Function
T64	$\overline{\text{PPIRQ}}$	Parallel Port Interrupt Request - Parallel port interrupt request output.
T74	$\overline{\text{GIRQW}}$	Global Interrupt Request W.
T75	$\overline{\text{GIRQX}}$	Global Interrupt Request X.
T76	$\overline{\text{GIRQY}}$	Global Interrupt Request Y.
T77	$\overline{\text{GIRQZ}}$	Global Interrupt Request Z.
T95	$\overline{\text{SSIDC}}$	Interrupt acknowledge daisy chain output from DUSCC 2 (serial ports C and D).
T107	$\overline{\text{PPIDC}}$	Parallel Port Interrupt Daisy Chain - Interrupt acknowledge signal propagated by parallel port.
T127	$\overline{\text{DMAIRQ}}$	DMAC Interrupt Request - 63450 DMAC interrrupt request output.
T131	$\overline{\text{DMAIACK}}$	DMAC Interrupt Acknowledge - 63450 DMAC interrupt acknowledge input.
T135	$\overline{\text{MFPIDC}}$	Interrupt acknowledge daisy chain output from 68901 MFP (serial port E).
T144	$\overline{\text{PPIACK}}$	Parallel Port Interrupt Acknowledge - Parallel port interrupt acknowledge input.
T146	$\overline{\text{EIACKDC}}$	Expansion Bus Interrupt Acknowledge Daisy Chain.
T147	$\overline{\text{EIRQW}}$	Expansion Bus Interrupt W.
T148	$\overline{\text{EIRQX}}$	Expansion Bus Interrupt X.
T149	$\overline{\text{EIRQY}}$	Expansion Bus Interrupt Y (1 of 2 pads).
T150	$\overline{\text{EIRQY}}$	Expansion Bus Interrupt Y (2 of 2 pads).

TABLE B-14. CONTINUED

Jumper	Signal	Function
T152	$\overline{EIRQZ}$	Expansion Bus Interrupt Z (1 of 2 pads).
T153	$\overline{EIRQZ}$	Expansion Bus Interrupt Z (2 of 2 pads).
T154	$\overline{EIACKY}$	Expansion Bus Interrupt Acknowledge Y.
T155	$\overline{EIACKZ}$	Expansion Bus Interrupt Acknowledge Z.

The default connections for the interrrupt logic jumpers are shown in Figure B-25.

The default jumpers connect the parallel port to $\overline{EIRQY}$ and make the the port first in the $\overline{EIACKY}$ daisy chain. The default jumpers also connect the DMAC to $\overline{EIRQY}$ and make the DMAC second in the $\overline{EIACKY}$ daisy chain. The parallel port propagates the acknowledge to the DMAC.

B.5.6 Clocks/Power

System I/O Module jumper pads supply Vcc, ground, and a 4 MHz clock (CLK4) as shown below.

Resource	Jumper
Vcc	T140
Ground	T15 T16 T17 T141 T142 T143
CLK4	T134

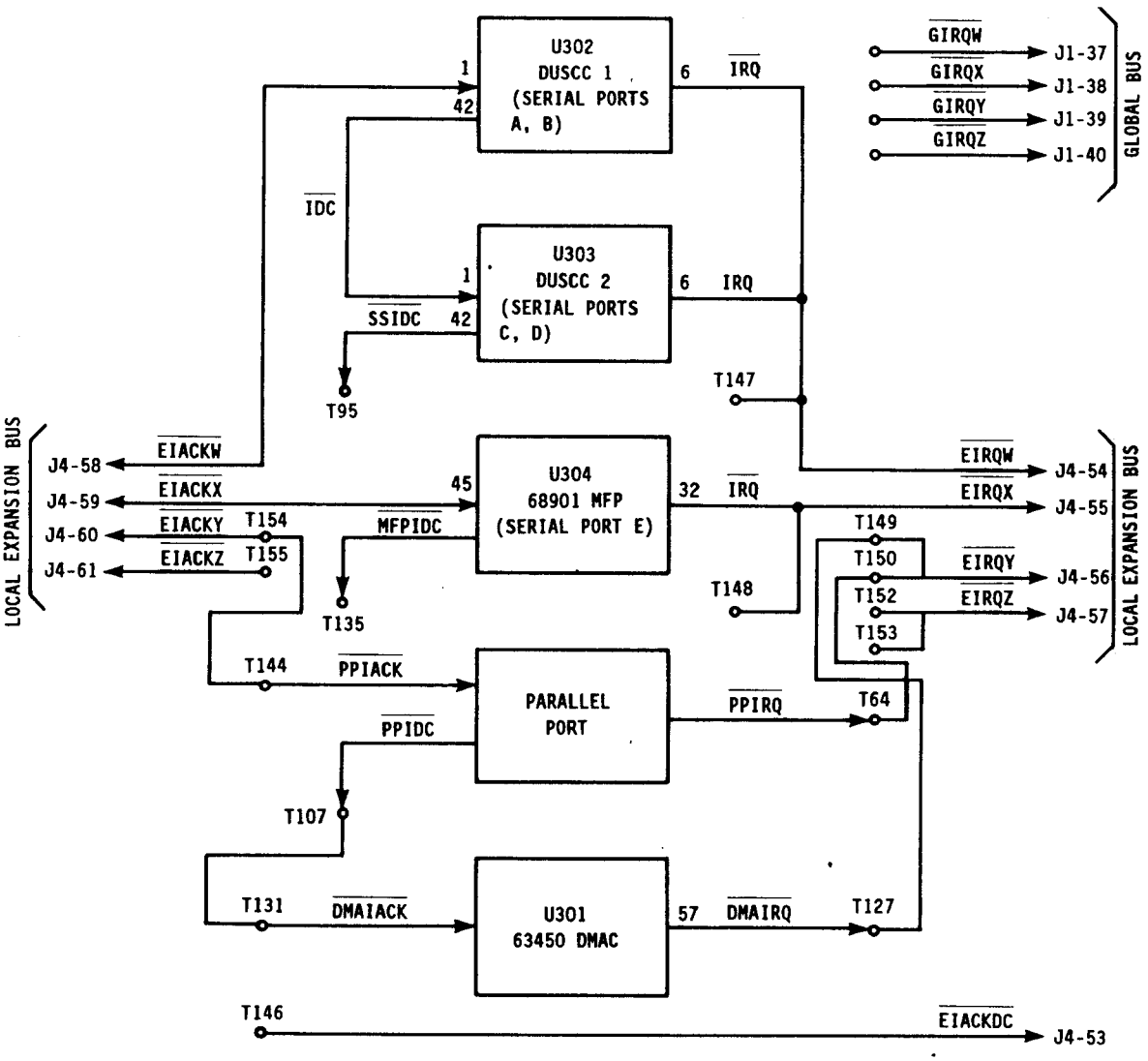


Figure B-25. System I/O Interrupt Default Jumpers

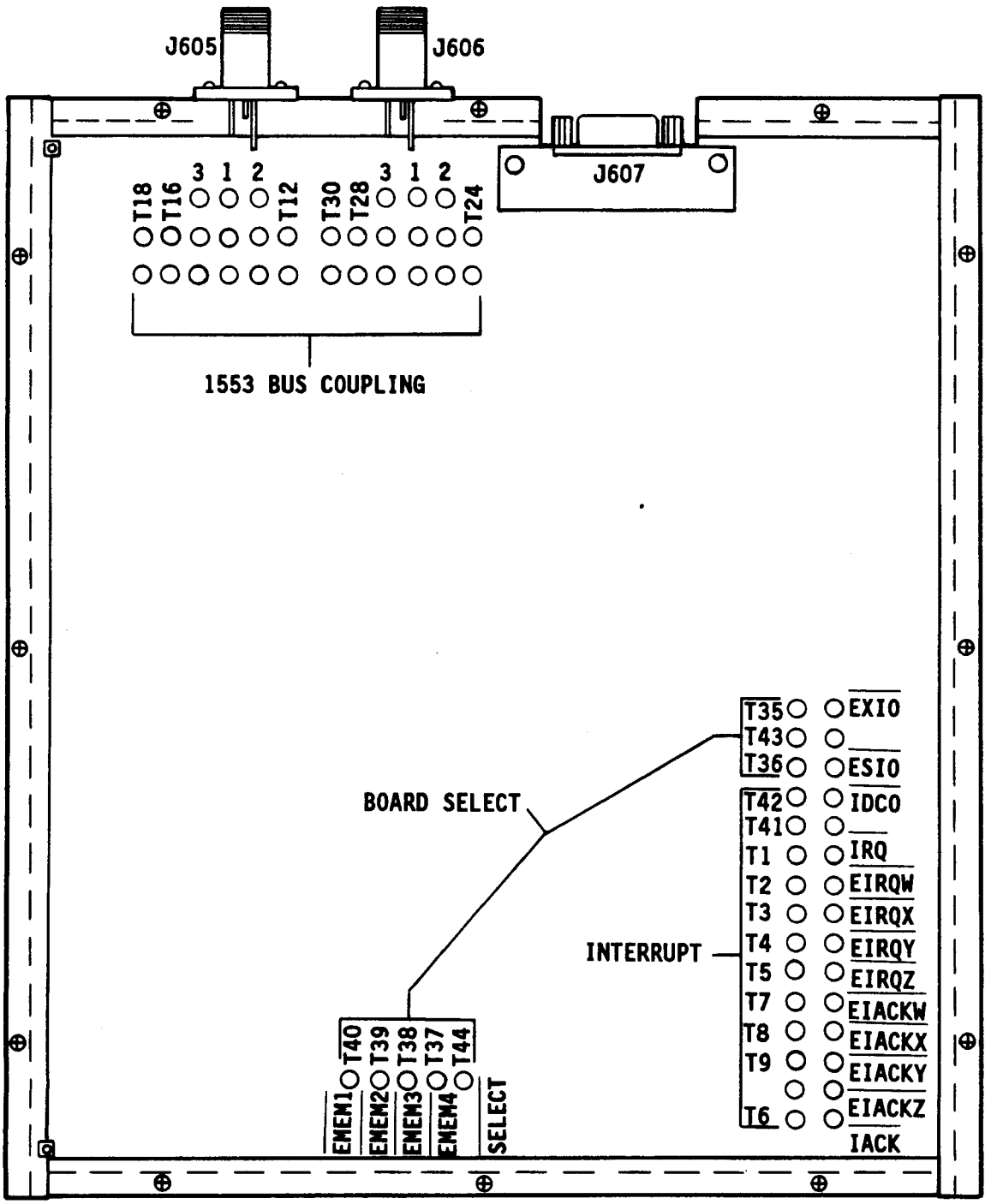


Figure B-26. MIL-STD-1553B Module Jumper Locations

B.6 MIL-STD-1553B MODULE

The MIL-STD-1553B Module has three groups of hardware jumpers that configure the following:

- Local Bus Interrupt Request/Acknowledge Level
- 1553 Bus Coupling
- Module Base Address

The location of the jumper groups is shown in Figure B-26 (facing page). Jumper settings are described in the following subsections.

B.6.1 Interrupt Request/Acknowledge

Figure B-27 illustrates the MIL-STD-1553B Module interrupt logic and associated hardware jumpers. Table B-15 describes the jumpers.

Default jumpers for the 1553B interrupt logic set the module for priority level Y (T1 to T4 and T6 to T9).

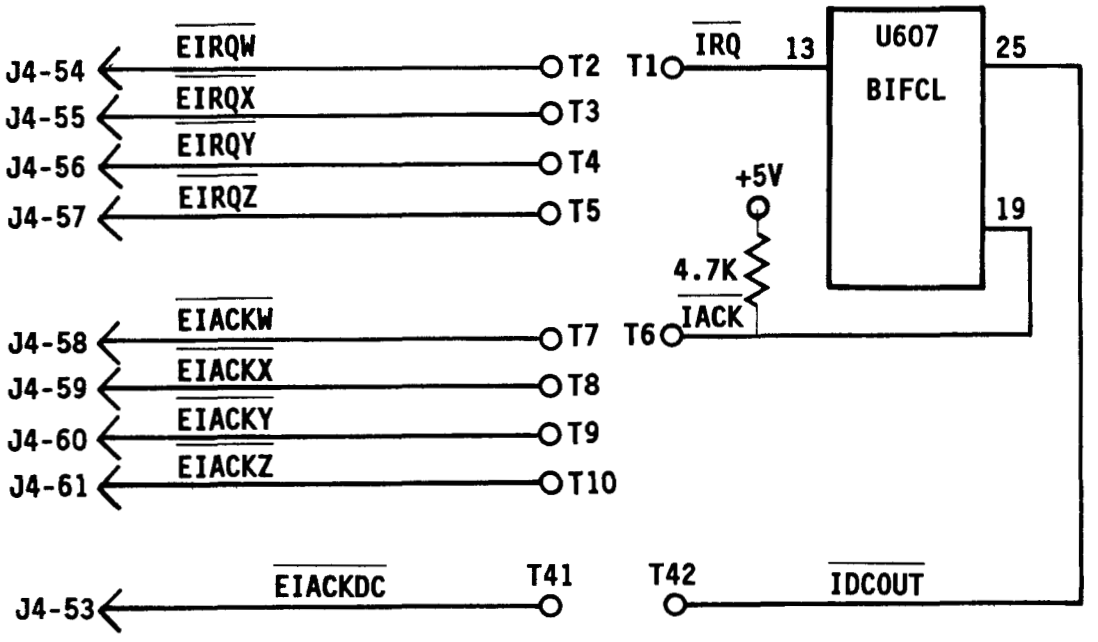


Figure B-27. MIL-STD-1553B Interrupt Jumpers

TABLE B-15. MIL-STD-1553B INTERRUPT JUMPERS

Jumper	Signal	Function
T1	$\overline{IRQ}$	Interrupt Request - 1553B interrupt request output.
T2	$\overline{EIRQW}$	Expansion Bus Interrupt W.
T3	$\overline{EIRQX}$	Expansion Bus Interrupt X.
T4	$\overline{EIRQY}$	Expansion Bus Interrupt Y.
T5	$\overline{EIRQZ}$	Expansion Bus Interrupt Z.
T6	$\overline{IACK}$	Interrupt Acknowledge - 1553B interrupt acknowledge input.
T7	$\overline{EIACKW}$	Expansion Bus Interrupt Acknowledge W.
T8	$\overline{EIACKX}$	Expansion Bus Interrupt Acknowledge X.
T9	$\overline{EIACKY}$	Expansion Bus Interrupt Acknowledge Y.
T10	$\overline{EIACKZ}$	Expansion Bus Interrupt Acknowledge Z.
T41	$\overline{EIACKDC}$	Expansion Bus Interrupt Acknowledge Daisy Chain.
T42	$\overline{IDCOUT}$	Interrupt acknowledge daisy chain output.

B.6.2 1553 Bus Coupling

Figure B-28 illustrates the MIL-STD-1553B Module bus coupling circuit and associated hardware jumpers.

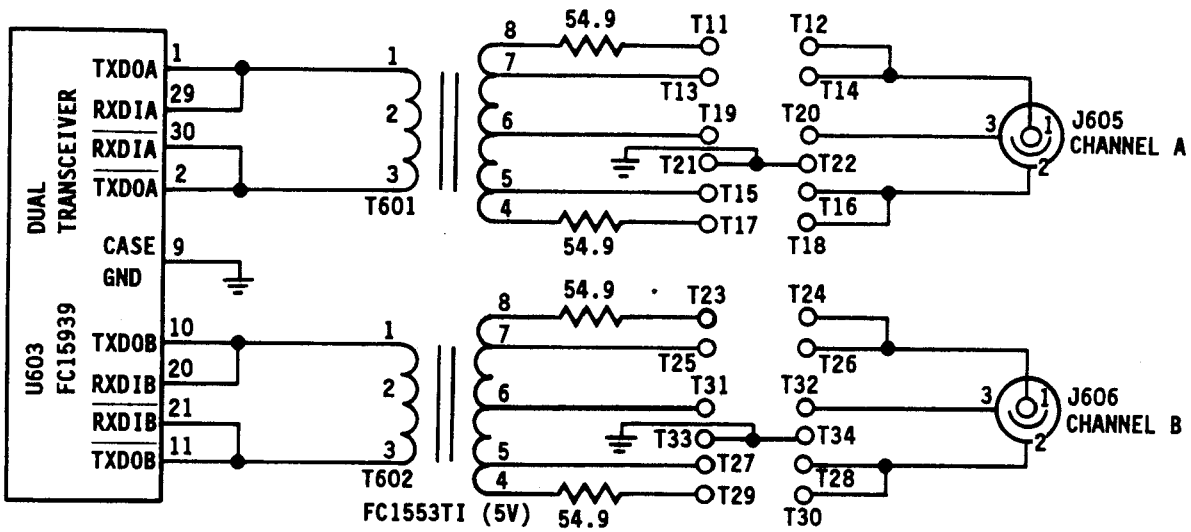


Figure B-28. MIL-STD-1553B Bus Coupling Jumpers

Direct coupling is accomplished with the following connections:

Channel A	T11 to T12
	T17 to T18
Channel B	T23 to T24
	T29 to T30

Transformer coupling is accomplished with the following connections:

Channel A	T13 to T14
	T15 to T16
Channel B	T25 to T26
	T27 to T28

The setting of jumpers T19 through T22 and T31 through T34 is determined by system requirements. These jumpers function as follows:

Cable sheilds are connected as follows:

Channel A	T20
Channel B	T32

Secondary winding center tap connections are made as follows:

Channel A	T19
Channel B	T31

SANDAC V ground is available through T21, T22, T33, and T34.

Default connections are for transformer coupling of both channels with both center taps connected to ground (T19 to T20 and T31 to T32).

B.6.3 Module Base Address

Figure B-29 illustrates the MIL-STD-1553B Module base address select logic and associated hardware jumpers. Table B-16 describes the jumpers.

The default setting for the 1553B module base address is through the $\overline{EXIO}$ line (T43 to T35) at 0n,FF0,000 where "n" is the Processor ID in hex.

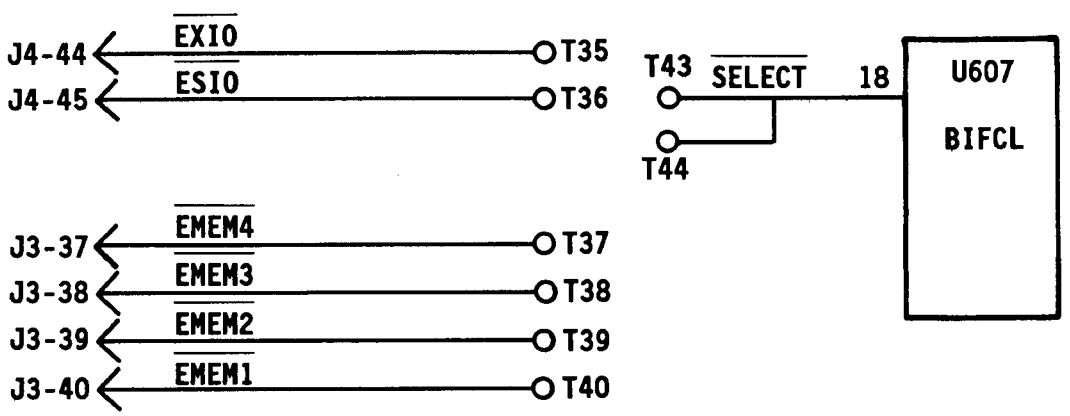


Figure B-29. MIL-STD-1553B Base Address Jumpers

TABLE B-16. MIL-STD-1553B BASE ADDRESS JUMPERS

Jumper	Signal	Function
T35	$\overline{\text{EXIO}}$	Expansion I/O Select - Active low select from host Processor Module when address 0n,FF0,000 is decoded.
T36	$\overline{\text{ESIO}}$	Expansion System I/O Select - Active low select from host Processor Module when address 0n,FFC,000 is decoded. Use of this base address is not recommended because it is the standard base address of the System I/O Module.
T37	$\overline{\text{EMEM4}}$	Expansion Memory Select - Active low select from host Processor Module when address 0n,200,000 is decoded. Use of this base address is not recommended because it is the standard base address of an Expansion Memory Module.
T38	$\overline{\text{EMEM3}}$	Expansion Memory Select - Active low select from host Processor Module when address 0n,180,000 is decoded. Use of this base address is not recommended because it is the standard base address of an Expansion Memory Module.
T39	$\overline{\text{EMEM2}}$	Expansion Memory Select - Active low select from host Processor Module when address 0n,100,000 is decoded. Use of this base address is not recommended because it is the standard base address of an Expansion Memory Module.
T40	$\overline{\text{EMEM1}}$	Expansion Memory Select - Active low select from host Processor Module when address 0n,080,000 is decoded. Use of this base address is not recommended because it is the standard base address of an Expansion Memory Module.
T43	$\overline{\text{SELECT}}$	MIL-STD-1553B Module select line used when either T35 or T36 are used.
T44	$\overline{\text{SELECT}}$	MIL-STD-1553B Module select line used when either T37, T38, T39 or T40 are used.

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