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SANDIA PROGRAMS RELEVANT TO MICROELECTRONICS FABRICATION

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SANDIA PROGRAMS RELEVANT TO MICROELECTRONICS FABRICATION

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Abstract

This report was prepared for the Semiconductor Industry and the National Laboratories Workshop held at the National Academy of Sciences, Washington, D.C., February 24, 1987. It details the current Sandia program activities relevant to microelectronics fabrication.

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I. LABORATORY OVERVIEW

Sandia National Laboratories is an engineering laboratory with a broad scientific research base and a diverse capability in many high-technology areas. It is one of the multiprogram national laboratories of the Department of Energy (DOE). Sandia currently employs about 8,300 people, approximately one third of whom are professional/technical staff. About 41% of our technical staff hold PhD degrees, and 43% hold MS degrees. Roughly 63% of the technical staff have engineering degrees, and 37% have degrees in physical sciences, materials science, computer science and mathematics. .

Sandia's major role is that of a systems engineering research and development laboratory with responsibility for the non-nuclear portions of nuclear weapons systems. The extensive engineering and scientific capabilities of the laboratories are also being directed toward a broad spectrum of non-nuclear energy areas, such as basic energy science, nuclear material security, solar energy, drilling technology, fossil fuel extraction, and combustion. There are major research and development programs in the areas of microelectronics, solid state science, materials science, nuclear reactor safety, and controlled thermo-nuclear fusion. Technology transfer to industry is emphasized in all of the above areas.

A wide range of the work is at the frontiers of science and at the state-of-the-art engineering level. In support of these energy and weapons projects, Sandia maintains large, modern scientific laboratories. Among the many modern laboratories are those for microelectronics; materials growth; ion implantation; shockwave science; pulsed power ion beam fusion; and aerodynamics. To support these laboratories and the engineers and scientists who operate them, Sandia has a large central network of main line computers, including several CRAY-1S systems and a CRAY X-MP/24. Sandia's major semiconductor facilities are centrally located within 15 minutes of Albuquerque International Airport, which has nonstop service to all the major industrial cities of the west and one stop service to the east coast.

SANDIA PROGRAMS IN MICROELECTRONICS COMPONENTS TECHNOLOGIES, PROCESSING, SCIENCE, MATERIALS, AND DIAGNOSTICS

AREA	FTE	FY87 TOTAL COSTS ($M)
SILICON IC PROCESSING	96	$13.0
IC DESIGN	50	8.0
TESTING & ASSEMBLY	40	8.0
SILICON TECHNOLOGY	40	7.3
IC PRODUCTION OPERATIONS (ALLIED BENDIX)	209	17.0
ROBOTICS & AUTOMATION	15	2.8
ENGINEERING MODELING	5	0.8
PROCESSING SCIENCE & MODELING	27	6.0
DIAGNOSTICS & MATERIALS	18	4.0
COMPOUND SEMICONDUCTOR RESEARCH	29	6.0
TOTALS	499	70.9

II. FABRICATION

A. SILICON IC PROCESSING

Program: 66MY, $13M

Facilities: Development and pilot production IC processing of 100mm diameter silicon wafers is currently being carried out in a 6000 sq. ft. Class 100 facility equipped with 1X stepper lithography, RIE etchers, direct digital control furnaces, high and low voltage/current ion implanters, plasma and low pressure CVD reactors, and automated measurement equipment. Currently 400 wafers are started into fabrication each month. An advanced 34,300 sq. ft. 150 mm diameter silicon wafer fabrication facility, with 12,500 sq. ft. of flexible Class 1 clean room, will become operational in early 1988 in Sandia's Radiation Hardened Integrated Circuit (RHIC) Facility. The RHIC clean room will be equipped with $30M of process equipment, including 5X stepper, multi-layer photoresist lithography, cassette load RIE etchers, SEM and automated inspection equipment, vertical diffusion and CVD furnaces, plasma enhanced CVD equipment, high and low voltage/current ion implanters, analytical equipment, and automated in-process parametric testers.

Major Activities:

1. Manufacturing Operations

A three shift per day, seven day per week operations staff of 40 Sandia and contract personnel supports a 400 wafer per month, 10 week in-process-time prototyping activity for two 10 mask technologies with 1.5 micron minimum features. Over 300 unique processes and associated equipment are supported by a staff of engineers and maintenance technicians.

2. Process Development

A staff of 20 engineers and technicians develop the advanced processes required for new CMOS IC technologies. Activities include advancements in manufacturable photoresist and lithography processes, deposited films, including selective tungsten and TaSi films and AR coatings, thermal processes, and RIE processes utilizing novel gas mixtures. A strong engineering program in contamination, defect identification and reduction, and in-process control measurements is also supported.

3. Automation

An automation activity has been established for the new RHIC wafer fabrication clean room. The program is based on commercially available hardware and software, including a Veeco AGV robotics and WIP system, the purchase of all RHIC wafer fabrication equipment with SEMI SECS communications interfaces and cassette to cassette wafer handling, the Consilium COMETS software package and associated DEC VAX computer cluster and peripherals, and complete Ethernet communications networking of the RHIC Facility. The RHIC clean room has been designed and equipment layouts planned to support the automation activity.

Selected Accomplishments:

1. The development, characterization, and transfer to a vendor of a novel new dyed photoresist for use in patterning highly reflective films.

2. The development of a new BBr_3/Cl_2 gas chemistry for reactive ion etching of aluminum films.

3. Identification and control of the diffuse reflectivity of reflective films as a means of establishing manufacturable processes for patterning the films.

4. Establishment of an automation strategy to fully automate the RHIC Facility.

B. INTEGRATED CIRCUIT DESIGN

Program: 50MY, $8.0M

Facilities: Engineering design environment includes: state-of-the-art computer aided engineering workstations, parallel processing mainframe computer for high speed computations, and special hardware accelerators for data verification and simulations. The hardware facilities are augmented by commercial, in-house developed and customized software.

Major Acitivities:

1. Cad Tool Development

The CAD effort provides a hardware and software environment for simulation and modeling of IC processes, devices, and circuits. Wherever possible, this environment is based on commercially available products. Special customization occurs when required, for example in simulations of severe radiation and temperature environments. State-of-the-art MOS models have been developed which more accurately represent actual performance.

2. Radiation Hardening of Commercial Products

Emulation of commercial products using radiation hardening design methods is accomplished when multiple systems can employ the same devices. This is especially true for microprocessors and other computing elements. Emulation is used in order to take advantage of commercially available development tools, to allow use of non-radiation hardened devices for system development, and to shorten the design cycle and reduce costs.

3. Design of Custom Products

For systems where unique functions are required, custom designs are created to satisfy those needs. These custom designs include complex logic functions, analog circuits, and devices exploiting mixed technologies. In addition, custom memory circuits are developed for both volatile and nonvolatile data applications.

Selected Accomplishment:

Numerous circuits have been designed in support of DOE weapon programs, verification and control space applications, and DOD military systems. In addition, NASA/JPL projects and research endeavors within Sandia's Center for Radiation Hardened Microelectronics have been supported.

C. PACKAGING AND TESTING

Program: 40MY, $6M

Facilities: Saw and die separators for 150 mm and smaller wafer separation; eutectic, epoxy, and silver-glass die attach equipment; belt furnace and hot platen equipment for Au/Sn solder reflow sealing of hermetic lids. In addition, mechanical and environmental test equipment for packages include: bond pull test, die shear test, centrifuge, particle impact noise detection test, both fine and gross hermetic leak tests, temperature cycling, and x-ray test. These are employed to assure high reliability, WR qaulity parts.

Radiation effects testing sources include: four laboratory sources of Cobalt 60, three laboratory sources of Cs137, and x-ray machine capable of wafer level testing and the Gamma Irradiation Facility for total dose testing; the Hermes II, SPEED, and Hydramite II machines for high dose rate testing; the ANNULAR Core Research Reactor and Sandia Pulse Reactor III for neutron and millisecond timescale total dose testing; and a Californium 252 laboratory source for cosmic ray testing.

Integrated circuit electrical test equipment includes 2-60 pin. 10 MHz testers; 2-60 pin, 20 MHz testers; and 1-160 pin, 40 MHz tester. These support fully functional digital and analog circuit tests and precision parametric measurements at the operating frequency of the integrated circuit. Four fully automatic, cassette-to-cassette, auto-aligning probers and four manual probers provide wafer level testing. A VAX-based local area network supports electrical test data acquisition and analysis.

Major Activities:

1. Packaging

Sandia's packaging activities include leadless chip carrier packages; side-brazed, dual-in-line packages; flat packs; and a pin grid array package currently under development. These capabilities permit packaging of ICs with up to 180 pins with a total packaging capability of 3200 parts/month.

2. Radiation Testing

The radiation testing emphasis has been on qualification of over 150 integrated circuits and discrete semiconductors for application to satellite systems, tactical nuclear weapons, and strategic nuclear weapons. Portable, computer-controlled test equipment is developed to permit radiation studies of integrated circuits to be conducted under electrical conditions representative of IC use conditions. In order to extrapolate radiation test results to actual threat environments, fully understand the measured response, and support the design of new ICs, computer modeling of radiation effects phenomena is emphasized. Currently a full range of circuit analysis tools are in use that permit maximization of dose rate upset levels, as well as maximization of SEU hardness. Two-dimensional, time-dependent device physics codes are utilized for latch-up, snap-back and SEU hardening of IC designs.

3. Electrical Testing

Complete electrical testing is performed for new IC design verification, device characterization, wafer process development, failure analysis and prototype deliveries. Testing capability exists for the full range of digital ICs including: microprocessors, minicomputers, volatile and nonvolatile memories, encryption devices, gate arrays, standard cell designs, and full custom designs. Data acquisition and analysis are provided to aid trouble-shooting and quality control. A program is underway to make this an on-line, interactive capability with electronic reading of packaged part serial numbers and robotic handling of nonstandard packages in elevated temperature tests.

Selected Accomplishments:

1. We have developed techniques for hermetic sealing of high reliability packages that result in significant improvements in package yield and are currently developing a high reliability package design that inhibits fission fragments induced by thermal neutron irradiation of package materials from reaching the sensitive regions of integrated circuits.

2. Modeling of dose rate upset in SRAM technology has been developed sufficiently to predict the dose rate at which the SRAM will upset, which memory cell will actually upset and the upset rate dependence on power supply voltage and radiation pulse width. Progress in device physics models of SEU, latch-up and snap-back now permit immunity to these effects to be achieved on the first integrated circuits that are fabricated.

3. Electrical and radiation characterization has been completed for all the semiconductor devices used in the Trident II, B61, CAP, and W82 weapons programs.

III. ENGINEERING

A. SILICON TECHNOLOGY

Program: 40MY, $7.3M

Facilities: Cambridge electron beam test system; two scanning electron microscopes; multiplexed, time-dependent transistor test system with positions for 900 transistors; three HP4062 parametric test systems with automatic wafer probing; Keithly 450 parametric tester with automatic wafer probing; wafer and transistor test network based on PDP 1173 with automatic wafer probe stations; complete failure analysis facilities including laser cutting apparatus for diagnostic studies; two Gammacell 220 Co^{60} radiation sources; Aracor x-ray radiation source; two variable dose rate Shepard cell radiation sources.

Major Activities:

1. CMOS Development

Sandia has developed a series of rad-hard CMOS technologies up to and including a single-level metal micron (1.5 micron minimum feature size) technology in which a single-event-upset free 16K SRAM is fabricated. Currently, a two level metal version of this technology is under development for fabrication of large logic chips such as 16 and 32-bit microprocessors and a single-chip microcontroller. These technology developments are based on extensive Sandia understanding of the relation between IC materials and

processes, and radiation-effects in silicon devices. Depending on the exact nature of the application they are hardened to 10^5 to 10^6 rads and are resistent to transient radiation effects to appropriate dose rates.

2. MNOS/SNOS Devlopment

Nonvolatile memories are important in many defense systems; however, when radiation tolerance is an issue many commercial approaches are not satisfactory. Sandia has developed several nonvolatile memory ICs based on MNOS (metal-nitride-oxide-semiconductor) or SNOS (polysilicon-nitride-oxide-semiconductor) nonvolatile transistors. A 16K electrically-erasable PROM has been developed which retains data for 10 years after 10^4 write-erase cycles and is hardened to levels well above 10^5 rads. Currently, a 256K EEPROM is under development.

3. Silicon-On-Insulator (SOI) Development

In collaboration with several other major laboratories, Sandia has initiated a substantial effort in the fabrication, processing, and characterization of SOI material. Our development of SOI involves using porous silicon (FIPOS), ion-implantation (SIMOX) and recrystallization of polysilicon (ZMR). Recently, we have demonstrated a solution to the difficult problem of stabilizing the sidewalls of SOI transistors to ionizing radiation environments.

4. Device Physics

In the course of developing CMOS and nonvolatile memory technologies, Sandia has established very productive device physics activities. Our researchers have shown with ESR techniques that trapped holes generated by ionizing radiation in MOS transistor gates correspond to certain well known defect centers in SiO_2. In processing studies, they have shown the close relationship between radiation-induced trapped charge, interface states and certain processing features such as thermal treatment ambients. In the nonvolatile memory area, numerical simulations and device studies have allowed accurate prediction of SNOS memory retention and radiation response. Applying a two-dimensional time-dependent multiple device computer program to the problem of single-event-upset has also enabled us to make important contributions to the understanding and prevention of this phenomenon.

<u>Selected Accomplishments</u>:

1. Developed a 4 micron metal line, 3 micron minimum feature size 10V rad hard CMOS technology. Delivered engineering and high reliability parts for $>2x10^5$ rad total dose requirements in several dozen designs with the most complex design containing 24,000 transistors.

2. Developed a 3 micron minimum feature size, 4 micron SNOS gate, radiation-hardened nonvolatile memory technology. Applied this technology to develop a 16K-bit EEPROM with 10-year retention at 80 C after 10^4 write-erase cycles.

3. Developed a 2 micron metal line, 1.5 micron minimum feature size 5V CMOS IIIA technology which uses a Sandia developed radiation-hardened field oxide instead of guardbands to prevent radiation-induced field inversion. Applied this technology to develop an SRAM immune to cosmic ray upset.

B. ROBOTICS AND AUTOMATION

Program: 15MY, $2.8M

Facilities: GCA Gantry Robto, Cincinnati Milacron Pedestal Robot, 2 Puma 560 Pedestal Robots, Machine Vision Computer Vision System, JR3 Force Sensing Wrists, 2 Symbolics Computers, 4 Micro Vax Computers, Sun 2 and Sun 3 Workstations.

Major Activites:

1. Robotic Transport

The Intelligent Machine Division has ongoing research in both the areas of robot mobility and dextrous manipulation. Sandia is applying its experience in the integration of force sensing into the control of commercial robot manipulatiors to the problem of reliable, damage-free placement of cassettes of silicon wafers onto process equipment. Sandia's research into zero turning-radius robot vehicles with intelligent obstacle avoidance and navigation could reduce the expense of constructing clean rooms by reducing the clean room floor area (elimination of room for turning), reducing programming time (through intelligent navigation), and improving reliability (through obstacle avoidance and error recovery). The RHIC-II commercial mobile robot manipulator system (VEECO Corp.) will serve as an initial system for integration of force sensing into robot control.

2. Equipment Interfaces

Advanced software interfaces must be made available to process programmers. Given that any silicon fabrication facility will contain many varied pieces of equipment a standard, easy to use high level programming language must be developed. Such programming languages interface between the high level CIM software and the individual equipment controllers. Such tools must also aid in the prevention of operator error. A start is already under way on such programming strategies in the robotic subsystem of RHIC-II. Sandia is currently designing both the hardware and software interfaces to monitor forces during the manual teaching of robot positions to prevent inadvertent striking of objects during the robot teaching process. This would allow less experienced operators to teach the robot. In addition, software is being developed to monitor operator initiated teach commands with a computer model of process equipment to protect against equipment damage and to speed robot programming.

3. CIM Systems

Although equipment and subsystems will be programmed on an individual basis to perform specific functions, integration of this equipment into a fully automated system for manufacturing is the role of the CIM system. A major difficulty lies in the fact that existing CIM systems are essentially very large data collection/manipulation systems (Automated Process Monitoring). They must take on the role of process planning and control (Automated Process Control). Sandia has ongoing research in distributed control in multiprocessor environments for robot system control. Development of a systems simulation model using object oriented programming techniques would be very useful for the development and testing of appropriate CIM software architectures.

Selected Accomplishment:

A maintenance robotic system has been developed for the Sandia Pulsed Reactor. In order to remove people from maintenance operations a robotic system was developed which performs removal and replacement of major subsystems on the reactor. The maintenance robotic system contains several key subsystems - a Puma robot arm with a force sensing wrist mounted on a programmable turntable, a programmable overhead hoist for moving heavy parts and a hierarchical supervisory control system. This system has been delivered to the Sandia reactor and the operators are in the process of training.

C. ENGINEERING MODELING

Program: 5MY, $0.8M

Facilities: Analytical capabilities include convection, conduction, and radiation heat transfer, Newtonian and nonNewtonian fluid mechanics, chemically reacting multiphase flow and structural mechanics. Laboratory facilities include fluids/heat transfer lab with optical diagnostics, rheology lab, and dynamic heating facility.

Major Activities:

1. Heat Transfer/Fluid Mechanics Code Development

A broad range of heat transfer/fluid mechanics/materials processing codes are avilable and development is continuing on new numerical techniques such as adaptive gridding and flux-corrected transport methods. Melting/ solidification phenomena in soldering and welding, suspended particle motion in processing flows, and solid-state diffusion are being modeled.

2. Structural and Materials Code Development

Structural analysis codes are being developed for advanced static and dynamic thermal/mechanical stress analyses of systems and components for a wide range of environmental conditions. Viscoelastic, viscoplastic and creep behavior are being modeled, along with failure mechanisms involving crack growth, erosion and brittle fracture.

Applications include materials processing, and thermal/mechanical concerns for packaging high density microelectronic circuits, hybrid circuits, printed circuit boards, and complete electronic systems. Thermal/structural and dynamics analyses are carried out on rigid-flex connectors, flex circuits, flat cables, solder joints, and encapsulants.

Selected Accomplishments:

1. One-, two-, and three-dimensional heat transfer and structural analysis codes have been developed and brought into production to solve high density thermal energy, static and dynamic problems, including those with highly nonlinear materials and large deformations.

2. Developed a material model to describe the general structural behavior of polyurethane foam used in encapsulating electronic components.

IV. SUPPORTING RESEARCH

A. PROCESSING SCIENCE & MODELING

Program: 27MY, $6.0M

Facilities: Research laboratories include: ion implantation; CVD, MOCVD, MBE, laser-enhanced MBE and CVD, and plasma-enhanced CVD; plasma-enhanced etching; laser-enhanced deposition and etching; rapid thermal processing; oxidation and nitridation; conventional CVD-, laser- and plasma-discharge-enhanced metallization; FIPOS, ZMR and SIMOX fabrication of SOI; and process simulation capabilities.

Major Activities:

1. Chemical Vapor Deposition

State-of-the-art laser diagnostics of silicon CVD have been coupled with computational methods to understand fundamental mechanisms of CVD. A detailed model has been developed that describes heat and mass transfer and chemical kinetics that occur in CVD reactors. The model predicts gas temperatures, flow velocities, reactant product and intermediate species concentrations and deposition rates as a function of process variables and has been correlated with laser-based diagnostic measurements. The modeling has been extended to CVD rotating disk reactor geometries. MOCVD and MBE studies are being conducted of ion, laser and electron beam-enhanced epitaxy. Tungsten CVD for low temperature, selective deposition is being investigated.

2. Etching and Deposition

Laser-enhanced etching and deposition of thin films is under investigation in a wide variety of configurations. For example, laser chemical etching of aluminum in chlorine gas atmosphere can remove aluminum thin films with a laser energy an order of magnitude less than required by ablative techniques without severe damage introduction. Lasers are also used for deposition of highly doped polysilcon conducting lines. Significant progress has been made in plasma-deposited dielectric films for planarizing surfaces. Tungsten deposition by abnormal glow discharge techniques is being studied for non-selective deposition with good adherence to insulators. Plasma-initiated laser etching and deposition is also under investigation.

3. Thin Films, Ion Implantation and Defects

Investigations are being made of ion implantation and defects in silicon, dielectrics and at silicon-dielectric interfaces and the correlation of these defects with electrical properties. Activities center on thermal donors in silicon, rapid thermal processing, defects at the Si/SiO_2 interface, radiation sensitivity and defect passivation, dielectrics, and the fabrication of silicon on insulator structures by implantation, electron beam zone melting and porous silicon oxidation. Metallization schemes for reducing electromigration and hillock formation for interconnects are being explored in terms of linewidth, lifetime, pulsed current and multilevel metallization.

Selected Accomplishment:

1. Design Fault Analysis with Laser Chemical Processing

Laser-initiated localized etching and deposition techniques have been developed to correct design errors in fabricated circuits and thereby provide rapid validation of design corrections. The laser microscope device allows cutting of aluminum metallization lines and formation of new interconnects through doped polysilicon deposition on VLSI circuits. The system is being developed into a commercial unit by Lasertechniques Inc., in a collaborative technology transfer agreement with Sandia.

B. DIAGNOSTICS AND MATERIALS

Program: 18MY, $4.0M

Facilities: Analytical capabilities include ion beam analysis, infrared and optical spectroscopies, photoluminescence, electron spin resonance, scanning and transmission electron microscopy, high resolution x-ray scattering, DLTS, electrical resistivity and Hall effect measurements, electron microprobe, SIMS, Auger, XPS, and a wide range of laser spectroscopies and various analytical chemical analyses. Major supporting materials activities involve ceramics, polymers and resists.

Major Activities:

1. Material Diagnostics

Major facilities exist for characterizing the composition and structure of materials, as well as the identity of electrically active defects. Three dimensional, submicron characterization of the composition of materials is obtained by ion beam and microbeam analysis, electron microprobe, scanning transmission electron microscopy, sputter Auger and SIMS. Electron diffraction, lattice imaging, high resolution x-ray rocking curves, ion channeling, infrared absorption, spin resonance and electrical techniques are used to characterize the structure of materials and to identify defects. Chemical and electronic properties of materials are examined by XPS, Auger, electron spin resonance, photoluminescence and transport measurements. Major areas include: fabrication and properties of silicon on insulator structures involving buried oxide, nitride and oxynitride dielectrics; the silicon dioxide-silicon interface; defects in silicon such as oxygen, nitrogen and carbon; defects thin oxides, nitrides and oxynitrides; and properties of thin films formed by low temperature processes.

2. Resists

A variety of polymers and photoresists are under investigation, including novel silicon containing resists for use with deep uv, e-beam and x-ray exposure tools. Emphasis is being given to the general area of radiation resists, which make use of electron or x-ray resists technology, and to the development of dyed resists which prevent loss of linewidth control due to light scattering at reflective surfaces.

3. Ceramics

A major program exists in the fabrication, characterization and tailoring of ceramic materials. While these activities are not specifically directed towards microelectronics, the work relates importantly to the development and improvement of packaging materials. Additional activities include such areas as spin cast carbon for possible electronic circuit resists with high chemical and thermal stability and ink jet printing of micron width conduction lines.

Selected Accomplishments:

1. Defects at the Si/SiO_2 Interface

Electron spin resonance has given the first positive identification of the structure and electronic character of the electrically active P_b center at the Si/SiO_2 interface. Correlations have been established between P_b centers and the electrically active defect density as a function of radiation, annealing, hydrogen passivation and interface strain.

2. New Photoresists

Two types of photoresists have recently been developed with significant implications. A dyed photoresist has been developed based on an absorber which is highly soluble in cellosolve acetate-based resist, acts as a strong absorber and has little affect on other processing parameters. This material used in the production of 256K EEPROM eliminates a severe notching problem by reducing loss of line width control over reflective surface regions. A second photoresist developed is a polysilane self-developing resist applicable to deep uv, e-beam and x-ray exposure tools. This resist self-develops in regions of exposure, thus substantially simplifying lithography by obviating solvent development and related process steps.

C. COMPOUND SEMICONDUCTOR RESEARCH

Program: 29MY, $6.0M

Facilities: We have a Compound Semiconductor Laboratory for device fabrication (existing facilities will be augmented with 4,000 sq ft of Class 100/1000 clean room schedule for completion February 1988.) MBE, MOCVD and LPE crystal growth facilities, and complete electrical optical and structural materials analysis capabilities.

Major Activities:

1. Materials Growth

MBE and MOCVD growth of a wide variety of compound semiconductor materials is being investigated with emphasis on strained-layer superlattices (SLS) includes GaAsP/GaP for high-temperature electronics, AlGaAs/GaAs systems for laser applications, InGaAs/GaAs for high-speed devices, and InAsSb/InSb systems for long-wavelength detector applications.

2. Materials Properties

A wide variety of experimental and theoretical studies of the unique properties of artificially structured materials, including strained quantum wells for high-speed devices, light holes for high-speed p-type devices, matched electron and hole transport properties for complementary logic and tailored bandgaps for optical detectors and emitters are being conducted.

3. Devices

A wide range of novel devices are under investigation including strained-quantum-well FETs for high-speed logic and microwave applications, light emitting diodes and detectors for radiation-hard optoelectronics at wave lengths from the infrared to the ultraviolet, integrated function SLS optical/electrical devices including narrow band filter/detectors or emitters, and surface emitting semiconductor laser structures.

Major Accomplishments:

1. Strained-Layer Superlattices

We pioneered the field of SLS materials for electronic and optoelectronic devices. SLSs represent a new class of materials for fundamental physics and device applications. These materials are unique in that they allow the energy bandgap to be tailored over a wide range from the far infrared to the near ultraviolet for optical applications and the band structure to be tailored for high mobility charge transport for electronic applications.

2. SLS-Based Devices

An important new class of devices based on strained-layer superlattice materials have been developed including high-frequency strained n-channel FETs for high speed logic and microwave applications, the first high performance strained p-channel FETs in compound semiconductors and integrated optoelectronic devices involving filters, detectors, emitters and laser structures.

V. MANAGEMENT

A. MANAGING ENGINEERING RESEARCH, DEVELOPMENT AND DESIGN FOR MANUFACTURE

Sandia has experience managing multidisciplinary engineering projects that integrate research, development, and manufacturing in many weapons and energy programs. Sandia has to deal with classified, proprietary, and unclassified research and development in its present work and has long experience in developing, safeguarding, transferring, and disseminating technical information as appropriate.

B. MANAGING INTELLECTUAL PROPERTY

Sandia has had considerable experience working with industry to develop and transfer technology that gives industry a differential competitive advantage. This has been done in many ways including workshops, specialized working groups, technology transfer agreements, patents and licensing. Many programs combine industrial proprietary information with Sandia R&D to achieve advanced engineering accomplishments. Examples of collaborative projects include the following.

Microelectronics:

Joint projects in microelectronics with companies and universities include National Semiconductor, Intel, Motorola, MIT, Hewlett Packard, TRW, Harris, GTE, AT&T and UNISYS. For example, design packages were exchanged with National on the 32000 microprocessor family and with Intel on the 80C51 microcontroller for developing rad hard versions. Proprietary rights were preserved and the companies retained the first right of refusal for manufacture of the rad hard parts.

Photovoltaics:

In the area of photovoltaics we have had collaborative projects with Varian, Applied Solar Energy Corp., Westinghouse, Spire, Mobil Tyco, Motorola, SERA Solar, ArcoSolar and others. We also have a strong interactive photovoltaics program with universities including Stanford, CalTech, Purdue, MIT, New Mexico State, CalPoly, University of Florida, Arizona State, Ohio State, SUNY, and North Carolina A&T.

Combustion:

The National Combustion Research Facility is operated by Sandia and has successfully integrated collaborative research between industry (GM, Ford, Cummins, Lennox) universities and the DOE national labs. Sandia in its interactions with industry at the Combustion Research Facility has established a track record of protecting industrial rights and intellectual property.

Sandia meets regularly and separately with GM and Ford in independent working groups to discuss topical issues in engine combustion. In these discussions the companies are responsible for protecting their proprietary materials but discuss freely their research which includes work on the single cylinder engine. Sandia does not publish or publicize the industrial results, but we are not responsible for protecting the industrial rights. The meetings are not open and in fact we have refused Nissan attendance. This example demonstrates that the CRF has established a mode of operation that entails trust with industry, appears workable, and yet does not inhibit the publication of advanced research.

C. SANDIA'S TECHNOLOGY TRANSFER POLICIES

Federal legislation and Department of Energy policies favor technology transfer that aids U.S. industrial competitiveness. The following are current practices which may particularly influence relationships between the participants in a semiconductor research effort.

1. Sandia will protect proprietary information provided by a participant, provided that such data are identified in writing and are acknowledged to not be previously known to the laboratory.

2. Improvements and new developments may be available on an exclusive basis to an entity that completely supports an area of research at a national laboratory. The degree of exclusivity will diminish when program expenses are shared by the DOE, and the exclusivity is subject to negotiations with the DOE. The current procedures are that the government and AT&T as the contractor that operates Sandia reserve royalty free licenses to use the technologies so developed.

3. When research costs are shared with the DOE, the results are published. However publication may be delayed or cancelled for security classification, patenting purposes, or to adhere to export control regulations.

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2000	L. K. Anderson
2100	B. L. Gregory (25)
2120	E. G. Franzak
2126	J. E. Gover
2130	D. L. Weaver
2140	C. F. Gibbon
4030	G. W. Kuswa
8340	W. Bauer
3141	S. A. Landenberger (5)
3154-1	C. H. Dalin
	DOE/OSTI (28)
8024	P. W. Dean