

# SANDIA REPORT

SAND87-0873 • UC-13

Unlimited Release

Printed March 1988

## Thermal Cycling Tests on Surface-Mount Assemblies

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Prepared by  
Sandia National Laboratories  
Albuquerque, New Mexico 87185 and Livermore, California 94550  
for the United States Department of Energy  
under Contract DE-AC04-76DP00789

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Printed in the United States of America  
Available from  
National Technical Information Service  
U.S. Department of Commerce  
5285 Port Royal Road  
Springfield, VA 22161

NTIS price codes  
Printed copy: A02  
Microfiche copy: A01

# Thermal Cycling Tests on Surface-Mount Assemblies

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## Abstract

The capability of surface-mount (SM) solder joints to withstand various thermal cycle stresses was evaluated through electrical circuit resistance changes of a test pattern and by visual examination for cracks in the solder after exposure to thermal cycling. The joints connected different electrical components, primarily leadless-chip carriers (LCCs), and printed wiring-board (PWB) pads on different laminate substrates. Laminate compositions were epoxy-glass and polyimide-glass with and without copper/Invar/copper (CIC) inner layers, polyimide-quartz, epoxy-Kevlar, and polyimide-Kevlar. The most resistant joints were between small LCCs (24 and 48 pins) and polyimide-glass laminate with CIC inner layers. Processing in joint formation was found to be an important part of joint resistance. Thermal cycling was varied with respect to both time and temperature. A few resistors, capacitors, and inductors showed opens after 500 30-min cycles between  $-65^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ . Appreciable moisture contents were measured for laminate materials, especially those of polyimide-Kevlar after equilibration in 100% relative humidity at room temperature. If not removed or reduced, moisture can cause delamination in vapor-phase soldering.

## **Acknowledgments**

This report represents the combined efforts of a number of people, and the author thanks them for their contributions, particularly Floyd Gentry, Printed Circuit Division, for board fabrication, Joe Dal Porto, Printed Circuit Division, for board assembly; and Roger Goode, Rotational Dynamics Division, Brent Williams, Packaging Technology Division, and Norbert Martinez, Printed Circuit Division, for thermal cycle testing.

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# Thermal Cycling Tests on Surface-Mount Assemblies

## Introduction

Surface mounting of components to printed wiring boards (PWBs) offers potential means for achieving smaller and more reliable electronic packages.<sup>1-12</sup> However, certain difficulties need to be overcome to achieve the high reliability required of these smaller assemblies; the principle one is the matching of the thermal coefficient of expansion (TCE) of the board to that of the ceramic-base components such as the alumina substrates of leadless-chip carriers (LCCs). Surface mounting is a developing technology and several laminate systems have been proposed and are under investigation for matching in the X-Y plane, the TCEs of the LCCs. Seven laminate compositions were evaluated, and are listed in Table 1. Component placement and soldering procedures used to join the components to the PWB were also being evaluated. Thermal cycling with electrical and visual monitoring were used to assess the reliability of the solder joints which provide both mechanical and electrical interconnections on the board.

This report is an interim report covering three phases of an on-going investigation of the effect of thermal cycling on the electrical and mechanical properties of solder joints made between various circuit components and different substrate materials.

## Phase I

In the first phase of this investigation, solder-joint cracking was seen when PWBs with surface-mounted LCCs were subjected to thermal cycling from  $-55^{\circ}\text{C}$  to  $75^{\circ}\text{C}$  and  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .<sup>13</sup> The PWBs had a special pattern to test surface-mounted 24-, 48-, 64-, and 100-pin LCCs. Three laminate compositions were used in the testing: (1) epoxy-glass, (2) polyimide glass, and (3) polyimide-quartz. Joint cracking was found to be a function of the difference in thermal coefficient of expansion of the laminate, size of the mounted components, and the time and temperature range of the cycling.

**Table 1. Substrate Materials**

	Source	X-Y TCE (ppm)	Z TCE (ppm)
Epoxy-Kevlar (EK)	Howe	6 to 8*	39 to 59
Polyimide-Kevlar (PK)	Howe	5 to 8*	74
Polyimide-Quartz (PQ)	Howe	6 to 12*	32 to 39
Epoxy-Glass, Copper/Invar/Copper (EG/CIC)	Oak Laminate	7 to 8*	63
Polyimide-Glass, Copper/Invar/Copper (PG/CIC)	Oak Laminate	6 to 12*	40
Al <sub>2</sub> O <sub>3</sub>		6.0 to 6.4	6.0 to 6.4
Epoxy-Glass	Synthane-Taylor	14 to 18*	56 to 59
Polyimide-Glass	MICA	12 to 17*	58 to 70
Copper	—	17 to 18	17.3
Sn/Pb Solder	—	22 to 25	22 to 25
Copper/Invar/Copper	—	3 to 6	

\*Depends on percent of constituents in composite.

The test board shown in Figure 1 contained 4 signal layers and 2 dummy metal layers. Land patterns consisted of one 24-pin, one 48-pin, two 64-pin, and one 100-pin LCC per side, along with two edge-clip leaded 2×2-in. alumina substrates to simulate a mother board. Continuity loops were formed with land patterns on the test LCCs and the PWB using a daisy-chain arrangement. The interconnecting loops on the PWB were either on the surface or to the inner layers through via-holes. The interconnections on the LCCs were made using 1-mil gold-wire bonds. A 60-Sn/40-Pb solder was screen-printed onto the PWB before vapor-phase soldering. Measurements indicated the solder thickness to be <5 mils. The soldering procedure will be detailed in a separate report by J. F. Dal Porto.

The thermal cycles used in this phase were from -55°C to 75°C for 100 cycles, followed by 200 cycles from -55°C to 105°C. The boards had 1 hr dwell at each temperature and 1 hr for each transition.

The ability of the solder joints to withstand thermal fatigue was measured by their change in electrical resistance during thermal cycling. To keep the data channels to a reasonable level, groups of components were connected in series on each board, that is, Channel 1 consisted of two 24-pin and two 48-pin LCCs in series, Channel 2 had four 64-pin LCCs, Channel 3 the two 100-pin LCCs, and Channel 4 the two, leaded alumina squares.

The first boards fabricated and mounted with components showed some defects. This was not unexpected as there were some new processing steps which had to be worked out, especially those relating to the vapor-phase soldering of the components to the PWB. Boards typical of the production processing, that is, without special treatment, were used in the evaluation. Defects and their location before cycling are shown in Table 2.

Misoriented components were reworked, and those components with open circuits were wired out of the continuity loops. A trend relating defects to a particular side or to a hole or surface interconnection was not apparent. The circuits which had opened after temperature cycling are indicated in Table 3.

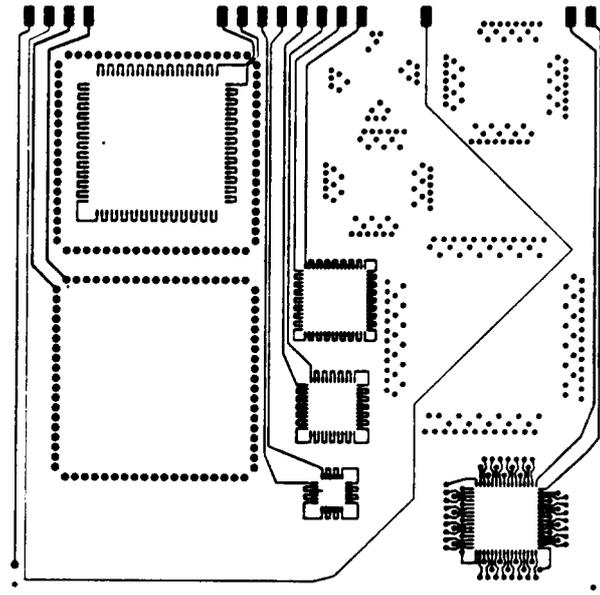


Figure 1 (Side A)

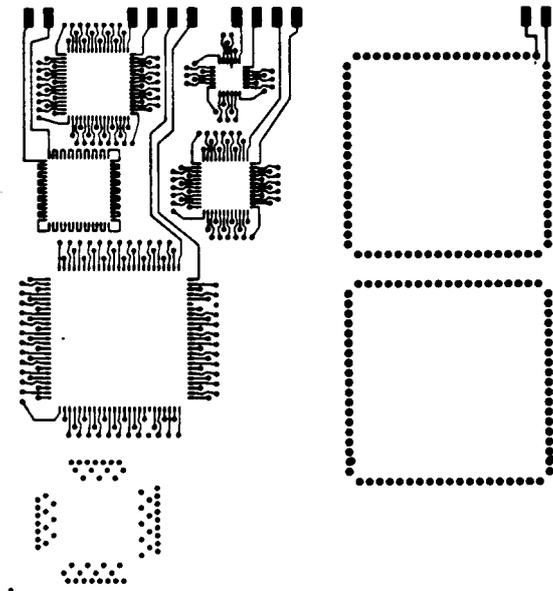


Figure 1 (Side B)

Figure 1. Test Board

**Table 2. Initial Open Circuits Which Were Eliminated Before Thermal Cycling**

Board No.	Type Laminate	Pin Outs Per LCC			Leaded $Al_2O_3$	Comments
		24 + 48	64	100		
1	PQ	A-S	A-S	—	—	Board Warped Cracked Joint
2	PQ	—	—	F-H	—	
3	PQ	—	F-S	—	—	Board Warped Solder Flux Residues
4	PQ	—	A-H	A-S/F-H	—	
11	PG	—	—	F-H	A	
33	PG	—	A-H	—	F	
44	EG	—	F-S	A-S	—	
22	EG	—	—	A-S	A	

A = Side A (top)  
 E = Epoxy  
 F = Side F (bottom)  
 G = Glass

H = Hole Interconnection  
 P = Polyimide  
 Q = Quartz  
 S = Surface Interconnection

Average thickness  
 EG = 0.0415 in.  
 PG = 0.0425 in.  
 PQ = 0.0445 in.

**Table 3. Circuits Defective per No. of Circuits Tested for Each LCC Pin Size After 100 Cycles of  $-55^{\circ}\text{C}$  to  $75^{\circ}\text{C}$  and 200 Cycles of  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$**

Board No.	Laminate Type	LCCs per Board				Leaded (2)
		2/24	2/48	4/64	2/100	
1	PQ	0/2	0/1	0/3	0/2	0/2
2	PQ	0/2	0/2	1/4	1/1	0/2
3	PQ	0/2	0/2	0/3	2/2	0/2
4	PQ	0/2	0/2	0/3	0/0	0/2
11	PG	0/2	2/2	4/4	1/1	0/1
33	PG	0/2	2/2	3/3	2/2	1/1
44	EG	0/2	2/2	3/3	1/1	1/2
22	EG	0/2	2/2	4/4	1/1	0/1

**Summary:**

Number of Boards

4	PQ	0/8	0/7	1/13	3/5	0/8
2	PG	0/4	4/4	7/7	3/3	1/2
	EG	0/4	4/4	7/7	2/2	1/3

E = Epoxy  
 G = Glass  
 P = Polyimide  
 Q = Quartz

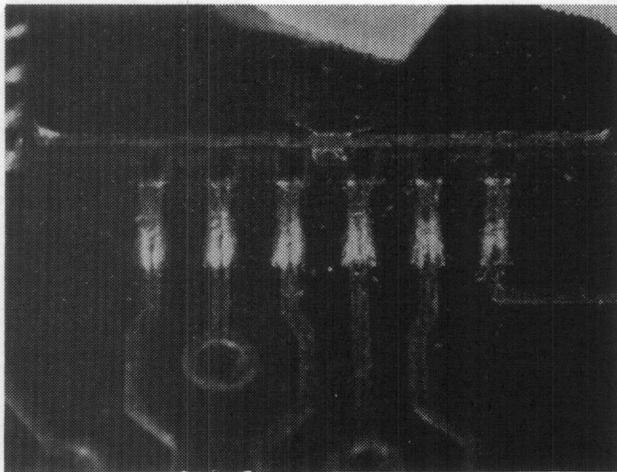
NOTE: There were no failures after 100 cycles of  $-55^{\circ}\text{C}$  to  $75^{\circ}\text{C}$  for 24- or 48-pin LCC or with any PQ laminate.

## Discussion

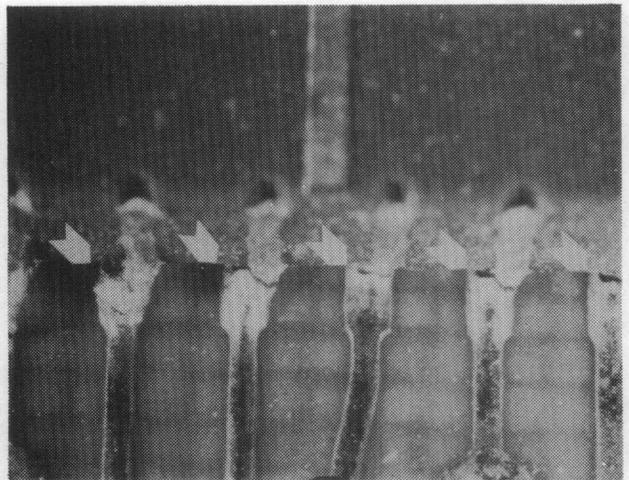
The  $-55^{\circ}\text{C}$  to  $75^{\circ}\text{C}$  test showed no failures for the 24- and 48-pin LCCs on any of the board types, and no failures of any of the chip carriers on the polyimide-quartz boards as a result of the cycling. The  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  cycling showed opens in the 64- and 100-pin LCCs on all of the substrate types. The opens in the higher-pin LCCs on polyimide and epoxy-glass boards were not unexpected because of the large mismatch in TCE. LCC failures were related to cracked solder joints. No correlation was apparent to particular location of the LCC on the board.

## Failure Analysis

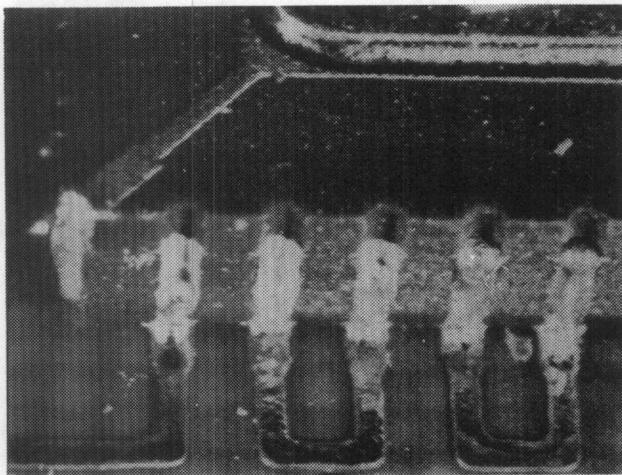
Figure 2 shows typical uncracked solder joints and Figure 3 shows badly cracked solder joints. LCCs showing electrical opens usually had multiple solder-joint cracking along one or more of the edges. Figure 4 shows misorientation of a 64-pin LCC on the board which contributed to its failure. The presence of a fat solder joint next to a starved joint as shown in Figure 5 was observed on several LCCs. The fat joint, which was located near the corner of the LCC where it should have received the highest stress, was not cracked, while the adjacent joints were badly cracked. The cross-section in Figure 6 shows the crack path through the solder of a failed joint.



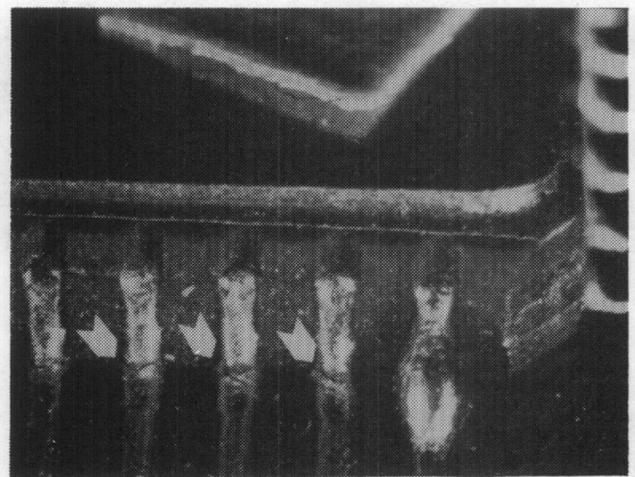
**Figure 2.** Noncracked Solder Joints on 24-Pin LCC



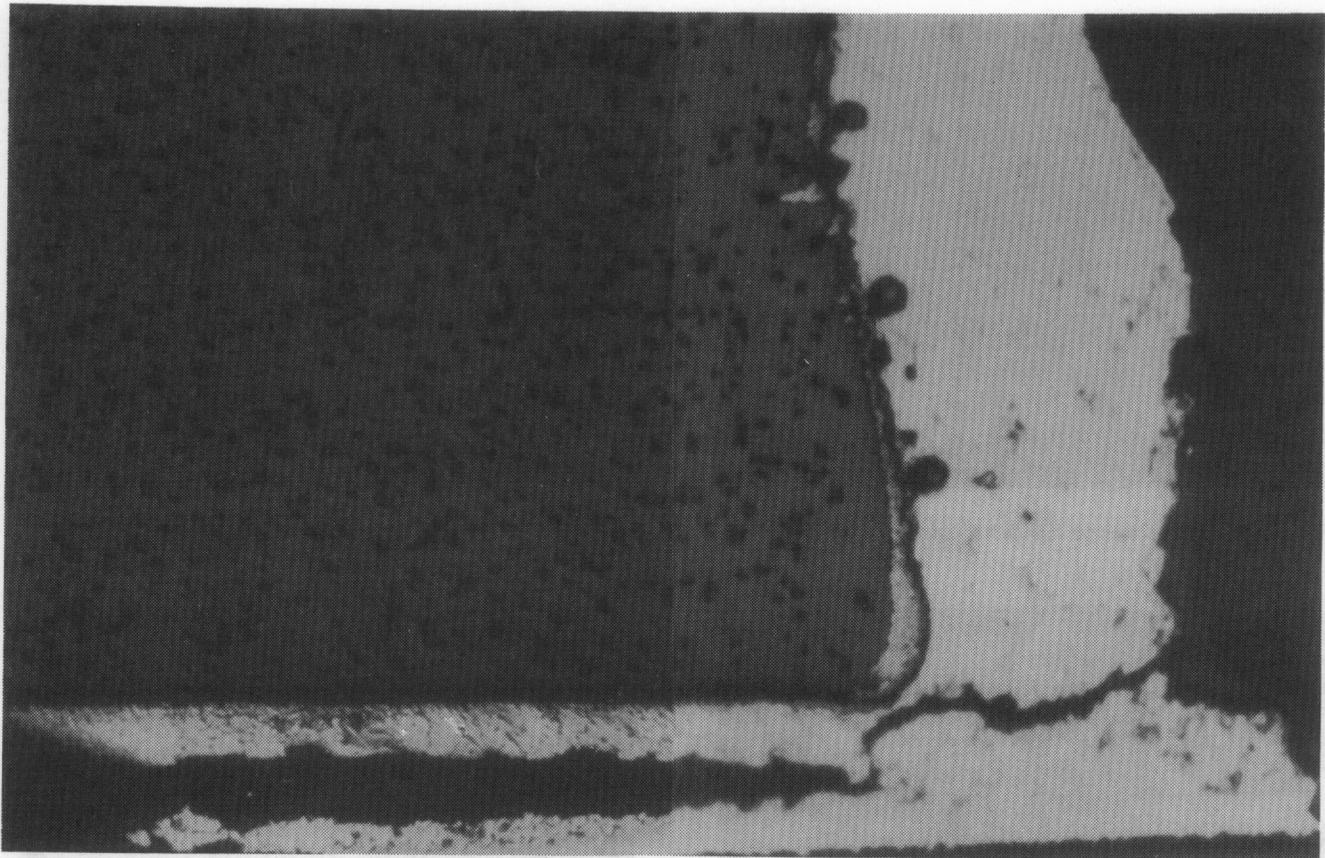
**Figure 3.** Cracked Solder Joints on 100-Pin LCC



**Figure 4.** Misorientation of 64-Pin LCC



**Figure 5.** Fat and Starved Solder Joints on 48-Pin LCC



**Figure 6.** Crack Path Across One of the 48-Pin Solder Joints

Optical examination of the pads on the LCC and laminate revealed voids in the solder, some extending to the interface. Examples of voids are shown in Figures 7 and 8. The deleterious effect of voids on the incidence of solder-joint failure has been reported.<sup>14</sup>

The first phase of this study indicated that some additional development work was needed to improve the orientation and placement of LCCs. Self-orientation through surface-tension forces in the solder has been reported for smaller-pin LCCs, but was of limited value for higher-pin LCCs. This was also observed in this investigation. Techniques are needed to increase the height of the solder column between the LCC and board lands, which should be beneficial to longer joint life in thermal cycling.

## Phase II

Other laminate systems that more nearly match the X-Y TCE of the LCCs were tested in Phase II. The testing procedure was similar to Phase I. The same test pattern was used with the same components

mounted on boards but with different laminate compositions. These compositions were epoxy-Kevlar, polyimide-Kevlar, polyimide-quartz, epoxy-glass with CIC, and polyimide-glass with CIC inner layers. They were commercially available and designed to match the X-Y TCE of the alumina substrates through the thermal expansion restraining effect of the Kevlar fibers, quartz fibers, and CIC layers. The TCEs of the laminate compositions are given in Table 1. In the Z direction, the TCEs of the laminates are in the 50- to 60-ppm range except for the polyimide-quartz, which is  $\sim 36$  ppm. Although these laminates give superior X-Y properties, their high Z expansion can cause difficulties with plated through-holes (PTH). The variations in TCE can be attributed to different polymer to fiber ratios and different measurement equipment.

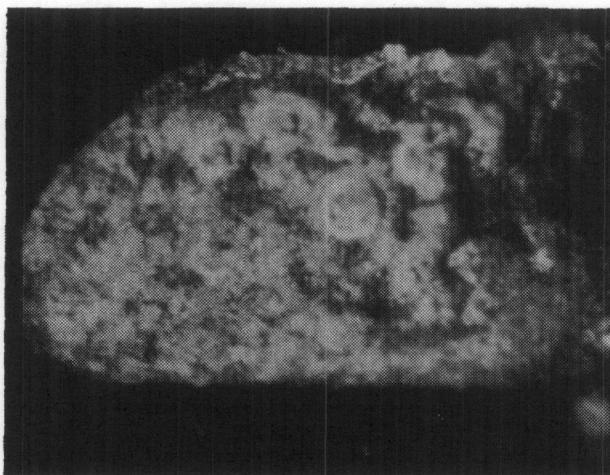
The temperature ranges for thermal cycling in this phase were extended to  $-65^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ , again with 1 hr at each limit and 1-hr transition.

Ten-mil-thick spacers were used to provide a more reproducible standoff of the LCC from the board. Circuit resistance was measured during each

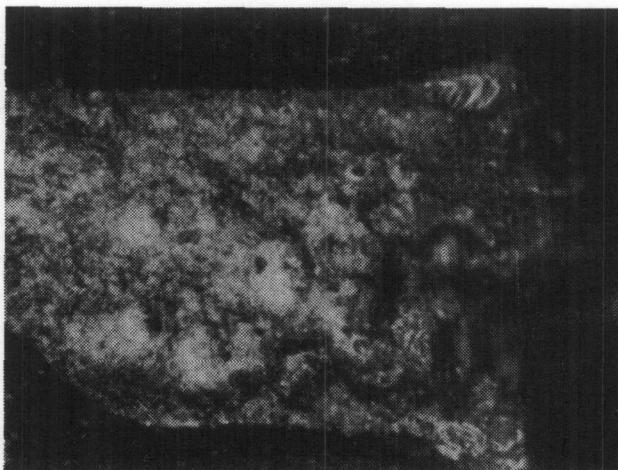
cycle after the boards were at 125°C for 45 min. Measurements were also made at 25°C before and after 100 cycles. Table 4 gives the initial circuit resistances at 125°C and Table 5 gives the percent changes in resistance after 100 cycles.

Failure was indicated by an open circuit or a large percentage change in resistance ( $>10\%$ ), or optically by the detection of cracks in the solder joints after 100 cycles. Defects such as misorientation of the LCCs to the pads on the board, shorting between pads, and joints with insufficient solder were either reworked or left as is and wired out of the circuit so the remainder of the LCCs could be monitored. The low resistances

for some of the 100-pin LCCs shown in Table 4 were the result of a 90-degree rotation of the LCC, causing the entire daisy chain of joints between the board and carrier to be shorted. Table 6 shows the types of defects found after cycling for 100 cycles. Included in this table are faults obtained by electrical pad-to-pad probing at 25°C. This was particularly needed for the misoriented 100-pin LCCs. Changes in electrical circuit resistance as a result of thermal cycling are not considered significant if they are  $\sim 1\%$ . This percent change could be caused by a 2.5°C temperature change in the copper conductors.



**Figure 7.** Voids in Solder Joint, on 64-Pin LCC Side



**Figure 8.** Voids in Solder Joint, on 64-Pin Laminate Side

**Table 4. Initial Circuit Resistances at 125°C in Ohms**

Board	Run	Component			
		2/24 + 2/48	4/64	2/100	2/Al <sub>2</sub> O <sub>3</sub>
EK-1	4	60.78	65.01	92.05	15.29
-2	3	23.89	95.65	3.20	0.49
-3	3	24.01	69.55	3.98	16.81
-4	-	-----Delaminated in Reflow Soldering-----			
PK-1	2	22.88	66.66	55.41	11.16
-2	2	21.00	200.3	41.42	17.13
-3	2	21.40	I-Open*	55.08	17.19
-4	3	22.11	65.28	3.68	10.23
-5	3	23.33	68.34	3.61	15.73
PQ-1	3	21.99	68.04	3.49	9.01
-2	3	22.45	67.08	3.36	19.18
-3	2	21.90	59.61	39.72	16.19
-4	2	22.08	63.81	I-Open*	17.46
-5	3	21.47	65.15	3.06	17.22
EG/CIC-1	4	21.89	67.18	65.50	14.35
-2	1	24.06	67.70	49.22	10.64
-3	1	23.52	67.99	3.81	19.44
-4	1	22.96	66.66	3.02	18.91
-5	1	23.06	66.88	99.07	8.56
PG/CIC-0	4	16.33	56.72	73.93	13.35
-1	4	21.61	52.66	77.12	13.42
-2	4	22.48	58.25	72.47	13.62
-3	4	21.71	59.14	75.13	12.65

\*Initial open

**Table 5. Percent Change in Circuit Resistance at 125°C After 100 Cycles of -65°C to 125°C**

Board	Run	Component			
		2/24 + 2/48	4/64	2/100	2/Al <sub>2</sub> O <sub>3</sub>
EK-1	4	Open	Open (2) <sup>†</sup>	Open	103.0
-2	3	Open	Open (1) <sup>†</sup>	0.3	46.0
-3	3	1.2	7.0	0.3	Opens (2) <sup>†</sup>
-4	-	-----Delaminated in vapor phase soldering-----			
PK-1	2	0.2	-0.1	Open (1) <sup>†</sup>	-35.0
-2	2	0.0	24.0	0.0	2.0
-3	2	0.1	I-Open (1) <sup>*†</sup>	2.3	0.9
-4	3	0.2	0.2	0.1	3.9
-5	3	0.2	0.2	0.3	1.9
PQ-1	3	0.2	Open (1) <sup>†</sup>	0.2	0.6
-2	3	0.2	0.2	0.2	0.9
-3	2	0.0	0.0	0.0	0.2
-4	2	0.0	0.8	I-Open*	Open (1) <sup>†</sup>
-5	3	0.0	11.0	Open (1) <sup>†</sup>	0.7
EG/CIC-1	4	0.4	0.6	Open (1) <sup>†</sup>	8.9
-2	1	0.6	0.2	0.4	11.0
-3	1	0.6	0.5	1.0	7.1
-4	1	1.3	1.1	1.2	16.0
-5	1	0.1	0.3	0.4	16.0
PG/CIC-0	4	0.0	0.0	0.0	2.0
-1	4	0.1	0.5	0.1	1.4
-2	4	0.1	0.2	0.0	1.4
-3	4	0.1	0.2	0.0	1.2

\*Initial open

<sup>†</sup>Number of opens

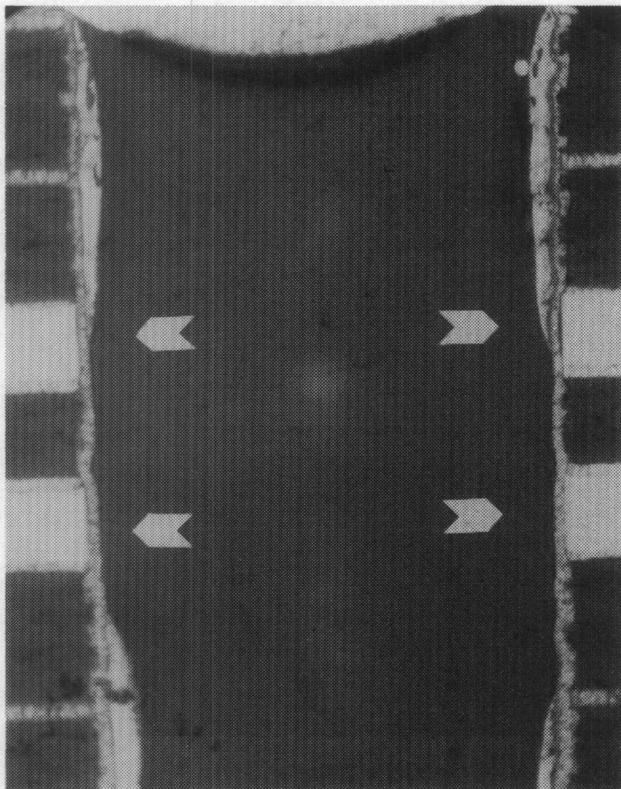
**Table 6. Electrical and Optical Observations at 25°C**

Board	Run	Component*				Notes
		2/24 + 2/48	4/64	2/100	2/Al <sub>2</sub> O <sub>3</sub>	
EK-1	4	OC	OC		RB	Delamination
-2	3	OC	OC,RB,RW	RB,MO	RB,IS	Poor (plated through-holes) PTHs
-3	3		RB	MO	RB,IS	Poor PTHs
-4	3					Delamination
PK-1	2	PB	MO	OC,PB,MO	IS,RW	Conductor missing
-2	2		RW	MO	IS	
-3	2		OC,IO,RW	MO		
-4	3			MO		
-5	3		CJ,RW,PB	CJ,PB,MO		
PQ-1	3		CJ	CJ,OC,MO	RW	
-2	3			CJ,MO		
-3	2	IS,PB	CJ,PB	MO		
-4	2		RW,PB,CJ	OC,RW,MO	RW	
-5	3		OC,RW,CJ,MO	OC,RW,CJ,MO	RW,CJ	Thin Cu plating
EG/CIC-1	4			OC,MO		
-2	1			MO		
-3	1			MO		
-4	1			MO		
-5	1			OC,CJ,MO	IS,OC	
PG/CIC-0	4					
-1	4		PB			
-2	4		RW			

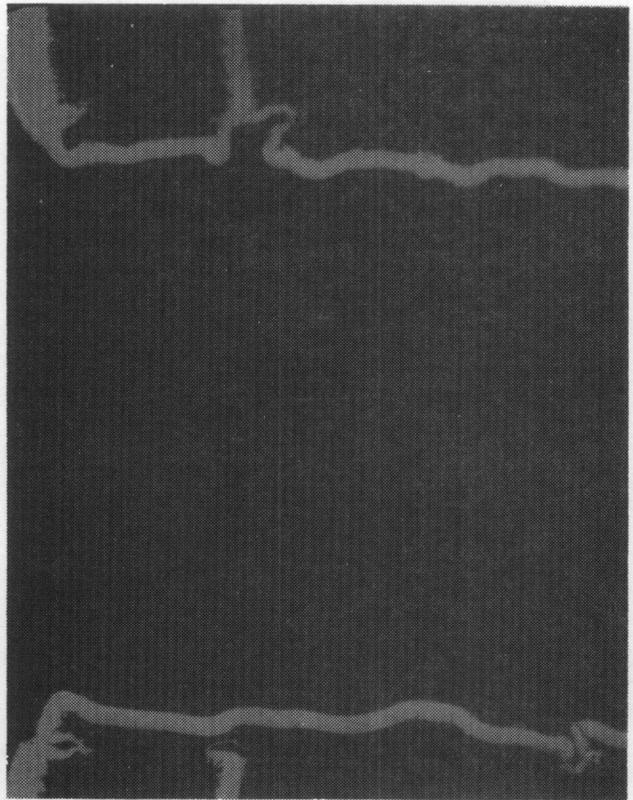
\*CJ = cracked joints  
 IO = initial open  
 IS = insufficient solder  
 MO = misorientation  
 OC = open seen optically  
 PB = pads bridged  
 RB = rough barrel wall in PTH  
 RW = rework

## Discussion

The polyimide-glass laminates with CIC-restraining layers (shown in Figure 9) had smaller circuit-resistance changes and no observable cracked solder joints. Next best were the epoxy-glass CIC boards. Laminates containing Kevlar fibers were not satisfactory in thermal cycling, however, they did not receive optimum processing in that there were problems in drilling uniform holes without fraying (Figure 10). Delamination was seen in two of the epoxy-Kevlar boards after vapor-phase soldering. The increase in faults with the polyimide-quartz laminates over that seen in Phase I could be attributed to the increase in the upper cycling temperature from 105°C to 125°C or from a difference in the quality of the processing given the boards in Phase II.



**Figure 9.** Copper/Invar/Copper Layers in Epoxy-Glass Laminate



**Figure 10.** Hole Wall of Epoxy-Kevlar Board

Again as in Phase I, defects were seen in the leaded alumina squares, some initially, and some after thermal cycling. There were PTHs containing the clip leads from the squares that did not appear to have sufficient solder.

Aside from the epoxy-Kevlar boards, there were no opens or cracked joints seen with the 24- or 48-pin LCCs. Few differences were evident in the percent changes between initial and final measurements made at 25°C and those at 125°C.

Some boards had solder bridges between pads, as seen in Figure 11. These bridges form from excessive solder flow in vapor-phase soldering. With this pattern they could be visually detected and removed with a soldering iron. As the space between LCCs decreases, visual detection becomes more difficult and x-ray inspection may be required.

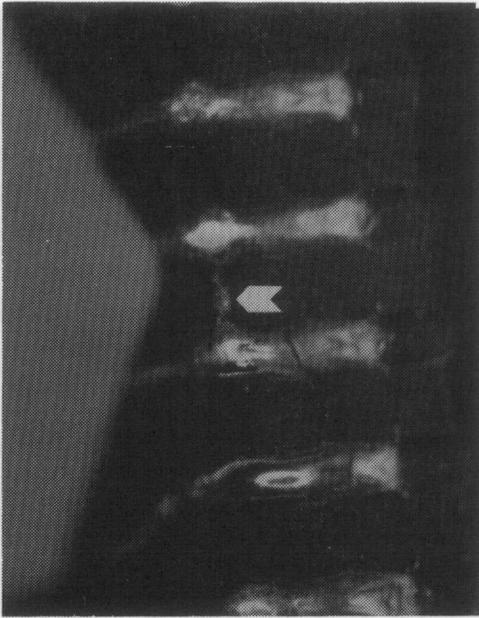


Figure 11. Short Between Pads on LCC

### Phase III

The capability of different types of SM components to withstand thermal cycling was investigated in this phase. The components (Table 7) consisted of resistors, resistor networks, capacitors, inductors, transistors, and diodes as well as LCCs. These were SM to PWBs with polyimide-quartz laminate. The test pattern was modified to accommodate these components by eliminating the alumina squares and the fine conductor line. Two 84-pin LCCs were substituted for the two less commonly used 100-pin LCCs. The components were hand-placed on solder-pasted pads on the PWBs and vapor-phase soldered. Ten-mil-thick spacers were used, as used in Phase II. Special care was taken to slowly preheat the boards in the vapor phase to avoid cracking of the large ceramic-chip capacitors, as this has been reported for soldering operations. A board with components is shown in Figure 12.

The testing for this phase consisted of cycling between  $-20^{\circ}\text{C}$  to  $80^{\circ}\text{C}$  for 100 cycles. Following optical and electrical examination, the boards were subjected to a  $-65^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  cycle for 500 cycles. During each of these cycles, the boards were held at the temperature limits for 15 min, with a transition time of 30 s. The  $-65^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  cycle is the same as called out for epoxy laminates in the thermal shock test in MIL-P-55110D and allows a comparison to the

results of other investigators. For both of the above cycles, circuit resistances were measured at room temperature after 10, 25, 50, and 100 cycles. For the higher temperature cycle, measurements were also made at 150, 200, 250, 300, 350, 400, 450, and 500 cycles. Each component was visually examined for evidence of cracked solder joints. Tables 8 and 9 show the number of cycles to open circuit.

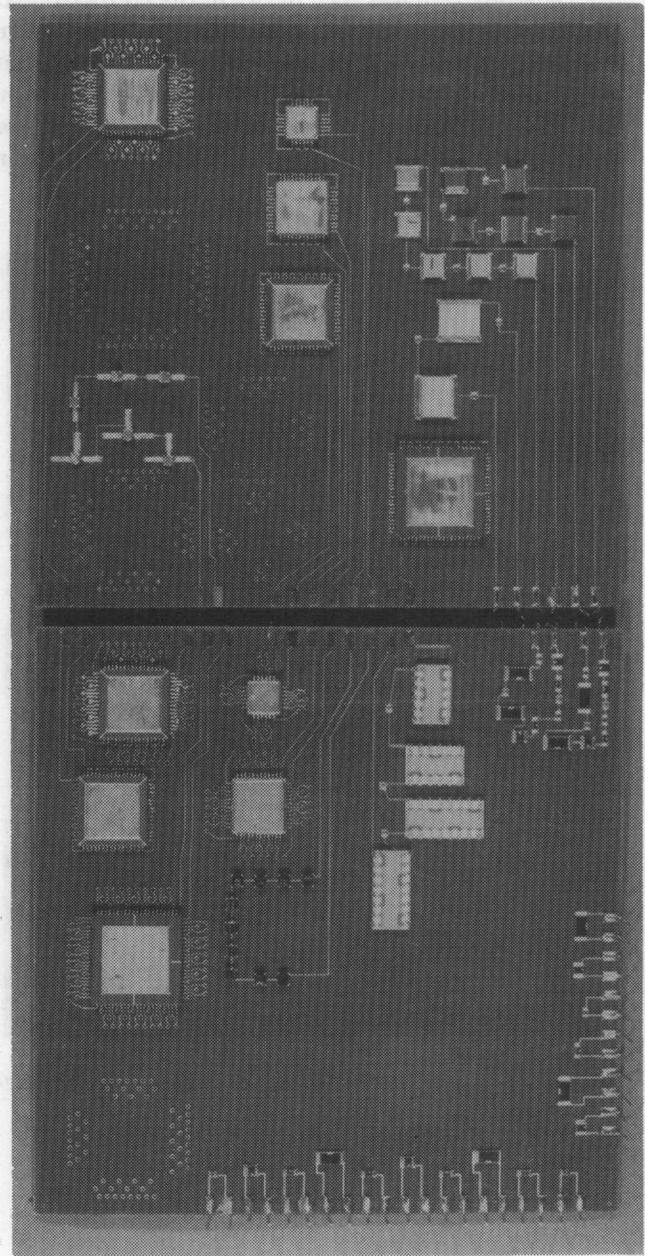


Figure 12. Board With Components

**Table 7. SM Components Tested in Thermal Cycling**

Source*	Designation	Size (in.) Length/Width/Thickness	End Cap
<b>Capacitors</b>			
A	Large NPO (0.05 $\mu$ F) SA2924-35	0.430/0.400/0.062	Pd-Ag/Cu/62 Sn-38 Pb
B	Small NPO (0.027 $\mu$ F) SA	0.250/0.225/0.085	Cu, Sn/Pb
C	Small XTR (1.0 $\mu$ F) SA2845-3	0.250/0.225/0.085	Cu, Sn/Pb
<b>Inductors</b>			
D	SA3490	0.105/0.105/0.064	Phosphor Bronze with Sn/Pb Coating & Mineral-Filled Epoxy
<b>Resistors, Individual and Network</b>			
E	1/8 W, SA3420	0.050/0.052/0.010	
	1/4 W, SA3421	0.110/0.052/0.015	
	1/2 W, SA3422	0.110/0.102/0.015	
	0.7 W, SA3423	0.254/0.1271/0.015	
<b>Ceramic Simulated Thick-Film Resistor Network</b>			
F		0.80/0.361, 0.60/0.361	
<b>Diode</b>			
G	SA3089		
<b>Transistor</b>			
H	SA3310	0.99/0.99	
<hr/> *A, B, C = US Microtech D = VanGuard Series 30,000 E = Dale, Series RCWM F = SNLA, Division 7411 G = Hewlett Packard MSD H = Texas Instruments LCCs = Kyocera			

**Table 8. Resistance Changes at 25°C for Indicated Number of Cycles Between -65°C and 125°C**

Board	24H	48H	64H	64S	84H	RNC	RN1	RN2	Inductor
1A	*	*	500 <sup>†</sup>	250 <sup>†</sup>	500 <sup>†</sup>	100 <sup>†</sup>	*	*	250 <sup>†</sup>
2A	*	*	*	*	†	300 <sup>†</sup>	*	*	*
3A	*	500 <sup>†</sup>	†	†	450 <sup>†</sup>	250 <sup>†</sup>	*	*	*
4A	*	*	*	350 <sup>†</sup>	*	*	*	*	*
5A	*	200 <sup>†</sup>	500 <sup>†</sup>	*	350 <sup>†</sup>	500 <sup>†</sup>	*	*	150 <sup>†</sup>
	24S	48S	64H	64S	84S	Transistor	Diodes	Individual Resistors	
1F	*	500 <sup>†</sup>	*	*	500 <sup>†</sup>	*	*		
2F	†	*	†	200 <sup>†</sup>	450 <sup>†</sup>	*	*		
3F	*	*	*	†	200 <sup>†</sup>	*	*	450 <sup>†</sup>	
4F	†	†	400 <sup>†</sup>	400 <sup>†</sup>	500 <sup>†</sup>	*	*		
5F	†	†	350 <sup>†</sup>	*	400 <sup>†</sup>	*	*	200 <sup>†</sup>	

H = hole (via) interconnection.

S = surface interconnection.

RNC = resistor network, ceramic.

RN = resistor network.

\* < 1% after 500 cycles.

† < 10% after 500 cycles

<sup>†</sup>Cycles to resistance change  $\geq 10\%$ .

**Table 9. Opens by Components Per Number Tested,  
–65°C to 125°C Cycling**

Components	Opens/Number Tested	Cycles to Open
24 H and S*	0/5	No opens
48 H	2/5	200, 500
48 S	1/5	500
64 H	4/10	500, 500, 350, 400
64 S	4/10	250, 350, 200, 400
84 H	3/5	350, 450, 500
84 S	5/5	200, 400, 450, 500, 500
Ceramic Simulated Resistor Networks 4 Networks/Circuit	4/20	100, 250, 300, 500
Resistor Circuit,-1	0/40	
Resistor Circuit,-2 8 Resistors/Circuit	0/40	
Inductor Circuit 10 Inductors/Circuit	2/50	150, 250
Individual Resistors 16/Board	2/80	200, 450

\*H = hole interconnection

S = surface interconnection

After thermal cycling, a twisting force was applied to the LCCs on the boards using a Snap-On-Tool torque meter. The force required to either shear through the solder or pull the pads from the laminate at the copper-epoxy interface or both, are given in Table 10. Of those joints which fractured in the solder, varying degrees of porosity in the solder were observed, similar to that shown in Figure 7.

In cutting test specimens from a board with a band saw, sufficient vibration was generated to cause all the pads on two of the 84-pin LCCs to fracture through the middle of the solder joints.

In the  $-20^{\circ}\text{C}$  to  $80^{\circ}\text{C}$  cycling no opens or cracked joints were evident after 100 cycles. The earliest failure in the  $-65^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  cycling was a simulated ceramic base thick-film resistor network at 100 cycles. The resistance changes in the remaining components were  $<10\%$  at 100 cycles as shown in Table 8. No opens or large resistance changes were seen for the two-resistor networks, the diodes, the transistors, or the 24-pin LCCs. Two opens occurred in the inductor networks. Two individual resistors, both 0.25 W, had cracks and were open at 200 and 450 cycles. No significant change was seen in the NPO capacitors, large or small. Two of the higher dielectric constant X7R capacitors had high-resistance paths measured after 150 cycles. The failure mode was internal to the component and not in the solder. The stress to failure was transmitted through the solder.

The greater resistance to cracking of the LCCs in this test could be the result of a shorter cycle, 30 min

versus 240 min, which reduced the time per cycle that the solder joints were subjected to fatigue. The boards were at  $125^{\circ}\text{C}$ , one-fourth as long as in the Phase II cycling. There was, however, a more abrupt transition for the cycling with the shorter dwell time.

A few measurements were made of changes in moisture content of the bare laminates from equilibration in 100% relative humidity at room temperature to a dry condition after a bake-out of 24 hr or more at  $100^{\circ}\text{C}$ . Changes in weight percent were:

Polyimide-Kevlar	3.8% to 4.0%
Polyimide-glass	1.6% to 1.8%
Polyimide-quartz	1.2%
Epoxy-Kevlar	2.0% to 2.2%
Epoxy-glass	0.8% to 1.0%

The sudden transformation of even a fraction of this moisture into steam is a potential source of board degradation as was seen in the delamination of the epoxy-Kevlar laminates during the vapor phase reflow process. If the above high-moisture laminates are used as a precautionary measure, the PWBs should be baked out at  $100^{\circ}\text{C}$  for no less than 16 hr before component assembly and soldering. Further work is underway at SNLA and BKC<sup>15</sup> to determine more specific bake-out conditions for boards equilibrated to different humidity environments. Board storage conditions to minimize reabsorption are also to be studied. Boards have been found to undergo dehydration during thermal cycle testing.

**Table 10. Torque Wrench Tests on Phase III Boards (in.-lb) After Thermal Cycling**

Board Number	24 Pin		48 Pin		64 Pin				84 Pin	
	HA*	SF*	HA	SF	HA	HF	SA	SF	HA	SF
1	10	—	25	20 <sup>†</sup>	31 <sup>†</sup>	70	40 <sup>†</sup>	15	—	—
3	20	17	27 <sup>†</sup>	60	47 <sup>†</sup>	48	50	30	72 <sup>†</sup>	11 <sup>†</sup>
4	17	32	13 <sup>†</sup>	41	46	5 <sup>†</sup>	26	15 <sup>†</sup>	>70	32 <sup>†</sup>
5	10	8	6 <sup>†</sup>	35	27 <sup>†</sup>	20 <sup>†</sup>	50	30	†	30 <sup>†</sup>

A = side A (top)  
 F = side F (bottom)  
 \*HA = hole interconnection  
 SF = side interconnection  
 †Joints fractured on bandsaw  
 ‡Open circuits or  $\Delta R/R > 0.1$

## Summary and Recommendations

SM test assemblies with different laminate compositions were thermal cycled to determine their resistance to testing and environmental thermal stresses. The assemblies had test circuits containing solder joints connecting LCCs and other ceramic components to PWB pads. Electrical and physical changes in the circuits were monitored after a specified number of cycles. The basis for evaluation was the degree to which solder joint cracking and open circuits occurred. Some of the evaluations are tentative as the number of assembly lots was limited, and the degree of control attained in placing and soldering of components was not as high as desired. Some uncertainty exists as to how much a change in solder joint integrity is attributed to assembly processing and how much to the laminate and component compositions. With these qualifications, the following test results, precautions, and recommendations are presented.

- Of the five different laminate compositions that were selected to more closely match the TCE of the ceramic components, circuits on polyimide-glass with CIC innerlayer had the smallest electrical resistance changes and no opens as a result of thermal cycling. The other laminates in order of increasing resistance changes are epoxy-glass with CIC, polyimide-quartz, polyimide-Kevlar, and epoxy-Kevlar. Although the polyimide-glass with CIC is the most promising laminate of those tested, further testing with improved assembly processing is recommended before this or any other laminate can be selected for general SM usage at SNL. Polyimide-quartz is already in use in SNL systems and should be included in future tests as the basis laminate.
- Thermal stress which causes solder-crack formation is a function of the difference in TCE between the PWB laminate and the ceramic component, the time and temperature of cycling, and the component size. The size effect is seen by comparing the smaller 24-pin LCCs which had no solder joint failures after 100 cycles between  $-55^{\circ}\text{C}$  and  $105^{\circ}\text{C}$ , and the larger 48-pin LCCs which had 100 % failures. Both were on epoxy-glass, the laminate with the highest TCE.
- Differences in circuit resistance were minimal between surface and via-hole interconnections, between the particular location of components on the board surface, and from the mismatch in TCE between the copper conductors and the board surface.
- In attaching LCCs to PWBs care needs to be exercised to control the quantity of solder in the joints, standoff height, and misorientation to prevent or minimize solder joint cracking.
- Cleaning and inspection procedures need to be established in assembly to assure the removal or prevention of solder residues and solder bridges between conductors.
- In view of the percent moisture absorption of these laminates, 1 to 4 wt. %, bake-out procedures need to be established to prevent damaging stresses from arising in the laminate from steam generated during thermal excursions.
- The formation of opens in circuits with resistors, capacitors, and inductors could not be clearly assigned to solder joint cracking. Future cycling tests will include unmounted parts along with parts mounted on assemblies, to determine the effect of mounting on open formation.
- Thermal shock testing,  $-65^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with a 30-min cycle needs to be correlated to the longer, 240-min test cycle and to the environment the assembly is expected to see in its end use. With small components, such as the 24-pin LCCs, the correlation is apparently not a problem as opens were not seen with any cycling condition.
- If a loss is evident in solder integrity from copper-tin intermetallic formation at the pad/solder interface during temperature cycling, more intermetallic should be seen for the cycle with 60-min dwell at  $125^{\circ}\text{C}$  than for the cycle with 15-min dwell. For an equivalent time at temperature, the 60-min dwell for 100 cycles should be comparable to the 15-min dwell for 400 cycles. There are, however, other important factors in the failure mechanism causing cracking, such as the solder-stress level and fatigue, shock from the sudden temperature change, and the associated temperature discontinuities.<sup>16,17</sup> Further tests are needed to sort out these effects on the solder joints during thermal cycling.

## Future Programs

Other than those studies for which a need has already been indicated, the following are proposed:

- Test other laminate compositions such as polyimide-glass CIC, with different component types.
- Test boards with components and foamed encapsulant.
- Investigate time and temperature for achieving specific moisture levels in the laminates.
- Compare boards with J-leaded devices with LCCs in their capability to withstand thermal cycling and other thermal testing.
- Examine the effect of copper intermetallic formation on the resistance of solder joints to thermal cycle stresses.

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