SANDIA REPORT
SAND86—2998 • UC—37
Unlimited Release
Printed August 1987

# TA489A Calibrator SANDUS

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Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550
for the United States Department of Energy
under Contract DE-AC04-76DP00789

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SF2900Q(8-81)

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Printed in the United States of America
Available from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

NTIS price codes
Printed copy: A03
Microfiche copy: A01

SAND86–2998
Unlimited Release
Printed August 1987

Distribution
Category UC–37

# TA489A Calibrator SANDUS

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## Abstract

The TA489A Calibrator, designed to operate in the MA164 Digital Data Acquisition System, is used to calibrate up to 128 analog-to-digital recording channels. The TA489A calibrates using a dc Voltage Source or any of several special calibration modes. Calibration schemes are stored in the TA489A memory and are initiated locally or remotely through a Command Link.

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# TA489A Calibrator SANDUS

# 1. General

This manual is intended for the use of individuals responsible for operating and maintaining the TA489A Calibrator.

Nine appendixes are included: Appendix A is a list of drawings for the TA489A; Appendix B is a list of DEC boards used with the TA489A; Appendix C is a list of the jumpers on the DEC board MXVII-1 used in the TA489A; Appendix D is a representation of the formatting of the status registers; Appendix E is a representation of the structuring of the TA489A digital memory; Appendix F presents the coding for the Calibration Step PROM; Appendix G lists the coding for the Step Response PROM; Appendix H presents the coding for the Calibration Sequence PROM; and Appendix I is a list of jumpers on the DEC board LSI-11/23 CPU.

## 1.1 System Definition

This manual contains the physical, functional, and programming information for the TA489A Calibrator, which forms part of the Common Equipment used in the MA164 Digital Data Acquisition System.*

The MA164 is capable of collecting data from up to 128 unique analog channels. Each input signal (dc to 10 MHz) has its own dedicated signal conditioner, amplifier, and data module. It can also collect data from up to 88 unique 8-bit digital channels. The entire system can be set up and controlled by either a local or a remote computer. Figure 1 shows the enclosure that contains the MA164 Digital Data Acquisition System. Figure 2 is a simplified diagram of the MA164 system. Figure 3, the rack layout, shows where the TA489A is located in the MA164 system.

A standard MA164 system contains all the equipment needed to set up and operate the Data Collection system. This includes the Data Collection elements, several elements referred to as Common Equipment, and the Setup and Playback Equipment.

The MA164 Digital Data Acquisition System is more commonly referred to as SANDUS (Sandia Digital Underground System). The TA489A is one element of SANDUS.

### 1.1.1 Data Collection Elements

The Data Collection elements comprise the source and translator couplers, signal conditioner/amplifier, data modules, and the crates. The signal conditioner/amplifiers provide for bridge completion, calibration, line termination, and amplification for analog signals. The data modules—up to 128 in the MA164—contain the presample filters, sample rate control, trigger controls, analog-to-digital converters, and the internal memory. The crates provide the Power and Decode commands, and interface the signal conditioner/amplifier and the data modules with the Common Equipment. Each crate can control up to eight signal conditioners or data modules. Analog data may be recorded in two ways: the signals may be digitized and output as real-time data to a remotely located recording facility or they may be stored in internal 16K memory for later readout and processing.

The MA164 also services up to 88 digital data channels of 8 bits each (704 bits). The data is output in the same manner as real-time data.

*J. M. Opalka, *SANDUS—MA164 Digital Data Acquisition System Specifications*, SAND83-2038 (Albuquerque, NM: Sandia National Laboratories, November 1983).

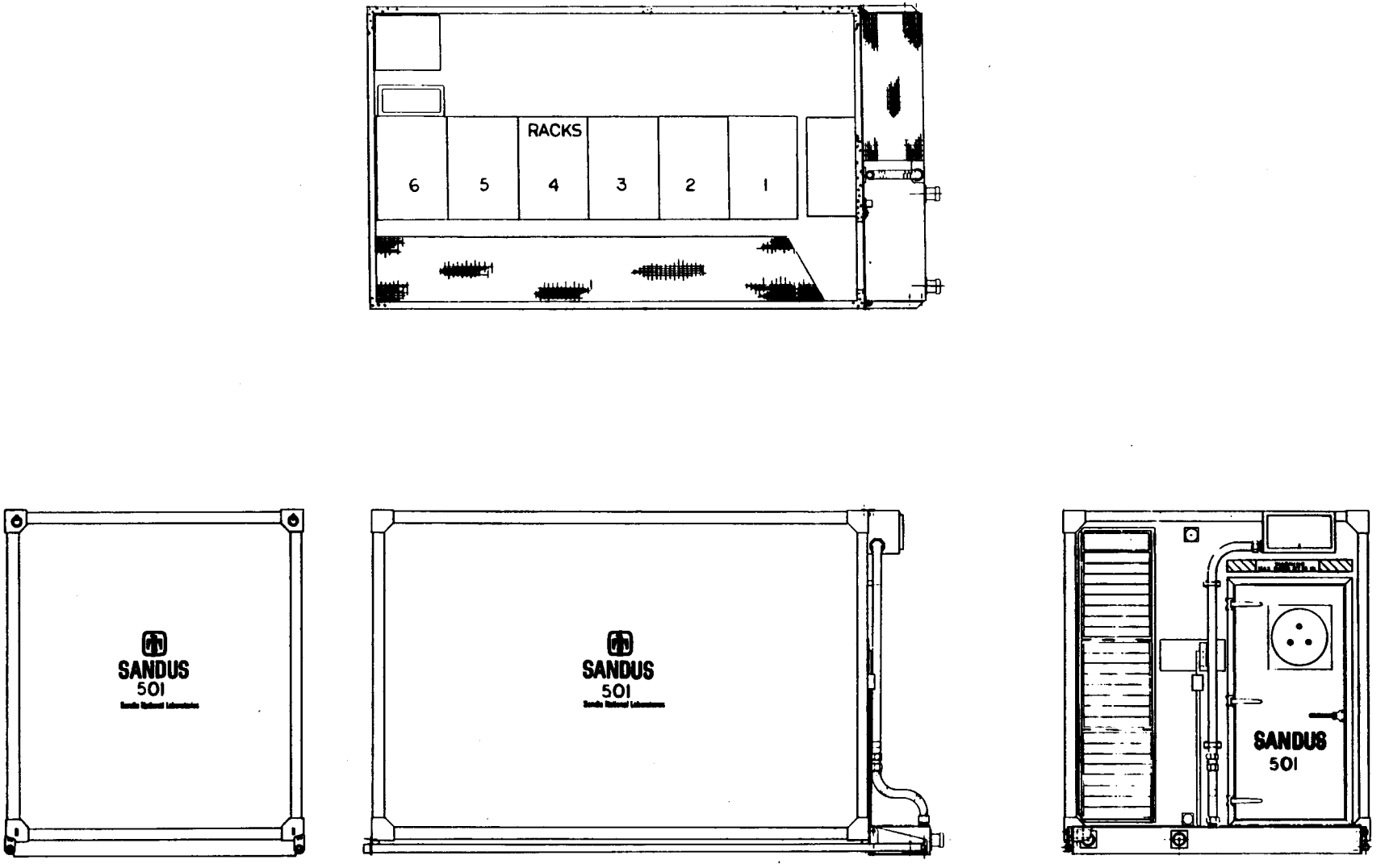


**Figure 1.** SANDUS

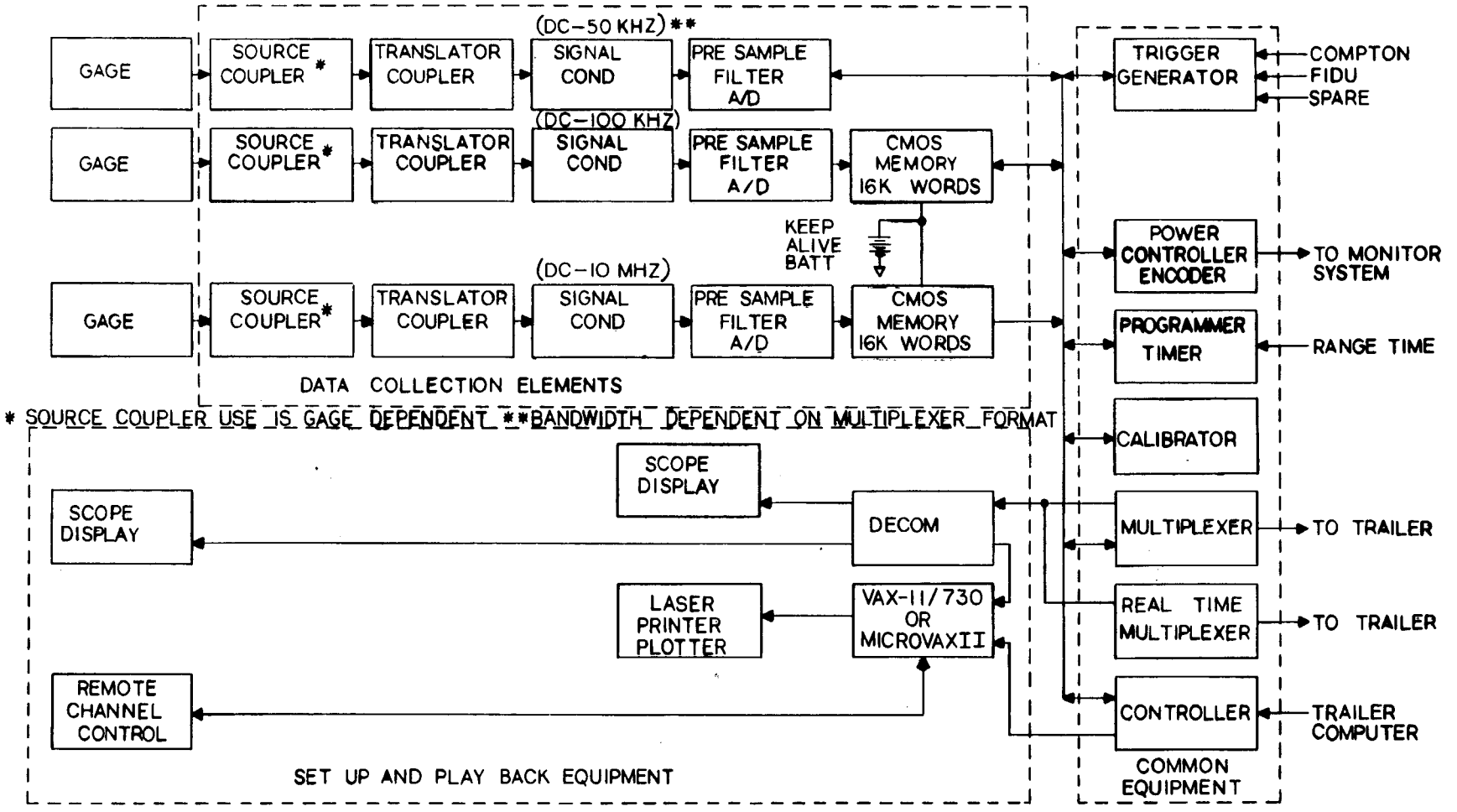


**Figure 2.** MA164 Block Diagram

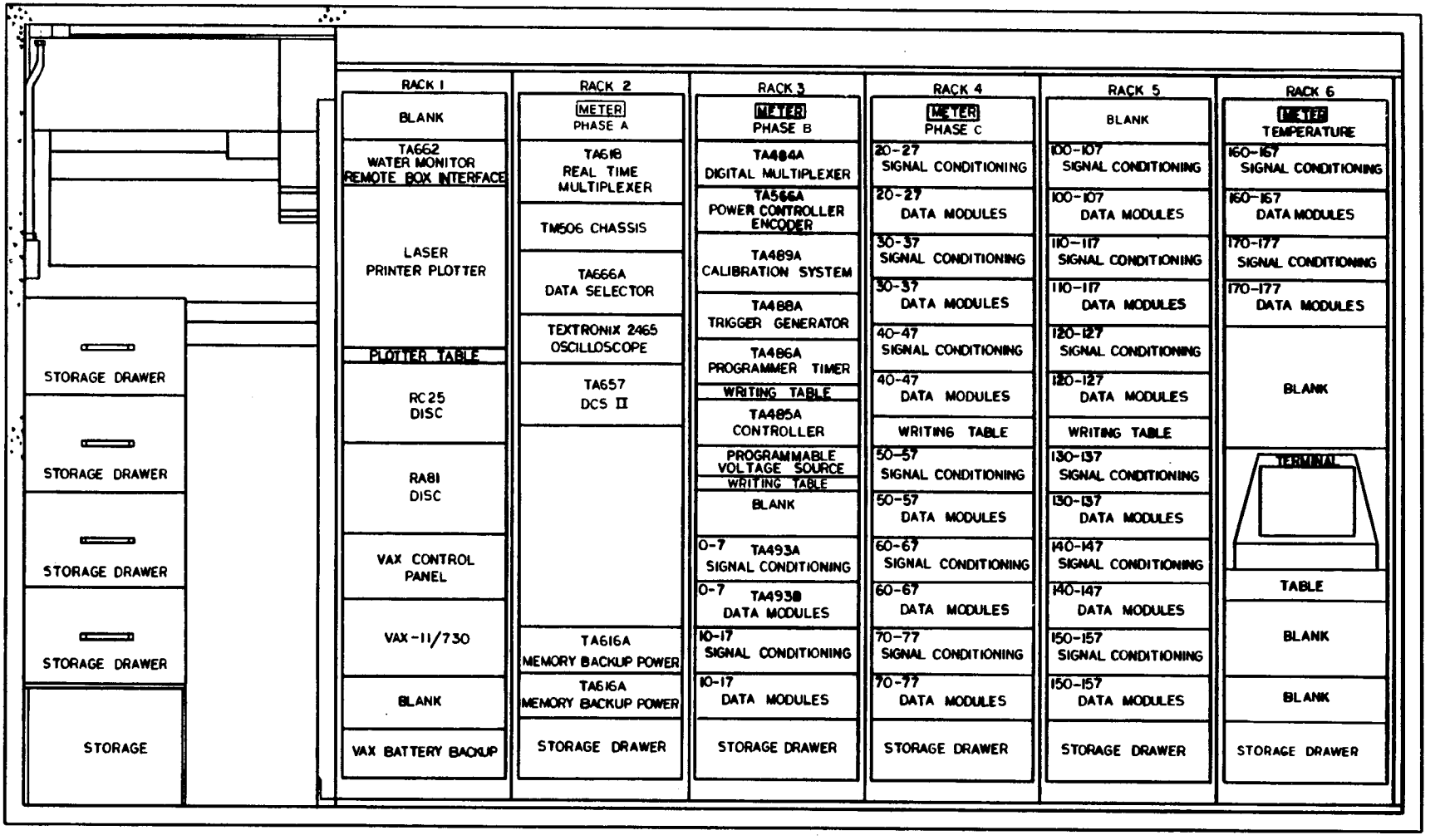


**Figure 3.** MA164 Rack Layout

### 1.1.2 Common Equipment Elements

The Common Equipment provides a means of operating the data system from remote locations as well as locally. The elements are the TA484A Multiplexer, TA485A Controller, TA486A Programmer/Timer, TA488B Trigger Generator, TA566A Power Controller/Encoder, and TA489A Calibrator. These elements initiate automatic countdowns, provide arms and triggers for data modules, calibrate systems, control system power, control setup parameters for each channel, and allow output of the digitized data to a remote location.

### 1.1.3 Setup and Playback Equipment

The computer provides a means to set up and test the individual channels. It also provides data playback and storage.

The test equipment provides communication and some of the calibration equipment. The TA666A Data Selector provides quick-look data displays for channel status.

## 1.2 Element Definition

The TA489A Calibrator provides internal calibration for the Data Collection channels of the MA164 Digital Data Acquisition System.

The Data Collection channels may be calibrated in any of four programmable memory blocks in the TA489A Calibrator.

# 2. Technical Description

## 2.1 Physical Description

The TA489A Calibrator is assembled in an all-metal chassis whose parts have been coated with conductive corrosion inhibitors. The chassis is 19 in. wide × 7 in. high × 26 in. deep and can be mounted on a standard rack (Figure 4). Removable top and bottom covers give access to its internal components. Chassis slides provide ready internal access and efficient installation, and make it easy to remove from equipment racks.

Two wire-wrap boards provide area for integrated circuits and input/output interfacing.

One +5-V power supply provides the operating voltage for the logic circuitry, the microprocessor elements, and the calibration relay matrix. A ±15-V modular power supply provides operating voltages for the FET switches used in the Step Response calibration mode. A +28-V power supply provides operating voltage for the calibration relays located witin the TA590 Signal Conditioner modules of the MA164 Digital Data Acquisition System.

A Digital Equipment Corporation (DEC) LSI 11/23 microprocessor monitors and generates all of the internal calibration functions in the TA489A (refer to Appendix B).

Two solid-state relays provide ac voltage control to the power supplies. The Calibration Relay matrix comprises three PC boards and two large can-type relays.

The front panel contains the local control switches, the indicator lights, and the visual displays. An Input Calibration Source connector is also available on the front panel. The input/output connectors, fan, and a power fuse are located on the rear panel.

## 2.2 Functional Description

The TA489A Calibrator provides means, both locally and remotely, for the Data Collection channels of the MA164 Digital Data Acquisition System to be calibrated. These calibrations serve as references for later data analysis.

Calibration parameters for the 128 individual recording channels of the MA164 Digital Data Acquisition System are stored in 8K of RAM memory in the TA489A Calibrator. This memory is divided into four sections: Block 0, Block 1, Block 2, and Block 3. For information concerning the reading and writing formats of the TA489A Calibrator, the reader is asked to refer to the MA164 Command System documentation, and to Appendix D.

Once a channel is calibrated, its data are stored in the digital memory of the channel calibrated.

Figure 5 shows a block diagram of the TA489A Calibrator.

## 2.3 Calibration Types

The TA489A can calibrate either locally or remotely.

Both general and special types of calibration are available. All are the result of a 4-bit PROM code in the TA489A and the calibration sequence of the TA489A. The PROM codes (called Cal Codes 0-3) are sent to the Amplifier/Signal Conditioners and the codes control relays at the Signal Conditioner. The relays allow data lines or attenuators or calibration lines to be applied to the Amplifier inputs.

The various types of calibrations performed by the TA489A Calibrator are defined by programming the TA489A memory for each individual channel in the MA164 Digital Data Acquisition System. Calibration type is dictated by bits 4 to 7 of sub-address 7. (Refer to Appendix E, the memory format, and to the MA164 command format.)

Figure 6 depicts the MA164 calibration flow.

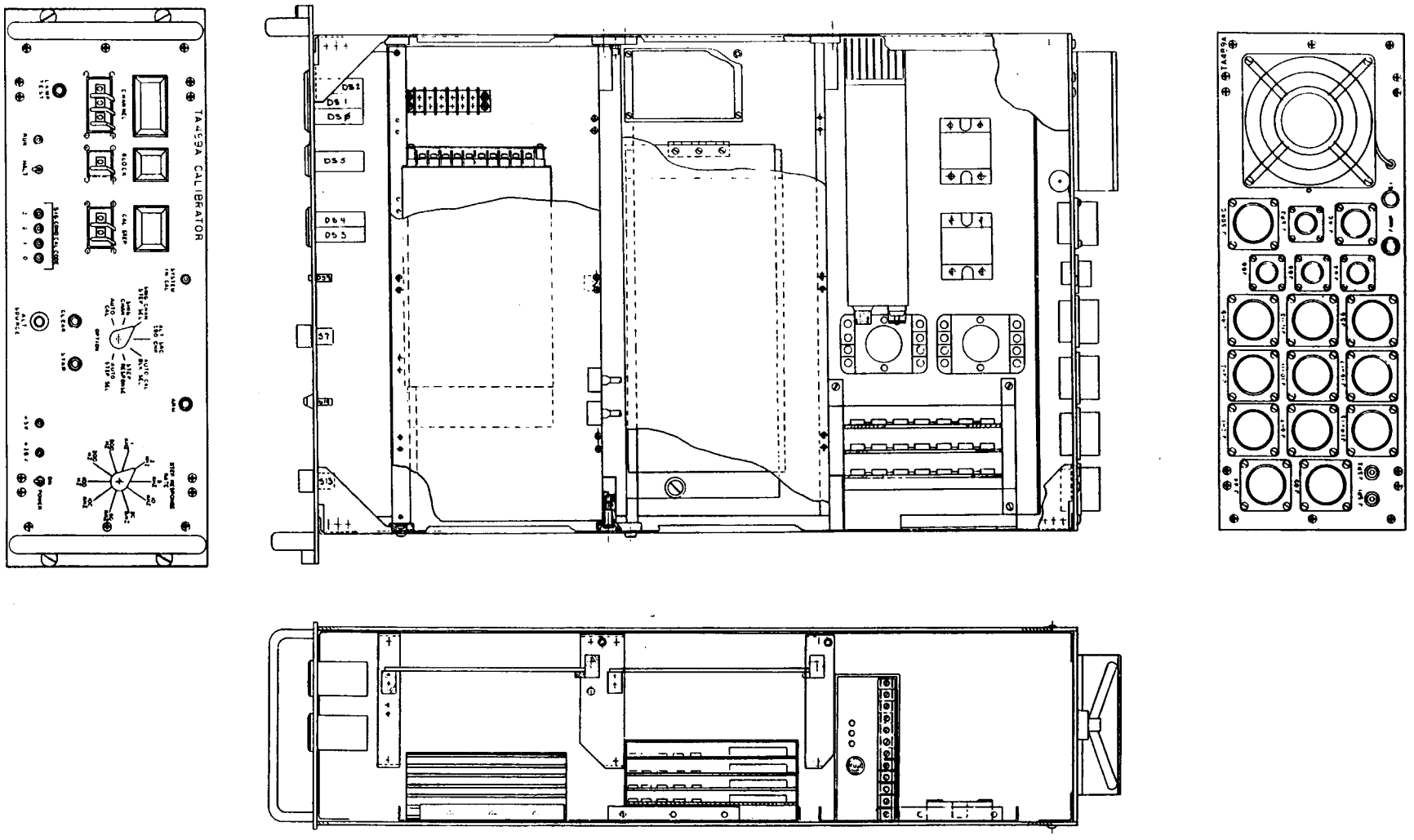


**Figure 4.** TA489A Calibrator

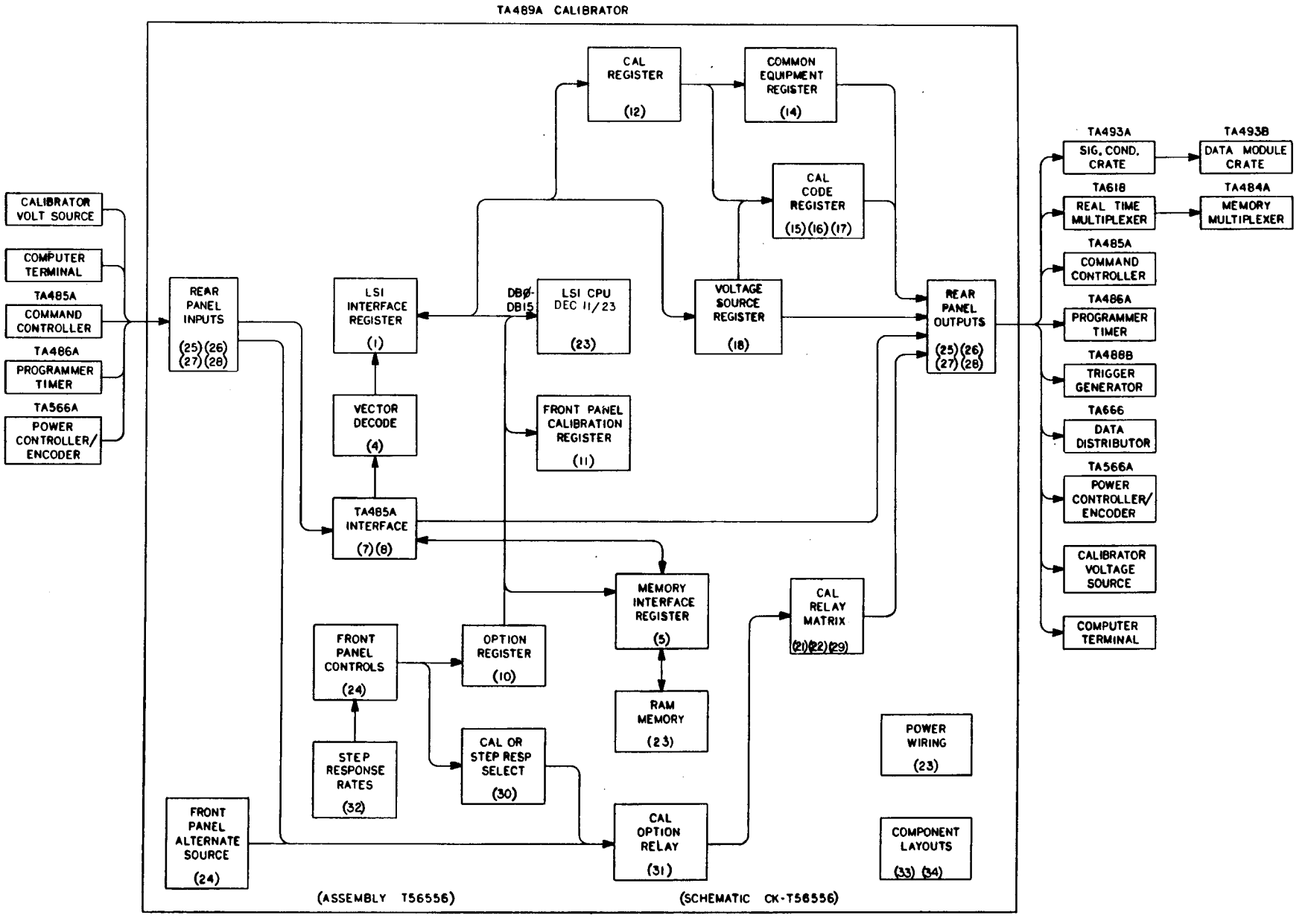


**Figure 5.** Block Diagram of TA489A

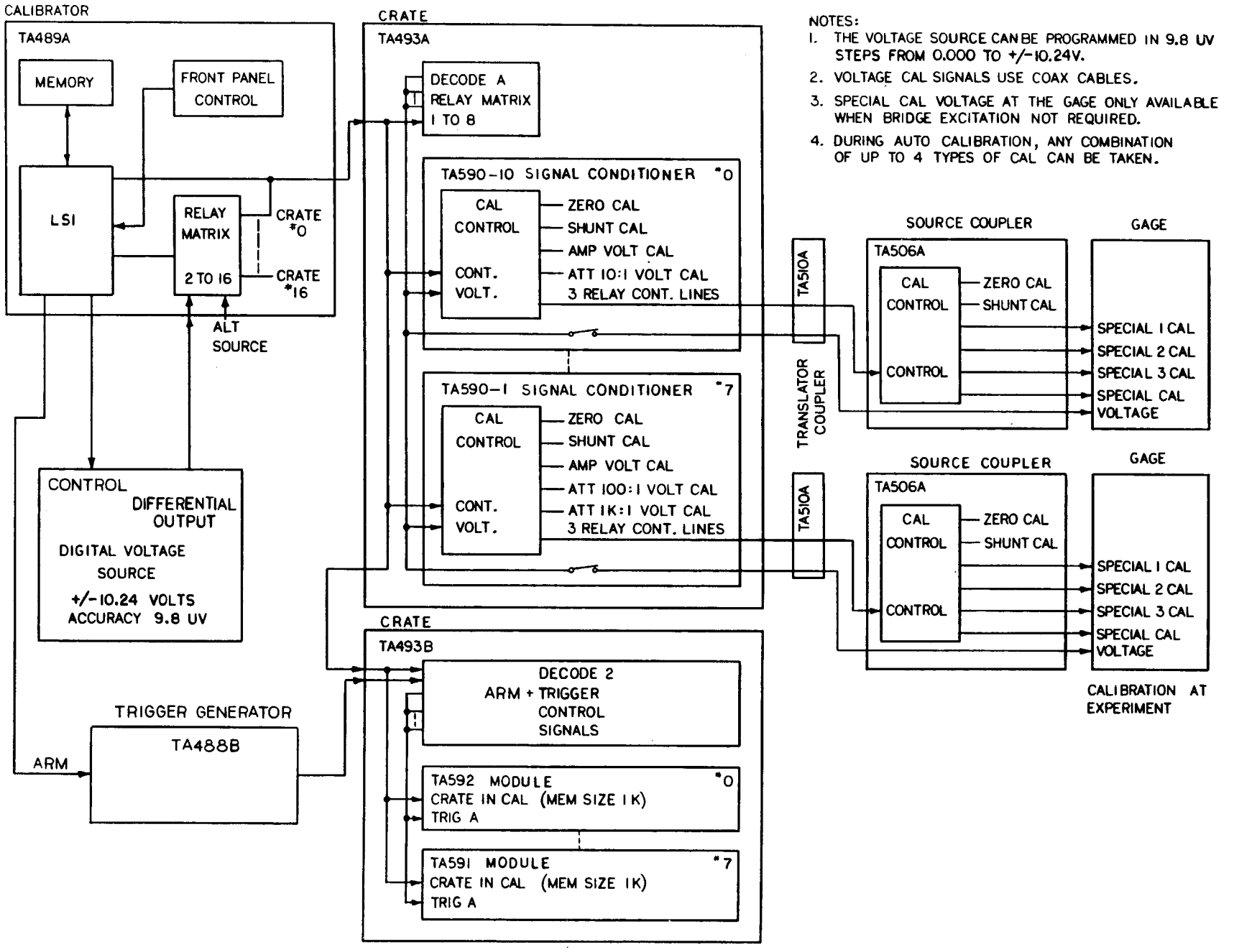


**Figure 6.** SANDUS (MA164) Calibration Flow

## 2.3.1 General Calibrations

### 2.3.1.1 Zero Cal (Cal Code 0000) (SK1)

This calibration removes the gage from the amplifier inputs and ties each input to ground by means of a resistor. This is accomplished by a relay in the Amplifier/Signal Conditioner controlled by the Cal Codes from the TA489A.

### 2.3.1.2 Shunt Cal (Cal Code 0001) (SK2)

This selection parallels one leg of a bridge with a known resistance. This is either accomplished at the Amplifier/Signal Conditioner or at the Source Coupler.

### 2.3.1.3 Step Cal (Cal Code 0010) (SK1 and SK3)

This selection applies a dc voltage from the Voltage Source through the Signal Conditioner to the Source Coupler excitation lines and controls a relay in the Source Coupler. That relay would then apply the dc voltage on the excitation lines and return on the data lines that provide the inputs to the Amplifier. This type of calibration is not considered very reliable if the signal is small because of the noise picked up from the long excitation and data lines. If this mode is selected, a toggle switch on the Amplifier/Signal Conditioner must be set to CAL. This type of calibration is a means of verifying continuity of the excitation and data lines.

### 2.3.1.4 (+) Internal Test (Cal Code 0011)

This function consists of removing the gage from the Amplifier inputs and applying a positive dc voltage to the inputs. The dc voltage is generated from within the Amplifier/Signal Conditioner module; the Amplifier Gain Code selects the level of voltage applied. This type of calibration may be performed by control from the TA489A, but it is not considered an accurate form of channel calibration.

### 2.3.1.5 (−) Internal Test (Cal Code 0100)

This calibration function is similar to that described in paragraph 2.3.1.4, except that a negative dc voltage is applied to the Amplifier inputs. The Amplifier then produces a corresponding negative output.

### 2.3.1.6 Amp Cal (1:1) (Cal Code 0101)

This calibration causes a precise dc voltage from the Voltage Source to be applied to the Amplifier input. The full value of the voltage programmed into the TA489A memory is applied to the Amplifier input, thus the 1:1 ratio. The input to the Amplifier is relay-controlled, determined by the Cal Codes from the TA489A.

### 2.3.1.7 Amp Cal (10:1) (Cal Code 0110)

This type of calibration functions the same as that described in paragraph 2.3.1.6, except that the dc voltage applied to the Amplifier inputs is first passed through a 10:1 attenuator. The attenuator is in the Signal Conditioner module and is selected by the Cal Codes from the TA489A. Only the TA590-10 Signal Conditioner has the 10:1 attenuator.

### 2.3.1.8 Amp Cal (100:1) (Cal Code 0111)

This calibration functions the same as that described in paragraph 2.3.1.6, except that the dc voltage applied to the Amplifier inputs is passed through a 100:1 attenuator. The attenuator is in the Signal Conditioner module and is selected by the Cal Codes from the TA489A. Only the TA590-1 Signal Conditioner has the 100:1 attenuator.

### 2.3.1.9 Amp Cal (1000:1) (Cal Code 1000)

This calibration functions the same as that described in paragraph 2.3.1.6, except that the dc voltage applied to the Amplifier inputs is passed through a 1000:1 attenuator. The attenuator is in the Signal Conditioner module and is selected by the Cal Codes from the TA489A. Only the TA590-1 Signal Conditioner has the 1000:1 attenuator.

### 2.3.1.10 Gage Cal (Cal Code 1111)

This calibration provides "real" channel reference. During this calibration, the Amplifier inputs are connected to the gage via the cable data lines. This calibration provides a realistic view of channel characteristics as influenced by external noise, offset parameters, induced voltages, etc. No voltage from the Voltage Source is applied to the Amplifier inputs.

## 2.3.2 Other Calibrations

The calibrations listed in Table 1 are available from the TA489A. These special calibrations are commanded by the same PROM that produces the Cal Codes for the General Calibration types described in section 2.3.1. The calibrations control relays K1, K2, and K3 in the Source Couplers, the interfaces to the gages and/or the Signal Conditioner. SK1, SK2 and SK3 mean Special K1, Special K2, and Special K3, respectively.

**Table 1. List of Special Calibrations**

| Relays | Cal Code |
|---|---|
| SK3 | 1001 |
| SK1, SK2 | 1010 |
| SK2, SK3 | 1011 |
| SK1, SK2, SK3 | 1100 |

## 2.3.3 Calibration Selections

Table 2 shows the TA489A memory blocks relative to the types of gages. This method of programming is not mandatory; the blocks may be programmed in any sequence desired, but the sequences shown in the table are historically the way the calibrations have been made.

**Table 2. TA489A Memory Blocks vs. Gages**

| | Type of Gage | | |
|---|---|---|---|
| Cal Block | Bridge | Voltage (Bipolar) | Voltage (Unipolar) |
| 0 | Zero Cal | Zero Cal | Zero Cal |
| 1 | Shunt Cal | +Step Cal | +Step Cal |
| 2 | Amp Cal | −Step Cal | +1/2 Step Cal |
| 3 | Gage Cal | Gage Cal | Gage Cal |

## 2.3.4 Inputs to TA489A Calibrator

### 2.3.4.1 Inputs From Voltage Source

The inputs to the TA489A Calibrator from the Voltage Source are made on two coaxial lines. The output of the Voltage Source is a differential voltage. Inputs are routed through a large relay and from there through the Calibration Relay matrix for proper routing to the crate selected for calibration. Most relay contacts are mercury-wetted to minimize voltage losses through the relays in the calibration lines.

### 2.3.4.2 Inputs From TA485A Controller

All inputs from the TA485A Controller to the TA489A Calibrator are negative true TTL levels using eight Command Data bits, four Function Code bits, four Sub-Address bits, one Power-On Reset line, and a 10-ms Strobe signal.

The Command Data bits, the Function Code bits, and the Sub-Address bits are used to read or write the TA489A memory through its Status Register. These bits also are used to begin or abort calibrations. The Strobe signal latches addresses, status bits, the Function Codes, the Sub-Addresses, and the Command Data bits. The Power-On Reset provides a clear-all to the TA489A logic for returning to the operational standby mode.

### 2.3.4.3 Inputs From TA566A Power Controller/Encoder

Only one signal line into the TA489A Calibrator is used from the TA566A Power Controller/Encoder. A positive true level is provided by the TA566A to enable a solid-state relay in the TA489A. This relay controls ac voltage to the TA489A power supplies.

### 2.3.4.4 Inputs From TA486A Programmer/Timer

All levels from the TA486A Programmer/Timer to the TA489A Calibrator are negative true TTL levels. Three signals are used: AUTO CAL, STOP CAL, and LOCKOUT. AUTO CAL begins the Automatic Calibration cycle; STOP CAL aborts the Calibration cycle; and LOCKOUT aborts the Calibration cycle if in progress and allows no more activity from the TA489A Calibrator until a system Power-On Reset is received via the TA485A Controller. The LOCKOUT signal also causes the +28-V power supply in the TA489A Calibrator to shut off for a predetermined time, usually ~18 s. At the end of this time, the +28 V is reinstated. This is done to ensure that the Amplifier/Signal Conditioner relays are in their relaxed state (data mode) at data collection time.

### 2.3.4.5 ac Input

The ac power input to the TA489A Calibrator is made up of one Hot line, one Neutral line, and one Ground line.

## 2.3.5 Outputs From the TA489A Calibrator

### 2.3.5.1 Outputs to Voltage Source

All outputs from the TA489A Calibrator to the Voltage Source are negative true TTL signals. Twenty value bits determine the level of the Voltage Source output, one bit determines the polarity of the output, and one bit swaps both lines of the differential output of the Voltage Source to the TA489A. This is done by a double-pole, double-throw relay in the Voltage Source.

#### 2.3.5.2 Outputs to TA485A Controller

Only one negative true TTL level output is used from the TA489A Calibrator to the TA485A Controller. It is called Cal Busy and is available to the TA485A register, but is not used by the firmware. This is a do-nothing signal.

#### 2.3.5.3 Outputs to TA484A Multiplexer

All outputs from TA489A Calibrator to the TA484A Multiplexer are negative true TTL levels. They include seven Channel Address bits, two Calibration Block bits, one System-In Cal bit, one Data Ready bit, and one Cal Stable bit. System-In Cal is asserted throughout the calibration cycle.

#### 2.3.5.4 Outputs to TA566A Power Controller/Encoder

All outputs from the TA489A Calibrator to the TA566A Power Controller/Encoder are negative true TTL levels, and include one SYSTEM-IN CAL signal and one POWER OK signal. Both signals are multiplexed into the health-monitor stream by the TA566A.

#### 2.3.5.5 Outputs to TA666A Data Selector

All outputs from the TA489A Calibrator to the TA666A Data Selector are negative true TTL levels, and include seven Channel Address bits and one Strobe. These are used to monitor the channel being calibrated.

#### 2.3.5.6 Outputs to TA488B Trigger Generator

All outputs from the TA489A Calibrator to the TA488B Trigger Generator are negative true TTL levels, and include one Trigger Inhibit Override bit and one Arm bit. The Trigger Inhibit Override bit disables the Inhibit bit in the TA488B and allows triggering of Memory Data modules during calibration; the Arm bit arms the data modules during calibration.

#### 2.3.5.7 Outputs to TA486A Programmer/Timer

All outputs from the TA489A Calibrator to the TA486A Programmer/Timer are negative true TTL levels, and include two Calibration Block bits, one System-In Cal bit, and one Outboard Calibration bit. These signals allow the TA486A to control special calibration equipment and/or experiments during calibration.

#### 2.3.5.8 Outputs to TA493A Crates

Most outputs from the TA489A Calibrator to the TA493A Signal Conditioner Crate are negative true TTL levels. They include four Cal Code bits, one Trigger Strobe bit, one Latch Strobe bit, three Cal Address bits, and one Crate-In Cal signal, ±Cal Sig from the Calibration Relay matrix, and an isolated voltage output from a +28-V power supply.

## 2.4 Calibration Sequences

### 2.4.1 Single-Channel Calibration

To calibrate a single channel, 16 steps are used in the calibration process. Each step is 10 ms long, for a total time of 160 ms.

The data module is armed at the beginning of the 16-step sequence via the TA488B Trigger Generator, which sends the ARM signal to the Data module via the TA493B Data Module Crate. The ARM signal is received at Decode 2 and routed to the proper channel within the TA493B.

At Step 6 in the sequence, a Trigger signal is sent to the Data module via the TA488B Trigger Generator in similar fashion as that described for the Arm signal.

The appropriate Cal Code from the calibration memory is sent to TA493A Signal Conditioner Crate for setup of the Signal Conditioner relays.

At the end of the 160-ms calibration period for the channel selected, the TA489A Calibrator returns to a Standby mode.

Figures 7 and 8 show the calibration cycles and sequence, respectively.

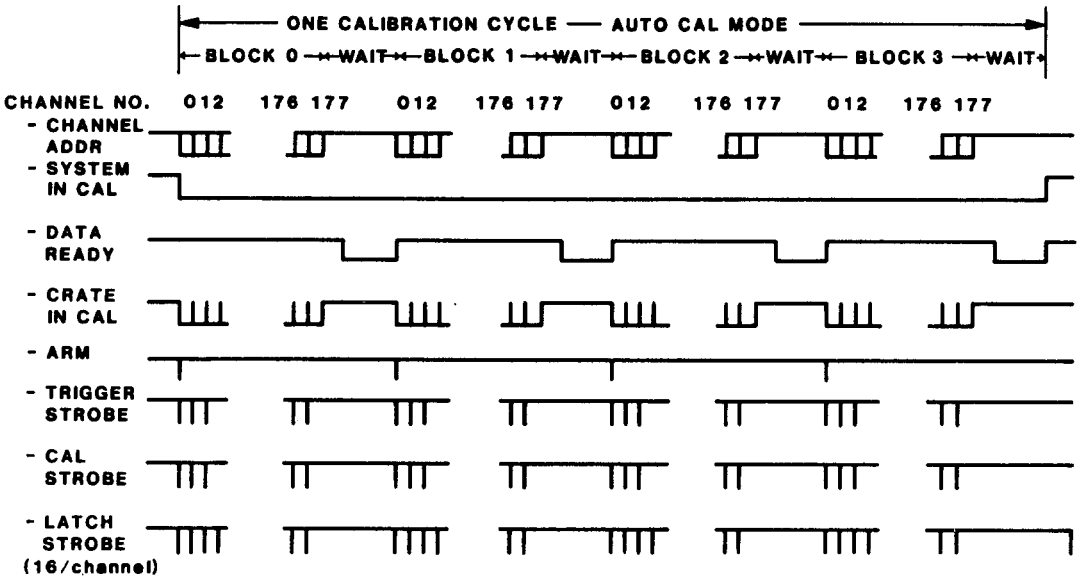


**Figure 7.** Calibration Timing

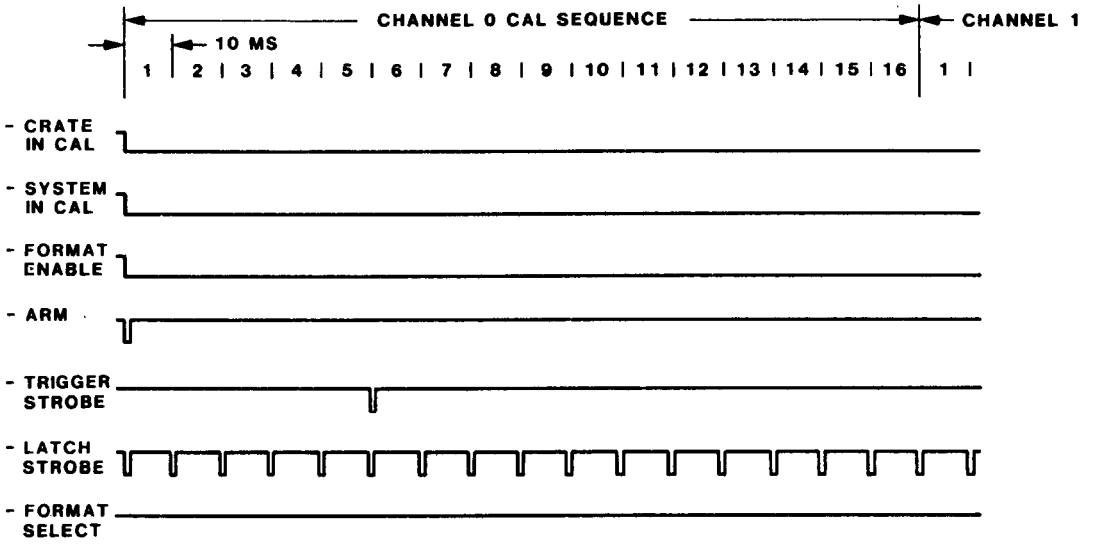


**Figure 8.** Calibration Sequence

## 2.4.2 Auto Calibration

In Auto Calibration, the time it takes to calibrate each channel is the same as described in paragraph 2.4.1. The difference is that all channels of the MA164 Digital Data Acquisition System will be calibrated. The sequence of that calibration process is described below:

1. Channels 0 through 177 (octal) are each sequentially subjected to a 160-ms calibration cycle using the information programmed into memory Block 0. Note that channels may be skipped by programming a "1" in sub-address 6, bit 7. Refer to Appendix E.
2. When calibration for Block 0 is completed, the TA489A goes into a Wait mode. This is a pause in the calibration process to allow the information from each channel memory to be read and transferred to a remote location for storage on tape. The TA484A Multiplexer reads, multiplexes, and sends the data to a remote trailer via a 20-Mbit data stream. If there are real-time channels, the TA618 Multiplexer is also used to transfer the data.
   The wait period is determined by the following process:
   A. If no channel was calibrated, the TA489A will proceed directly into the next block.
   B. If at least one channel was calibrated, Data Ready to the TA484A is set 410 ms after the final calibration step of the block in progress.
   C. Data Ready is set for 200 ms, multiplied by the number of channels that were calibrated.
   D. Data Ready is removed after Setp C and another wait period of 160 ms takes place before the TA489A begins the next calibration block.
3. At the end of the wait period, the TA489A Calibrator again goes into a calibration cycle (described in Step 1 above) but uses the memory information in Block 1. At the end of calibration for Block 1, the TA489A Calibrator returns to the Wait mode for Memory Data transfer.
4. The TA489A repeats the process described in Steps 1 and 2 for Blocks 2 and 3. At the end of the wait period for the Block 3 calibration, the TA489A reverts to a Standby mode.

## 2.4.3 Signals Asserted During Calibrations

These signals are given in Table 3. Refer also to Figures 7 and 8.

**Table 3. Signals Asserted During Calibration Cycles**

| Signal | Function |
|---|---|
| System-In Cal | Signals several elements in the MA164 that a calibration cycle is in progress. The signal is asserted throughout the entire calibration period. |
| Crate-In Cal | This signal is sent by the TA489A to the appropriate TA493A Crate during a calibration cycle. The signal is asserted for each channel; it is calibrated and the signal is dropped at the end of the 160-ms calibration cycle for that channel. |
| Arm | The signal is asserted at the beginning of the calibration cycle. This is considered a Broadside Arm to all Data Module memories. |
| Trigger Strobe | This signal is asserted to the Data Module memory 50 ms into the calibration cycle. It alerts the memory to store the calibration data. |
| Latch Strobe | This signal is asserted at the beginning of each channel calibration cycle so that it may latch in the address of the module to be calibrated. It is asserted 16 times during one channel calibration and is used at the respective TA493A Crate Decode Board. |

## 2.5 Calibration Options

The options described below may be initiated from the front panel of the TA489A Calibrator, or remotely via the command link through the TA485A Controller. All the options listed are engraved on the TA489A's front panel and may be initiated by pushing the START switch. The option may be cancelled by the operator by pushing the CLEAR switch. As already noted, the options may also be initiated or cancelled remotely.

When a CLEAR signal is received, the microprocessor allows calibration of the channel in progress to be completed before allowing the TA489A Calibrator to revert to a Standby mode.

### 2.5.1 Auto Cal

This mode of calibration causes all channels in the MA164 Digital Data Acquisition System to be calibrated in the same manner described in paragraph 2.4.2.

### 2.5.2 Single Channel

This mode of calibration performs exactly as described in paragraph 2.4.1.

### 2.5.3 Single-Channel Step Select

This calibration is similar to the Single-Channel Mode, except that it can be selected via the front panel or the command link. The calibration will stop at the step selected and wait until the calibration is cancelled by a CLEAR. The TA489A Calibrator will finish the channel calibration in progress and then revert to a Standby mode.

### 2.5.4 Alternate Source/TA590 Check

This calibration mode allows the operator to choose an external signal and apply it to the front panel connector, labeled ALT SRC, to verify channel function. When this mode is initiated, the TA489A moves to Step 7 of the calibration process and remains there until a CLEAR is received.

The signal applied at connector ALT SRC is routed through the TA489A Calibrator's relay matrix and is applied to the calibration lines going to the appropriate amplifier inputs for channel calibration.

This mode is useful in determining if a channel is functioning within the MA164 Digital Data Acquisition System (SANDUS), but a word of caution is in order. This is not a fool-proof verification of channel functioning. Since differential input lines to the amplifier are used, data would be displayed at the Data module even if one input to the amplifier were open or shorted to ground. Therefore, discretion and experience are determining factors in whether the channel is functioning properly.

When using this mode, the channel gain, filter, offsets, etc. must be taken into account. The signal level applied should also be considered.

### 2.5.5 Auto Cal/Block Select

This mode of calibration is similar to Auto Cal described in paragraph 2.5.1, except that a Calibration Memory block must be selected by the operator via the front panel or the command link. When initiated, this mode will then calibrate channels 0 through 177 (octal) sequentially, using only the calibration information stored in the memory block selected. At the end of the calibration sequence, the TA489A will revert to a Standby mode.

### 2.5.6 Step Response

This mode allows the operator to apply a square wave to the inputs of the amplifier for calibration. This square wave is generated by the TA489A Calibrator by two methods:

1. If the Step Response mode is selected from the front panel, the square wave is generated from the output of the precision dc Voltage Source being applied through two FET switches that chop the dc voltage at a rate selected by the operator. The resulting square wave is applied across the calibration lines so that it may be routed to the amplifier inputs through the Calibration Relay matrix. The algorithm that determines the dc voltage to be applied to the FET switches is described in paragraph 2.5.6.1.

2. If the Step Response mode is selected remotely from the command link, the square wave is generated from two 30-Ω transmission line drivers, which are switching at a rate selected by the operator through the command link. The algorithm that determines the input to the calibration lines is described in paragraph 2.5.6.2.

The operator selects the frequency at which the dc voltage is chopped, and can choose from 15 rates if the mode is selected remotely via the command link, but only 10 rates can be selected from the front panel. Refer to Appendix D.

#### 2.5.6.1 Step Response Algorithm/Front Panel Selection

If Step Response is selected from the front panel, the Cal Code determines which of the two methods described below is to be used in directing the output of the dc Voltage Source.

1. If Cal Code *is not* a 5, 6, 7, or 10:
   - The channel number is taken from the front panel switch.
   - The front panel is set up to display the channel number, Block 2, and Step 7.
   - The calibration is taken from Block 2 of the TA489A Calibrator memory.
   - The Cal Code is set to 5.
   - The binary output to the Voltage Source is set for a voltage output of +3.75 V.
   - The FET chop rate is determined from the front panel switch.
   - The Step Response FET switches are enabled, and the strobes are sent to the crates and to the TA666A Data Selector.
2. If the Cal Code *is* a 5, 6, 7, or 10:
   - The channel number is taken from the front panel switch.
   - The front panel is set up to display the channel number, Block 2, and Step 7.
   - The calibration is taken from Block 2 of the TA489A Calibrator memory.
   - If the voltage value stored in memory is positive, it is doubled, but limited to 10 V.
   - If the voltage value stored in memory is negative, it is inverted.
   - The Cal Code is sent out unchanged to the TA493A Signal Conditioner Crate.
   - The FET chop rate is determined at the front panel switch.
   - The FET switches are enabled and the strobes are sent to the crates and to the TA666A Data Selector.

#### 2.5.6.2 Step Response Algorithm/Command Link Selection

When Step Response is selected from the command link, the signal fed into the input of the amplifier from the calibration lines is obtained from two 30-Ω line drivers within the TA489A Calibrator. The sequence of events follows:

- The channel number is taken from the command link.
- The front panel is set up to display the channel number, Block 2, and Step 7.
- The Cal Code is set to a value of 5.
- The binary output to the Voltage Source is set for a 0-V output from the Voltage Source.
- The 30-Ω driver switching rate is read from the command link.
- The two 30-Ω drivers are enabled and the strobes are sent to the crates and to the TA666A Data Selector.

### 2.5.7 Auto Cal/Step Select

This calibration mode allows the operator to select a calibration step for the cycle; this step can be selected from the front panel or through the command link. The TA489A will then perform an Auto Cal and stop on Step 7 of the first channel (Channel 0) until a Start is once again initiated. The TA489A will then advance to the next sequential channel and wait for another Start. This process continues until the last channel (Channel 177) has been calibrated, at which time the TA489A will revert to Standby mode.

## 2.6 Aborting Calibration Sequences

During the calibration sequence initiated by any of the options, calibrations in progress can be aborted in two ways:

1. If a "Clear" command is received from the front panel or a "Stop Cal" is received from the command link, the TA489A Calibrator will continue with the sequence in progress through the 16 steps of calibration for the channel currently being addressed, and then revert to a Standby mode.

2. If a LOCKOUT timing signal is received from the TA486A Programmer/Timer, the TA489A Calibrator immediately drops out of calibration and remains locked out from front panel or remote control until a system POWER-ON RESET signal is received from the TA485A Controller. The isolated +28-V power supply in the calibrator is disabled for ~18 s, then the +28-V output is reinstated. This method of aborting calibrations is more definitive and abrupt.

   The firmware in the TA489A will prevent calibrations for ~10s after LOCKOUT is removed.

## 2.7 Associated Equipment

### 2.7.1 dc Voltage Source

The precision dc Voltage Source referred to in the calibration process is a highly versatile reference source. It is the Model 501 Programmable dc Voltage Standard manufactured by Electronic Development Corporation (EDC).

The Voltage Source was specially modified by EDC for Sandia National Laboratories to provide a differential output. It was further modified at Sandia to enable inverting the differential output, which is controlled only by the TA489A Calibrator.

Solid-state circuitry is used except for a mercury-wetted contact relay installed during the inverting retrofit that Sandia employs.

The output is limited to ±5.12 V for a differential output of 10.24 V. It may be controlled locally from the front panel or from the calibrator interface.

Accuracy of the resolution is 10 μV (see Appendix E).

# 3. Description of the TA489A Calibrator

## 3.1 Physical Description

Here we define the mechanical assembly including the electronic components, mechanical parts, and connectors used in the TA489A Calibrator.

### 3.1.1 Chassis

The TA489A chassis is located in Rack 3 of the MA164 Digital Data Acquisition System. It is in the fourth location from the top of Rack 3 (Figure 3).

The calibrator is equipped with an aluminum chassis mounted on a standard rack with dimensions of 19 in. wide × 7 in. high × 26 in. deep (Figure 4). Side panels are made of corrosion-inhibited steel; all other parts are made of corrosion-inhibited aluminum.

The front and rear panels are made of 0.125-thick aluminum. The labeling is engraved and filled in black. The front and all four edges of the front panel are painted with two coats of epoxy, color 23617, per Federal Standard 595. The top and bottom covers are also made of 0.125-thick aluminum, with slots milled out at the front for airflow into the chassis. Both covers are corrosion-inhibited and can be removed for internal access to the chassis.

Cooling is provided by a 113-CFM Rotron fan. Airflow is from front to rear within the chassis; air is drawn into the chassis through slots in the top and bottom front covers, and is expelled at the rear panel. The intake air is not filtered.

### 3.1.2 Internal Parts

Two universal wire-wrap Schottky TTL Augat boards (P/N 8136-SCH109-54) provide area for logic circuitry. The boards are hinge-mounted for access to the wire-wrap and components underneath, and are installed one behind the other at the same level within the chassis (Figure 4).

One +5-V 10-A, +12-V 1-A, −12-V 1-A KEPCO switching power supply provides operating voltage for the digital logic, calibration relay matrix, microprocessor, and the other calibration relays in the chassis.

One +28-V 2.5-A KEPCO switching power supply provides operating voltage outputs to all TA590 Signal Conditioners. The output from this supply is isolated from ground and all other voltage sources within the TA489A chassis. The reason this supply is isolated is to prevent back EMF from the TA590 Signal Conditioner relays being introduced into system ground.

One modular ±15-V 1-A power supply provides operating voltage for the FET switches used in the Step Response circuitry of the calibrator.

### 3.1.3 Cabling

All interface connections are made through 17 rear-panel mounted connectors (Figure 4). One connector applies ac power to the TA489A. A "giant banana" jack provides quick connect/disconnect grounding of the TA489A to the MA164 ground bars. Eight connectors provide interfacing to all Data Collection Crates for calibration controls and signals. One connector interfaces to the TA666A Data Selector for proper addressing of the channel during calibration. Another interfaces to the precision dc Voltage Source so that binary values can be sent to the Voltage Source and the differential voltage output can be returned to the TA489A.

One connector interfaces the TA486A Programmer/Timer, one interfaces the TA484A Multiplexer, one interfaces the TA488B Trigger Generator, and another interfaces the TA485A Controller.

One connector provides direct link to an external terminal for communication with the microprocessor.

Two BNC connectors are also provided. One is used as a return for the +28-V power supply for use with the TA665 zero-time simulator. The other is unused.

One BNC interface connector is provided on the front panel to supply a calibration input other than the dc Voltage Source to the TA489A Calibrator.

### 3.1.4 Connector Types

Except for the BNC connectors and the banana jack, the interface connectors on the rear panel are plastic. Manufactured by AMP Special Industries, they are rugged, molded plastic circular connectors that provide quick connect/disconnect mating. They can accept a variety of pins and sockets, including machined and stamped parts. Sockets and pins that provide a direct interface for coax are also used. Coax and normal PVC-wired pins or sockets may be intermixed within the connector.

# APPENDIX A

# List of Drawings for TA489A Calibrator

Following is a list of drawings for the TA489A Calibrator:

| Drawing No. | Title |
|---|---|
| T56556 | TA489A Calibrator Assembly |
| CK T56556 | TA489A Calibrator Schematic |
| AL T56556 | TA489A Calibrator Parts List (Augat Boards) |
| T69394 | TA489A Calibrator Chassis Modifications |
| CK T67334 | TA489A Calibrator Relay Matrix Schematic |
| T67334 | TA489A Calibrator Relay Matrix Assembly |

# APPENDIX B

# DEC Boards Used in TA489A Calibrator

| | |
|---|---|
| M8186 | Central Processing Unit |
| M8047-AA | Memory and Asynchronous Serial Line Interface |
| M9401 | Buss Extender |
| 1822, Rev. 1 | RAM Memory (This is not a DEC board; the manufacturer is ADAC) |

# APPENDIX C

# Jumpers on DEC Board M8047-AA (MXVII-A)

| | |
|---|---|
| J6 – J7 | Halt on framing error |
| J10 – J11 | 2716 EProm |
| J15 – J29 | |
| J33 – J37 | |
| J36 – J38 | |
| J39 – J40 | |
| J13 – J27 | SLU Ch 1 Address 177560 |
| J14 – J25 | |
| J15 – J26 | |
| J19 – J28 | |
| J19 – J24 | SLU Ch 0 Address 176500 |
| J18 – J23 | |
| J20 – J21 | ROM Memory (000000 Starting Address) |
| J30 – J34 | RAM Memory (100000 Starting Address) |
| J31 – J34 | |
| J32 – J34 | |
| J51 – J56 | SLU Vectors (Ch-0, 300; Ch-1, 60) |
| J52 – J54 | |
| J54 – J55 | |
| J53 – J57 | |
| | SLU CH 0 Parameters |
| J64 – J66 | Even parity |
| J62 – J66 | 8 bits, no parity |
| J63 – J65 | One-stop bit |
| J45 – J50 | Baud rate (38,400) |
| | SLU CH 1 Parameters |
| J59 – J66 | 8 bits, no parity |
| J61 – J66 | Even parity |
| J60 – J65 | One-stop bit |
| J46 – J48 | Baud rate (9600) |
| J67 – J68 | Crystal clock |
| W1, W3 | Installed |

# APPENDIX D

## TA489A Status Register Format

| SUB ADDRESS NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | MESSAGE BYTE NUMBER |
|---|---|---|---|---|---|---|---|---|---|
| 0 | MEMORY BLOCK (0 - 3) | | STEP RE-SPONSE | SINGLE CHANNEL STEP SELECT | AUTO CAL BLOCK SELECT | STOP CAL | SINGLE CHANNEL CAL | AUTO CAL | 5 |
| 1 | X | SLOT ADDRESS (000 - 177) | | | | | | | 6 |
| | | 1 | 4 | 2 | 1 | 4 | 2 | 1 | |
| 2 | STEP RESPONSE RATE | | | | LAST STEP (0 - 15) | | | | 7 |
| | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | |
| 3 | X | X | X | X | X | X | X | X | 8 |

| BIT NUMBER 3 | 2 | 1 | 0 | STEP RESPONSE PULSE RATE | BIT NUMBER 3 | 2 | 1 | 0 | STEP RESPONSE PULSE RATE |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 5.0 Hz | 1 | 0 | 0 | 0 | 2.0 KHz |
| 0 | 0 | 0 | 1 | 10.0 Hz | 1 | 0 | 0 | 1 | 5.0 KHz |
| 0 | 0 | 1 | 0 | 20.0 Hz | 1 | 0 | 1 | 0 | 10.0 KHz |
| 0 | 0 | 1 | 1 | 50.0 Hz | 1 | 0 | 1 | 1 | 20.0 KHz |
| 0 | 1 | 0 | 0 | 100.0 Hz | 1 | 1 | 0 | 0 | 50.0 KHz |
| 0 | 1 | 0 | 1 | 200.0 Hz | 1 | 1 | 0 | 1 | 100.0 KHz |
| 0 | 1 | 1 | 0 | 500.0 Hz | 1 | 1 | 1 | 0 | 200.0 KHz |
| 0 | 1 | 1 | 1 | 1,000.0 Hz | 1 | 1 | 1 | 1 | FRONT PANEL CONTROL |

FUNCTION CODES:
1 - Write One (7-Byte Message)
2 - Read One (7-Byte Message)
5 - Write Four(9-Byte Message)
6 - Read Four (9-Byte Message)

```
 SUB                                                                  MESSAGE
ADDRESS                                                                 BYTE
 NUMBER                                                               NUMBER
      ***************************************************************
      *   7   *   6   *   5   *   4   *   3   *   2   *   1   *   0   *
      *       *       *       *       *       *       *       *       *
  0   * MEMORY BLOCK  *   X   *   X   *   X   *   X   *   X   *   X   *   5
      *    (0 - 3)    *       *       *       *       *       *       *
      *       *       *       *       *       *       *       *       *
      ***************************************************************

      ***************************************************************
      *       *       *       *       *       *       *       *       *
      *       *       *                       *                       *
  1   *   X   *  S L O T   A D D R E S S  ( 0 0 0   -   1 7 7 )   *   6
      *       *       *                       *                       *
      *       *   1   *   4   *   2   *   1   *   4   *   2   *   1   *
      ***************************************************************

      ***************************************************************
      *       *       *       *       *       *       *       *       *
      *       *       *       *       *       *       *       *       *
  2   *   X   *   X   *   X   *   X   *   X   *   X   *   X   *   X   *   7
      *       *       *       *       *       *       *       *       *
      *       *       *       *       *       *       *       *       *
      ***************************************************************

      ***************************************************************
      *       *       *       *       *       *       *       *       *
      *       *       *       *       *       *       *       *       *
  3   *   X   *   X   *   X   *   X   *   X   *   X   *   X   *   X   *   8
      *       *       *       *       *       *       *       *       *
      *       *       *       *       *       *       *       *       *
      ***************************************************************

      ***************************************************************
      *       *       *       *       *       *       *       *       *
      *       *       *       *       *       *       *       * LSB   *
  4   * SVB 7 * SVB 6 * SVB 5 * SVB 4 * SVB 3 * SVB 2 * SVB 1 * SVB 0 *   9
      * 1.25MV* 625uV *312.5uV*~156uV * ~78uV * ~39uV * ~20uV * ~10uV *
      *       *       *       *       *       *       *       *       *
      ***************************************************************
      SVB 4 = 156.25uV
      SVB 3 = 78.125uV
      SVB 2 = 39.0625uV
      SVB 1 =  19.53125uV
      SVB 0 =  9.765625uV
```

# APPENDIX E

## TA489A Memory Format

```
   SUB                                                                  MESSAGE
ADDRESS                                                                   BYTE
 NUMBER                                                                 NUMBER
      ***********************************************************************
      *   7   *   6   *   5   *   4   *   3   *   2   *   1   *   0   *
      *       *       *       *       *       *       *       *       *
   5  * SVB15 * SVB14 * SVB13 * SVB12 * SVB11 * SVB10 * SVB 9 * SVB 8 *  10
      * 320MV * 160MV *  80MV *  40MV *  20MV *  10MV *   5MV * 2.5MV *
      *       *       *       *       *       *       *       *       *
      ***********************************************************************
      20 BIT UNSIGNED NUMBER - POLARITY DETERMINED FROM SIGN BIT

      ***********************************************************************
      *       *       *       *       *       *       *       *       *
      *       *       *       *POLARITY  MSB  *       *       *       *
   6  * JUMP  *   X   *   X   *REVERSE* SVB19 * SVB18 * SVB17 * SVB16 *  11
      *  CAL  *       *       * (SIGN)* 5.12V * 2.56V * 1.28V * 640MV *
      *       *       *       *  BIT  *       *       *       *       *
      ***********************************************************************
      0 - CAL                 0 - NORMAL (PLUS)
      1 - SKIP (JUMP) THIS    1 - REVERSE (MINUS)
      CHANNEL FOR THIS BLOCK

      ***********************************************************************
      *       *       *       *       *       *       *       *       *
      *                       *       *       * CALIB.*       *
   7  *   CALIBRATION PROM PROGRAMS   *   X   *   X   * SOURCE*SPECIAL*  12
      * PRMA3   PRMA2   PRMA1   PRMA0 *       *       * SELECT*  CAL  *
      *       *       *       *       *       *       *       *       *
      ***********************************************************************
         NORMAL                    SPECIAL                0 - VOLTAGE SOURCE
      0000 - ZERO CAL                SK1                    1 - ALTERNATE SOURCE
      0001 - SHUNT CAL               SK2
      0010 - STEP CAL                SK1 & SK3
      0011 - +INT TEST               N/A
      0100 - -INT TEST               N/A
      0101 - AMP CAL (1/1)           N/A
      0110 - ATTEN CAL (10/1)        N/A
      0111 - ATTEN CAL (100/1)       N/A
      1000 - ATTEN CAL (1000/1)      N/A
      1001 - N/A                     SK3
      1010 - N/A                     SK1 & SK2
      1011 - N/A                     SK2 & SK3
      1100 - N/A                     SK1, SK2 & SK3
      1101 - N/A                     N/A
      1110 - N/A                     EXTERNAL
      1111 - GAGE                    N/A
                                  FUNCTION CODES:  11 - MEMORY WRITE
                                                   12 - MEMORY READ
                                                   (13-Byte MESSAGES)
```

# APPENDIX F

# TA489A Calibration Step PROM Program

| OCT ADDR | HEX ADDR | OCT DATA | HEX DATA | STEP |
|---|---|---|---|---|
| 00 | 00 | 01 | 01 | 01 |
| 01 | 01 | 02 | 02 | 02 |
| 02 | 02 | 03 | 03 | 03 |
| 03 | 03 | 04 | 04 | 04 |
| 04 | 04 | 05 | 05 | 05 |
| 05 | 05 | 06 | 06 | 06 |
| 06 | 06 | 07 | 07 | 07 |
| 07 | 07 | 10 | 08 | 08 |
| 10 | 08 | 11 | 09 | 09 |
| 11 | 09 | 12 | 0A | 10 |
| 12 | 0A | 21 | 11 | 11 |
| 13 | 0B | 22 | 12 | 12 |
| 14 | 0C | 23 | 13 | 13 |
| 15 | 0D | 24 | 14 | 14 |
| 16 | 0E | 25 | 15 | 15 |
| 17 | 0F | 36 | 16 | 16 |

PROM Information:

Type —82S123
Location —CK-T56556 Sh 15 (2AC14)

# APPENDIX G

## TA489A Step Response PROM Program

| OCT ADDR | HEX ADDR | OCT DATA | HEX DATA | RATE SELECTED |
|---|---|---|---|---|
| 1776 | 3FE | 04 | 04 | 100 Hz |
| 1775 | 3FD | 05 | 05 | 200 Hz |
| 1773 | 3FB | 06 | 06 | 500 Hz |
| 1767 | 3F7 | 07 | 07 | 1 kHz |
| 1757 | 3EF | 10 | 08 | 2 kHz |
| 1737 | 3DF | 11 | 09 | 5 kHz |
| 1677 | 3BF | 12 | 0A | 10 kHz |
| 1577 | 37F | 13 | 0B | 20 kHz |
| 1377 | 2FF | 14 | 0C | 50 kHz |
| 0777 | 1FF | 15 | 0D | 100 kHz |

PROM Information:

Type —2716
Location —CK-T56556 Sh 32
(2EG19)

# APPENDIX H

## TA489A Calibration PROM Code

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00000000000 | 000 | 00000000 | |
| 00000000001 | 001 | 00000000 | |
| 00000000010 | 002 | 00000000 | |
| 00000000011 | 003 | 00000000 | |
| 00000000100 | 004 | 00000000 | |
| 00000000101 | 005 | 00000000 | |
| 00000000110 | 006 | 00000000 | Zero Cal |
| 00000000111 | 007 | 00000000 | |
| 00000001000 | 008 | 00000000 | |
| 00000001001 | 009 | 00000000 | |
| 00000001010 | 00A | 00000000 | |
| 00000001011 | 00B | 00000000 | |
| 00000001100 | 00C | 00000000 | |
| 00000001101 | 00D | 00000000 | |
| 00000001110 | 00E | 00001111 | |
| 00000001111 | 00F | 00001111 | |
| 00000010000 | 010 | 00000001 | |
| 00000010001 | 011 | 00000001 | |
| 00000010010 | 012 | 00000001 | |
| 00000010011 | 013 | 00000001 | |
| 00000010100 | 014 | 00000001 | |
| 00000010101 | 015 | 00000001 | |
| 00000010110 | 016 | 00000001 | |
| 00000010111 | 017 | 00000001 | Shunt Cal |
| 00000011000 | 018 | 00000001 | |
| 00000011001 | 019 | 00000001 | |
| 00000011010 | 01A | 00000001 | |
| 00000011011 | 01B | 00000001 | |
| 00000011100 | 01C | 00000001 | |
| 00000011101 | 01D | 00000001 | |
| 00000011110 | 01E | 00001111 | |
| 00000011111 | 01F | 00001111 | |

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00000100000 | 020 | 00000010 | |
| 00000100001 | 021 | 00000010 | |
| 00000100010 | 022 | 00000010 | |
| 00000100011 | 023 | 00000010 | |
| 00000100100 | 024 | 00000010 | |
| 00000100101 | 025 | 00000010 | |
| 00000100110 | 026 | 00000010 | |
| 00000100111 | 027 | 00000010 | Step Cal |
| 00000101000 | 028 | 00000010 | |
| 00000101001 | 029 | 00000010 | |
| 00000101010 | 02A | 00000010 | |
| 00000101011 | 02B | 00000010 | |
| 00000101100 | 02C | 00000010 | |
| 00000101101 | 02D | 00000010 | |
| 00000101110 | 02E | 00001111 | |
| 00000101111 | 02F | 00001111 | |
| 00000110000 | 030 | 00000011 | |
| 00000110001 | 031 | 00000011 | |
| 00000110010 | 032 | 00000011 | |
| 00000110011 | 033 | 00000011 | |
| 00000110100 | 034 | 00000011 | |
| 00000110101 | 035 | 00000011 | |
| 00000110110 | 036 | 00000011 | + Internal Test |
| 00000110111 | 037 | 00000011 | |
| 00000111000 | 038 | 00000011 | |
| 00000111001 | 039 | 00000011 | |
| 00000111010 | 03A | 00000011 | |
| 00000111011 | 03B | 00000011 | |
| 00000111100 | 03C | 00000011 | |
| 00000111101 | 03D | 00000011 | |
| 00000111110 | 03E | 00001111 | |
| 00000111111 | 03F | 00001111 | |
| 00001000000 | 040 | 00000100 | |
| 00001000001 | 041 | 00000100 | |
| 00001000010 | 042 | 00000100 | |
| 00001000011 | 043 | 00000100 | |
| 00001000100 | 044 | 00000100 | |
| 00001000101 | 045 | 00000100 | |
| 00001000110 | 046 | 00000100 | - Internal Test |
| 00001000111 | 047 | 00000100 | |
| 00001001000 | 048 | 00000100 | |
| 00001001001 | 049 | 00000100 | |
| 00001001010 | 04A | 00000100 | |
| 00001001011 | 04B | 00000100 | |
| 00001001100 | 04C | 00000100 | |
| 00001001101 | 04D | 00000100 | |
| 00001001110 | 04E | 00001111 | |
| 00001001111 | 04F | 00001111 | |

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00001010000 | 050 | 00000101 | |
| 00001010001 | 051 | 00000101 | |
| 00001010010 | 052 | 00000101 | |
| 00001010011 | 053 | 00000101 | |
| 00001010100 | 054 | 00000101 | |
| 00001010101 | 055 | 00000101 | |
| 00001010110 | 056 | 00000101 | |
| 00001010111 | 057 | 00000101 | AMP Cal (1:1) |
| 00001011000 | 058 | 00000101 | |
| 00001011001 | 059 | 00000101 | |
| 00001011010 | 05A | 00000101 | |
| 00001011011 | 05B | 00000101 | |
| 00001011100 | 05C | 00000101 | |
| 00001011101 | 05D | 00000101 | |
| 00001011110 | 05E | 00001111 | |
| 00001011111 | 05F | 00001111 | |
| 00001100000 | 060 | 00000110 | |
| 00001100001 | 061 | 00000110 | |
| 00001100010 | 062 | 00000110 | |
| 00001100011 | 063 | 00000110 | |
| 00001100100 | 064 | 00000110 | |
| 00001100101 | 065 | 00000110 | |
| 00001100110 | 066 | 00000110 | |
| 00001100111 | 067 | 00000110 | Attenuation Cal |
| 00001101000 | 068 | 00000110 | (10:1) |
| 00001101001 | 069 | 00000110 | |
| 00001101010 | 06A | 00000110 | |
| 00001101011 | 06B | 00000110 | |
| 00001101100 | 06C | 00000110 | |
| 00001101101 | 06D | 00000110 | |
| 00001101110 | 06E | 00001111 | |
| 00001101111 | 06F | 00001111 | |
| 00001110000 | 070 | 00000111 | |
| 00001110001 | 071 | 00000111 | |
| 00001110010 | 072 | 00000111 | |
| 00001110011 | 073 | 00000111 | |
| 00001110100 | 074 | 00000111 | |
| 00001110101 | 075 | 00000111 | |
| 00001110110 | 076 | 00000111 | |
| 00001110111 | 077 | 00000111 | Attenuation Cal |
| 00001111000 | 078 | 00000111 | (100:1) |
| 00001111001 | 079 | 00000111 | |
| 00001111010 | 07A | 00000111 | |
| 00001111011 | 07B | 00000111 | |
| 00001111100 | 07C | 00000111 | |
| 00001111101 | 07D | 00000111 | |
| 00001111110 | 07E | 00001111 | |
| 00001111111 | 07F | 00001111 | |

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00010000000 | 080 | 00001000 | |
| 00010000001 | 081 | 00001000 | |
| 00010000010 | 082 | 00001000 | |
| 00010000011 | 083 | 00001000 | |
| 00010000100 | 084 | 00001000 | |
| 00010000101 | 085 | 00001000 | |
| 00010000110 | 086 | 00001000 | |
| 00010000111 | 087 | 00001000 | Attenuation Cal |
| 00010001000 | 088 | 00001000 | (1000:1) |
| 00010001001 | 089 | 00001000 | |
| 00010001010 | 08A | 00001000 | |
| 00010001011 | 08B | 00001000 | |
| 00010001100 | 08C | 00001000 | |
| 00010001101 | 08D | 00001000 | |
| 00010001110 | 08E | 00001111 | |
| 00010001111 | 08F | 00001111 | |
| 00010010000 | 090 | 00001001 | |
| 00010010001 | 091 | 00001001 | |
| 00010010010 | 092 | 00001001 | |
| 00010010011 | 093 | 00001001 | |
| 00010010100 | 094 | 00001001 | |
| 00010010101 | 095 | 00001001 | |
| 00010010110 | 096 | 00001001 | |
| 00010010111 | 097 | 00001001 | Special Cal |
| 00010011000 | 098 | 00001001 | (K3) |
| 00010011001 | 099 | 00001001 | |
| 00010011010 | 09A | 00001001 | |
| 00010011011 | 09B | 00001001 | |
| 00010011100 | 09C | 00001001 | |
| 00010011101 | 09D | 00001001 | |
| 00010011110 | 09E | 00001111 | |
| 00010011111 | 09F | 00001111 | |
| 00010100000 | 0A0 | 00001010 | |
| 00010100001 | 0A1 | 00001010 | |
| 00010100010 | 0A2 | 00001010 | |
| 00010100011 | 0A3 | 00001010 | |
| 00010100100 | 0A4 | 00001010 | |
| 00010100101 | 0A5 | 00001010 | |
| 00010100110 | 0A6 | 00001010 | |
| 00010100111 | 0A7 | 00001010 | Special Cal |
| 00010101000 | 0A8 | 00001010 | (K1 & K2) |
| 00010101001 | 0A9 | 00001010 | |
| 00010101010 | 0AA | 00001010 | |
| 00010101011 | 0AB | 00001010 | |
| 00010101100 | 0AC | 00001010 | |
| 00010101101 | 0AD | 00001010 | |
| 00010101110 | 0AE | 00001111 | |
| 00010101111 | 0AF | 00001111 | |

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00010110000 | 0B0 | 00001011 | |
| 00010110001 | 0B1 | 00001011 | |
| 00010110010 | 0B2 | 00001011 | |
| 00010110011 | 0B3 | 00001011 | |
| 00010110100 | 0B4 | 00001011 | |
| 00010110101 | 0B5 | 00001011 | |
| 00010110110 | 0B6 | 00001011 | |
| 00010110111 | 0B7 | 00001011 | Special Cal |
| 00010111000 | 0B8 | 00001011 | (K2 & K3) |
| 00010111001 | 0B9 | 00001011 | |
| 00010111010 | 0BA | 00001011 | |
| 00010111011 | 0BB | 00001011 | |
| 00010111100 | 0BC | 00001011 | |
| 00010111101 | 0BD | 00001011 | |
| 00010111110 | 0BE | 00001111 | |
| 00010111111 | 0BF | 00001111 | |
| 00011000000 | 0C0 | 00001100 | |
| 00011000001 | 0C1 | 00001100 | |
| 00011000010 | 0C2 | 00001100 | |
| 00011000011 | 0C3 | 00001100 | |
| 00011000100 | 0C4 | 00001100 | |
| 00011000101 | 0C5 | 00001100 | |
| 00011000110 | 0C6 | 00001100 | Special Cal |
| 00011000111 | 0C7 | 00001100 | (K1, K2 & K3) |
| 00011001000 | 0C8 | 00001100 | |
| 00011001001 | 0C9 | 00001100 | |
| 00011001010 | 0CA | 00001100 | |
| 00011001011 | 0CB | 00001100 | |
| 00011001100 | 0CC | 00001100 | |
| 00011001101 | 0CD | 00001100 | |
| 00011001110 | 0CE | 00001111 | |
| 00011001111 | 0CF | 00001111 | |
| 00011010000 | 0D0 | 00000000 | |
| 00011010001 | 0D1 | 00000000 | |
| 00011010010 | 0D2 | 00000000 | |
| 00011010011 | 0D3 | 00000000 | |
| 00011010100 | 0D4 | 00000000 | |
| 00011010101 | 0D5 | 00000000 | |
| 00011010110 | 0D6 | 00000000 | |
| 00011010111 | 0D7 | 00000000 | (Not Used) |
| 00011011000 | 0D8 | 00000000 | |
| 00011011001 | 0D9 | 00000000 | |
| 00011011010 | 0DA | 00000000 | |
| 00011011011 | 0DB | 00000000 | |
| 00011011100 | 0DC | 00000000 | |
| 00011011101 | 0DD | 00000000 | |
| 00011011110 | 0DE | 00001111 | |
| 00011011111 | 0DF | 00001111 | |

| Binary Address | Hexadecimal Address | Binary Data | Calibration Type |
|---|---|---|---|
| 00011100000 | 0E0 | 00000000 | |
| 00011100001 | 0E1 | 00000000 | |
| 00011100010 | 0E2 | 00000000 | |
| 00011100011 | 0E3 | 00000000 | |
| 00011100100 | 0E4 | 00000000 | |
| 00011100101 | 0E5 | 00000000 | |
| 00011100110 | 0E6 | 00000000 | |
| 00011100111 | 0E7 | 00000000 | (Not Used) |
| 00011101000 | 0E8 | 00000000 | |
| 00011101001 | 0E9 | 00000000 | |
| 00011101010 | 0EA | 00000000 | |
| 00011101011 | 0EB | 00000000 | |
| 00011101100 | 0EC | 00000000 | |
| 00011101101 | 0ED | 00000000 | |
| 00011101110 | 0EE | 00001111 | |
| 00011101111 | 0EF | 00001111 | |
| 00011110000 | 0F0 | 00001111 | |
| 00011110001 | 0F1 | 00001111 | |
| 00011110010 | 0F2 | 00001111 | |
| 00011110011 | 0F3 | 00001111 | |
| 00011110100 | 0F4 | 00001111 | |
| 00011110101 | 0F5 | 00001111 | |
| 00011110110 | 0F6 | 00001111 | |
| 00011110111 | 0F7 | 00001111 | Gage Cal |
| 00011111000 | 0F8 | 00001111 | |
| 00011111001 | 0F9 | 00001111 | |
| 00011111010 | 0FA | 00001111 | |
| 00011111011 | 0FB | 00001111 | |
| 00011111100 | 0FC | 00001111 | |
| 00011111101 | 0FD | 00001111 | |
| 00011111110 | 0FE | 00001111 | |
| 00011111111 | 0FF | 00001111 | |

# APPENDIX I

## Jumpers on DEC Board LSI-11/23 CPU (M8186)

| | | |
|---|---|---|
| W1 | In | Internal Master Clock Enabled |
| W2 | Out | Memory Management Delay |
| W3 | In | Memory Management Delay |
| W4 | In | Line Time Clock Disabled |
| W5 | Out | Power-Up Mode 0, PC@24, PS@26 |
| W6 | Out | Power-Up Mode 0, PC@24, PS@26 |
| W7 | Out | ODT on Halt |
| W8 | In | Boostrap to 173000 |
| W9 | In | Bits 9–15 of Bootstrap address (If W8 is out) |
| W10 | In | |
| W11 | In | |
| W12 | In | |
| W13 | In | |
| W14 | In | |
| W15 | In | |
| W16 | In | TTL Clock to Chip E39 |
| W17 | In | TTL Clock to Chip E48 |
| W18 | Out | Wake-up Circuit Enabled |

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