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Thermal Cycle Tests on Double Sided and Multilayer Printed Wiring Boards

Charles W. Jennings

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THERMAL CYCLE TESTS ON DOUBLE SIDED AND MULTILAYER PRINTED WIRING BOARDS

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April 1976

ABSTRACT

Substantial differences were found in the capability of plated-through holes in both double sided and multilayer printed wiring boards to withstand thermal cycling between -65° and 125°C. The circuit pattern used for the test contained 240 holes connected in series, 80 each of 0.51 mm (.020), 0.76 mm (.030) and 1.02 mm (.040) diameter. Double sided glass-epoxy and glass-polyimide boards withstood 544 cycles with a total circuit resistance increase of 2 percent. However, paper-epoxy boards revealed many open circuits and substantial electrical resistance increases for the same number of cycles. Considerable variation in electrical resistance increases in glass-epoxy multilayer boards was detected. Analysis of the behavior of the multilayer boards was clouded by the poor quality of the plated-through holes used. Current carrying capability provided a useful indication of hole degradation after cycling. A critical factor effecting plated-through hole reliability in thermal cycling environment appears to be laminate composition. Further testing is suggested to determine the necessity for additional property requirements for laminate procurement specifications, such as minimum glass transition temperature and/or designation of resin composition. Glass-polyimide laminates should be considered for multilayer boards which must withstand extreme thermal cycling environments.

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INTRODUCTION

In recent years there has been considerable interest in the effect of thermal cycling on the reliability of plated-through holes (PTHs) in printed wiring boards (PWBs). The number of cycles the PTHs must withstand is often indefinite and the temperature limits uncertain, so arbitrary test procedures have been adopted to evaluate PTH reliability. These procedures are usually designed to provide a thermal overstress to the board. Failure criteria is typically a change in circuit resistance above some selected level. In most instances this is not as arbitrary as it might appear for when a circuit resistance begins to change significantly, an open circuit or very high resistance usually forms within a few cycles.

This report presents the results of thermal cycle tests run on PTH circuits on both double sided and multilayer PWBs. The thermal cycle selected was from -65°C to 125°C. Three different types of laminate compositions were used in the double sided board tests. The boards were fabricated by a panel plate, solder dip and liquid level process. Multilayer boards were made from the typical GE grade laminate material used for fabricating boards of this type. Both pattern and panel plating of the external layers and holes was used for the multilayer boards. The number and type of boards tested and their materials and processing are shown in Figure 1 and Table 1.

TABLE 1

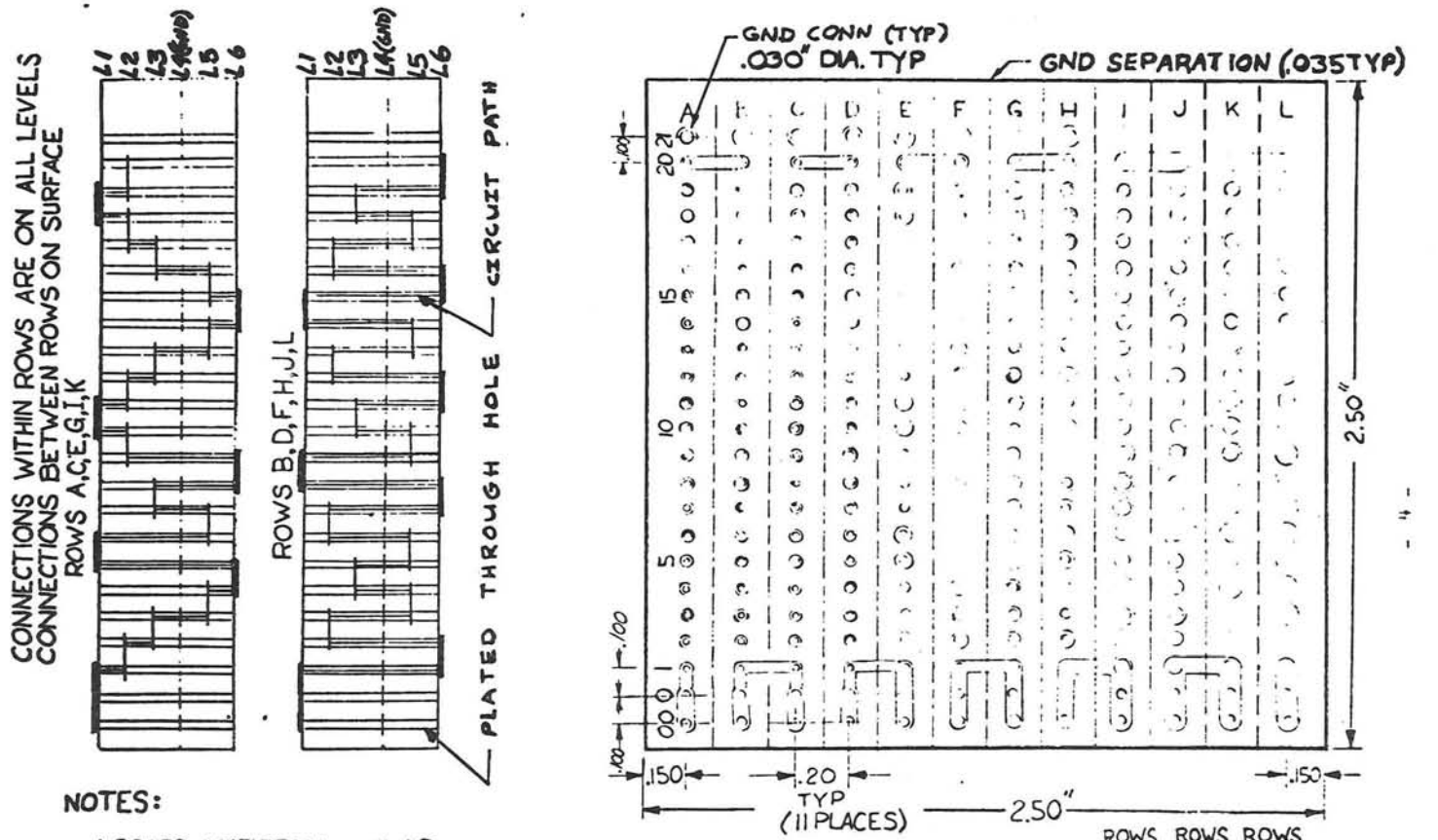
BOARDS FABRICATED FOR THERMAL CYCLE TESTS

Double Sided

Number	Laminate Type and Grade	Processing	Plated Copper Thickness
2	Glass-epoxy, GH	Panel Plate Copper, Solder Dip and Liquid Level	25 μm (.001)
2	"	"	38 μm (.0015)
2	Glass-polyimide	"	25 μm
2	"	"	38 μm
2	Paper-epoxy, FR 3	"	25 μm
2	"	"	38 μm

Multilayer

2	Glass-epoxy, GE	Panel Plate Copper, Solder Dip and Liquid Level	25 μm
2	"	"	38 μm
2	"	Pattern Plate Copper and Solder	25 μm
2	"	"	38 μm
2	"	Panel Plate Copper (no solder coating)	25 μm



NOTES:

1. BOARD MATERIAL - G 10
2. LAMINATED THICKNESS .062 ±.007
3. INTERNAL LAYERS 1 OZ.
4. TERMINALS A-L 0 & 00 FOR WIRE CONNECTION
5. 12 SEPARATE GROUNDS AS INDICATED CONNECTION AT A-L 21
6. ALL CONDUCTORS SAME AS LAND SIZE

	ROWS A-D	ROWS E-H	ROWS I-L	
HOLE DIA. (AFTER PLATING)	.020	.030	.040	80 HOLES
PAD DIA.	.050	.060	.070	80 HOLES
CLEAR HOLE (GND)	.050	.060	.070	80 HOLES

PTH TEST PATTERN

Figure 1

Plated-Through Hole Test Pattern

The multilayer test circuit pattern consisted of 240 PTHs connected in series, 80 each of 0.51 mm (.020)*, 0.76 mm (.030)*, and 1.02 mm (.040)* diameter. This circuitry consisted of a serpentine stitch pattern connecting hole to hole at various internal and external planes. There were 6 copper conductive layers, 3 internal and an internal ground plane, all 1 Oz copper cladding.

The circuit for the double sided boards consisted of a stitch pattern connecting the same number and size holes as in the multilayer pattern. All holes were drilled on a numerically controlled drill. Two levels of copper plating thickness were specified for each type of board, 0.025 mm (.0010) and 0.038 mm (.0015). The multilayer test pattern was used in Round Robin Tests conducted by the Institute of Printed Circuits (IPC) and is similar to that used in other investigations of the effects of thermal cycling on the reliability of PTHs in printed wiring boards.[1] [2] [3]

The objective of the IPC tests was to provide industry wide data on the performance and reliability of multilayer boards at the current level of development. Two types of stress were applied in these tests, thermal cycling for 25 cycles between -65°C and 125°C, and 175 cycles between -65°C and 150°C; and with separate specimens, 10 cycles of 10 seconds each of solder shock at 287°C. The results of IPC Round Robin Tests III and IV showed no correlation between the thermal cycling and solder shock tests. Failure was indicated in the tests when circuit resistance increased from its initial value to

*Values in parentheses are in inch

1 ohm and a hole resistance exceeded 0.2 ohm. There were 31 sample sets tested which were from different suppliers or were fabricated by the same supplier with different laminate composition. Of these, 4 showed no failures in thermal cycling. This showed that PTHs in multilayer boards with proper materials and fabrication can withstand cycling between such temperature extremes. Unfortunately the laminate materials and processing used for the IPC sample sets was not detailed because of proprietary and other considerations. The boards used in these tests did not have a solder coating on the surface or in the holes. The 150°C upper temperature limit of the IPC tests was considered too much of overstress for the type of boards used in Sandia applications; a 125°C upper limit was adopted for the tests of this investigation. The 125°C limit was also used by Wild (3) and Roos (4) in their thermal cycle tests on ML boards.

EXPERIMENTAL

Thermal cycling was carried out in a Blue M Model WSP-1098 -3X Thermal Shock Test Chamber. The cycle sequence consisted of 15 minutes at each temperature extreme and a transfer time of 2 seconds. Approximately 14 cycles were run each work day. Total circuit resistance was measured at room temperature after each test day. Resistance for each 80 hole circuit was measured at the beginning, after any failure, and at the end of the test. Any hole which exceeded the failure limit was jumpered by means of a soldered wire and the test continued.

At the completion of the test, hole resistance was measured on 4 holes of each diameter using a Model CD-3CA/CPD 5 Caviderm. From this resistance and hole geometry, average copper thickness in the hole wall could be determined. Copper thicknesses were also obtained from microscopic cross-section measurements of PTHs on cycled boards.

Glass transition temperature was determined on the laminates using a Perkin-Elmer Model TMS-1 Thermal Mechanical Analyzer (TMA). Current carrying capability of the circuits was determined by measuring the resistance changes associated with increasing constant current steps.

Three different types of copper clad laminate were selected for double sided boards to represent different glass transition temperatures and coefficients of thermal expansion: (1) Glass-epoxy type GH classification of MIL-P-13949 (NEMA grade FR 5), obtained from Westinghouse, Industrial Plastics Division as Grade 65M50. GH laminate is specified for Sandia's high reliability applications but not necessarily from this supplier, (2) Glass-polyimide from Atlantic Laminates grade AL 300 (Gemon L) reported to have a very high glass transition temperature and low coefficient of expansion, and (3) Paper-epoxy grade FR 3 from General Electric Co. reported to have a moderate glass transition temperature and high coefficient of expansion.

RESULTS

Quality of Boards As Fabricated

Similar to the experience of the IPC Round Robin program, not all the boards met the fabrication specifications. Fifty percent of the double sided boards and 80 percent of the multilayer boards in this investigation were below the required minimum copper plating thickness in the holes. Cross sections from sample holes in glass-epoxy double sided boards showed several discontinuities at the PTH - terminal area corner as shown in Figure 2. However, glass-polyimide boards showed no discontinuities and the hole walls were straight as shown in Figure 3. Paper-epoxy boards had numerous discontinuities in the hole walls and at the hole corners as shown in Figures 4 and 5. Several open circuits were detected on these boards.

On 6 of the 10 multilayer boards one of the external layers contained the artwork pattern for the double sided board instead of the multilayer pattern. This necessitated the soldering of jumper wires across six hole positions on each board. The multilayer hole wall plating was irregular and contained numerous breaks as shown in Figures 6 and 7. Chemical cleaning with concentrated sufuric acid was used after drilling to remove epoxy smear. The protruding glass fibers which are not etched with this treatment were not covered with the same thickness of copper plate as the copper or epoxy in the hole wall, causing thickness variations as shown in Figures 8 and 9. With the exception of corrections necessary because of the artwork error on the external layers, all boards displayed circuit

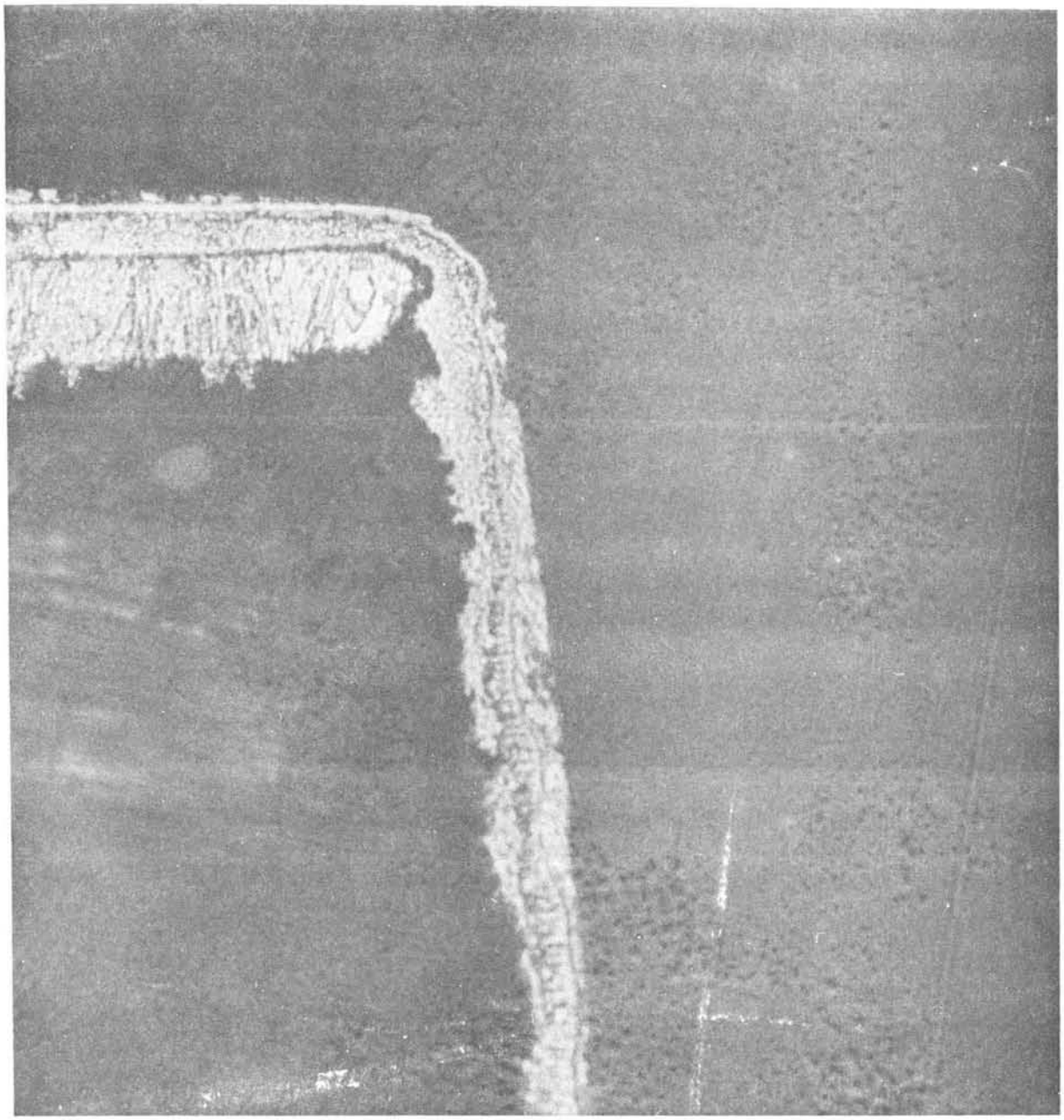


Figure 2

Double Sided Glass-Epoxy Plated Through Hole With Corner Discontinuity, 300X

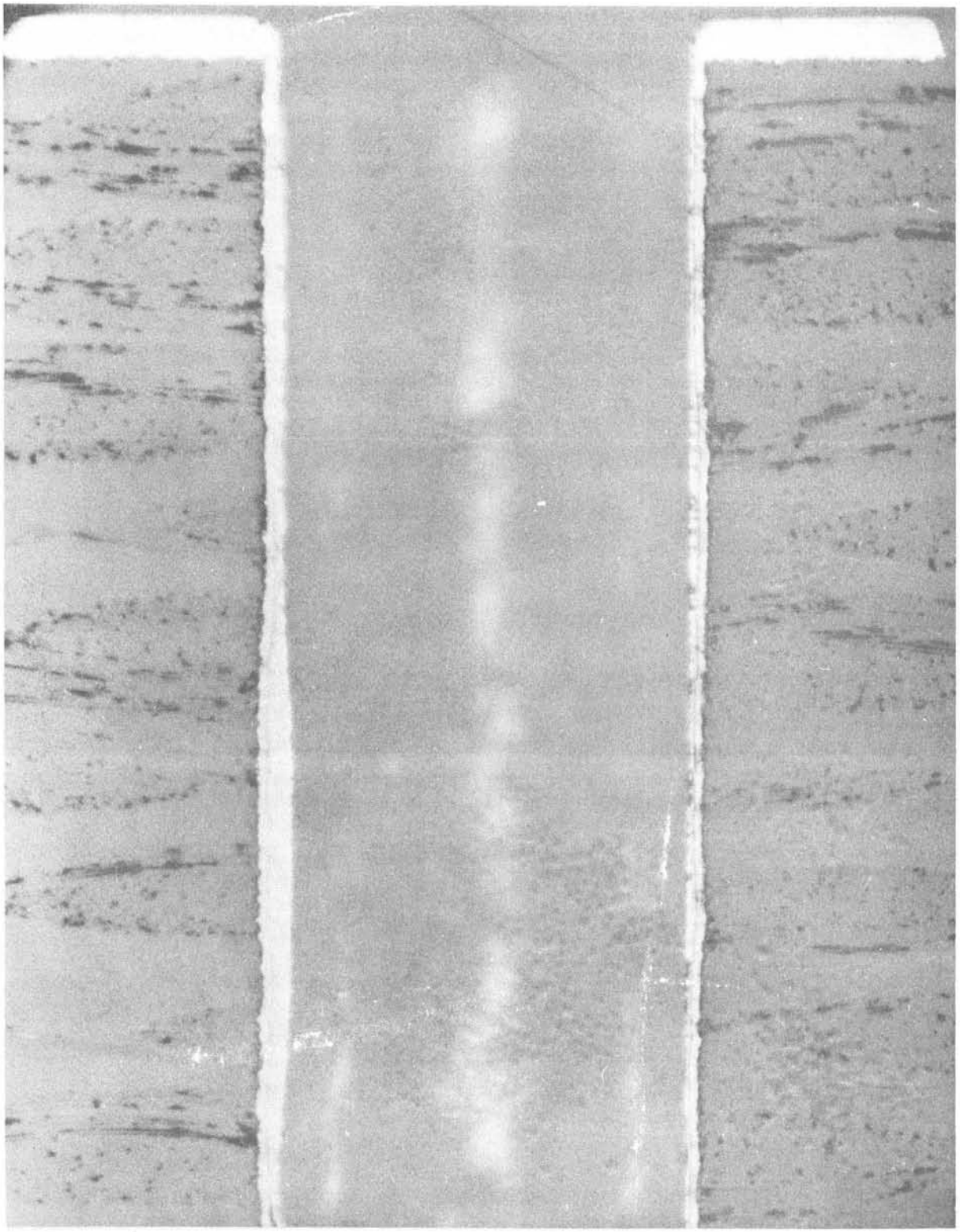


Figure 3
Double Sided Glass-Polyimide Plated-Through Hole, 75X

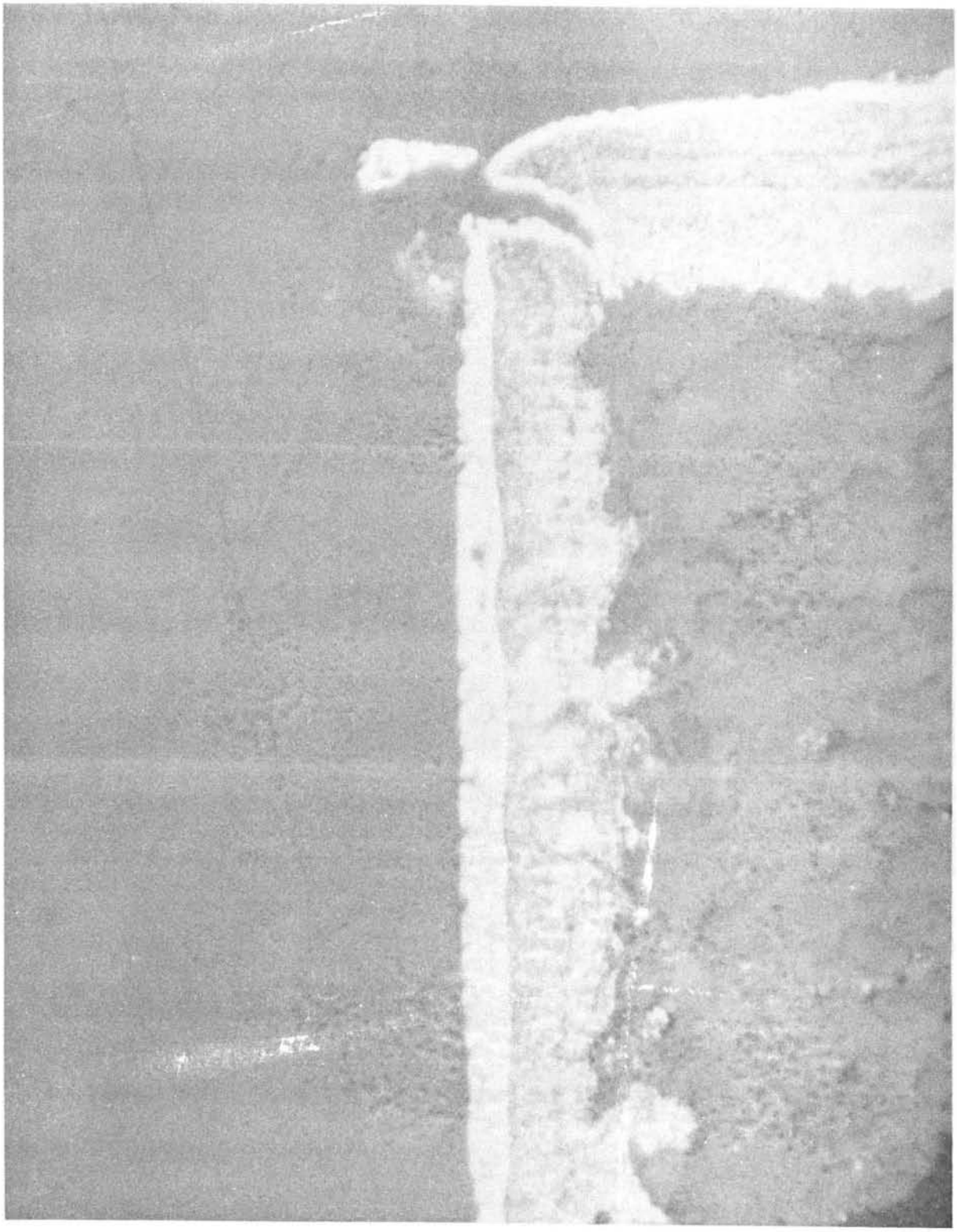


Figure 4

Double Sided Paper-Epoxy Board Plated-Through Hole With Corner Discontinuity, 300X

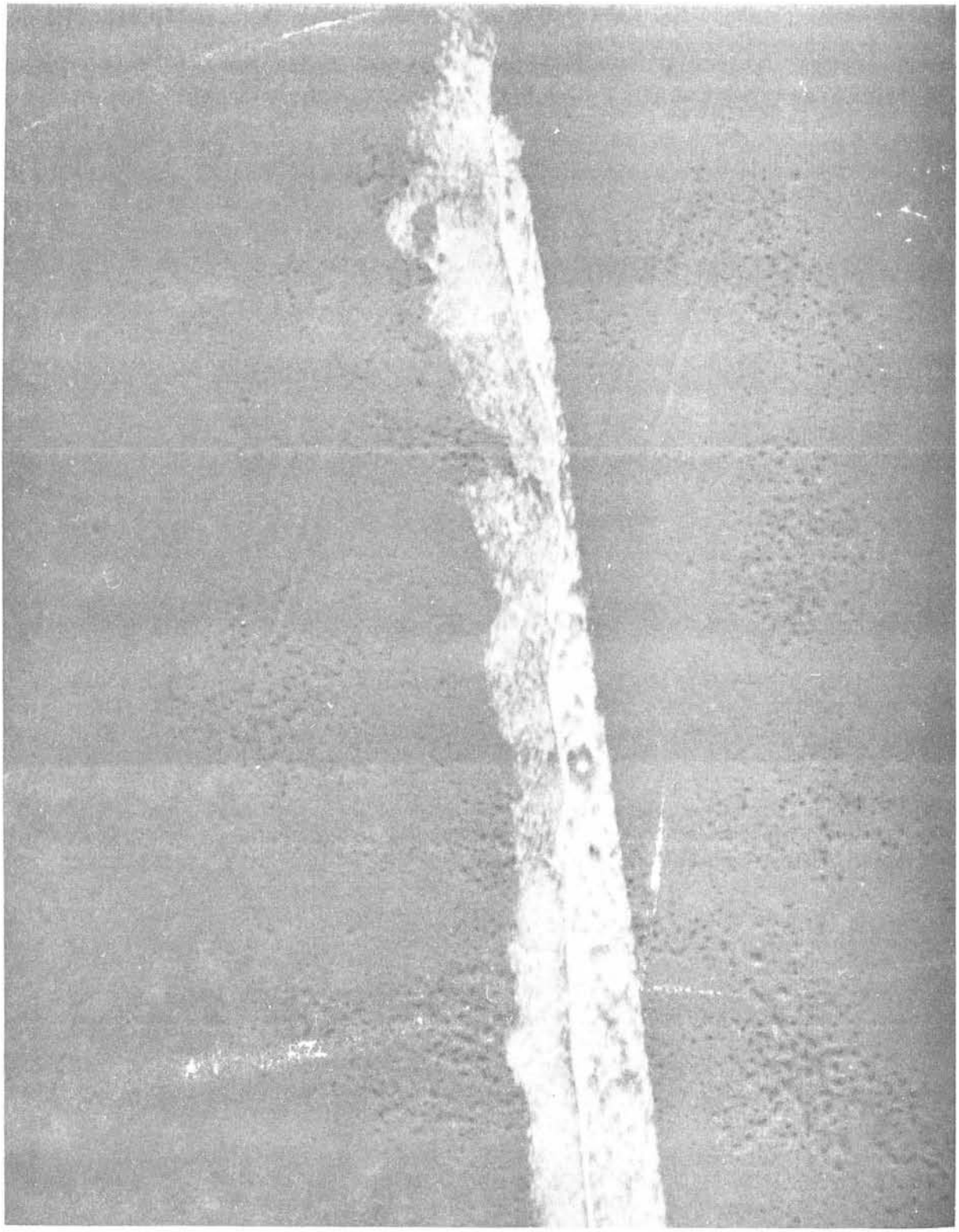


Figure 5

Double Sided Paper-Epoxy Board Plated-Through Hole With Wall Discontinuity, 300X

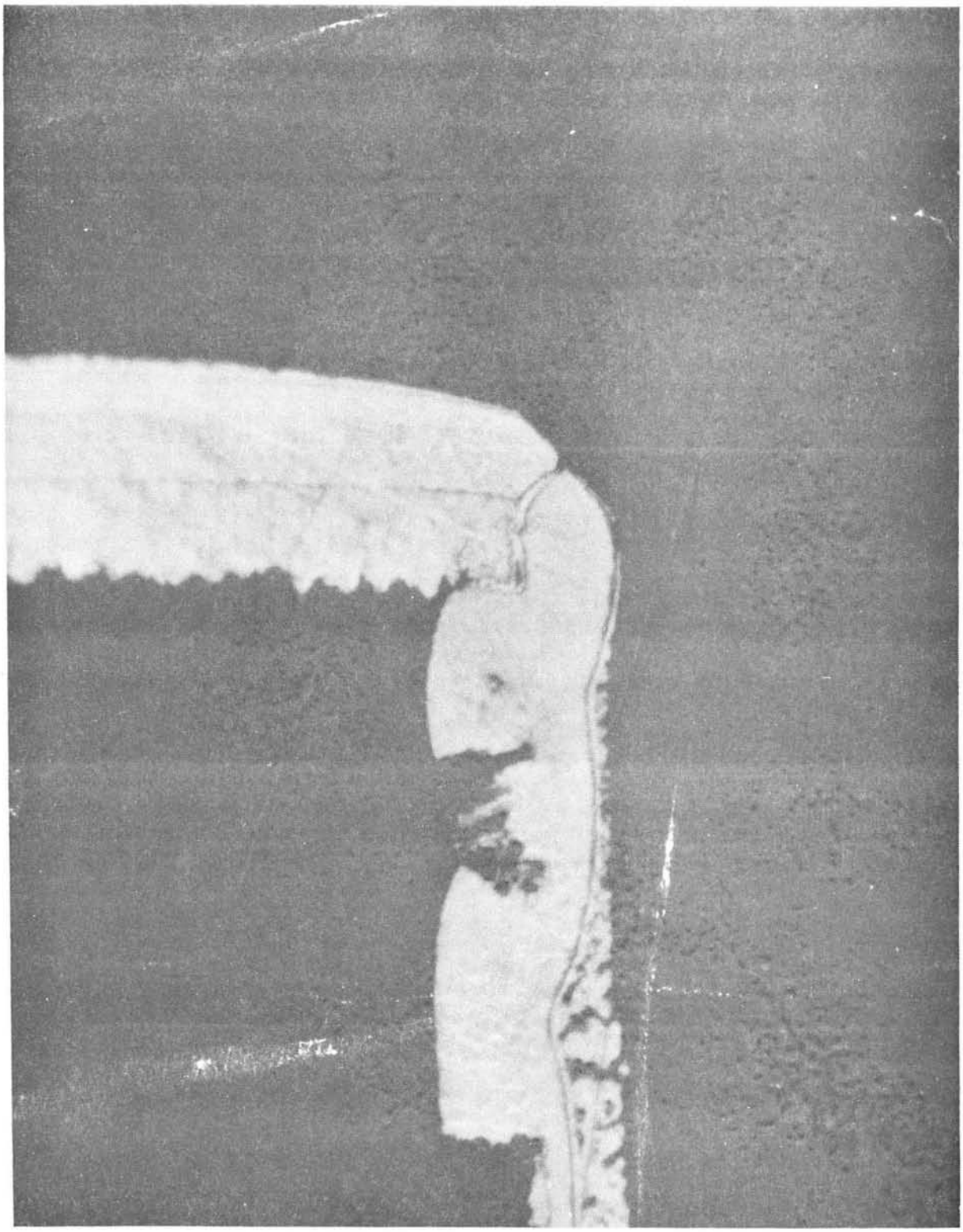


Figure 6
ML 3 Board Plated-Through Hole With Corner Break, 300X

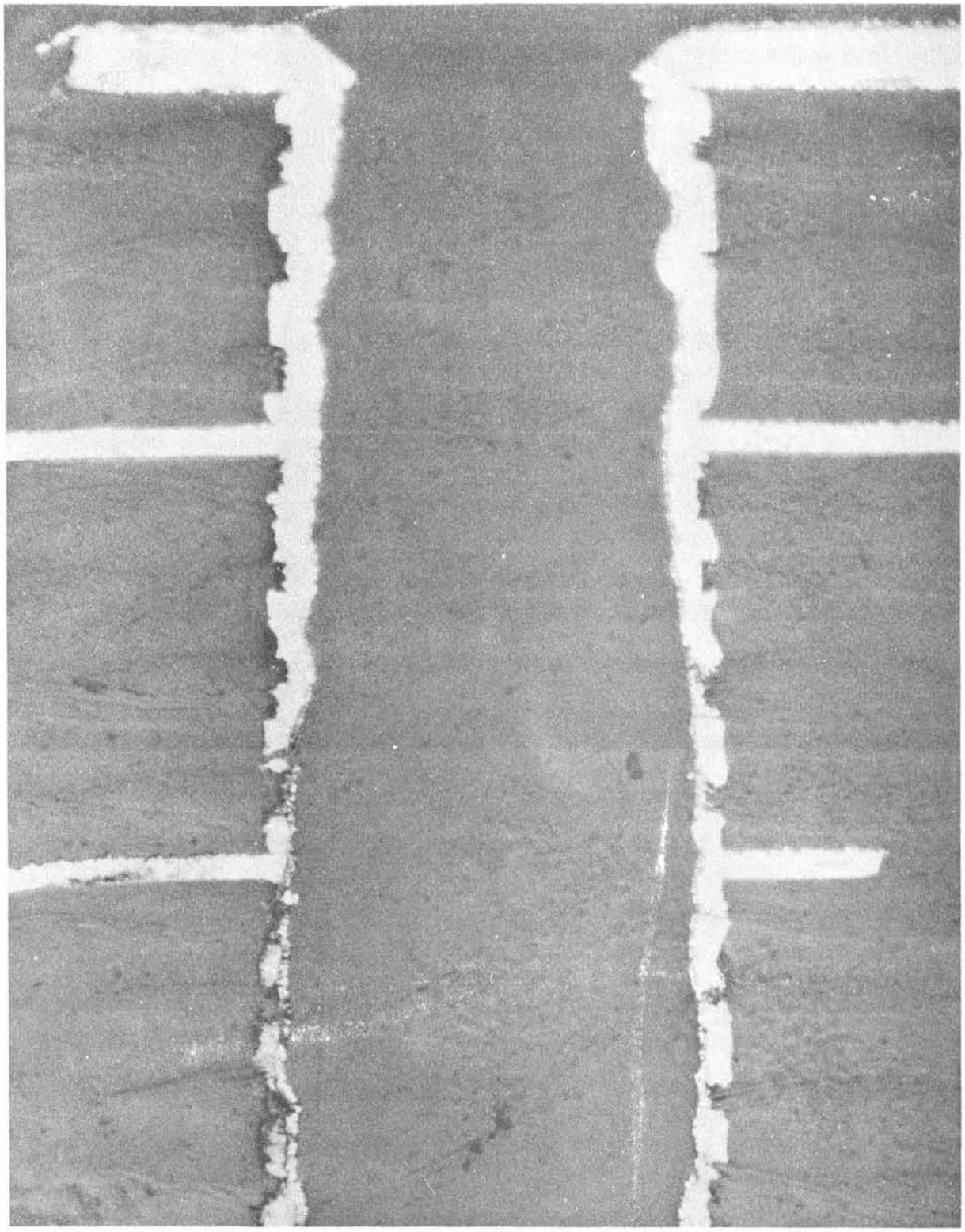


Figure 7
ML 7 Board Plated-Through Hole With Irregular Hole Wall, 300X

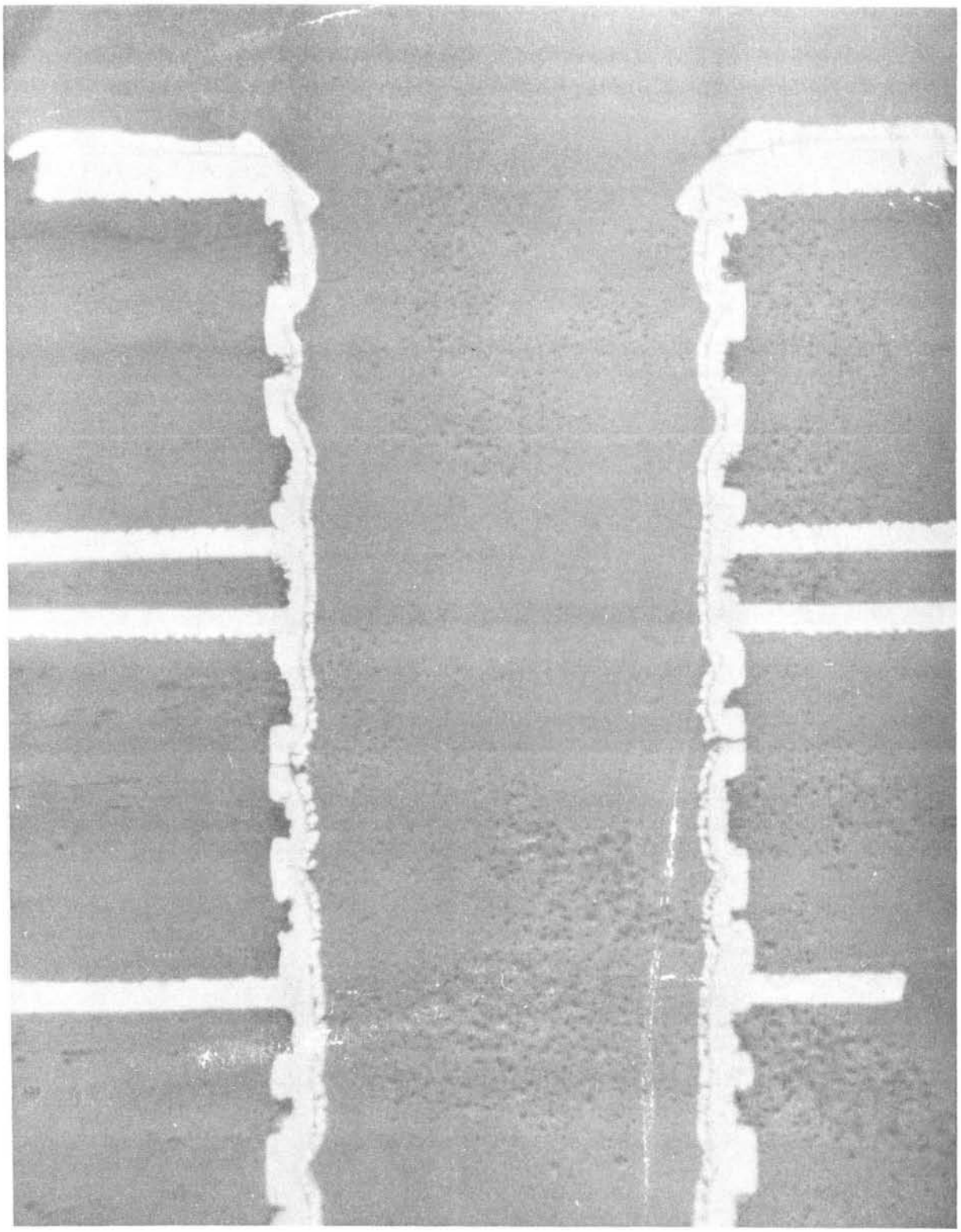


Figure 8

ML 1 Board Plated-Through Hole With Protruding Glass Fibers, 75X

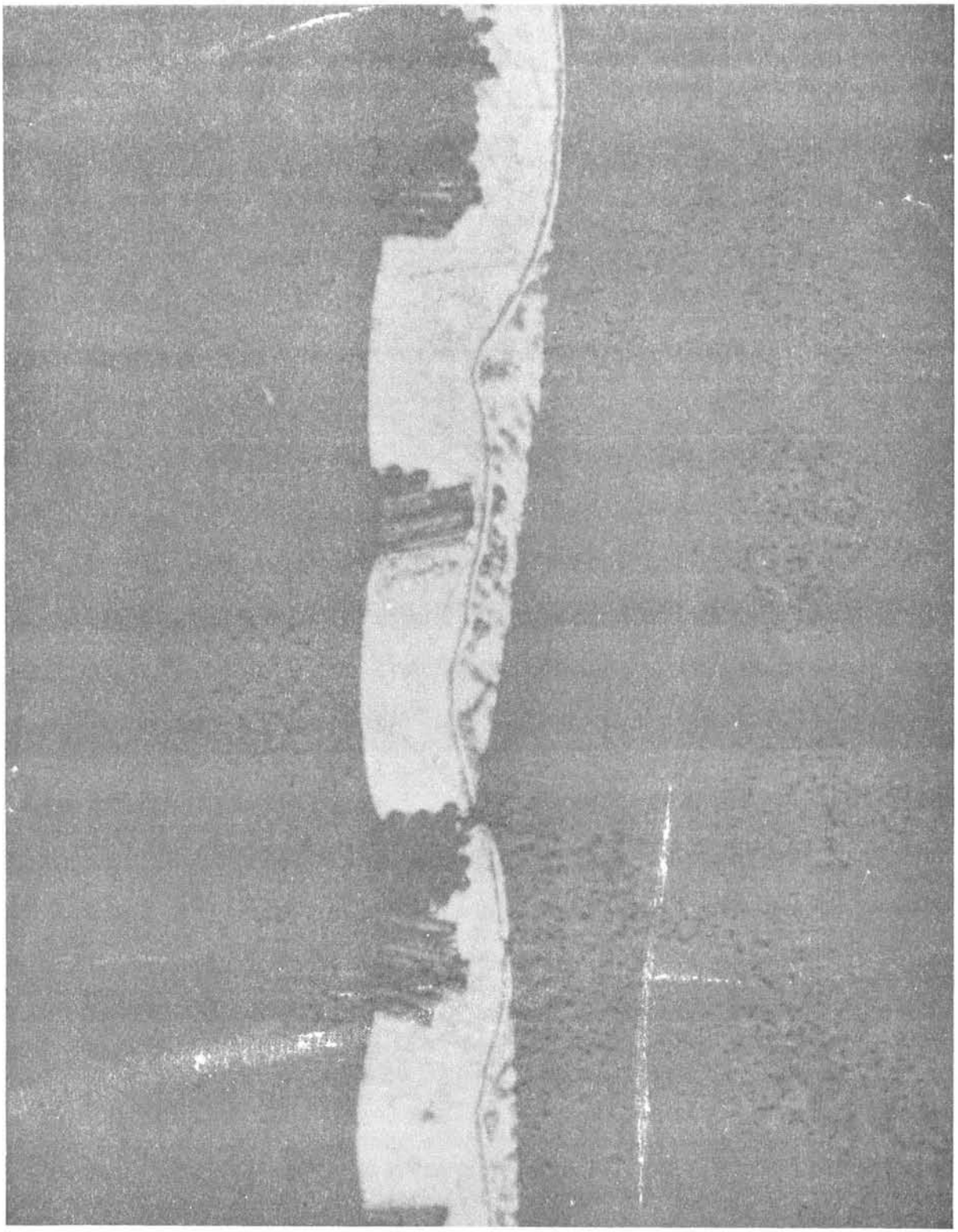


Figure 9

ML 3 Board Plated-Through Hole With Thin Plating Over Glass Fibers, 300X

continuity and electrical circuit resistances within an acceptable range.

The initial 80 hole double sided circuit resistances varied from board to board primarily because of hole wall copper thickness variations as shown in Figure 10. Also shown are calculated circuit resistance curves for different plating thicknesses with nominal hole diameters and conductors widths, and 1.55 mm (.061) thick laminate. From cross section measurements the average copper clad thickness of surface layers was found to be 0.032 mm (.00125). Surface plating thickness was taken to be the same as hole plating thickness for circuit resistance calculations. For the double sided circuit pattern the 0.51 mm (.020) holes with 0.025 mm (.001) thick walls, account for 57 percent of the total calculated circuit resistance. With 0.038 mm (.0015) thick hole walls it is 44 percent. For the 1.02 mm (.040) hole series the holes with average wall thickness of 0.025 mm (.001) account for 43 percent of the calculated circuit resistance and with 0.038 mm (.0015) walls, 38 percent.

Caviderm thickness values for hole walls compared favorably with cross section results in the region of 0.013 to 0.025 mm (.0005 to .001) thick copper. For thicknesses greater than 0.025 mm the deviations are not expected to be larger than 0.005 to 0.008 mm. Large deviations are attributed to obvious defects which could be seen in the cross sections. Table 2 lists copper thicknesses from Caviderm and cross section measurements along with initial circuit resistances. Average laminate thickness for the multilayer boards was also 1.55 mm (.061).

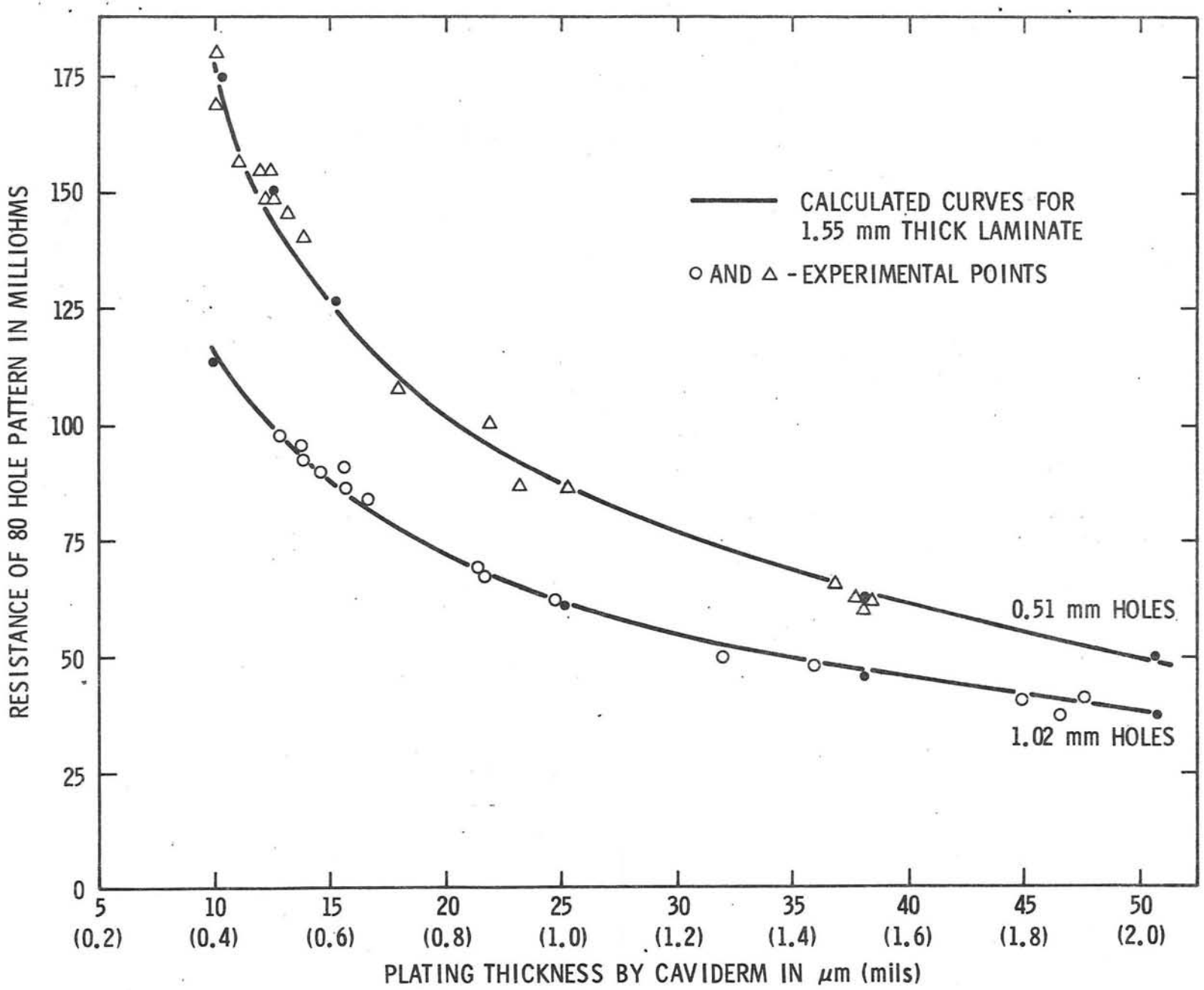


Figure 10

Circuit Resistance for Different Plating Thicknesses

TABLE 2

COPPER THICKNESSES AND CIRCUIT RESISTANCES OF TEST BOARDS

Board		Min Spec. (μm)	Copper Thickness: Cu Clad	Cross Section (μm): Surface Plate	Cross Section (μm): 0.51 mm Holes	Cross Section (μm): 1.02 mm Holes	Cavidermm (μm): 0.51 mm Holes	Cavidermm (μm): 1.02 mm Holes	Initial Circuit Resistance (milliohms): 0.51 mm Holes	Initial Circuit Resistance (milliohms): 1.02 Holes
1A1	SD	25	31.2	14/15	13	13	14	16	147	90
1A2	SD	25					12	14	153	92
5A5	SD	38	32.3	58/66	53	53	40	43	61	40
5A6	SD	38					37	47	65	41
5B1	SD	25	33.8	13	15	14	12	14	156	95
5B2	SD	25					10	13	167	97
5B3	SD	38					13	16	146	84
5B4	SD	38					14	15	142	84
5C3	SD	25	31.0	51/63	25	39	17	22	103	68
5C4	SD	25					15	22	108	68
5C5	SD	38	31.2	49			24	36	184	49
5C6	SD	38					23	32	74	49
ML1	SP	25	30.7	37	26		19	25	91	57
ML2	SP	25	31.0	39	30		16	28	87	55
ML7	SP	38	30.5	40	18		15	25	93	57
ML8	SP	38					13	28	87	56
ML3	SD	25	30.5	40	27		26	25	75	47
ML4	SD	25	29.7	45		31	33	30	72	44
ML5	SD	38	29.2	30	25		11	22	89	52
ML6	SD	38					12	21	79	54
ML9	C	25	29.5	37	15		-	-	90	48
ML10	C	25							86	51

SD = Panel Plate Copper Solder Dip and Level
SP = Pattern Plate Copper and Solder
C = Panel Plate Copper, No Solder

Circuit Resistance Changes from Thermal Cycling

Tables 3 and 4 give the increases in circuit resistance after over 500 cycles between -65°C and 125°C. Glass-epoxy and glass-polyimide boards (Sets A and B) had around 2 percent increase. This is a small resistance change, about the same as that from a 5°C rise in temperature. There was little difference in resistance change for two different plating thicknesses. Paper-epoxy boards (Set C) had significant resistance increases with cycling and these increases appeared to be related to hole wall thickness. A few of the holes of this set had to be jumpered prior to the test and after only a few cycles. The large difference between sets A and B and set C is attributed to the higher glass transition temperature and lower coefficient of expansion of sets A and B over those of set C. The effects of less than optimum quality hole walls of set C on circuit resistance were amplified by the greater thermal stress which the holes were subjected to because of their laminate composition. The glass-epoxy boards which experienced little change in resistance also had less than optimum quality hole walls but not to the degree of those of set C. There did not appear to be a correlation between percent change in resistance and hole diameter for the double sided boards.

Circuit resistance increases from thermal cycling were appreciable for most of the multilayer boards. Six of the boards required jumpers across 0.51 mm (.020) holes which became defective during the cycling so that the tests could be completed. This hole size showed the highest percent change in resistance. Note that the

TABLE 3

RESISTANCE OF PWBs AFTER MORE THAN 500 THERMAL CYCLES
BETWEEN -65°C and 125°C

D = Discontinued J - Jumpered

Board Double Sided*	Initial Circuit Resistance (m ohm) Hole Size 0.51 mm	0.16 mm	1.02 mm	Total	Mean Thickness (mm) Hole Size 0.51 mm	0.76 mm	1.02 mm	% Change in Resistance Hole Size 0.51 mm	0.76 mm	1.02 mm	Total	Board Fabrication Process	Average Glass Transition Temperature
1A1	146.5	116.1	89.2	347.8	.013	.014	.015	1.4	0	1.1	1.7	SD	167°C
1A2	151.4	118.3	89.9	358.3	.012	.014	.014	2.4	.6	2.7	2.4		
5A5	60.6	53.0	39.7	152.5	.039	.039	.041	1.0	.8	2.0	1.5		
5A6	65.2	55.4	40.6	158.7	.037	.039	.048	.9	2.0	2.2	1.8		
5B1	156.3	124.0	93.6	371.0	.011	.012	.013	.8	.5	2.9	2.0	SD	328°C
5B2	161.5	126.5	95.2	388.2	.010	.011	.013	4.8	2.5	3.3	2.6		
5B3	143.9	107.5	81.8	333.8	.013	.015	.016	2.4	.1	1.8	1.6		
5B4	140.0	109.6	82.0	332.3	.014	.015	.016	1.0	.6	2.3	1.5		
5C3	103.0	81.9	66.9	252.7	.016	.020	.022	197	398	1340	562 DJ	SD	123°C
5C4	105.7	84.7	66.7	258.5	.015	.020	.022	384	2320	2545	1555 DJ		
5C5	173.4	58.8	47.2	278.4	.023	.030	.036	334	224	76	269 DJ		
5C6	71.9	60.3	48.2	181.5	.023	.029	.032	124	171	164	144		
Multilayer†													
1	90.7	71.9	56.7	221.9	.018	.028	.025	29	21	27	13 J	SP	105°C
2	86.5	68.3	55.3	211.8	.015	.031	.028	1185	5	3	486 J		
3	75.2	56.6	47.0	178.2	.026	.025	.025	5	4	7	6	SD	105°C
4	72.3	53.9	44.2	170.6	.033	.031	.031	79	4	3	35		
5	89.0	64.3	51.8	202.8	.011	.021	.022	94	4	5	46 J		
6	79.3	62.1	53.6	195.4	.012	.018	.021	937	16	7	384 J		
7	93.1	72.8	57.2	221.8	.015	.013	.025	238	48	12	48 J	SP	112°C
8	86.8	68.4	55.6	210.3	.013	.018	.027	195	26	10	91 J		
9	89.8	61.7	47.5	195.5	-	-	-	95	41	18	61	C	110°C
10	86.0	63.9	50.6	198.0	-	-	-	198	47	10	104		

SD - Panel Plate Copper, Solder Dip, Liquid Level
SP - Pattern Plate Copper and Solder
C - Panel Plate Copper, No Solder

TABLE 4

FAILURE* RATE OF PWBs ON THERMAL CYCLING BETWEEN -65°C and 125°C

Double Sided Boards - All processed by panel plating of copper, solder dip, liquid level.

4 Boards Tested Per Set

Set A Glass-epoxy GH laminate, T_g# of 167°C, Z-axis CTE of 6×10^{-5}/°C

Copper hole thickness†, 0.012 to 0.048 mm

No failures, 1.5 to 2.4% total circuit resistance change after 544 cycles

Set B Glass-polyimide laminate, T_g of 325°C, Z-axis CTE of 1×10^{-5}/°C

Copper thickness, .010 to .016 mm

No failures, 1.5 to 2.6% circuit resistance change after 544 cycles

Set C Paper-epoxy FR 3 laminate, T_g of 123°C, Z-axis CTE not known,

Copper wall thickness, 0.015 to 0.036 mm

Total of 4 jumpers required across holes on 2 boards before testing

First failure at 12 cycles, 1 board discontinued at 300 cycles, 1 at 400 cycles and 1 at 516 cycles from general resistance buildup

150 to 1500% circuit resistance change after jumpering.

Multilayer Boards - GE Grade Laminate, T_g of 107°C, Z-axis CTE not known

4 Boards, Pattern Plating of Copper and Solder

Copper thickness, .013 to .028 mm

First failure at 190 cycles, 21 failures occurred in 4 boards between 190 and 544 cycles.

13 to 490% change in circuit resistance

*Failure indicated when the circuit resistance exceeded 1 ohm. All failures occurred with 0.51 mm holes. Failed holes were jumpered and the test continued

#T_g = Glass Transition Temperature, CTE = Coefficient of Thermal expansion

†By Caviderm

TABLE 4 (Cont'd)

4 Boards, Panel Plated Copper, Solder Dip and Liquid Level

Copper thickness, 0.010 to 0.033 mm

No failures on 2 boards, 3 failures on 2 boards

First failure at 444 cycles, 6 to 390% resistance change (with jumpers)

2 Boards, Panel Plate Copper, (no solder coating)

Copper thickness, 0.018 mm

No failures, 60 to 100% resistance change

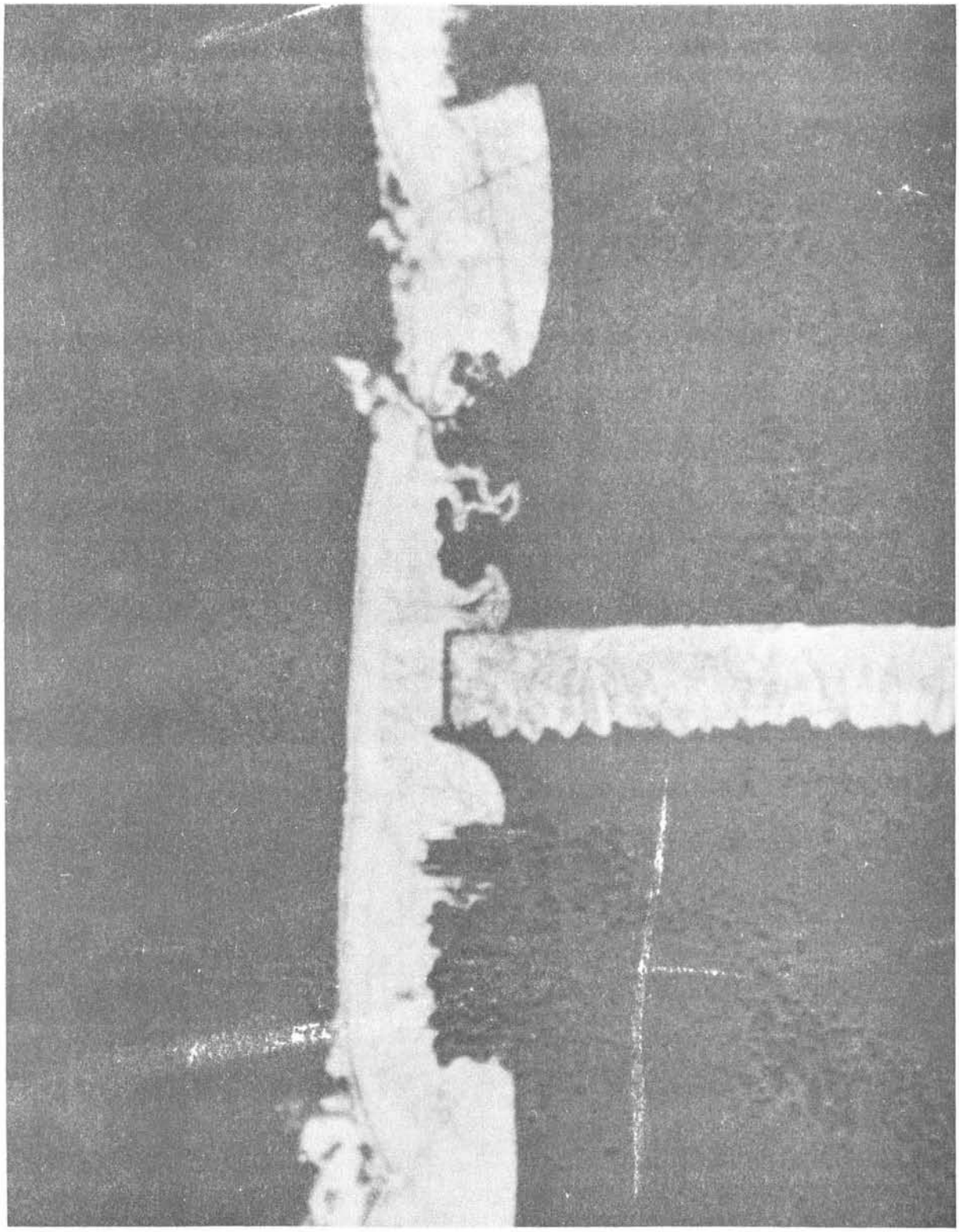


Figure 11
Typical Break in Plated-Through Hole Wall on ML 3 Board, 300X

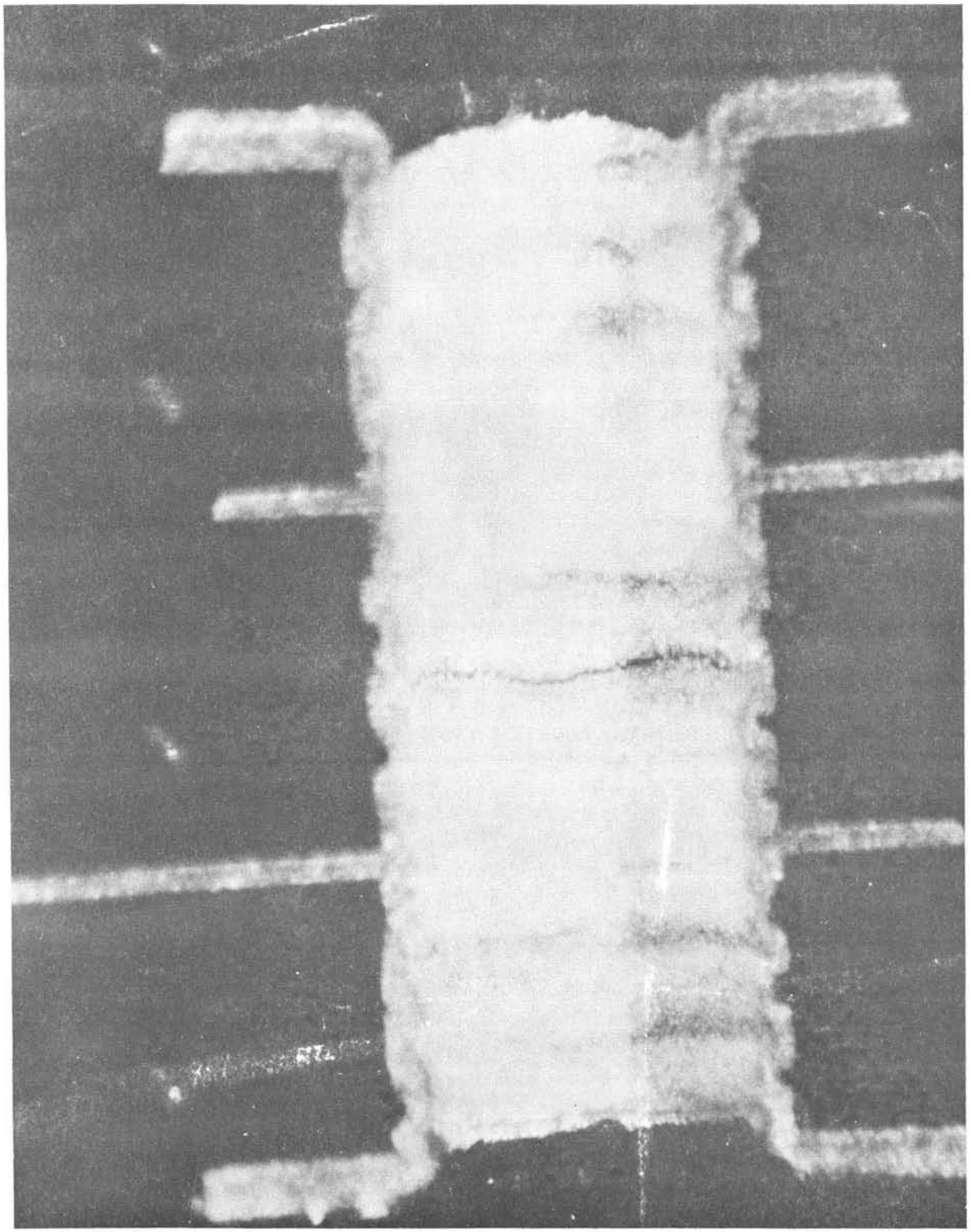
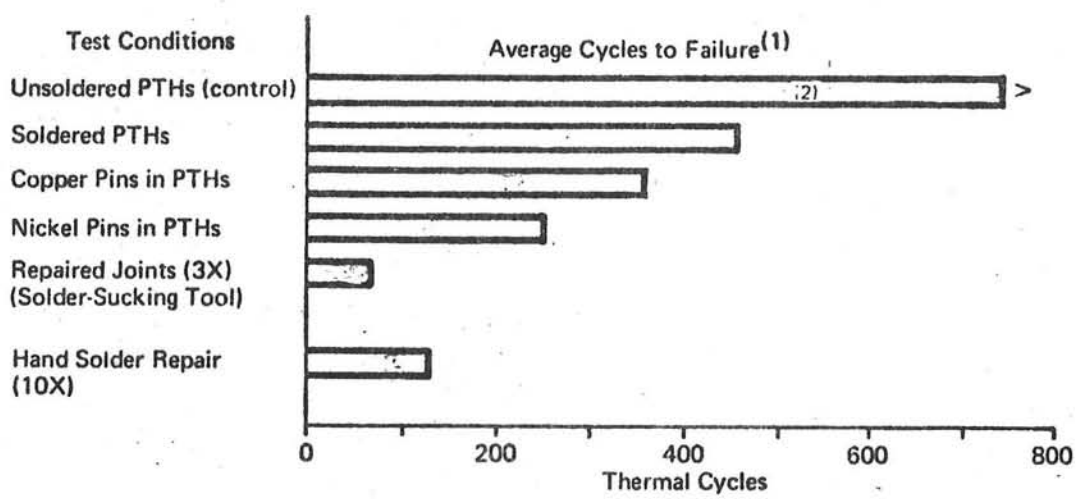


Figure 12
Circumferential Break in Plated Through Hole Wall on ML 1 Board, 54X

of GH laminate from other suppliers, so a direct comparison between double sided and multilayer boards both with glass-epoxy may be misleading. Glass transition temperature on GH laminate samples ranged from 85°C to 167°C.

Wild[3] reported thermal cycle tests on GE grade multilayer boards with soldered and unsoldered PTHs. The cycle was -62°C to 125°C over a 2 hour interval. His results are shown below for a 0.54 mm (.100) thick laminate. As can be seen from the chart, solder filling reduced reliability of PTHs. For a 1.52 mm (.060) thick laminate, failure point was more than 1300 cycles. Reducing the upper test temperature to 115°C increased the first failure point to over 1400 cycles.



Notes: (1) Test boards were 0.100-inch thick. Second PTH electrical failure was considered a board failure (Failure ≥10% ΔΩ).
(2) First board failure of ~6 specimens.

Soldering Effects on Thermal Cycling Reliability (-62°C to +125°C Cycle)

Roos[4] thermal cycled multilayer board assemblies with flat-packs and dual-in-line packages between -65°C and 100°C, and -65°C and 125°C. Multilayer boards with 6366 holes and GE grade laminate showed no failures after 2200 cycles of -65°C to 100°C. The cycle was over a 1.5 hour interval. For a -65°C to 125°C - 3 hour cycle, 22 failures occurred after 838 cycles, the first after 385 cycles.

An earlier study for NASA[5] indicated multilayer board thermal fatigue life to be 200 cycles and a recommendation was made that multilayer boards should not be used in long-life hardware which experiences a greater number of temperature cycles.

The Wild and Roos studies show that multilayer boards can be fabricated which will withstand without failure a much larger number of cycles to temperature extremes greater than those the boards are expected to experience in their system applications. The results of this study and the NASA and IPC studies show that PWBs can also be fabricated which will fail in 200 or less cycles from either poor PTH quality or from the use of resin laminate with low glass transition temperature and high coefficient of expansion. Hole quality and resin composition need to be further evaluated to determine their relative contribution to circuit failures in thermal cycling.

Current Carrying Tests on Cycled and Uncycled Boards

The 0.51 mm (.020) and 1.02 mm (.040) hole circuits were subjected to increasing constant current steps to assess PTH degradation which may not have shown up from resistance readings. Average temperature rise from 25°C was calculated for the circuits from the resistance increase after 30 seconds at each constant

current step. For some of the current steps resistance was also measured until the circuit equilibrated with the environment or the circuit opened or the temperature approached high values indicating circuit failure would eventually occur. The intervals covered were minutes to hours. The results are given in Tables 5 and 6.

There was little difference in current carrying capacity between the cycled and uncycled double sided glass-epoxy boards. Comparison could not be made for the glass-polyimide boards but from the temperature rises of the cycled board, there appears to be little if any effect of thermal cycling. Paper-epoxy boards were definitely degraded by thermal cycling. This set and multilayer boards had comparable or greater hole wall thicknesses, yet had poorer current carrying capability than the double sided glass-epoxy or glass-polyimide boards. How much of this difference is attributable to poorer hole quality and how much to the difference in laminate composition is now known.

The current carrying capability of these circuits in addition to being a function of hole and surface geometry is also a function of time of current flow. High currents which can be carried for short intervals frequently cause board degradation or burnouts on longer intervals. Holes with regions of thin copper or with breaks are likely to experience local heating and thermal fatigue effects so thermal equilibration may not be achieved.

resistance changes in Table 3 are after jumper wires were inserted into the board. The variability in copper hole wall thickness was greater for the pattern plated boards than the panel plated boards. An uneven hole wall thickness distribution in the circuit places greater stress on some holes than others.

The poor hole quality of the multilayer boards clouds any correlation between processing variables and resistance changes with thermal cycling. This quality however appears to be comparable to that of many of the boards used in the IPC tests. It is of significance that despite the poor board quality, the first observed failure occurred after 190 cycles. Typical breaks in the hole wall, some circumferential, are shown in the cross sections in Figures 11 and 12. Although board ML 3 showed only a small increase in resistance, cross sections of holes from this board had numerous breaks in the hole walls.

The general failure mode of PTHs was barrel and corner crack formation. There were a few instances in which the inner conductor separated from the hole wall on ML boards as seen in Figure 11. There was no indication in the cross sections of Z axis expansion causing permanent lifting of the perpheral edges of the terminal areas, for example: Some of the corner or rim cracking could have been from Z-axis expansion; however, the presence of solder in some of the cracks indicate that the cracking occurred in fabrication prior to or during solder application. The glass transition temperature of the double sided glass-epoxy laminate used in this investigation is higher than the values measured on samples

TABLE 5

CURRENT CAPABILITY OF 0.51 mm HOLE CIRCUIT

Temperature Rise°C

Board D.S.	Mean Thickness (μm)	$R_{25°C}$ (mohm)	Current (amps) 1	2	4	4 10 min	4 at equi.	6	6 10 min	
1A2	13	153.7	2.5	7.0	27.6			74.5	182	- (to 346°C at 6 amps then burn through in 300 minutes)
5A12*	13	155.2	1.3	5.7	24.6	52	53	75.6	237	
5A6	38	66.1	0.4	2.1	10.2			26.0	53.4	71° in 30 sec, 101 in 10 min.
5A8*	39	61.0		1.5	9.4			21.8		44° 8 amp/30 sec.
5B2	10	171.2	1.1	5.8	26.3			71.8	182	- to 453° at 6 amps then burn through
5C7*	23	81.9J*	0.6	2.0	13.7	23.5		38 →	64	87° in 30 sec, 155 in 10 min. at 8 amp
5C4	15	297.8	2.3	17.6	B					
5C14*	18	99.7	0.9	4.9	25.1→	open				
ML2	15	110.9J	0.8	5.8	28.4	B				
ML3	25		0.6	2.9	13.4	24.6	26.2			
†ML4	33	87.6	0.4	4.6	20.3			B		
†ML6	13	148.1	1.2	6.7	31.0			B		
ML8	15	142.5J	.4	5.2	27.7	53.6				
†ML10		183.6	3.7	11.9	46.2			B		

#Measurements for 30 seconds unless indicated otherwise, 10 minute measurements were made after all 30 second measurements.

†Modified IPC RR on Top Layer

B = Burn Through

*Jumper Necessary to Continue Test

TABLE 6

CURRENT CARRYING CAPABILITY OF 1.02 mm HOLE CIRCUIT

Temperature Rise in °C

Board No.	Mean Thickness (μm)	Meas $R_{25°C}$	Current (amps)† 2	4	6	6 (10 min)	8	8 (10 min)	10	10 (10 min)	12	12
1A2	14	92.4	3.5	15	39		78	(169)				
5A12*	15	90.4	3.6	15	37	(79)	73					
5A6	47	41.8	1.4	6	15		30		52		81	(143)
5A8*	46	36.8	.8	5	12		25		43		70	
5B4	15	85.7	3	13	35		70	(151)				
5C4	22	37.5	22	294	burn through at 4 amp in 1 min.							
5C14*	21	69.2	2	10	27	(75)	56		126			
5C7*	25	61.9	2	8	22		44	(103)	82			
ML2	28	56.9	2	10	27		55		96	(burnout at 289°C/10 amp)		
ML4	30	46.2	1	7	20		41		71	125 (equilibration of 132°C at 10 amp)		
ML6	20	57.7	1	9	25		51		89	(burnout at 272°/8 amp)		
ML8	28	61.4	2	9	25		52		92	(burnout at 10 amp)		
ML10	15	55.9	5	9	25		50		97	(burnout at 10 amp)		

†Unless otherwise indicated all measurement were for 30 seconds 10 minute measurements, in parentheses, were made after all the 30 second measurements were made.

*No thermal cycling, all other boards were thermal cycled between -65° and 125°C.

SUMMARY

Laminate composition appears to be the most important variable affecting the ability of PTHs to withstand thermal cycling. Laminates with high glass transition temperature and low coefficient of thermal expansion are more forgiving of hole wall defects or deviations in wall thickness than are laminates with high coefficient of expansion or a glass transition temperature below the maximum temperature of the test cycle.

Measured circuit resistance provided a quick and effective indicator of the deviations of conductors and holes from their design requirements, especially when this resistance can be compared to that calculated from the specified nominal or minimum circuit dimensions.

Relating the results of this study to application temperatures below those used here requires judgement on the part of the designer. Certainly the effect of thermal cycling to a lower temperature range should be no worse than shown here. For a laminate composition in which the glass transition temperature is above the upper test or application temperature and Z-axis expansion coefficient is around 60×10^{-6} cm/cm^{o}C, then the PTHs should show little effect from thermal cycling. For laminate with a glass transition temperature below the upper required temperature then one should expect to see an effect on the PTH quality. Further work is required to substantiate these preliminary indications.

Circuits which showed significant increases in resistance from thermal cycling also showed poorer current carrying capability. Whether this can be attributed to poor hole quality or laminate

composition was not determined. Localized heating at defective regions of hole walls is believed to be the cause of hole failures when the circuits were subjected to high constant currents for extended intervals.

RECOMMENDATIONS FOR FUTURE STUDIES

1. Double sided boards with GH grade laminate having a glass transition temperature lower than the maximum temperature of the test cycle should be thermal cycled. Processing should be typical of production boards. Thin clad laminate boards should also be included in the test as the measured glass transition temperature of laminate from one supplier averaged 78°C. If the results show glass transition temperature to be critical to PTH reliability after thermal cycling, then a minimum glass transition temperature should be specified for incoming laminates.
2. Thermal cycle tests should be repeated with multilayer boards having proper circuit patterns and better hole quality. For the latter it is recommended that etchback rather than sulfuric acid chemical cleaning be used after drilling. Laminates from different suppliers should be used as measurements have indicated variations in glass transition temperature.
3. Measured circuit resistance should be compared to resistance calculated from specified nominal or minimum circuit dimensions and hole wall thickness.
4. The use of a temperature indicating medium such as infra-red or liquid crystals should be explored as a means for detecting

local hot spots when a fixed current is applied to a circuit pattern such as used in this investigation.

5. Further consideration should be given to glass-polyimide laminates for boards which are subjected to high temperatures in subsequent processing or system applications. Their low coefficient of thermal expansion and high glass transition temperature commend them for such environments.

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